XR79206

40V, 6A Synchronous Step-Down COT Power Module

Description

The XR79206 is part of a family of 40V synchronous step-down power modules combining the controller, drivers, inductor, passive components and MOSFETs in a single package for point-of-load supplies. This module requires very few external components leading to ease of design and fast time to market. The XR79206 has load current rating of 6A. A wide 5V to 40V input voltage range allows for single supply operation from industry standard 24V ±10%, 18V to 36V and rectified 18VAC and 24VAC rails.

With a proprietary emulated current mode Constant On-Time (COT) control scheme, the XR79206 provides extremely fast line and load transient response using ceramic output capacitors. It requires no loop compensation, simplifying circuit implementation and reducing overall component count. The control loop also provides 0.2% load and 0.1% line regulation and maintains constant operating frequency. A selectable power saving mode, allows the user to operate in Discontinuous Current Mode (DCM) at light current loads significantly increasing the converter efficiency.

A host of protection features, including overcurrent, over temperature, short-circuit and UVLO, help achieve safe operation under abnormal operating conditions.

The XR79206 is available in a RoHS-compliant, green/halogen-free space-saving 10mm x 10mm x 4mm QFN package.

FEATURES

- 6A step-down power module
  - 5V to 40V wide single input voltage
  - ≥0.6V adjustable output voltage
- Controller, drivers, inductor, passive components and MOSFETs integrated in one package
- Proprietary constant on-time control
  - No loop compensation required
  - Stable with ceramic output capacitors
  - Programmable 100ns to 1µs on-time
  - Constant 400kHz to 800kHz frequency
  - Selectable CCM or DCM/CCM operation
- Precision enable and power-good flag
- Programmable soft-start
- 10mm x 10mm x 4mm QFN package

APPLICATIONS

- Drones and remote vehicles
- Automotive displays
- FPGA/DSP/processor supplies
- Industrial control and automation
- Telecommunications and infrastructure equipment
- Distributed power architecture

Typical Application

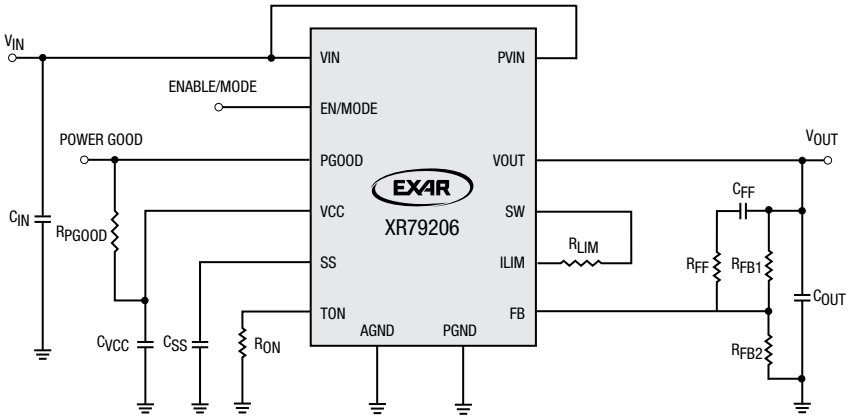


Figure 1. Typical Application

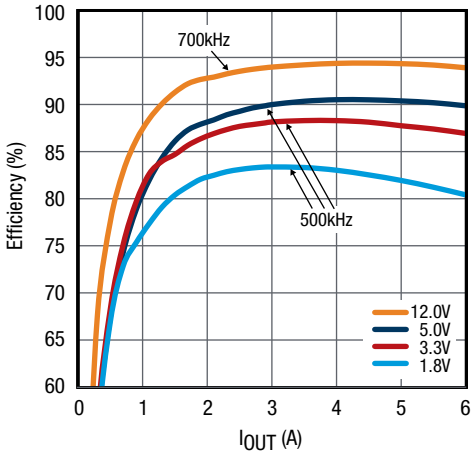


Figure 2. Efficiency, $24V_{IN}$

Absolute Maximum Ratings

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to any absolute maximum rating condition for extended periods may affect device reliability and lifetime.

PV_{IN}, V_{IN} ..... -0.3V to 43V

V_{CC} ..... -0.3V to 6.0V

BST ..... -0.3V to 48V(1)

BST-SW ..... -0.3V to 6V

SW, ILIM ..... -1V to 43V(1)(2)

All other pins ..... -0.3V to V_{CC} + 0.3V

Storage temperature ..... -65°C to 150°C

Junction temperature ..... 150°C

Power dissipation ..... Internally limited

Lead temperature (soldering, 10 seconds) ..... 300°C

ESD rating (HBM – human body model) 2kV

ESD rating (CDM – charged device model) 2kV

Operating Conditions

PV_{IN}, V_{IN} ..... 5V to 40V

SW, ILIM ..... -1V to 40V(1)(2)

PGOOD, V_{CC}, TON, SS, EN, FB ..... -0.3V to 5.5V

Switching frequency ..... 400kHz-800kHz(3)

Junction temperature range (T_J) ..... -40°C to 125°C

Package power dissipation max at 25°C 5.5W

Package thermal resistance θ_{JA} ..... 18.1°C/W

NOTES:
1. No external voltage applied.
2. SW pin's DC range is -1V, transient is -5V for less than 50ns.
3. Recommended frequency for optimum performance.

Electrical Characteristics

T_J = 25°C, V_{IN} = 24V, BST = V_{CC}, SW = AGND = PGND = 0V, C_{VCC} = 4.7µF, unless otherwise specified. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Power Supply Characteristics							
V_{IN}	Input voltage range	V_{CC} regulating	•	5		40	V
I_{VIN}	V_{IN} supply current	Not switching, V_{IN} = 24V, V_{FB} = 0.7V	•		0.7	2	mA
		f = 500kHz, R_{ON} = 124kΩ, V_{FB} = 0.58V			10		mA
I_{OFF}	Shutdown current	Enable = 0V, P_{VIN} = V_{IN} = 24V			1		µA
Enable and Undervoltage Lock-Out (UVLO)							
$V_{IH\_EN\_1}$	EN pin rising threshold		•	1.8	1.9	2.0	V
$V_{EN\_HYS\_1}$	EN pin hysteresis				70		mV
$V_{IH\_EN\_2}$	EN pin rising threshold for DCM/CCM		•	2.8	3.0	3.1	V
$V_{EN\_HYS\_2}$	EN pin hysteresis				110		mV
	V_{CC} UVLO start threshold	Rising edge	•	4.00	4.25	4.40	V
	V_{CC} UVLO hysteresis		•		195		mV

Electrical Characteristics (Continued)

T_J = 25°C, V_{IN} = 24V, BST = V_{CC}, SW = AGND = PGND = 0V, C_{VCC} = 4.7µF, unless otherwise specified. Limits applying over the full operating temperature range are denoted by a •.

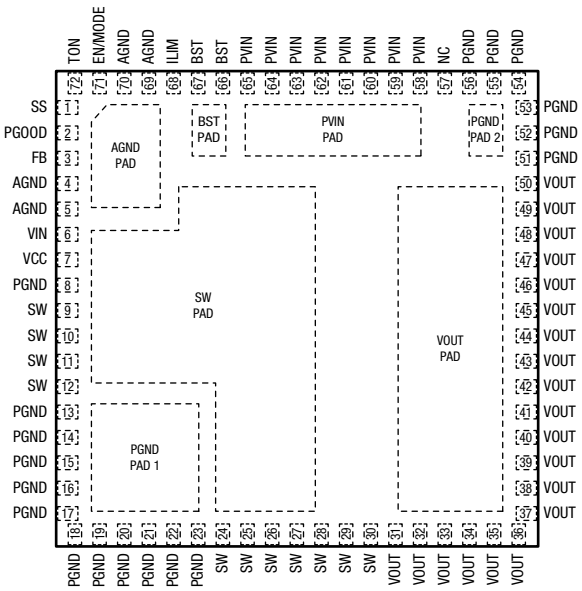
Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Reference Voltage							
V_{REF}	Reference voltage	V_{IN} = 5V to 40V, V_{CC} regulating		0.596	0.600	0.604	V
			•	0.594	0.600	0.606	V
	DC load regulation	CCM operation, closed loop, applies to any C_{OUT}			±0.2		%
	DC line regulation				±0.1		%
Programmable Constant On-Time							
$T_{ON(MIN)}$	Minimum programmable on-time	R_{ON} = 14kΩ, V_{IN} = 40V			120		ns
T_{ON1}	On-time 1	R_{ON} = 14kΩ, V_{IN} = 24V	•	180	200	220	ns
T_{ON2}	On-time 2	R_{ON} = 35.7kΩ, V_{IN} = 24V	•	420	470	520	ns
	On-time 2 frequency	R_{ON} = 35.7kΩ, V_{IN} = 24V, V_{OUT} = 5.0V, I_{OUT} = 6A		425	470	525	kHz
$T_{OFF(MIN)}$	Minimum off-time		•		250	350	ns
Diode Emulation Mode							
	Zero crossing threshold	DC value measured during test			-2		mV
Soft-Start							
	SS charge current		•	-14	-10	-6	µA
	SS discharge current	Fault present	•	1			mA
V_{CC} Linear Regulator							
	V_{CC} output voltage	V_{IN} = 6V to 40V, I_{LOAD} = 0 to 30mA	•	4.8	5.0	5.2	V
		V_{IN} = 5V, I_{LOAD} = 0 to 20mA	•	4.51	4.8		
Power Good Output							
	Power good threshold			-10	-7	-5	%
	Power good hysteresis				1.5	4	%
	Power good sink current			1			mA

Electrical Characteristics (Continued)

T_J = 25°C, V_{IN} = 24V, BST = V_{CC}, SW = AGND = PGND = 0V, C_{VCC} = 4.7µF, unless otherwise specified. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Protection: OCP, OTP, Short-Circuit							
	Hiccup timeout				110		ms
	I_{LIM}/R_{DS}			2.40	2.85	3.20	µA/mΩ
	I_{LIM} current temperature coefficient				0.4		%/°C
	I_{LIM} comparator offset		•	-8	0	8	mV
	Current limit blanking	GL rising >1V			100		ns
	Thermal shutdown threshold	Rising temperature			150		°C
	Thermal hysteresis				15		°C
	Feedback pin short-circuit threshold	Percent of V_{REF}, short circuit is active. After PGOOD is asserted	•	50	60	70	%
Output Power Stage							
R_{DSON}	High-side MOSFET R_{DSON}	I_{DS} = 2A			41	59	mΩ
	Low-side MOSFET R_{DSON}				17.6	21.5	mΩ
I_{OUT}	Maximum output current		•	6			A
L	Output inductance			1.8	2.2	2.6	µH
C_{IN}	Input capacitance				1		µF
C_{BST}	Bootstrap capacitance				0.1		µF

Pin Configuration



Pin Functions

Pin Number	Pin Name	Type	Description
1	SS	A	Soft-start pin. Connect an external capacitor between SS and AGND to program the soft-start rate based on the 10µA internal source current.
2	PGOOD	OD, O	Power-good output. This open-drain output is pulled low when V_{OUT} is outside the regulation.
3	FB	A	Feedback input to feedback comparator. Connect with a set of resistors to VOUT and AGND in order to program V_{OUT}.
4, 5, 69, 70, AGND Pad	AGND	A	Analog ground. Control circuitry of the IC is referenced to this pin. Connect to PGND.
6	VIN	PWR	IC supply input. Provides power to internal LDO. Connect to PVIN pins.
7	VCC	PWR	The output of LDO. Bypass with a 4.7µF capacitor to AGND.
8	PGND	PWR	Controller low-side driver ground. Connect with a short trace to closest PGND pins or PGND pad.
13-23, 51-56, PGND Pads	PGND	PWR	Ground of the power stage. Should be connected to the system's power ground plane.
9-12, 24-30, SW Pad	SW	PWR	Switching node. It internally connects the source of the high-side FET, the drain of the low-side FET, the inductor and bootstrap capacitor. Use thermal vias and/or sufficient PCB land area in order to heatsink the low-side FET and the inductor.
31-50, VOUT Pad	VOUT	PWR	Output of the power stage. Place the output filter capacitors as close as possible to these pins.
58-65, PVIN Pad	PVIN	PWR	Power stage input voltage. Place the input filter capacitors as close as possible to these pins.
66, 67, BST Pad	BST	A	Controller high-side driver supply pin. It is internally connected to SW via a 0.1µF bootstrap capacitor. Leave these pins floating.
68	ILIM	A	Overcurrent protection programming. Connect with a short trace to SW pins.
71	EN/MODE	I	Precision enable pin. Pulling this pin above 1.9V will turn the IC on and it will operate in Forced CCM. If the voltage is raised above 3.0V, then the IC will operate in DCM or CCM depending on load.
72	TON	A	Constant on-time programming pin. Connect with a resistor to AGND.

NOTE:
A = Analog, I = Input, O = Output, OD = Open Drain, PWR = Power.

Typical Performance Characteristics

T_A = 25°C, V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 6A, f = 500kHz, unless otherwise specified. Schematic shown in Figure 27.

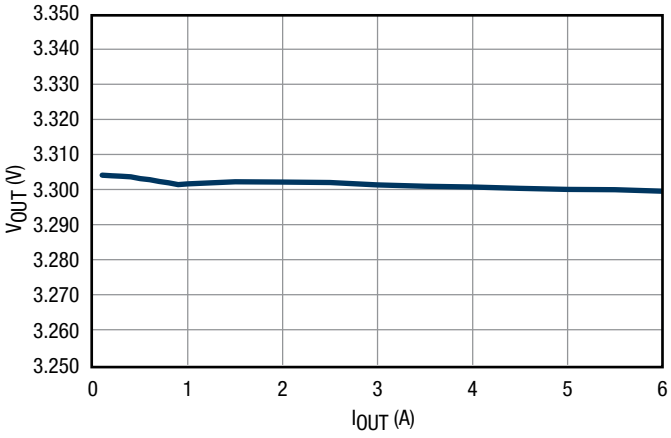


Figure 3. Load Regulation

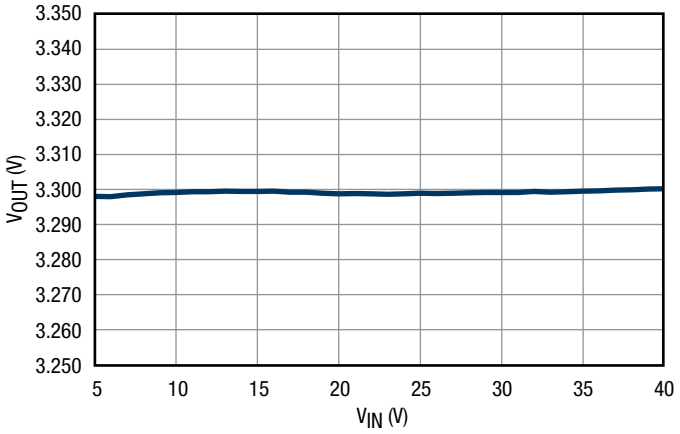


Figure 4. Line Regulation

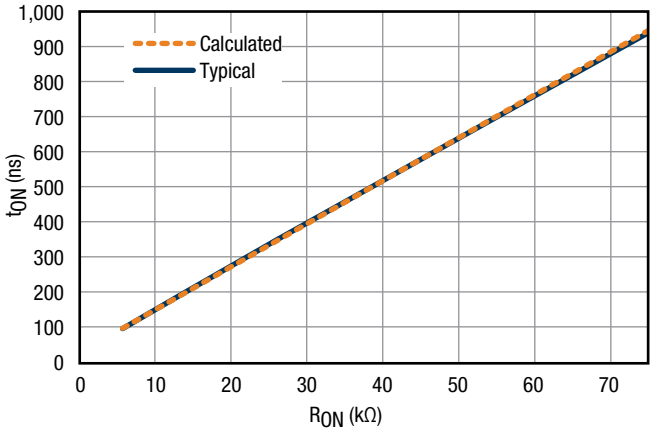


Figure 5. t_{ON} vs. R_{ON}

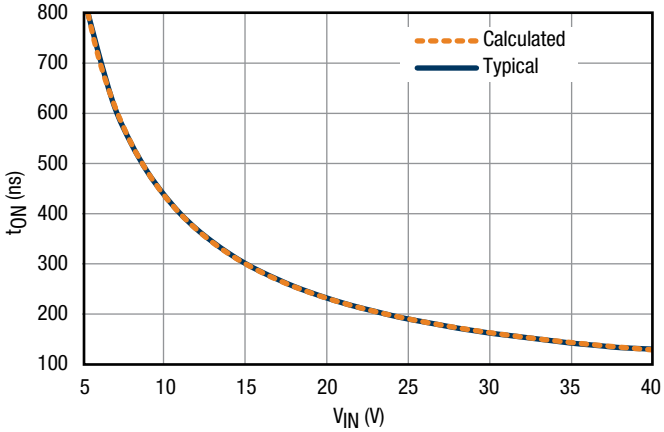


Figure 6. t_{ON} vs. V_{IN}, R_{ON} = 14kΩ

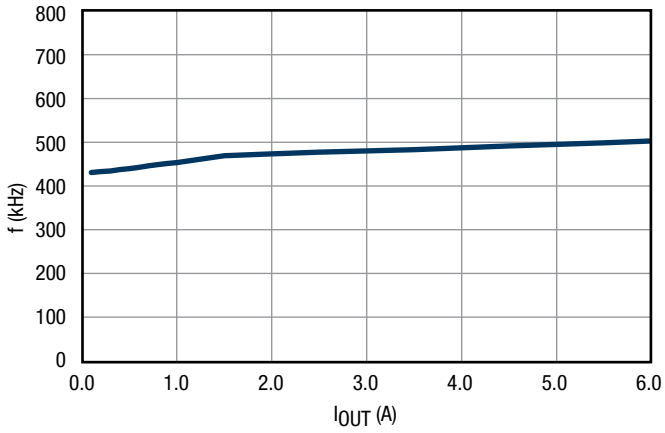


Figure 7. Switching Frequency vs. I_{OUT}

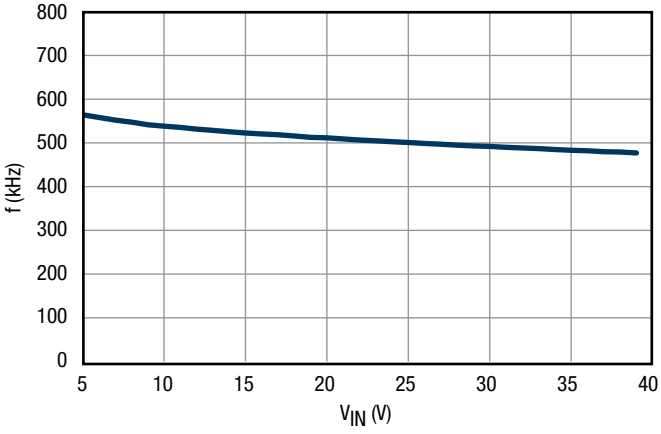


Figure 8. Switching Frequency vs. V_{IN}

Typical Performance Characteristics (Continued)

T_A = 25°C, V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 6A, f = 500kHz, unless otherwise specified. Schematic shown in Figure 27.

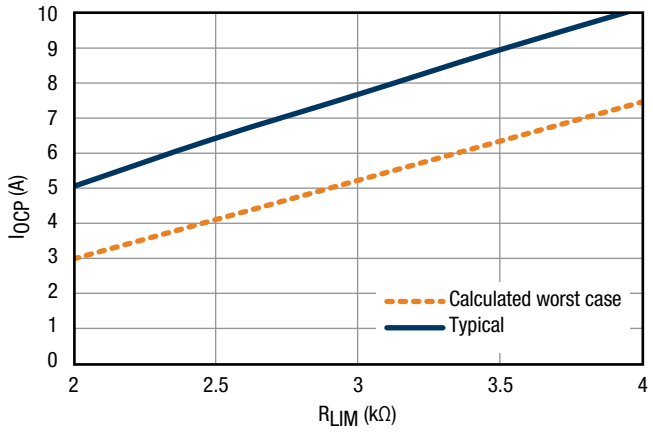


Figure 9. I_{OCP} vs. R_{LIM}

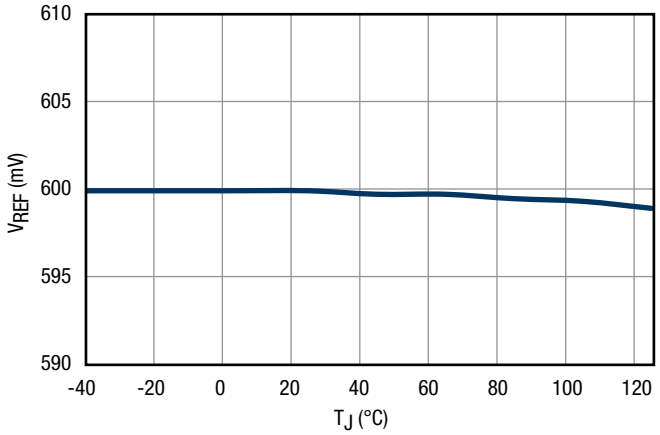


Figure 10. V_{REF} vs. Temperature

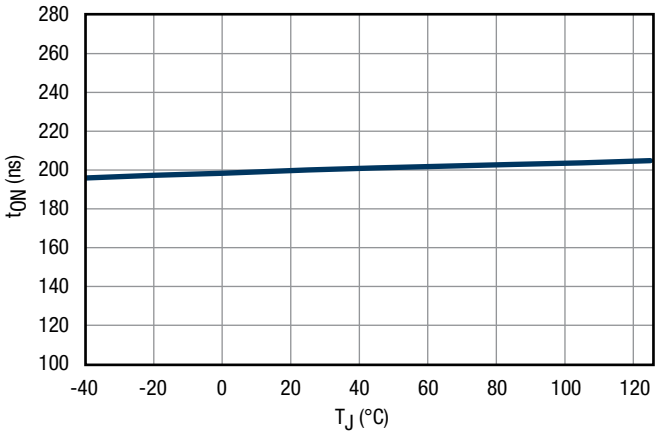


Figure 11. t_{ON} vs. Temperature, R_{ON} = 14kΩ

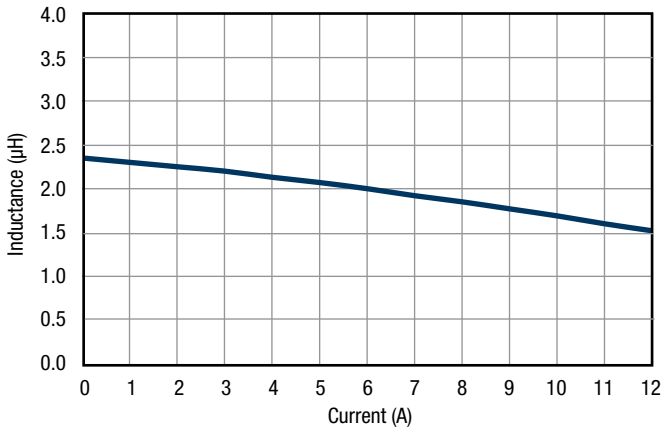


Figure 12. Inductance vs. Current

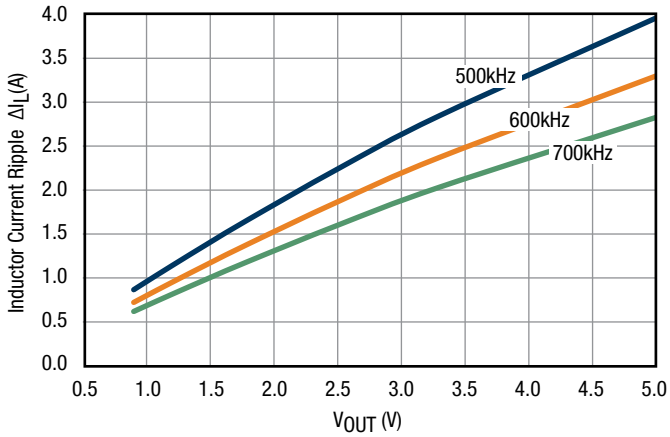


Figure 13. Inductor Current Ripple vs. V_{OUT}

Typical Performance Characteristics (Continued)

T_A = 25°C, V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 6A, f = 500kHz, unless otherwise specified. Schematic shown in Figure 27.

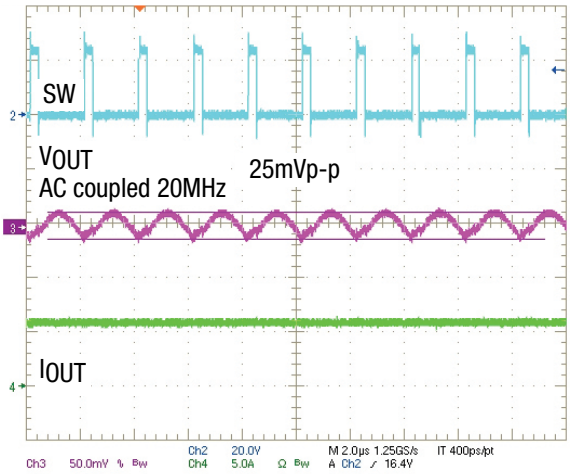


Figure 14. Steady State CCM, I_{OUT} = 6A

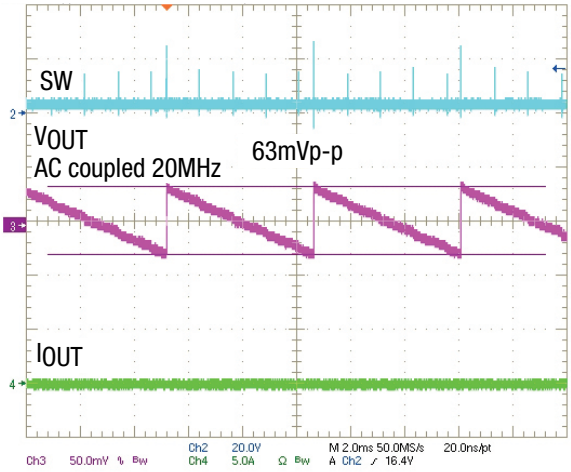


Figure 15. Steady State DCM, I_{OUT} = 0A

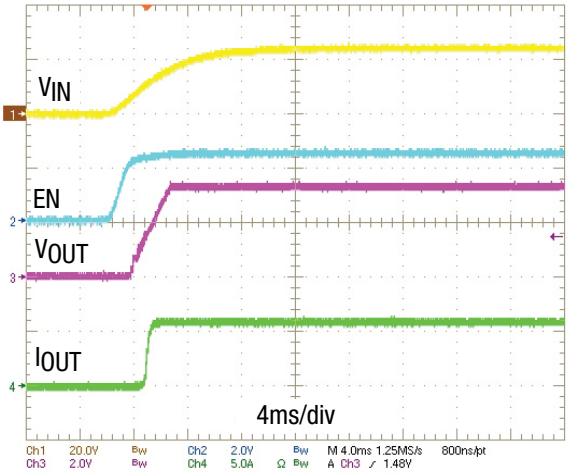


Figure 16. Power Up, I_{OUT} = 6A

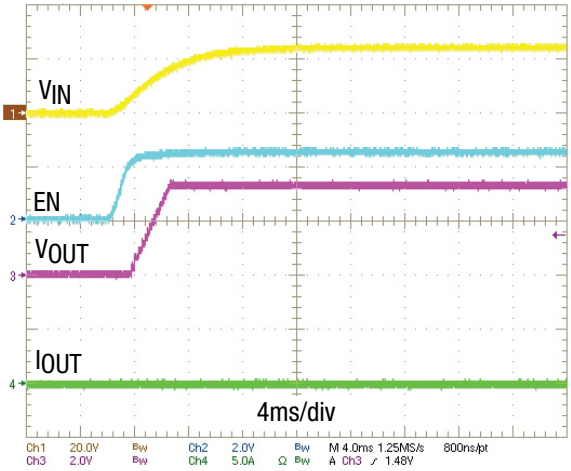


Figure 17. Power Up, I_{OUT} = 0A

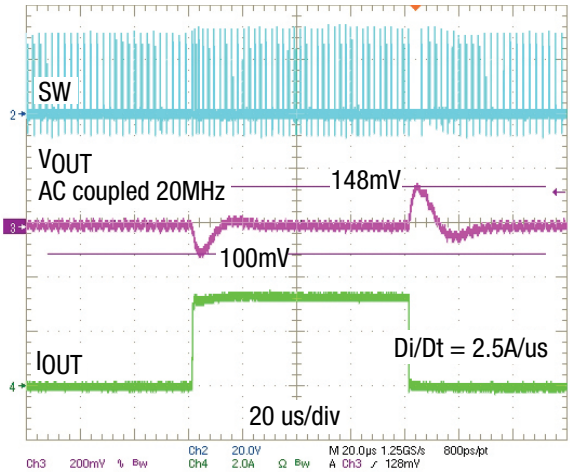


Figure 18. Load Step, CCM, 0A-3A-0A

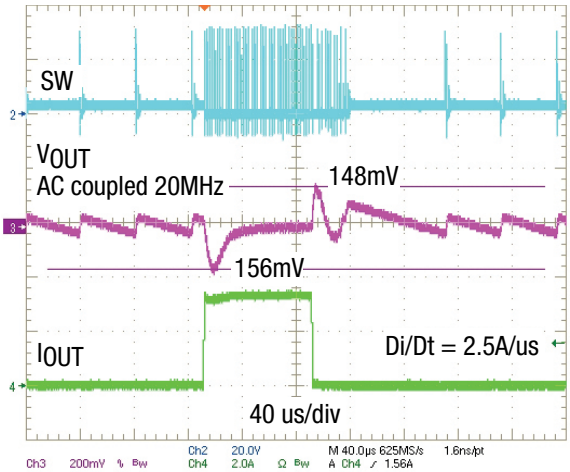


Figure 19. Load Step, DCM/CCM, 0.05A-3A-0.05A

Typical Performance Characteristics (Continued)

Efficiency and Package Thermal Derating

T_A = 25°C, No airflow, f = 500kHz, unless otherwise specified. Schematic shown in Figure 27.

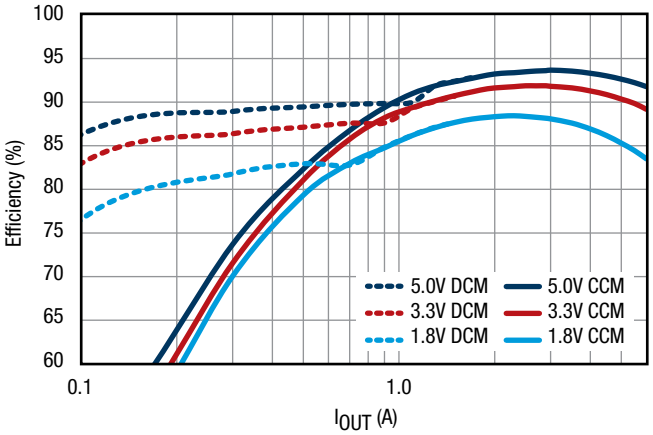


Figure 20. Efficiency, V_{IN} = 12V

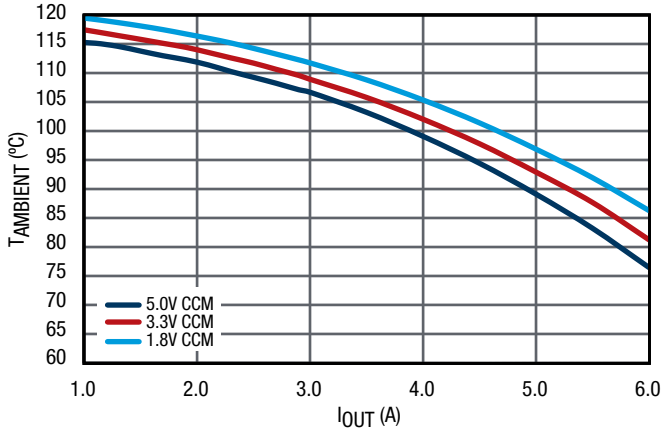


Figure 21. Maximum $T_{AMBIENT}$ vs. I_{OUT}, V_{IN} = 12V

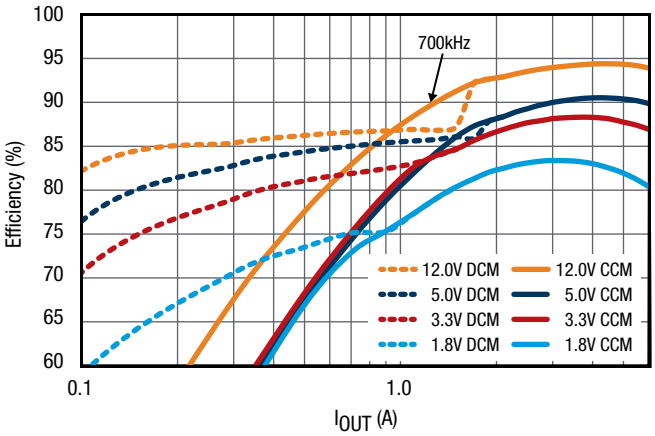


Figure 22. Efficiency, V_{IN} = 24V

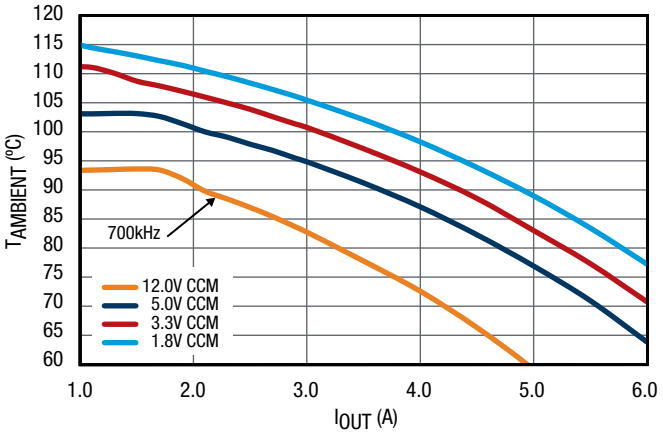


Figure 23. Maximum $T_{AMBIENT}$ vs. I_{OUT}, V_{IN} = 24V

Functional Block Diagram

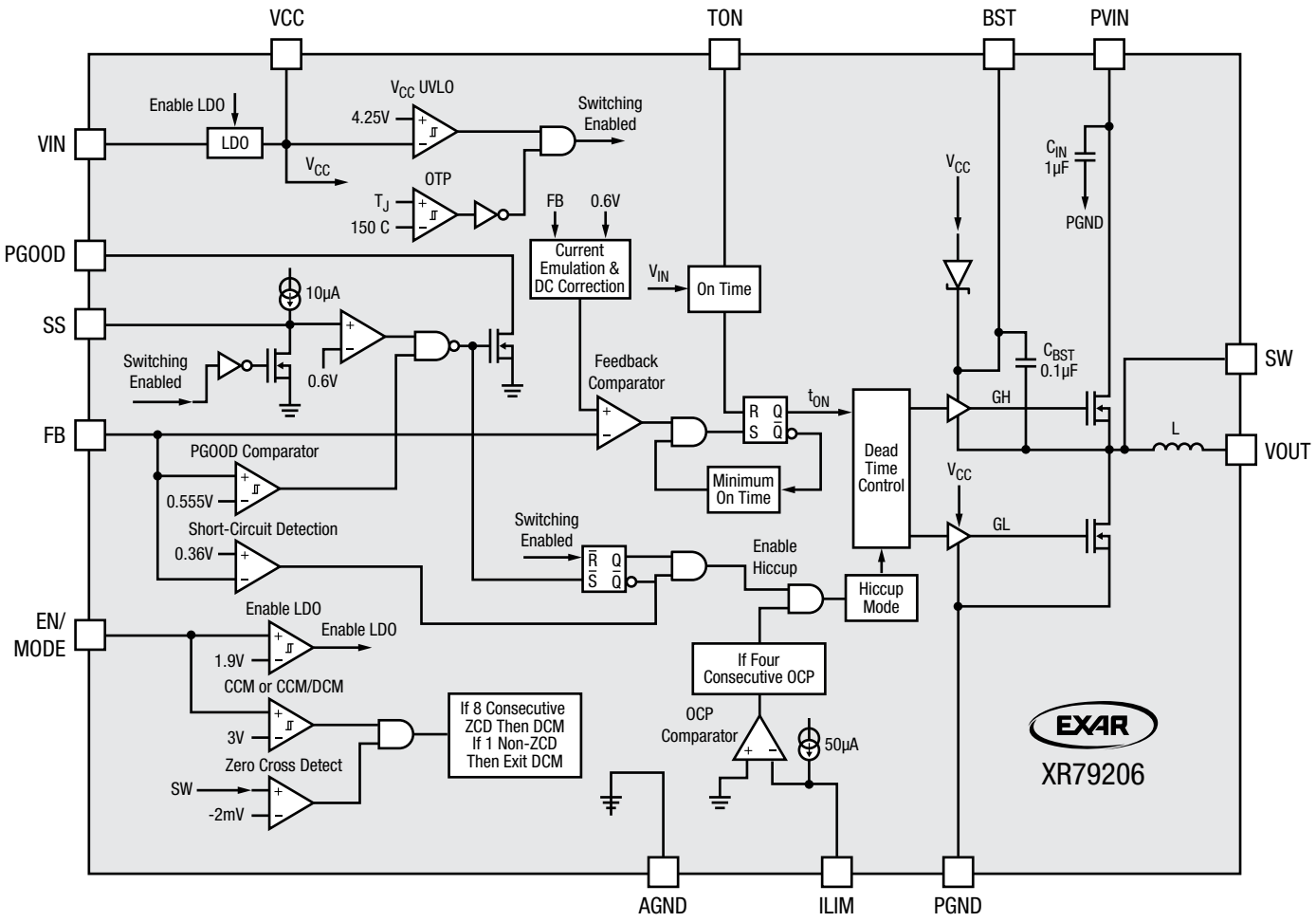


Figure 24. Functional Block Diagram

Applications Information

Functional Description

XR79206 is a synchronous step-down proprietary emulated current-mode Constant On-Time (COT) module. The on-time, which is programmed via R_{ON}, is inversely proportional to V_{IN} and maintains a nearly constant frequency. The emulated current-mode control is stable with ceramic output capacitors.

Each switching cycle begins with GH signal turning on the high-side (switching) FET for a preprogrammed time. At the end of the on-time, the high-side FET is turned off and the low-side (synchronous) FET is turned on for a preset minimum time (250ns nominal). This parameter is termed minimum off-time. After the minimum off-time, the voltage at the feedback pin FB is compared to an internal voltage ramp at the feedback comparator. When V_{FB} drops below the ramp voltage, the high-side FET is turned on and the cycle repeats. This voltage ramp constitutes an emulated current ramp and makes possible the use of ceramic capacitors, in addition to other capacitor types, for output filtering.

Enable/Mode Input (EN/MODE)

EN/MODE pin accepts a tri-level signal that is used to control turn on/off. It also selects between two modes of operation: forced CCM and DCM/CCM. If EN is pulled below 1.8V, the module shuts down. A voltage between 2.0V and 2.8V selects the forced CCM mode which will run the module in continuous conduction at all times. A voltage higher than 3.1V selects the DCM/CCM mode which will run the module in discontinuous conduction at light loads.

Selecting the Forced CCM Mode

In order to set the module to operate in forced CCM, a voltage between 2.0V and 2.8V must be applied to EN/MODE. This can be achieved with an external control signal that meets the above voltage requirement. Where an external control is not available, the EN/MODE can be derived from V_{IN}. If V_{IN} is well regulated, use a resistor divider and set the voltage to 2.5V. If V_{IN} varies over a wide range, the circuit shown in Figure 25 can be used to generate the required voltage. Note that at V_{IN} of 5.0V and 40V the nominal Zener voltage is 4.0V and 5.0V respectively. Therefore for V_{IN} in the range of 5.0V to 40V, the circuit shown in Figure 25 will generate V_{EN} required for forced CCM.

Selecting the DCM/CCM Mode

In order to set the module operation to DCM/CCM, a voltage between 3.1V and 5.5V must be applied to EN/MODE pin. If an external control signal is available, it can be directly connected to EN/MODE. In applications where an external control is not available, EN/MODE input can be derived from V_{IN}. If V_{IN} is well regulated, use a resistor divider and set the voltage to 4V. If V_{IN} varies over a wide range, the circuit shown in Figure 26 can be used to generate the required voltage for DCM/CCM operation.

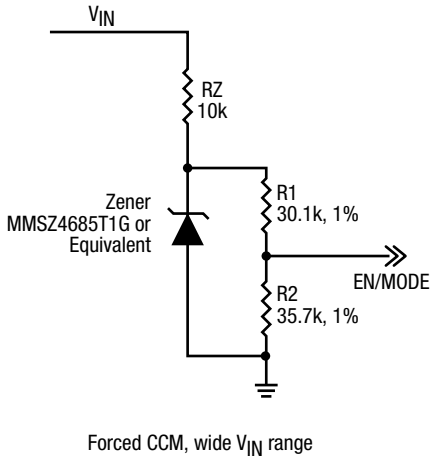


Figure 25. Selecting Forced CCM by Deriving EN/MODE from V_{IN}

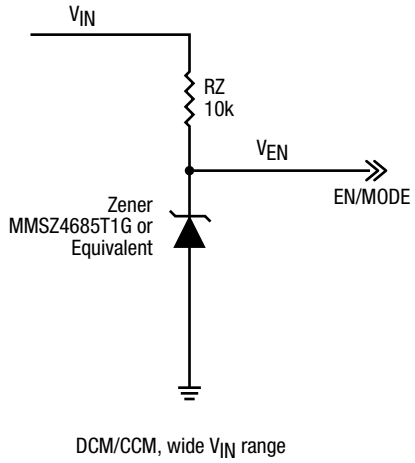


Figure 26. Selecting DCM/CCM by Deriving EN/MODE from V_{IN}

Applications Information (Continued)

Programming the On-Time

The on-time t_{ON} is programmed via resistor R_{ON} according to following equation:

$$R_{ON} = \frac{V_{IN} \times [t_{ON} - (2.5 \times 10^{-8})]}{2.95 \times 10^{-10}}$$

A graph of t_{ON} vs. R_{ON}, using the above equation, is compared to typical test data in Figure 5. The graph shows that calculated data matches typical test data within 3%.

The t_{ON} corresponding to a particular set of operating conditions can be calculated based on empirical data from:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times 1.06 \times f \times Eff.}$$

Where:

- f is the desired switching frequency at nominal I_{OUT}
- Eff. is the converter efficiency corresponding to nominal I_{OUT}

Substituting for t_{ON} in the first equation we get:

$$R_{ON} = \frac{\left(\frac{V_{OUT}}{1.06 \times f \times Eff.}\right) - [(2.5 \times 10^{-8}) \times V_{IN}]}{(2.95 \times 10^{-10})}$$

Now R_{ON} can be calculated in terms of operating conditions V_{IN}, V_{OUT}, f and Eff. using the above equation. At V_{IN} = 24V, f = 500kHz, I_{OUT} = 6A and using the efficiency numbers from Figure 22 we get the following R_{ON}:

V_{OUT} (V)	Eff. (%)	f (kHZ)	R_{ON} (kΩ)
12.0	94	700	56.3
5.0	90	500	33.5
3.3	87	500	22.2
1.8	80	500	12.4

Overcurrent Protection (OCP)

If the load current exceeds the programmed overcurrent threshold I_{OCP} for four consecutive switching cycles, the module enters the hiccup mode of operation. In hiccup mode the MOSFET gates are turned off for 110ms (hiccup timeout). Following the hiccup timeout a soft-start is attempted. If OCP persists, hiccup timeout will repeat. The module will remain in hiccup mode until load current is reduced below the programmed I_{OCP}. In order to program overcurrent protection use the following equation:

$$R_{LIM} = \left[\frac{(I_{OCP} + (0.5 \times \Delta I_L))}{\left(\frac{I_{LIM}}{R_{DS}}\right)}\right] + 0.16k\Omega$$

Where:

- R_{LIM} is resistor value in kΩ for programming I_{OCP}
- I_{OCP} is the overcurrent value to be programmed
- ΔI_L is the peak-to-peak inductor current ripple
- I_{LIM}/R_{DS} = 2.4µA/mΩ is the minimum value of the parameter specified in the tabulated data
- 0.16kΩ accounts for OCP comparator offset

The above equation is for worst-case analysis and safeguards against premature OCP. Typical value of I_{OCP}, for a given R_{LIM}, will be higher than that predicted by the above equation. Graph of calculated I_{OCP} vs. R_{LIM} is compared to typical I_{OCP} in Figure 9.

Short-Circuit Protection (SCP)

If the output voltage drops below 60% of its programmed value, the Module will enter hiccup mode. Hiccup will persist until short-circuit is removed. SCP circuit becomes active after PGOOD asserts high.

Over Temperature Protection (OTP)

OTP triggers at a nominal controller temperature of 150°C. The gate of switching FET and synchronous FET are turned off. When controller temperature cools down to 135°C, soft-start is initiated and operation resumes.

Applications Information (Continued)

Programming the Output Voltage

Use an external voltage divider as shown in Figure 27 to program the output voltage V_{OUT}.

$$R_{FB1} = R_{FB2} \times \left(\frac{V_{OUT}}{0.6V} - 1 \right)$$

Where R_{FB2} has a nominal value of 2kΩ.

Programming the Soft-Start

Place a capacitor C_{SS} between the SS and AGND pins to program the soft-start. In order to program a soft-start time of t_{SS}, calculate the required capacitance C_{SS} from the following equation:

$$C_{SS} = t_{SS} \times \frac{10\mu A}{0.6V}$$

Feed-Forward Capacitor (C_{FF})

The feed-forward capacitor C_{FF} is used to set the necessary phase margin when using ceramic output capacitors. Calculate C_{FF} from the following equation:

$$C_{FF} = \frac{1}{2 \times \pi \times R_{FB1} \times 5 \times f_{LC}}$$

Where f_{LC}, the output filter double-pole frequency is calculated from:

$$f_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

You must use manufacturer's DC derating curves to determine the effective capacitance corresponding to V_{OUT}. A load step test and/or a loop frequency response test should be performed and if necessary C_{FF} can be adjusted in order to get a critically damped transient load response.

In certain conditions an alternate compensation scheme may need to be employed using ripple injection from the inductor. An application note is being developed to provide more information about this compensation scheme.

Feed-Forward Resistor (R_{FF})

R_{FF}, in conjunction with C_{FF}, functions similar to a high frequency pole and adds gain margin to the frequency response. Calculate R_{FF} from:

$$R_{FF} = \frac{1}{2 \times \pi \times f \times C_{FF}}$$

Where f is the switching frequency.

If R_{FF} >0.02 x R1 then calculate R_{FF} value from R_{FF} = 0.02 x R1.

Maximum Allowable Voltage Ripple at FB Pin

Note that the steady-state voltage ripple at feedback pin FB ($V_{FB,RIPPLE}$) must not exceed 50mV in order for the module to function correctly. If $V_{FB,RIPPLE}$ is larger than 50mV then C_{OUT} should be increased as necessary in order to keep the $V_{FB,RIPPLE}$ below 50mV.

Applications Information (Continued)

Typical Application Circuit

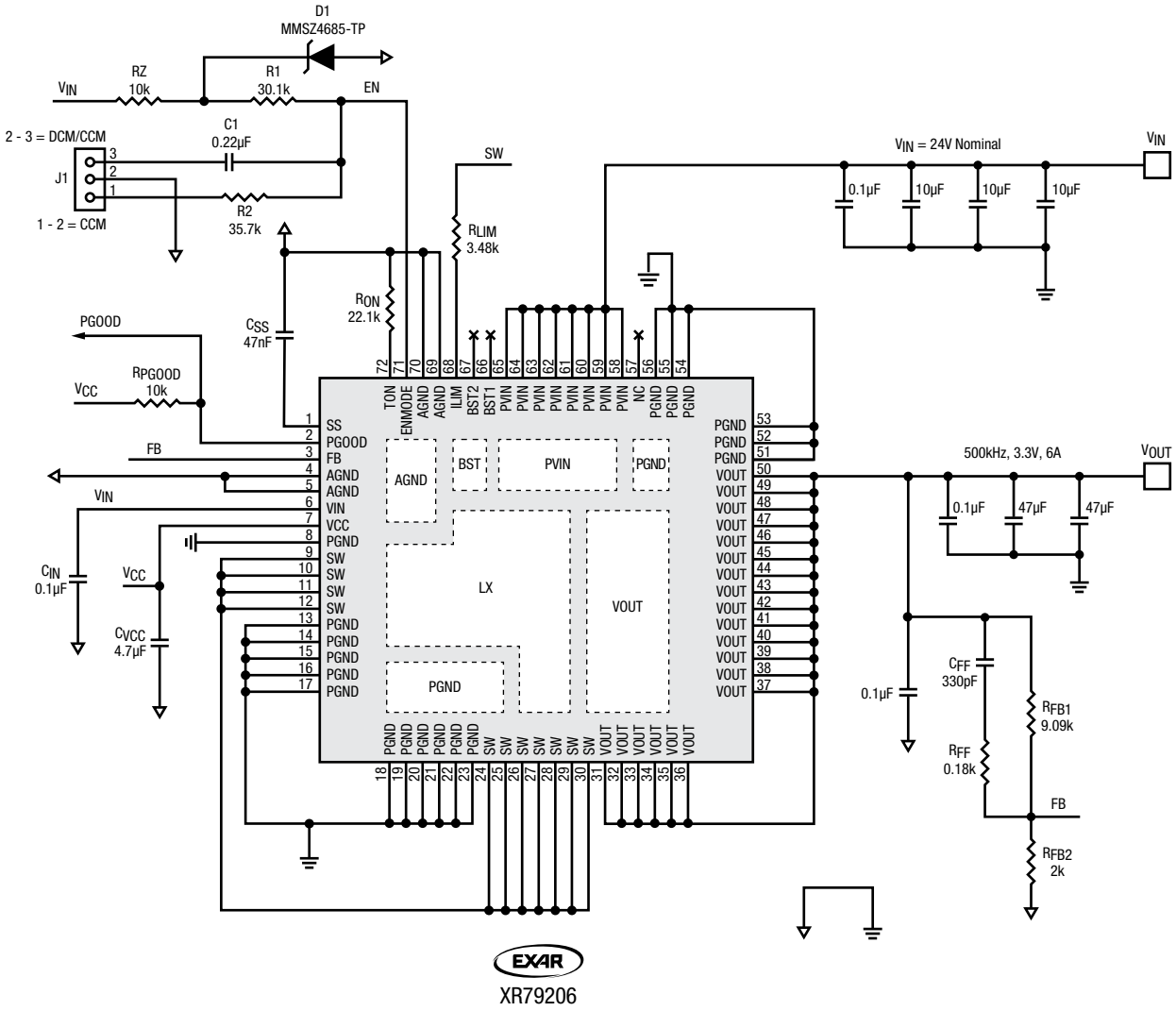
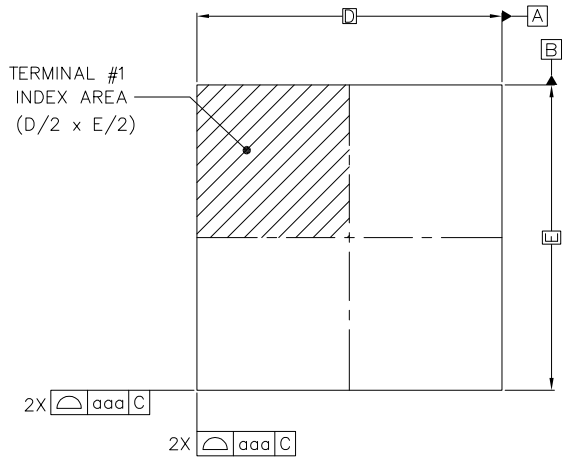


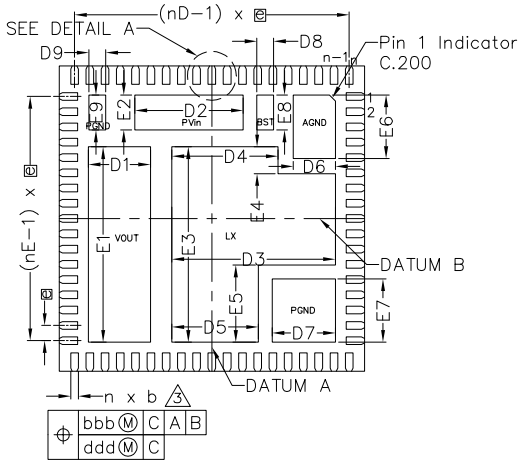
Figure 27. Application Circuit

Package Description

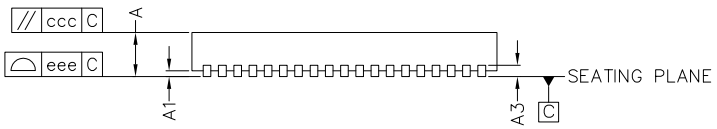
TOP VIEW



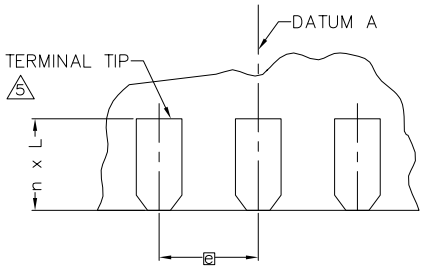
BOTTOM VIEW



SIDE VIEW



DETAIL A

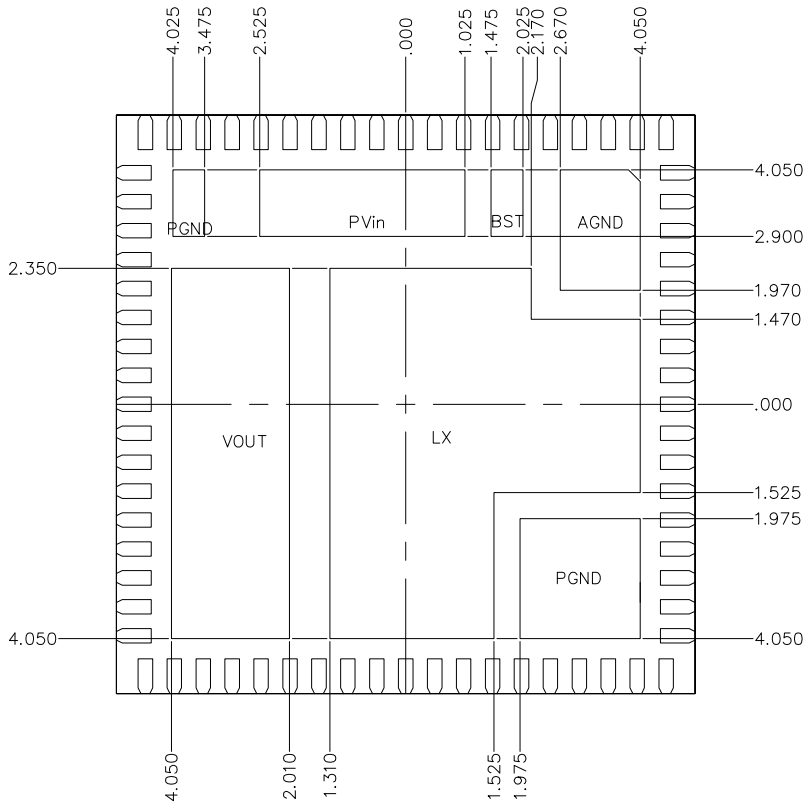


PACKAGE	72L 10x10 SIP-LPCC			
REF.	MIN.	NOM.	MAX.	
A	3.90	4.00	4.10	
b	0.20	0.25	0.30	5
L	0.50	0.60	0.70	
D		10.00 BSC		
D1	1.94	2.04	2.14	
D2	3.45	3.55	3.65	
D3	5.26	5.36	5.46	
D4	3.38	3.48	3.58	
D5	2.735	2.835	2.935	
D6	1.28	1.38	1.48	
D7	1.975	2.075	2.175	
D8	0.45	0.55	0.65	
D9	0.45	0.55	0.65	
E		10.00 BSC		
E1	6.30	6.40	6.50	
E2	1.05	1.15	1.25	
E3	6.30	6.40	6.50	
E4	0.78	0.88	0.98	
E5	2.425	2.525	2.625	
E6	1.98	2.08	2.18	
E7	1.975	2.075	2.175	
E8	1.05	1.15	1.25	
E9	1.05	1.15	1.25	
e		0.50 BSC		
n		72		3
nD		19		
nE		17		

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A1	0	0.02	0.05	
A3		0.20 REF.		
TOLERANCES OF FORM AND POSITION				
aaa		0.10		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		

Package Description (Continued)

TERMINAL AND PAD EDGE DETAILS

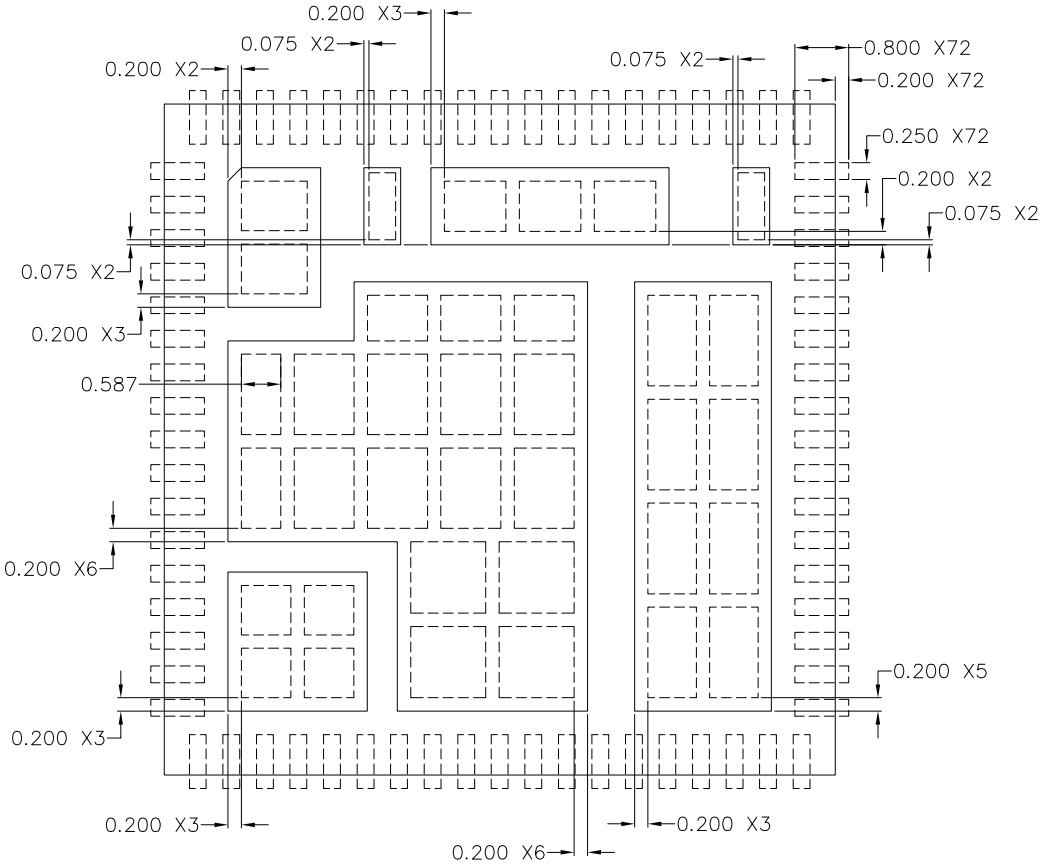


NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. n IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC PUBLICATION 95 SPP–002. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. nD AND nE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. TOLERANCE FOR EXPOSED DAP EDGE LOCATION DIMENSION IN PAGE 2 IS +/–0.1MM.
9. DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OR CUTTING BURR

Package Description (Continued)

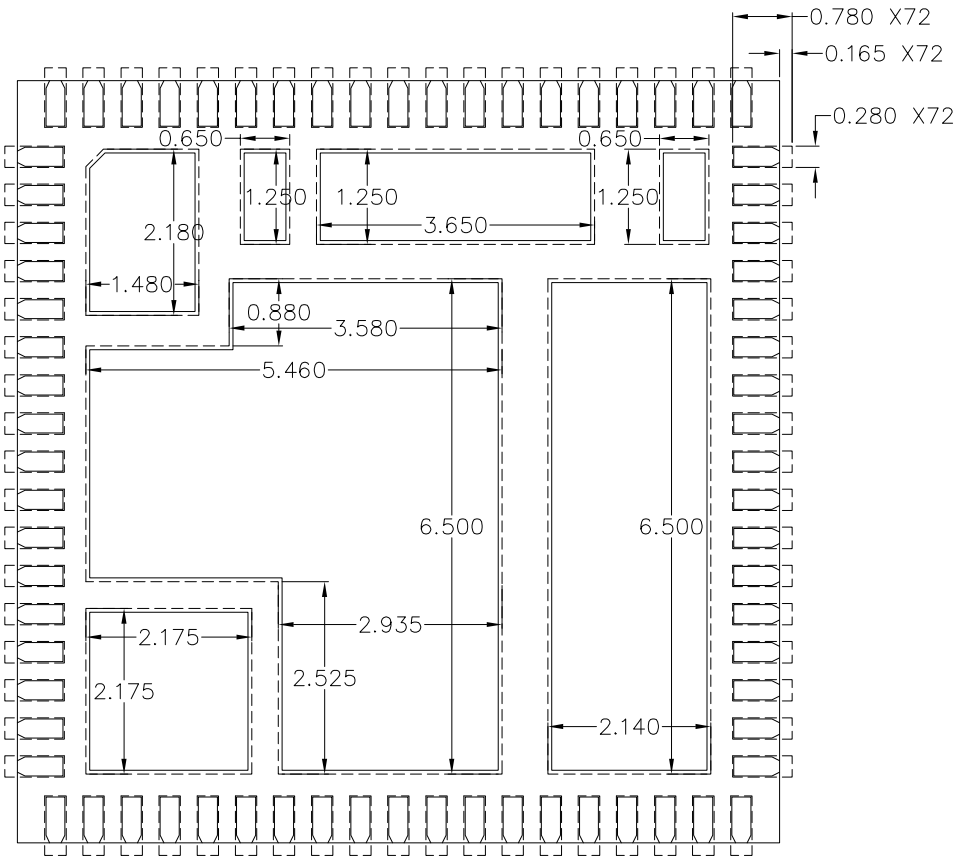
RECOMMENDED STENCIL DESIGN



NOTE: Dashed line refers to solder stencil opening.

Package Description (Continued)

RECOMMENDED LAND PATTERN



NOTE: Dashed line refers to land pattern.

Ordering Information

Part Number	Operating Temperature Range	Environmental Rating	Package	Packaging Quantity	Marking
XR79206EL-F	-40°C ≤ T_J ≤ 125°C	RoHS	10mm x 10mm x 4mm QFN package	Tray	XR79206EL YYWWF XXXXXXXX
XR79206EVB	XR79206 evaluation board				

NOTE:
YY = Year, WW = Work Week, F = Lead Free and Halogen Free, XXXXXXXX = Lot Number.

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