XR829MQ Module Datasheet

Single-Chip IEEE 802.11 b/g/n WLAN, Bluetooth 2.1/4.0/4.1

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1 Introduction

XR829MQ product is designed base on XR829 chipset .It is a fully integrated SoC to support 2.4G WLAN 802.11 b/g/n and Bluetooth 2.1+EDR/4.1. It is optimized for mobile applications such as PDAs and portable media players. High sensitivity and transmitting power ensure long distance and robust connection. Highest level of integration allows very compact and cost effective reference designs delivering fast time-to-market for new WLAN and Bluetooth enabled products.

2 Features

2.1 WLAN Features

- Compatible with IEEE 802.11 b/g/n standard
- 802.11n support for 20/40MHz bandwidth
- Support for Short Guard Interval
- Support for 802.11n MCS0~MCS7
- 6M~54M data rate for 802.11g
- DSSS, CCK modulation with long and short preamble
- Support frame aggregation using A-MSDU, A-MPDU
- Supports MAC enhancements including
  - 802.11d - Regulatory domain operation
  - 802.11e - QoS including WMM
  - 802.11h - Transmit power control dynamic and frequency selection
  - 802.11i - Security including WPA2 and WAPI compliance
  - 802.11r - Roaming
  - 802.11w - Management frame protection
- Support for Station, SoftAP and P2P mode
- Support for Wi-Fi Direct

2.2 Bluetooth Features

- Bluetooth Dual Mode support with 2.1/4.0/4.1
- Class 1, Class 2 and Class 3 transmitter operation
- Host Controller Interface using a high-speed UART, maximum baud rate of 4 Mbps
- Adaptive Frequency Hopping
- SCO and eSCO support
- 1, 3 and 5 slots all packet types support
- Audio interfaces: PCM, I2S
- Transcoders for A-law, μ-law and CVSD voice over air

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- Piconet and scatternet support
- Secure simple pairing
- Sniff/Hold/Sniff-Sub-rating low power mode support

3 Applications

- Tablet PC
- Smart internet TV box
- Portable media player(PMP)
- Portable gaming device(PGD)
- Internet of Thing (IOT)

4 Product appearance

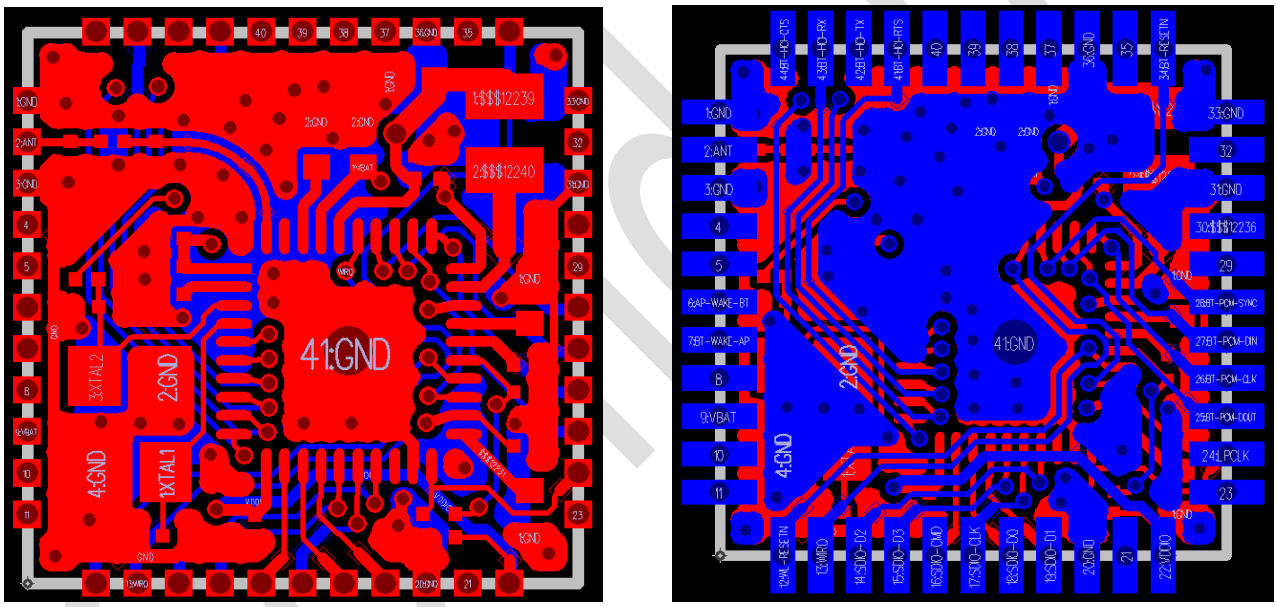

Figure 4-1 XR829MQ Top and Bottom View

5 Pin Assignments

5.1 Pin Outline

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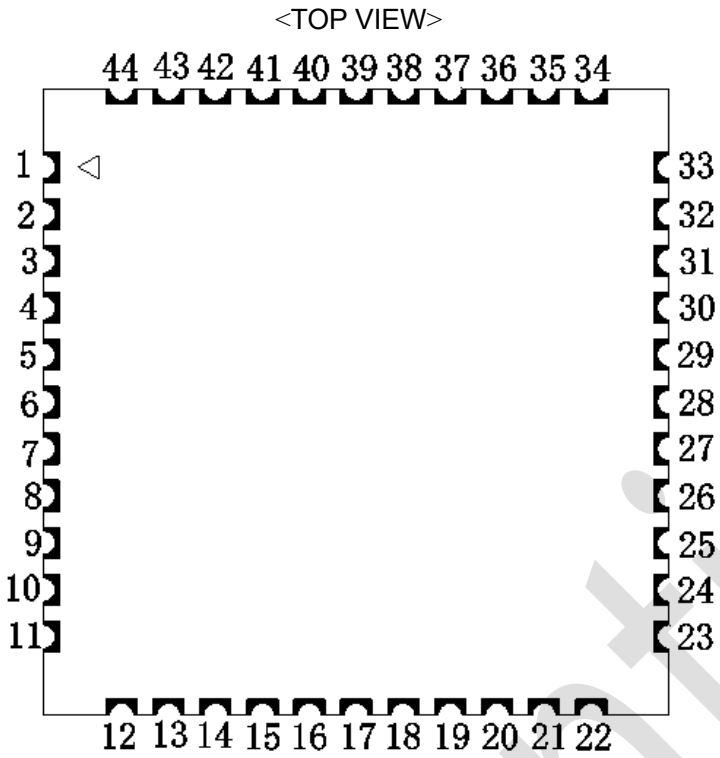

Figure 5-1 XR829MQ Pin Outline

5.2 Pin Definition

Table 5-1 XR829MQ Pin List

Pin	Name	Type	Description
1	GND1	-	Ground connetctions
2	ANT	I/O	2.4 GHz RF input/output
3	GND2	-	Ground connetctions
4	NC1	-	Floating(Don’t connected to ground)
5	NC2	-	Floating(Don’t connected to ground)
6	BT-WAKE	I	Host wakes up Bluetooth subsystem
7	BT-HOST-WAKE	O	Bluetooth subsystem wakes up host
8	NC3	-	Floating(Don’t connected to ground)
9	VBAT	P	Supply for on-chip-PMU
10	NC4	-	Floating(Don’t connected to ground)
11	NC5	-	Floating(Don’t connected to ground)
12	WL-REG-ON	I	WLAN Reset, active low
13	WL-HOST-WAKE	O	WLAN interrupt request
14	SDIO-DATA2	I/O	SDIO data line2
15	SDIO-DATA3	I/O	SDIO data line3
16	SDIO-DATA-CMD	I/O	SDIO command line

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17	SDIO-DATA-CLK	I	SDIO clock line
18	SDIO-DATA-DATA0	I/O	SDIO data line0
19	SDIO-DATA-DATA1	I/O	SDIO data line1
20	GND3	-	Ground connetctions
21	NC6	-	Floating(Don't connected to ground)
22	VDDIO	P	Supply for IO
23	NC7	-	Floating(Don't connected to ground)
24	LPO	I	Low power clock input, 32.768 kHz, or be grounded
25	PCM-OUT	O	Bluetooth PCM data output
26	PCM-CLK	I/O	Bluetooth PCM clock
27	PCM-IN	I	Bluetooth PCM data input
28	PCM-SYNC	I/O	Bluetooth PCM synchronization control
29	NC8	-	Floating(Don't connected to ground)
30	TCXO-IN	I	Reference clock input or XTAL inputs
31	GND4	-	Ground connetctions
32	NC9	-	Floating(Don't connected to ground)
33	GND5	-	Ground connetctions
34	BT-RST-N	I	Bluetooth Reset, active low
35	NC10	-	Floating(Don't connected to ground)
36	GND6	-	Ground connetctions
37	NC11	-	Floating(Don't connected to ground)
38	NC12	-	Floating(Don't connected to ground)
39	NC13	-	Floating(Don't connected to ground)
40	NC14	-	Floating(Don't connected to ground)
41	UART-RTS-N	O	Bluetooth Uart RTS
42	UART-TXD	O	Bluetooth Uart transmit
43	UART-RXD	I	Bluetooth Uart receive
44	UART-CTS-N	I	Bluetooth Uart CTS

6 General Specification

6.1 General Specification

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Table 6-1 XR829MQ Module general Specification

Item	Description
Product Name	XR829MQ
Major Chipset	XR829
Product Description	Support WiFi/Bluetooth functionalities
Dimension(L*W*H)	12 x12x 1.5mm (LxWxH) ； Tolerance: +-0.1mm
Working Temperature	-40°C ~ +85°C
Storage temperature	-55°C ~ +125°C

6.2 Voltages

6.2.1 Absolute Maximum Ratings

Table 6-2 Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
VBAT	Power supply for module	-0.3	5.8	V
VDDIO	IO power supply	-0.3	4.0	V

6.2.2 Recommended Operating Rating

The module requires two power supplies:VBAT and VDDIO

Table 6-3 Recommended Operating Rating

Symbol	Parameter	Min	Typ	Max	Unit
VBAT	Power supply for module	2.7	3.6	5.5	V
VDDIO	IO power supply	1.62	3.3	3.6	V

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7 Clocks

XR829 uses a reference clock and a low power clock.

For the reference clock, XR829 can either use an external reference clock source or generate its own reference using a XTAL and a built-in oscillator.

For the low power clock, XR829 can either use an external 32.768 KHz clock or generate its internal RCOSC. If use internal RCOSC, the LPCLK pin should be grounded. The low power clock is used during power save modes and used only for power controller module .

7.1 Reference Clock

Table 7-1 External Reference Clock Specifications

Symbol	Parameter	Min	Typ	Max	Unit
F_{IN}	Clock input frequency list using an external clock source	13	24	52	MHz
	Clock input frequency list using a XTAL and the built-in oscillator	19.2	24	52	MHz
F_{INTOL}	Tolerance on input frequency without trimming	-20	-	+20	ppm
T_{stable}	Clock stabilization time	-	-	10	ms
I_{LEAK}	Input leakage current, both for analog and digital	-	-	1	uA

Clock frequency detection

An integrated automatic detection algorithm detects the reference clock frequency using the low power clock after a hardware reset.

Clock source detection

An integrated automatic detection mechanism detects the clock source from the connections of the XTAL1 and XTAL2 pins:

• When an external reference clock source is used, the clock input pin is XTAL2. The XR829 supports both an analog and digital source. An analog source shall be AC coupled to XTAL2 while a digital source shall be DC coupled to XTAL2. In both cases, XTAL1 shall be DC grounded.

• When a XTAL and the built-in oscillator are used, the XTAL shall be DC coupled to XTAL1 and XTAL2.

External Clock Source

• Requirements

Table 7-2 External Clock Requirements

Symbol	Parameter	Min	Typ	Max	Unit
AC coupled signal					
F_{IN}	Frequency	13	24	52	MHz
V_{APP}	Peak-to-peak voltage range of the AC coupled analog input	0.4	0.5	1.2	Vpp
N_H	Total harmonic content of the input signal	-	-	-25	dBc

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DC coupled signal					
V_{IL}	input low voltage on XTAL2	0	-	0.3*V18	V
V_{IH}	input low voltage on XTAL2	0.7*V18	-	V18	V
T_r/T_f	10%-90% rise and fall time	-	-	5	ns
Duty cycle	Cycle-to-cycle	40	50	60	%
Both analog and digital signals					
Z_{INRE}	Real part of parallel AC input impedance at the pin	30	-	-	KOhm
Z_{INIM}	Imaginary part of parallel AC input impedance at the pin	-	3.5	5	pF
Z_{DC}	DC input impedance	1	-	-	MOhm
Phase noise	Ref clock @ 24 MHz, 2.4 GHz 802.11b/g/n operation @1 kHz @10 kHz @100 kHz @1 MHz	-	-	 -123 -133 -138 -138	dBc/Hz

External XTAL and Built-in Oscillator

Table 7-3 External Crystal Characteristics Requirements

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range		13	-	52	MHz
ESR		-	-	60	Ohm
C_{in_xtal}(1)	Single-ended	3.5	18	36	pF
Load capacitance(1)		-	16	27	pF
Oscillator tuning range(2)		+/-20	+/-50	+/-70	ppm
Crystal frequency accuracy at nominal temperature	25 °C	-10	-	+10	ppm
Crystal drift due to temperature	-20 °C to +85 °C	-10	-	+10	ppm
Crystal pull ability		10	-	150	ppm/pF

(1). The load capacitance value (C_{load}) depends on XTAL model, XTAL1 and XTAL2 pin have extra capacitance(C_{in_xtal}), so external added load capacitance value $C_{load\_ext}=C_{load}-C_{in\_xtal}$. C_{in_xtal} has tuning range about 7pF, which is controlled by software, for details please go to software user manual.

(2). Tuning range depends on XTAL load capacitance requirement, typical case is based on 26MHz XTAL, 8pF C_{load}.

7.2 Low Power Clock

Table 7-4 Low Power Clock Specifications

Symbol	Parameter	Min	Typ	Max	Unit

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F_{IN}	Frequency	-	32.768	-	KHz
F/F_{IN}	Frequency accuracy	-250	-	+250	ppm
Duty cycle		30	-	70	%
Jitter	Cycle-to-cycle	-40	-	+40	ns
R_{in}	Input resistance	1	-	-	MOhm
C_{in}	Input capacitance	-	-	5	pF
V_{IL}	Input low voltage on LPCLK	0	-	0.4	V
V_{IH}	Input high voltage on LPCLK	VDD_IO- 0.4	-	VDD_IO	V

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8 WLAN Specification

Conditions：VBAT=3.6V; VDDIO=3.3V; Temp:25° C

Table 8-1 Wi-Fi RFSpecification

Parameter	Description	
Host Interface	SDIO 2.0	
Standard	IEEE 802.11b,IEEE 802.11g,IEEE 802.11n	
Frequency range	2.412GHZ~2.484GHZ	
Modulation Type	802.11b：CCK,DQPSK,DBPSK 802.11g/n：64-QAM,16-QAM,QPSK,BPSK	
Data Transfer Rate	1,2,5.5,6,11,12,18,22,24,30,36,48,54,SGI/HT40,65Mbps	
RX Sensitivity (802.11b) @8% PER	1Mbps	PER@-97dBm,typical
	2Mbps	PER@-95dBm,typical
	5.5Mbps	PER@-93dBm,typical
	11Mbps	PER@-90dBm,typical
RX Sensitivity (802.11g) @10% PER	6Mbps	PER@-92dBm,typical
	9Mbps	PER@-92dBm,typical
	12Mbps	PER@-91dBm,typical
	18Mbps	PER@-88dBm,typical
	24Mbps	PER@-86dBm,typical
	36Mbps	PER@-82dBm,typical
	48Mbps	PER@-78dBm,typical
	54Mbps	PER@-76dBm,typical
RX Sensitivity (802.11n,20MHz) @10% PER	MCS0	PER@-91dBm,typical
	MCS1	PER@-87dBm,typical
	MCS2	PER@-85dBm,typical
	MCS3	PER@-83dBm,typical
	MCS4	PER@-79dBm,typical
	MCS5	PER@-75dBm,typical
	MCS6	PER@-74dBm,typical
	MCS7	PER@-72dBm,typical
RX Sensitivity (802.11n,40MHz) @10% PER	MCS0	PER@-89dBm,typical
	MCS1	PER@-87.5dBm,typical
	MCS2	PER@-84.5dBm,typical

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	MCS3	PER@-81.5dBm,typical
	MCS4	PER@-78dBm,typical
	MCS5	PER@-74dBm,typical
	MCS6	PER@-72dBm,typical
	MCS7	PER@-71dBm,typical
Maximum Input Level	802.11b：-10dBM	
	802.11g/n：-20dBM	
TX Power	802.11b/11Mbps ： 16dBm±1.5dB @EVM≦-9dB	
	802.11g/54Mbps ： 15dBm±1.5dB @EVM≦-25dB	
	802.11n/64Mbps：14dBm±1.5dB @EVM≦-28dB	

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9 Bluetooth Specification

Conditions：VBAT=3.6V; VDDIO=3.3V; Temp:25° C

Table 9-1 Bluetooth Specification

Parameter	Description
Host Interface	UART/PCM
Standard	Bluetooth 2.1/4.0/4.1
Frequency range	2.402GHZ~2.480GHZ
Modulation Type	GFSK, π/4-DQPSK,8DPSK,GFSK
RX Sensitivity (BR)	1Mbps GFSK：-91dBm,typical
RX Sensitivity (EDR)	2Mbps π/4-DQPSK：-93dBm,typical
	3Mbps 8DPSK：-85dBm,typical
RX Sensitivity (BLE)	1Mbps GFSK ：-93dBm,typical
TX Power	Class1, Class2, Class3@BR, EDR：-17~7dBm; BLE：7dBm.
Maximum Input Level	1Mbps GFSK：-20dBm
	2Mbps π/4-DQPSK：-20dBm
	3Mbps 8DPSK：-10dBm

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10 Reference design circuit

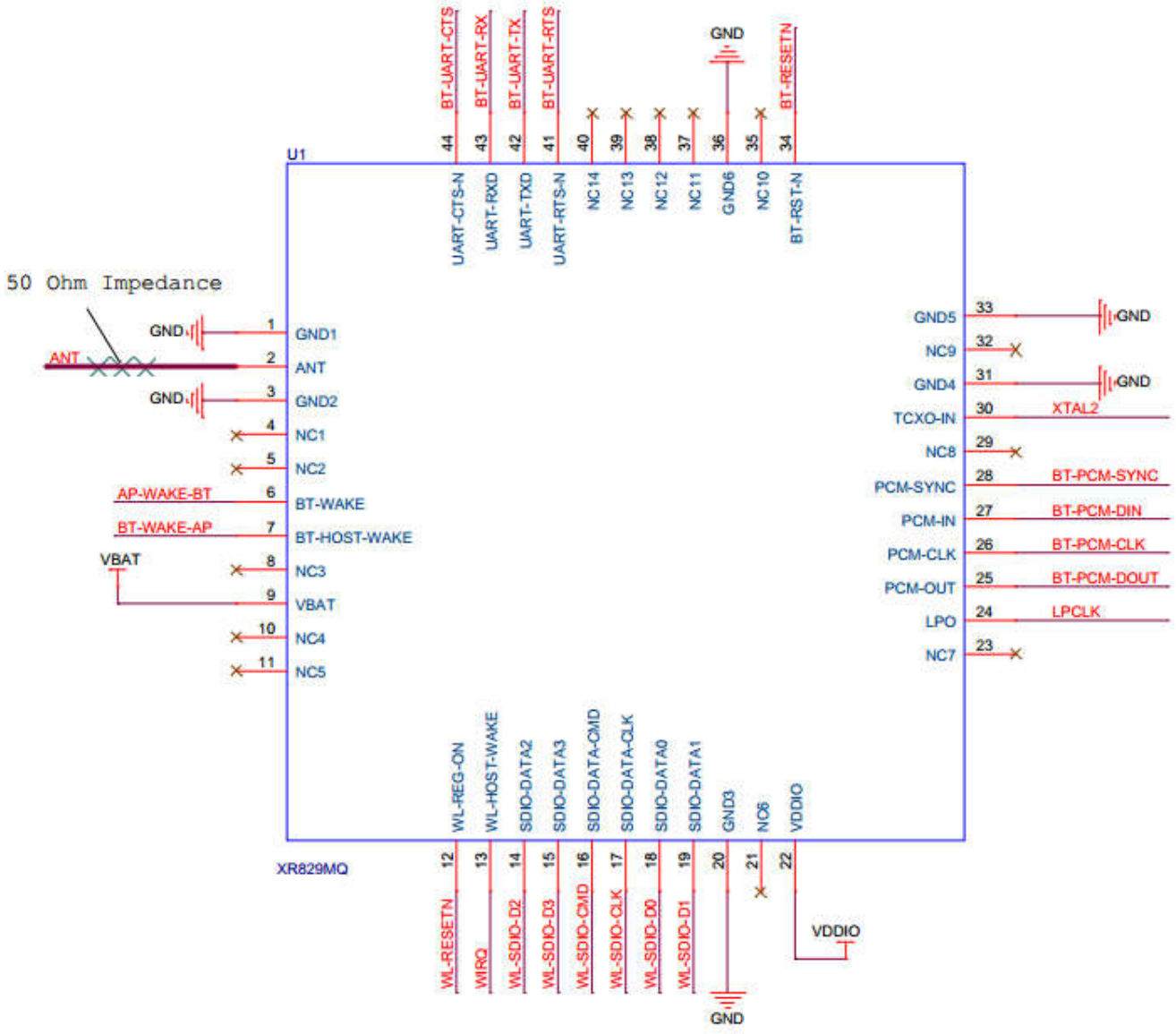

Figure 10-1 Reference design circuit_1

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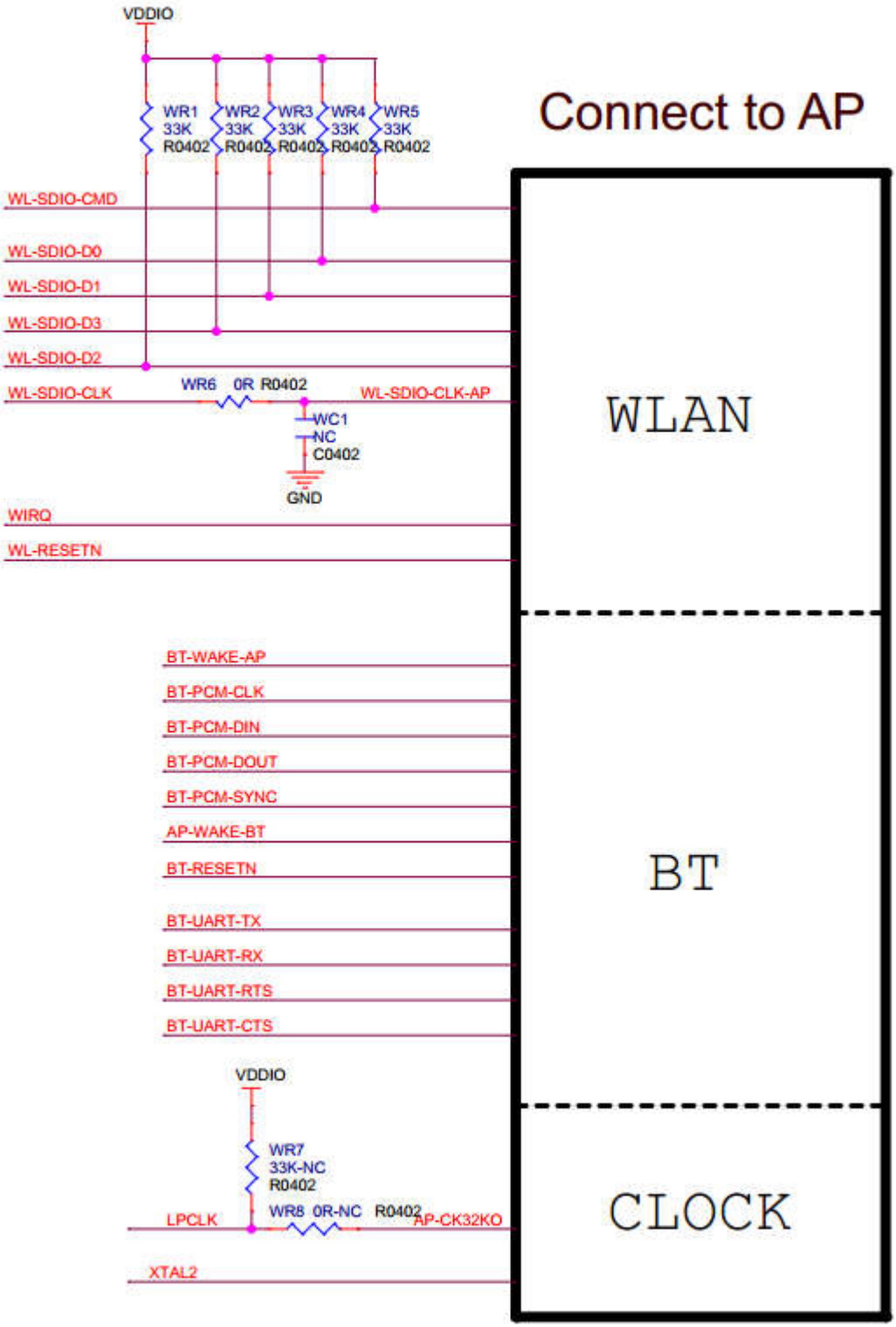

Figure 10-2 Reference design circuit_2

design note:

1、The impedance of ANT line must be 50 ohm.

2、The voltage supplied through the pin VBAT should between 2.7V-5.5V.

3、SDIO line cannot be longer than 150mm.

4、VCCIO voltage to be consistent with the HOST I/O voltage between1.62V-3.6V

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11 Dimensions

11.1 Physical Dimensions

Table 11-1 Physical Dimensions

	Length	Width	Height
Dimensions(mm)	12 (Tolerance:±0.1mm)	12 (Tolerance:±0.1mm)	1.5 (Tolerance:±0.1mm)

(Unit:mm)

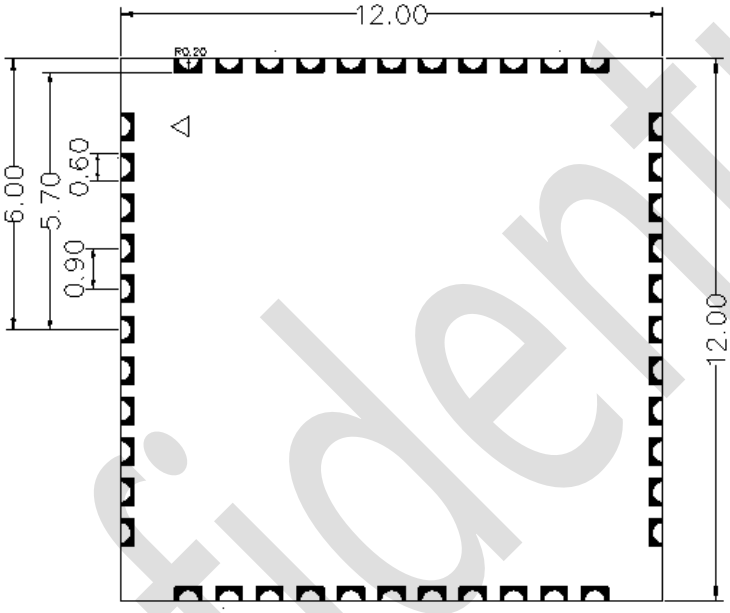

Figure 11-1 XR829MQ Dimensions<TOP VIEW>

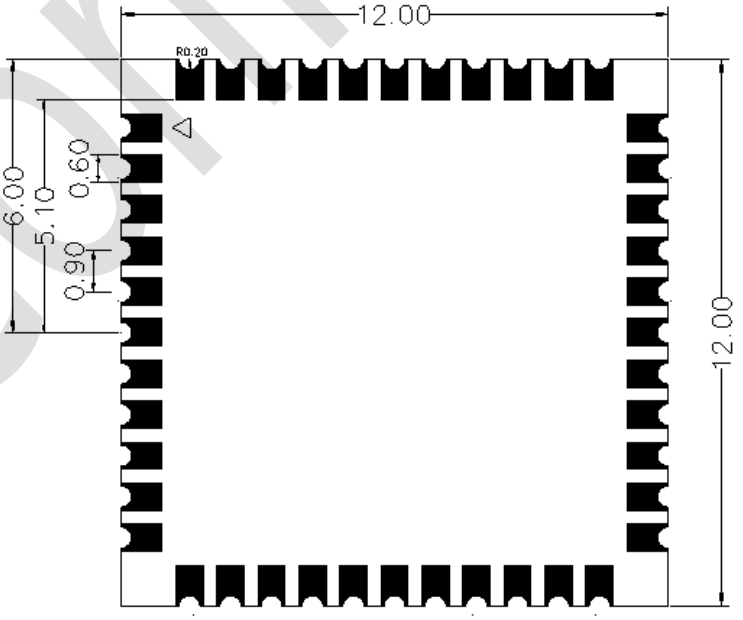

Figure 11-2 XR829MQ Dimensions<Bottom VIEW>

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11.2 Layout Recommendation

(Unit:mm)

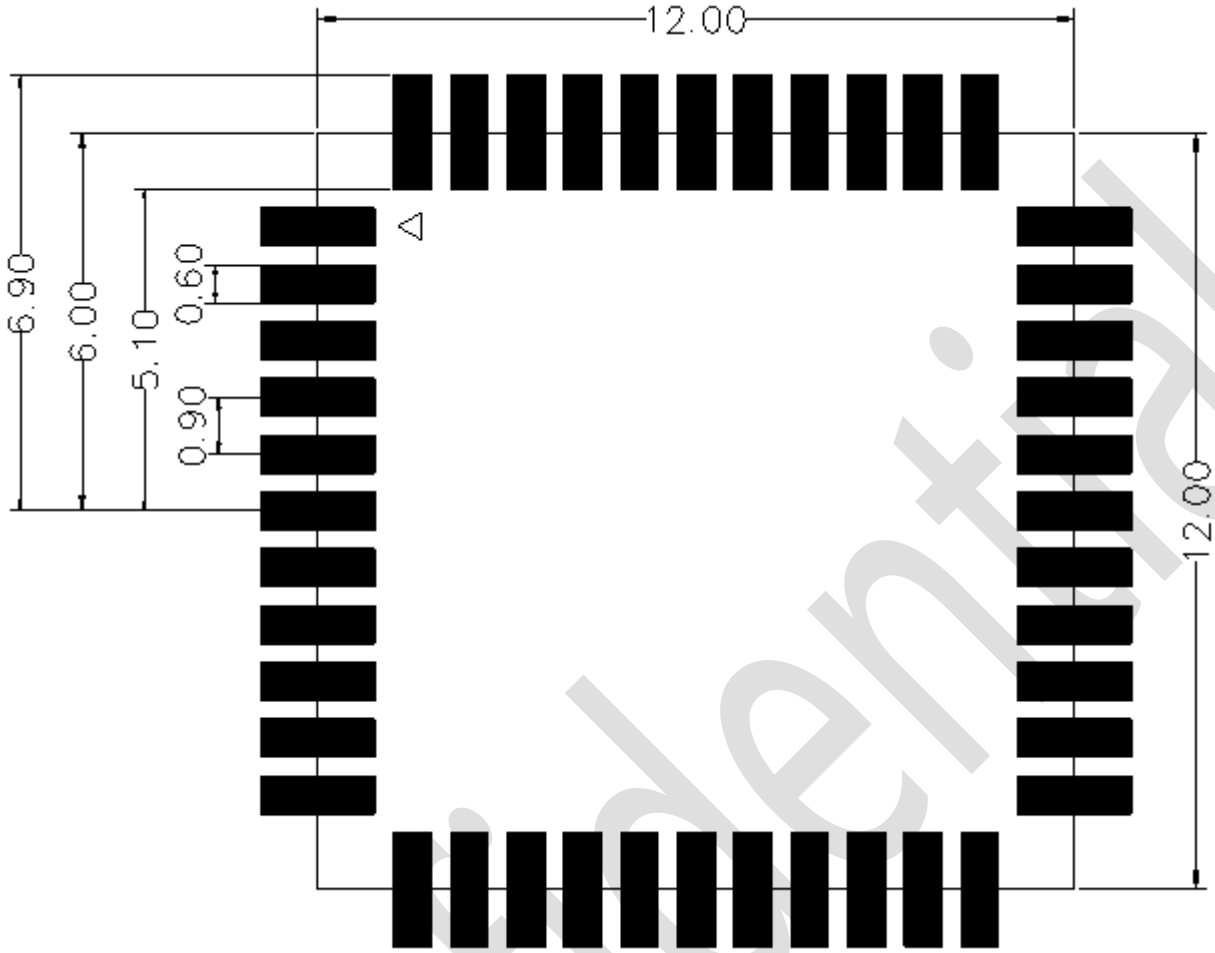

Figure 11-3 XR829MQ layout recommendation<TOP VIEW>

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