



# XRD54L08/L10/L12

3V, Low Power, Voltage Output  
Serial 8/10/12-Bit DAC Family

May 2000-2

## FEATURES

- 8/10/12-Bit Resolution
- Operates from a Single 3V Supply
- Buffered Voltage Output: 13 $\mu$ s Typical Settling Time
- 145 $\mu$ W Total Power Consumption (typ)
- Guaranteed Monotonic Over Temperature
- Flexible Output Range: 0V to  $V_{DD}$
- 8 Lead SOIC and PDIP Package
- Power On Reset
- Serial Data Output for Daisy Chaining

## APPLICATIONS

- Digital Calibration
- Battery Operated Instruments
- Remote Industrial Devices
- Cellular Telephones
- Motion Control
- VXCO Control
- Comparator Level Setting

## GENERAL DESCRIPTION

The XRD54L08/L10/L12 are low power, voltage output digital-to-analog converters (DAC) for +3V power supply operation. The parts draw only 50 $\mu$ A of quiescent current and are available in both an 8-lead PDIP and SOIC package.

The XRD54L08/L10/L12 have a 3 wire serial port with an

output allowing the user to daisy chain several of them together. The serial port will support both Microwire™, SPI™, and QSPI™ standards.

The outputs of the XRD54L08/L10/L12 are set at a gain of +2. The output short circuit current is 7mA typical.

## ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XRD54L08AID	8 Lead 150 Mil JEDEC SOIC	-40°C to +85°C
XRD54L08AIP	8 Lead 300 Mil PDIP	-40°C to +85°C
XRD54L10AID	8 Lead 150 Mil JEDEC SOIC	-40°C to +85°C
XRD54L10AIP	8 Lead 300 Mil PDIP	-40°C to +85°C
XRD54L12AID	8 Lead 150 Mil JEDEC SOIC	-40°C to +85°C
XRD54L12AIP	8 Lead 300 Mil PDIP	-40°C to +85°C

## BLOCK DIAGRAM

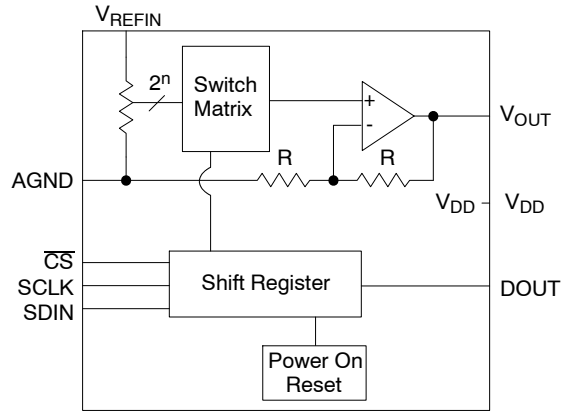
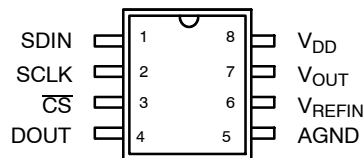
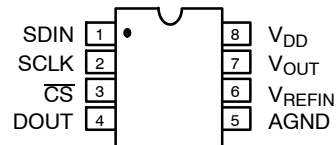


Figure 1. Block Diagram

## PIN CONFIGURATION



8 Lead SOIC (Jedec, 0.150")



8 Lead PDIP (0.300")

## PIN DESCRIPTION

Pin #	Symbol	Description
1	SDIN	Serial Data Input
2	SCLK	Serial Data Clock
3	$\overline{CS}$	Chip Select (Active High)
4	DOUT	Serial Data Output
5	AGND	Analog Ground
6	VREFIN	Voltage Reference Input
7	VOUT	DAC Output
8	VDD	Supply Voltage

## ELECTRICAL CHARACTERISTICS

Test Conditions:  $V_{DD} = 3V$ ,  $GND = 0V$ ,  $REFIN = 1.000V$  (External),  $R_L = 10k\Omega$ ,  $C_L = 100pF$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
<b>Static Performance XRD54L08</b>						
N	Resolution	8			Bits	Guaranteed Monotonic  $2.5V \leq V_{DD} \leq 3.5V$
INL	Relative Accuracy		0.25	0.5	LSB	
DNL	Differential Nonlinearity		0.25	0.5	LSB	
$V_{OS}$	Offset Error	0	3	8	mV	
$TCV_{OS}$	Offset Tempco		2		ppm/°C	
PSRR	Offset-Error Power-Supply Rejection Ratio		0.5	1	mV	
GE	Gain Error		0.1	0.4	%FS	
TCGE	Gain-Error Tempco		10		ppm/°C	
PSRR	Power-Supply Rejection Ratio		0.1	1.25	mV	
<b>Static Performance XRD54L10</b>						
N	Resolution	10			Bits	Guaranteed Monotonic  $2.5V \leq V_{DD} \leq 3.5V$
INL	Relative Accuracy		0.5	1	LSB	
DNL	Differential Nonlinearity		0.50	0.75	LSB	
$V_{OS}$	Offset Error	0	3	8	mV	
$TCV_{OS}$	Offset Tempco		2		ppm/°C	
PSRR	Offset-Error Power-Supply Rejection Ratio		0.5	1	mV	
GE	Gain Error		0.1	0.4	%FS	
TCGE	Gain-Error Tempco		10		ppm/°C	
PSRR	Power-Supply Rejection Ratio		0.1	1.25	mV	
<b>Static Performance XRD54L12</b>						
N	Resolution	12			Bits	Guaranteed Monotonic  $2.5V \leq V_{DD} \leq 3.5V$
INL	Relative Accuracy		2	4	LSB	
DNL	Differential Nonlinearity		0.5	-1	LSB	
$V_{OS}$	Offset Error	0	3	8	mV	
$TCV_{OS}$	Offset Tempco		2		ppm/°C	
PSRR	Offset-Error Power-Supply Rejection Ratio		1.0	1.25	mV	
GE	Gain Error		0.1	0.4	%FS	
TCGE	Gain-Error Tempco		10		ppm/°C	
PSRR	Power-Supply Rejection Ratio		0.1	1.25	mV	

## ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions:  $V_{DD}= 3V$ ,  $GND= 0V$ ,  $REFIN= 1.000V$  (External),  $R_L= 10k\Omega$ ,  $C_L= 100pF$ ,  $T_A= T_{MIN}$  to  $T_{MAX}$ , Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
<b>Voltage Output (<math>V_{OUT}</math>) XRD54L08/L10/L12</b>						
$V_O$	Output Voltage Range	0		$V_{DD}-0.4$	V	
$V_{REG}$	Output Load Regulation		2	4	mV	$V_{OUT} = 2V$ , $R_L=2k\Omega$
$+I_{SC}$	Short-Circuit Current, Sink		11		mA	$V_{OUT} = V_{DD}$
$-I_{SC}$	Short-Circuit Current, Source		2.5		mA	$V_{OUT} = GND$
<b>Voltage Reference Input (<math>V_{REFIN}</math>) XRD54L08/L10/L12</b>						
$V_{REFIN}$	Voltage Range	0		$V_{DD}$	V	Output Swing Limited, Not Code Dependent
$R_{IN}$	Input Resistance	40	65		k $\Omega$	
$TCR_{IN}$	Input Resistance Tempco		1500		ppm/ $^{\circ}C$	
$C_{IN}$	Input Capacitance		32	40	pF	Not Code Dependent
$AC_{FT}$	AC Feedthrough		-80		dB	$REFIN = 1kHz$ , $2Vp-p$ , $SD_{IN}=000h$
<b>Digital Inputs (<math>SDIN</math>, <math>SCLK</math>, <math>\overline{CS}</math>) XRD54L08/L10/L12</b>						
$V_{IH}$	Input High	2.0			V	
$V_{IL}$	Input Low			0.8	V	
$I_{IN}$	Input Current			1	$\mu A$	$V_{IN}=0V$ or $V_{DD}$
$C_{IN}$	Input Capacitance		10		pF	
<b>Digital Output (DOUT) XRD54L08/L10/L12</b>						
$V_{OH}$	Output High	$V_{DD}-1$			V	$I_{SOURCE}=4mA$
$V_{OL}$	Output Low			0.4	V	$I_{SINK}=4mA$
<b>Dynamic Performance XRD54L08/L10/L12</b>						
SR	Voltage-Output Slew Rate	0.13	0.21		V/ $\mu s$	$T_A=+25^{\circ}C$
$t_s$	Voltage-Output Settling Time		13	15	$\mu s$	$\sim 1/2LSB$ , $V_{OUT}=2V$
$D_{FT}$	Digital Feedthrough		1		nV-s	$\overline{CS}=V_{DD}$ , $SDIN=SCLK=100kHz$
SINAD	Signal-to-Noise Plus Distortion		68		dB	$V_{REFIN}=1kHz$ , $2Vp-p$ F.S., $SDIN=Full$ Scale $-3dB$ BW= $250kHz$
<b>Power Supply XRD54L08/L10/L12</b>						
$V_{DD}$	Positive Supply Voltage	2.5		3.5	V	
$I_{DD}$	Power Supply Current		35	60	$\mu A$	All Inputs= $0V$ or $V_{DD}$ , Output=No Load, $V_O=0V$ , $I_{REF}$ Not Included
<b>Switching Characteristics XRD54L08/L10/L12</b>						
$t_{CSS}$	$\overline{CS}$ Setup Time	10	20		ns	
$t_{CSH0}$	SCLK Fall to $\overline{CS}$ Fall Hold Time	5			ns	
$t_{CSH1}$	SCLK Fall to $\overline{CS}$ Rise Hold Time	0			ns	

### Notes:

<sup>1</sup> Total supply current consumption =  $I_{DD} + I_{REF} + (V_{OUT} / 70K.)$

## ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions:  $V_{DD}= 3V$ ,  $GND= 0V$ ,  $REFIN= 1.000V$  (External),  $R_L= 10k\Omega$ ,  $C_L= 100pF$ ,  $T_A= T_{MIN}$  to  $T_{MAX}$ , Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$t_{CH}$	SCLK High Width	20	35		ns	$C_L= 50pF$
$t_{CL}$	SCLK Low Width	20	35		ns	
$t_{DS}$	$D_{IN}$ Setup Time	10	45		ns	
$t_{DH}$	$D_{IN}$ Hold Time	0			ns	
$t_{DO}$	$D_{OUT}$ Valid Propagation Delay		8	15	ns	
$t_{CSW}$	$\overline{CS}$ High Pulse Width	20	40		ns	
$t_{CS1}$	$\overline{CS}$ Rise to SCLK Rise Setup Time	10	20		ns	

Specifications are subject to change without notice

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$  to GND ..... -0.3V, +5V  
 Digital Input Voltage to GND ..... -0.3V,  $V_{DD} + 0.3V$   
 $V_{REFIN}$  ..... -0.3V,  $V_{DD} + 0.3V$   
 $V_{OUT}^1$  .....  $V_{DD}$ , GND  
 Continuous Current, Any Pin ..... -20mA, +20mA

Package Power Dissipation Ratings ( $T_A= +70^\circ C$ )  
     PDIP (derate 9mW/ $^\circ C$  above  $+70^\circ C$ ) .... 117mW  
     SOIC (derate 6mW/ $^\circ C$  above  $+70^\circ C$ ) ... 155mW  
 Operating Temperature Range .....  $-40^\circ C$  to  $+85^\circ C$   
 Storage Temperature Range .....  $-65^\circ C$  to  $+165^\circ C$   
 Lead Temperature (soldering, 10 sec) .....  $+300^\circ C$

### Notes

<sup>1</sup> Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

<sup>2</sup> Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100 $\mu s$ .

## TIMING

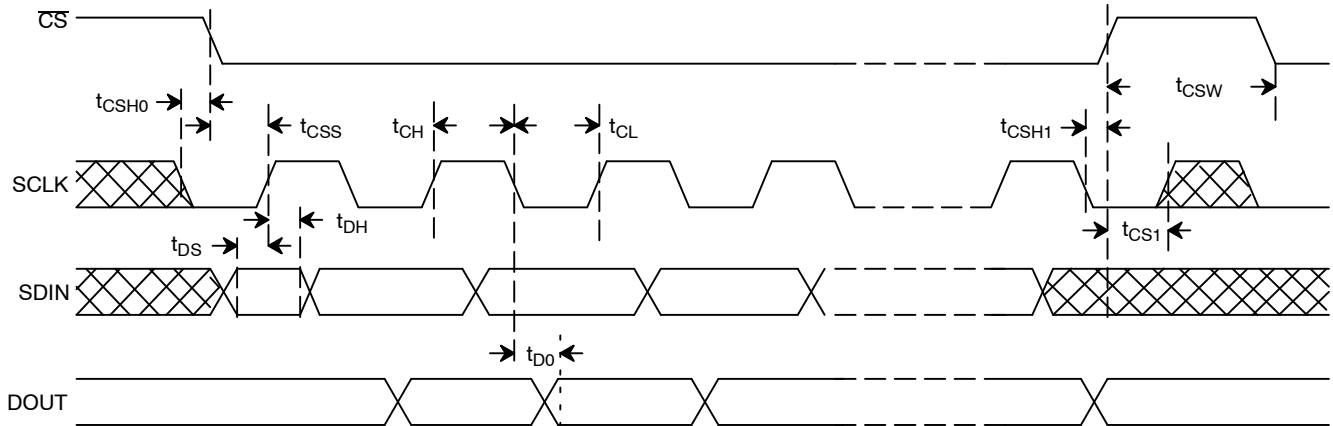


Figure 2. Timing Diagram

Input			Output
1111	1111	(0000)	$+ 2 (V_{REFIN}) \frac{255}{256}$
1000	0001	(0000)	$+ 2 (V_{REFIN}) \frac{129}{256}$
1000	0000	(0000)	$+ 2 (V_{REFIN}) \frac{128}{256} = + V_{REFIN}$
0111	1111	(0000)	$+ 2 (V_{REFIN}) \frac{127}{256}$
0000	0001	(0000)	$+ 2 (V_{REFIN}) \frac{1}{256}$
0000	0000	(0000)	0V

**Note:**  
Write 8-bit data words with four sub-LSB 0s because the DAC input latch is 12 bits wide.

Table 1. Binary Code Table

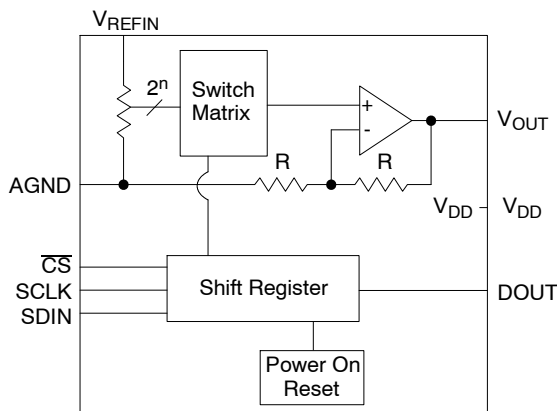
**THEORY OF OPERATION**

**XRD54L08/L10/L12 Description**

The XRD54L08/L10/L12 are micro-power, voltage output, serial daisy-chain programmable DACs operating from a single 3V power supply. The DACs are built on a 0.6 micron CMOS process. The features of these DACs make it well suited for industrial control, low distortion audio, battery operated devices and cost sensitive designs that want to minimize pin count on ICs.

**Resistor String DAC**

A resistor string architecture converts digital data using a switch matrix to an analog signal as shown in *Figure 3*.



**Figure 3. XRD54L08/L10/L12 DAC Architecture**

The resistor string architecture provides a non-inverted output voltage ( $V_{OUT}$ ) of the reference input ( $V_{REFIN}$ ) for single supply operation while maintaining a constant input resistance. Unlike inverted R-2R architectures the reference input resistance will remain constant independent of code. This greatly simplifies the analog driving source requirements for the reference voltage and minimizes distortion. Similarly input capacitance varies only approximately 4pF over all codes.

**Fixed Gain +2 Voltage Output Amplifier**

A high open-loop gain operational amplifier buffers the resistor string with a stable, fixed gain of +2. The voltage output will settle within 13µs. The output is short circuit protected and can regulate an output load of 2V into 2kΩ within 2mV at 25°C.

While the reference input will accept a voltage from rail-to-rail, the linear input voltage range is constrained by the output swing of the fixed +2 closed-loop gain amplifier. Full scale output swing is achieved with an external reference of approximately 1/2  $V_{DD}$ . The reference voltage must be positive because the XRD54L08/L10/L12 DAC is non-inverting.

**Serial Daisy-Chainable Digital Interface**

The three wire serial interface includes a DOUT to enable daisy-chaining of several DACs. This minimizes pin count necessary of digital asics or controllers to address multiple DACs. The serial interface is designed for CMOS logic levels. Timing is shown in *Figure 2*. The binary coding table (*Table 1*) shows the DAC transfer function.

A power on reset circuit forces the DAC to reset to all “0”s on power up.

**APPLICATION NOTES**

**Serial Interface**

The XRD54L08/L10/L12 family has a three wire serial interface that is compatible with Microwire™, SPI™ and QSPI™ standards. Typical configurations are shown in *Figure 4 and Figure 5*. Maximum serial port clock rate is limited by the minimum pulse width of  $t_{CH}$  and  $t_{CL}$ . Feedthrough noise from the serial port to the analog output ( $V_{OUT}$ ) is minimized by lowering the frequency of the serial port and holding the digital edges to >5ns.

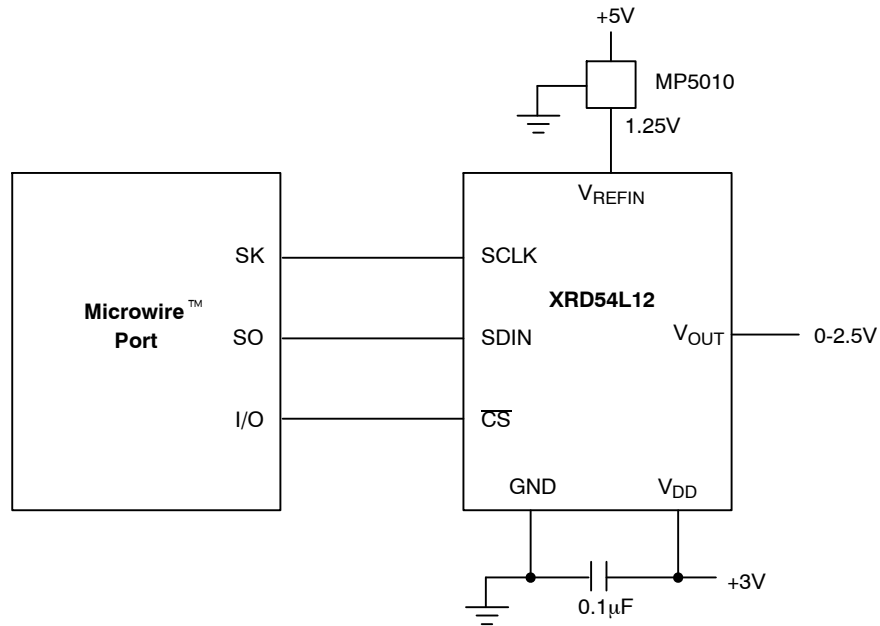


Figure 4. Typical Microwire™ Application Circuit

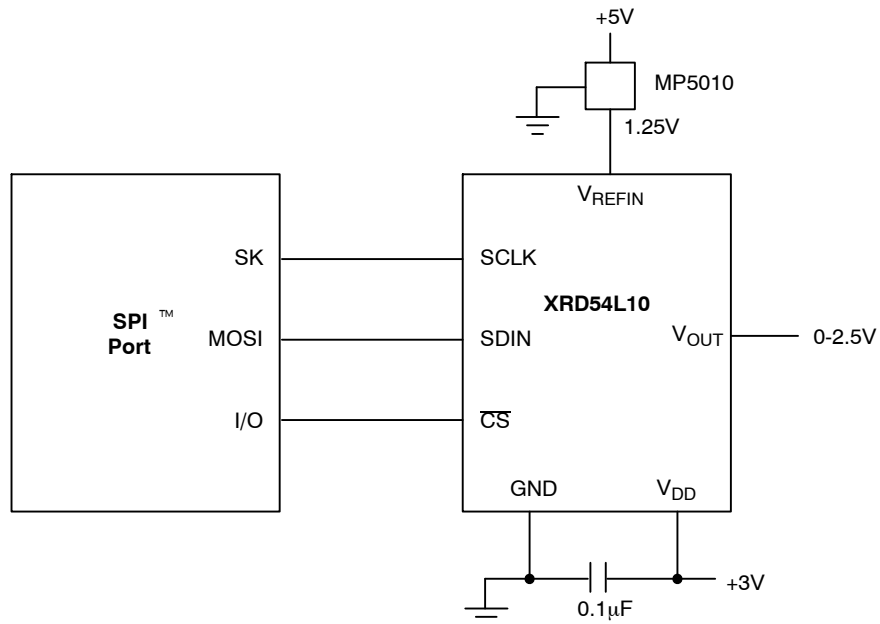


Figure 5. Typical SPI™ Application Circuit



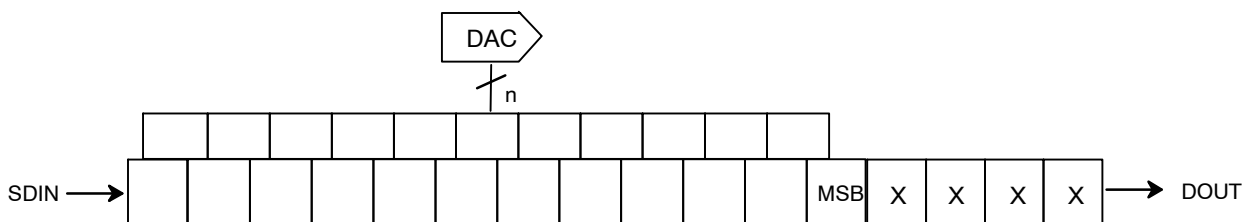


Figure 6. Shift Register Format

The DACs are programmed by a 16 bit word of serial data. The format of the serial input register is shown in Figure 6. The leading 4 bits are not used to update the DAC. If the DAC is not daisy-chained then only a 12 bit serial word is needed to program the DAC. The next 8, 10 or 12 bits after the 4 leading bits are data bits. The XRD54L08's first 8 bits are valid data and the trailing 4 bits must be set to 0. Figure 7 demonstrates the 16 bit digital word for the 8, 10, 12 bit DACs.

Part	Leading Unused Bits	Data Bits		Trailing "0" Bits
		MSB	LSB	
XRD54L12	XXXX	XXXXXXXX		None
XRD54L10	XXXX	XXXXXXXX		00
XRD54L08	XXXX	XXXXXXXX		0000

Table 2. 16-Bit Digital Word Register for XRD54L08, XRD54L10, XRD54L12.

SCLK should be held low when  $\overline{CS}$  transitions low. Data is clocked in on the rising edge of SCLK when  $\overline{CS}$  is low. SDIN data is held in a 16 bit serial shift register. The DAC is updated with the data bits on the rising edge of  $\overline{CS}$ . When  $\overline{CS}$  is high data is not shifted into the XRD54L08/L10/L12.

**Daisy-Chaining**

The digital output port (DOUT) has a 4mA drive for greater fan-out capability when daisy-chaining. DOUT allows cascading of multiple DACs with the same serial data stream. The data at SDIN appears at DOUT after 16 clock cycles plus one clock width ( $t_{CH}$ ) and a propagation delay ( $t_{DO}$ ). DOUT remains in the state of the last data bit when  $\overline{CS}$  is high. DOUT changes on the falling edge of SCLK when  $\overline{CS}$  is low.

Any number of DACs can be connected in this way by connecting DOUT of one DAC to SDIN of the next DAC.

**AC<sub>FT</sub> Feedthrough (DAC Code = 0)**

AC Feedthrough from  $V_{REFIN}$  to  $V_{OUT}$  is minimized with low impedance grounding as shown in Figure 7. If the DAC data is set to all "0"s then  $V_{OUT}$  is a function of the divider between the DAC string impedance and ground impedance. See the Power Supply and Grounding section for recommendations. The typical AC feedthrough for a 1kHz 2Vpp signal with code = 0 is -80dB.

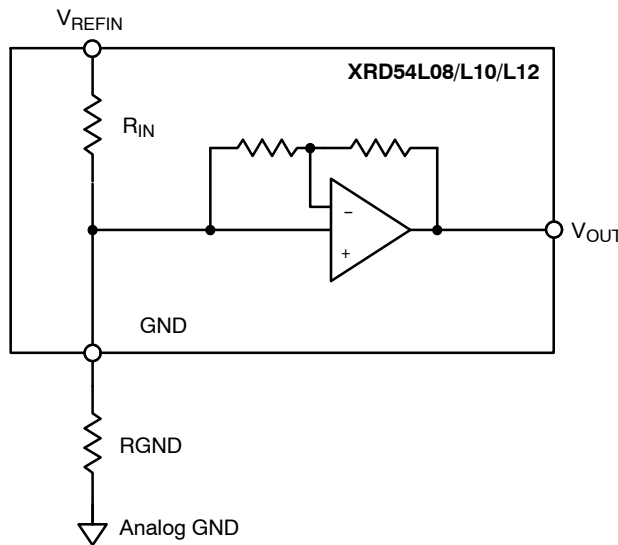


Figure 7. AC<sub>FT</sub> Feedthrough Equivalent Circuit, DAC Code = 0

**Compatible with MAX515 & MAX539**

The XRD54L08/L10/L12 family of DACs are functionally compatible with the MAX515 & MAX539 while providing significant improvements. The XRD54L08/L10/L12 DACs have lower power, faster serial ports, and a constant reference impedance to minimize the reference driving requirements and maximize system linearity while

operating from a 3V supply versus 5V for the MA515 and MAX539. The DOUT port also has 4mA driving capability for greater fan-out when daisy-chaining to other digital inputs.

## Monotonicity

The XRD54L08/L10/L12 family of DACs are monotonic over the entire temperature range.

## Micro-Power Operation

The XRD54L08/L10/L12 are the lowest power DACs in their class. The quiescent current rating does not include the reference ladder current. Power can be saved when the part is not in use by setting the DAC code to all “0”s assuming the output load is referenced to ground. This minimizes the DAC output load current. An analog switch placed in series with the reference ladder can toggle the reference voltage off when the circuit is inactive to minimize power consumption.

## Power Supply and Grounding

Best parametric results are obtained by powering the XRD54L08/L10/L12 family of DACs from an analog +3V power supply and analog ground. Digital power supplies and grounds should be separated or connected to the analog supplies and grounds only at the low-impedance power-supply source. This is best accomplished on a multilayer PCB with dedicated planes to ground and power. The DACs should be locally bypassed with both 0.1  $\mu$ F and 2.2  $\mu$ F capacitors mounted as close as possible to the power supply pin ( $V_{DD}$ ). Surface mount ceramic capacitors are recommended for low impedance, wide band power supply bypass. If only one +3V power supply is available for both analog and digital circuitry isolate the analog power supply to the XRD54L08/L10/L12 DAC with an inductor or ferrite bead before the local bypass capacitors.

## PERFORMANCE CHARACTERISTICS

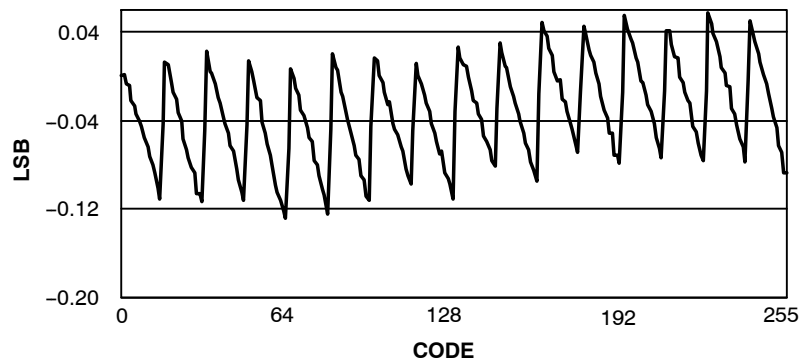


Figure 8. XRD54L08 INL (For XRD54L10 and XRD54L12, Scale Axes Accordingly)

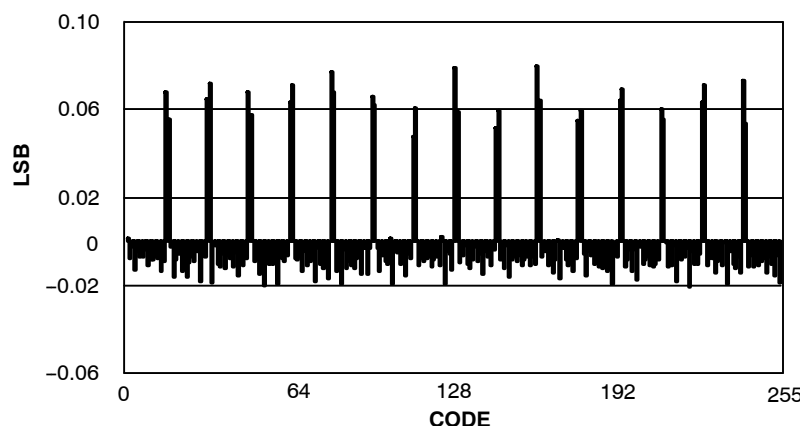
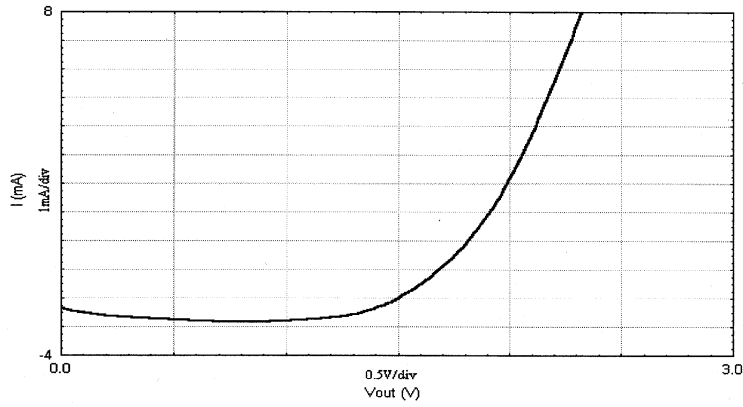
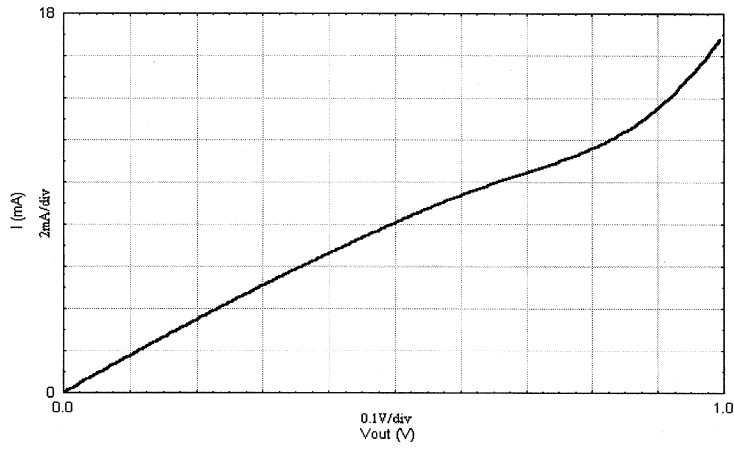


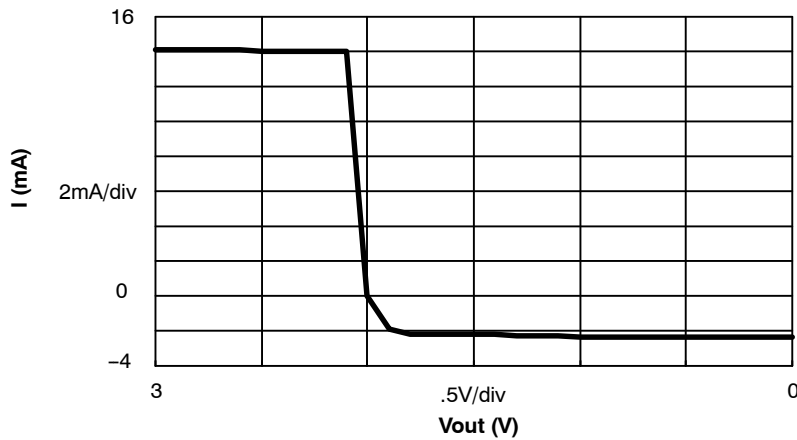
Figure 9. XRD54L08 DNL (For XRD54L10 and XRD54L12, Scale Axes Accordingly)



**Figure 10. Output Source Current vs. Output Voltage**



**Figure 11. Output Sink Current vs. Output Voltage**



**Figure 12. Output Sink and Source Current vs. Output Voltage**

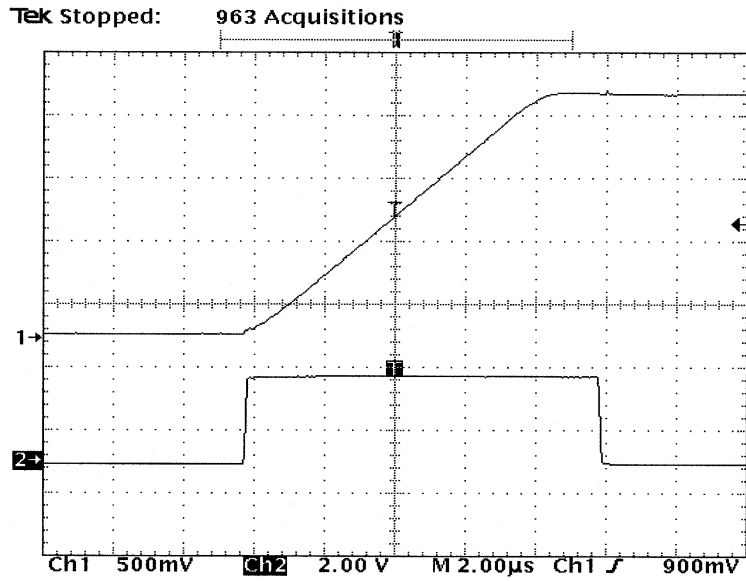


Figure 13. Voltage Output Settling Time ( $t_s$ ),  
 $V_{DD} = 5V$ ,  $V_{REFIN} = 1V$ , No Load

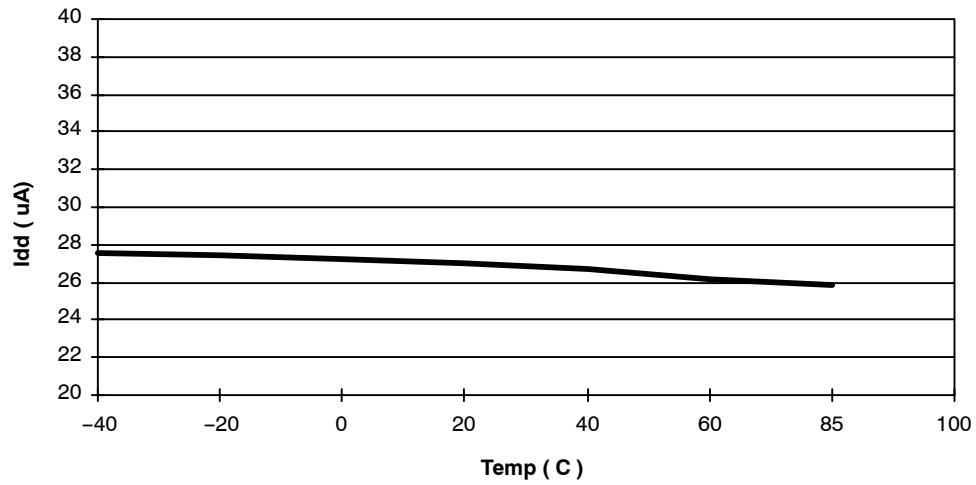
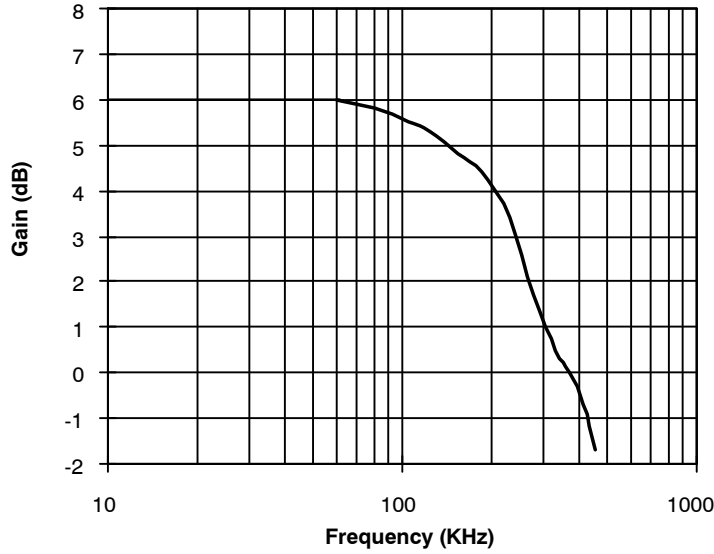
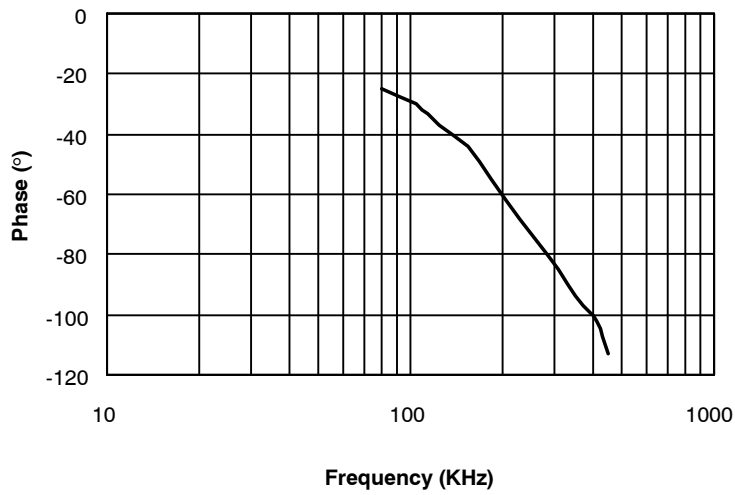


Figure 14.  $I_{DD}$  vs. Temperature



**Figure 15. Closed Loop Gain vs. Frequency**



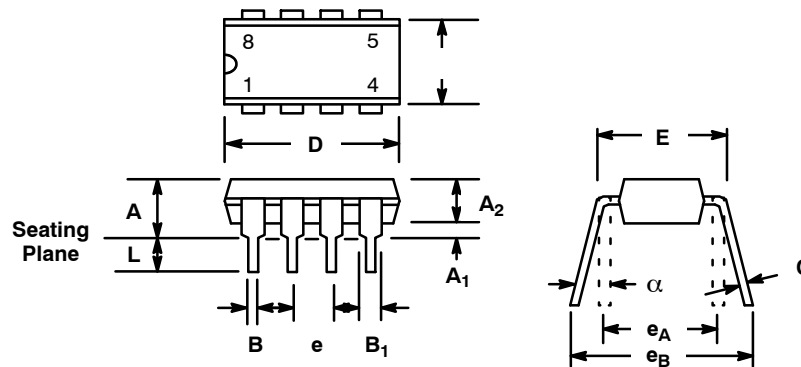
**Figure 16. Closed Loop Phase vs. Frequency**

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**SPI™** and **QSPI™** are trademarks of Motorola Corporation.

## 8 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 2.00

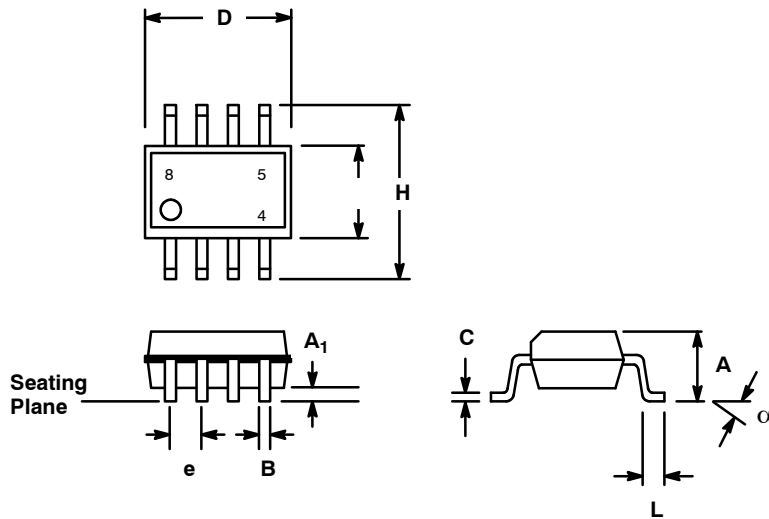


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A <sub>1</sub>	0.015	0.070	0.38	1.78
A <sub>2</sub>	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B <sub>1</sub>	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.348	0.430	8.84	10.92
E	0.300	0.325	7.62	8.26
E <sub>1</sub>	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e <sub>A</sub>	0.300 BSC		7.62 BSC	
e <sub>B</sub>	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

**8 LEAD SMALL OUTLINE  
(150 MIL JEDEC SOIC)**

*Rev. 1.00*



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A <sub>1</sub>	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

*Note: The control dimension is the millimeter column*

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