Preliminary

XRD64L44

Dual 10-Bit 50MSPS CMOS ADC

March 2000-1

FEATURES

- 10-Bit Resolution
- Two Monolithic Complete 10-Bit ADCs
- 50 MSPS Conversion Rate
- On-Chip Track-and-Hold
- On-Chip Voltage Reference
- Low 5 pF Input Capacitance
- TTL/CMOS Outputs
- Tri-State Output Buffers
- Single +3V or +5V Power Supply Operation
- Low Power Dissipation: 250mW-typ @ 3.0V
- -40°C to +85°C Operation Temperature Range

APPLICATIONS

- Medical Ultrasound Imaging
- I & Q Modems

BENEFITS

- Reduction of Components
- Reduction of System Cost
- High Performance @ Low Power Dissipation
- Long Term Time and Temperature Stability

GENERAL DESCRIPTION

The XRD64L44 is two 10-bit, monolithic, 50 MSPS ADCs. Manufactured using a standard CMOS process, the XRD64L44 offers low power, low cost and excellent performance. The on-chip track-and-hold amplifier(T/H) and voltage reference (VREF) eliminate the need for external active components, requiring only an external ADC conversion clock for the application. The XRD64L44 analog input can be driven with ease due to the high input impedance of RIN = 25KOhms and CIN = 5pF.

The design architecture uses 17 time- interleaved 10-bit SAR ADCs in each converter to achieve high conversion rate of 50 MSPS minimum. In order to insure and maintain accurate 10-bit operation with respect to time and temperature, XRD64L44 incorporates an auto-calibration circuit which continuously adjusts and matches the offset and linearity of each ADC. This auto-calibration circuit is transparent to the user after the initial 3.4ms calibration (168,000 initial clock cycles).

The power dissipation is only 250mW at 50 MSPS and 225mW at 40 MSPS with +3.0V power supply.

The digital output data is straight binary format, and the tri-state disable function is provided for common bus interface.

The XRD64L44 internal reference provides cost savings and simplifies the design/development. The output voltage of the internal reference is set by two external resistors. The internal reference can be disabled if an external reference is used for a power savings of 50mW.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
XRD64L44AIV	64-Lead TQFP	-40°C to +85°C

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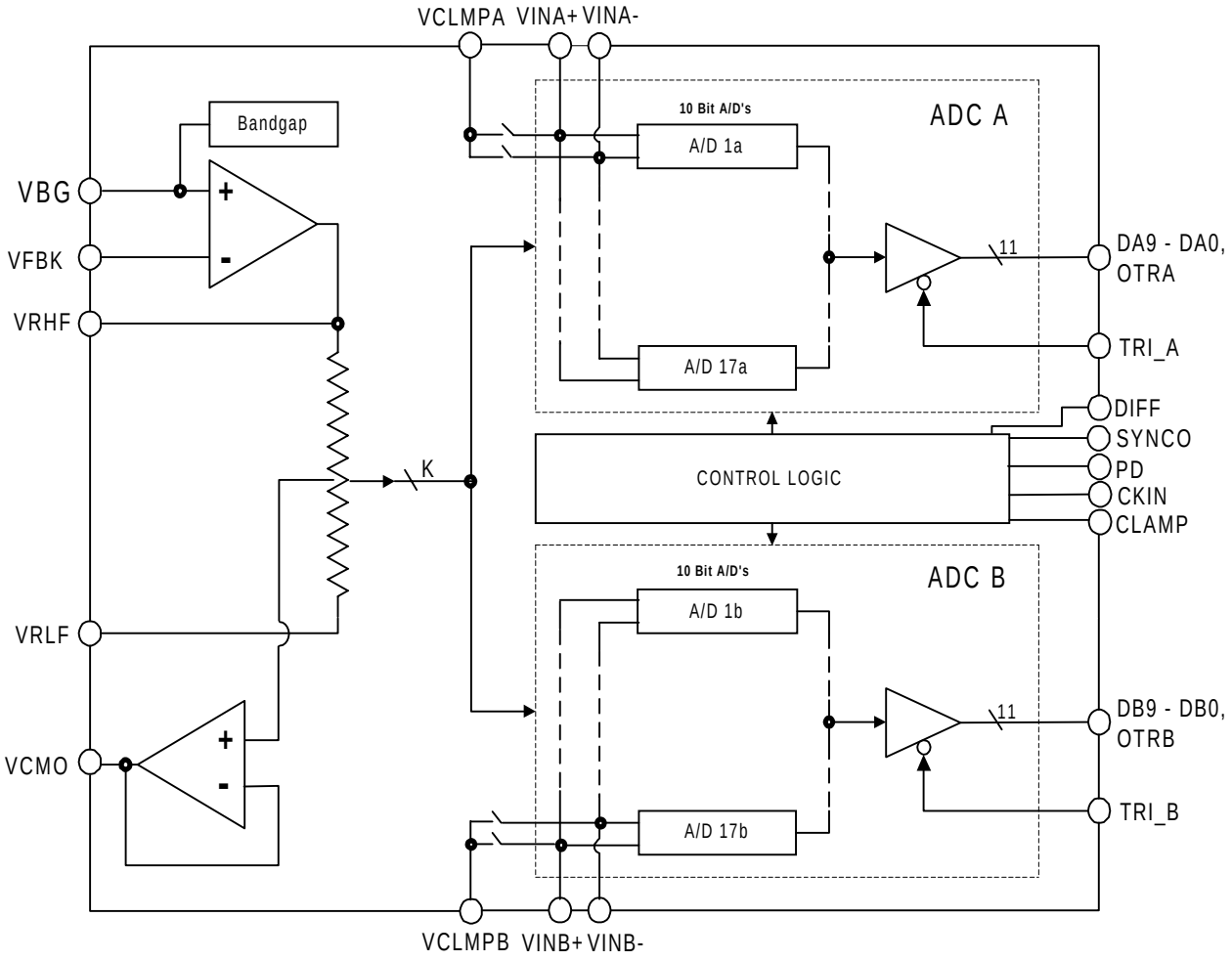
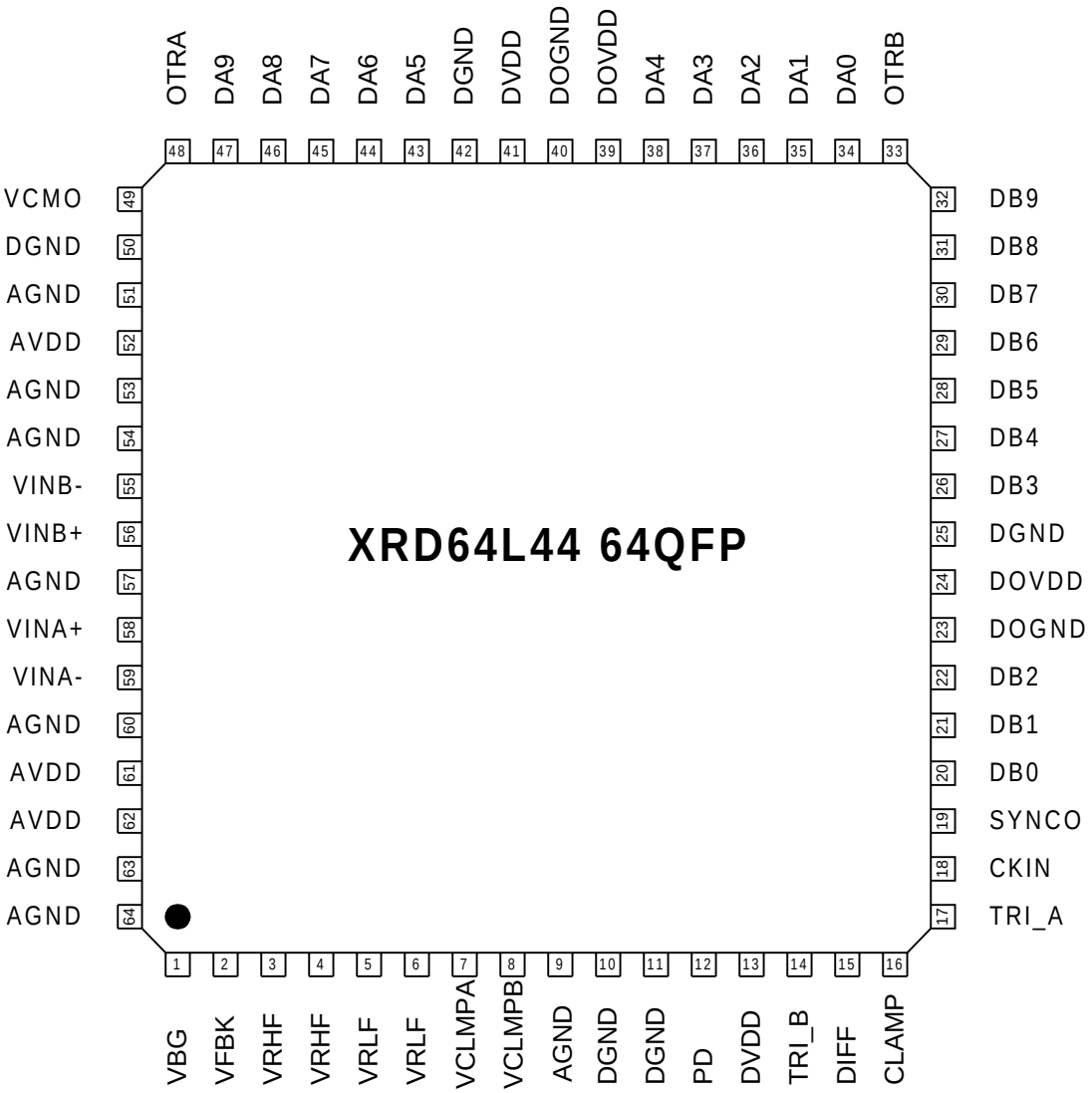


Figure 1. XRD64L44 Simplified Block Diagram


OTRA 48
DA9 47
DA8 46
DA7 45
DA6 44
DA5 43
DGND 42
DVDD 41
DOGND 40
DOVDD 39
DA4 38
DA3 37
DA2 36
DA1 35
DA0 34
OTRB 33
VCMO 49
DGND 50
AGND 51
AVDD 52
AGND 53
AGND 54
VINB- 55
VINB+ 56
AGND 57
VINA+ 58
VINA- 59
AGND 60
AVDD 61
AVDD 62
AGND 63
AGND 64
DB9 32
DB8 31
DB7 30
DB6 29
DB5 28
DB4 27
DB3 26
DGND 25
DOVDD 24
DOGND 23
DB2 22
DB1 21
DB0 20
SYNCO 19
CKIN 18
TRI_A 17
XRD64L44 64QFP
VBG 1
VFBK 2
VRHF 3
VRHF 4
VRLF 5
VRLF 6
VCLMPA 7
VCLMPB 8
AGND 9
DGND 10
DGND 11
PD 12
DVDD 13
TRI_B 14
DIFF 15
CLAMP 16

PIN DESCRIPTION

Pin #	Symbol	Description
1	VBG	Bandgap Voltage Output
2	VFBK	Analog Reference Feedback
3	VRHF	Top Voltage Reference Force
4	VRHF	Top Voltage Reference Force
5	VRLF	Bottom Voltage Reference Force
6	VRLF	Bottom Voltage Reference Force
7	VCLMPA	Analog Input Clamp A
8	VCLMPB	Analog Input Clamp B
9	AGND	Analog Ground
10	DGND	Digital Ground
11	DGND	Digital Ground
12	PD	Power Down
13	DVDD	Digital Supply Voltage
14	TRI_B	Tri-state for the B Channel Outputs
15	DIFF	Differential / Single-Ended Input Mode
16	CLAMP	Digital Clamp Control
17	TRI_A	Tri-state for the A Channel Outputs
18	CKIN	Clock Input
19	SYNCO	Data Valid Output
20	DB0	Digital Output Bit 0 (LSB) ADC B
21	DB1	Digital Output Bit 1 ADC B
22	DB2	Digital Output Bit 2 ADC B
23	DOGND	Digital Output Ground
24	DOVDD	Digital Output Supply Voltage
25	DGND	Digital Ground
26	DB3	Digital Output Bit 3 ADC B
27	DB4	Digital Output Bit 4 ADC B
28	DB5	Digital Output Bit 5 ADC B
29	DB6	Digital Output Bit 6 ADC B
30	DB7	Digital Output Bit 7 ADC B
31	DB8	Digital Output Bit 8 ADC B
32	DB9	Digital Output Bit 9 (MSB) ADC B
33	OTRB	Over Range Digital Output Bit ADC B
34	DA0	Digital Output Bit 0 (LSB) ADC A
35	DA1	Digital Output Bit 1 ADC A
36	DA2	Digital Output Bit 2 ADC A
37	DA3	Digital Output Bit 3 ADC A
38	DA4	Digital Output Bit 4 ADC A
39	DOVDD	Digital Output Supply Voltage
40	DOGND	Digital Output Ground
41	DVDD	Digital Supply Voltage

PIN DESCRIPTION (CONT'D)

Pin #	Symbol	Description
42	DGND	Digital Ground
43	DA5	Digital Output Bit 5 ADC A
44	DA6	Digital Output Bit 6 ADC A
45	DA7	Digital Output Bit 7 ADC A
46	DA8	Digital Output Bit 8 ADC A
47	DA9	Digital Output Bit 9 ADC A
48	OTRA	Over Range Digital Output Bit ADC A
49	VCMO	Differential Common Mode Voltage Output
50	DGND	Digital Ground
51	AGND	Analog Ground
52	AVDD	Analog Supply Voltage
53	AGND	Analog Ground
54	AGND	Analog Ground
55	VINB-	Analog Input B(-)
56	VINB+	Analog Input B(+)
57	AGND	Analog Ground
58	VINA+	Analog Input A(+)
59	VINA-	Analog Input A(-)
60	AGND	Analog Ground
61	AVDD	Analog Supply Voltage
62	AVDD	Analog Supply Voltage
63	AGND	Analog Ground
64	AGND	Analog Ground

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Test Conditions (Unless Otherwise Specified)

T_A = 25°C AV_{DD} = DV_{DD} = +3.3V, VIN = GND to +2.5V, V_{RLF} = GND, V_{RHF} = +2.5V and Fs = 50 MSPS, 50% Duty Cycle, Differential Input Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions/Comments
DC ACCURACY						
DNL	Differential Non-Linearity	-1.0	+/-0.4	1.0	LSB	
INL	Integral Non-Linearity		+/-1.1		LSB	
MON	Monotonicity		No Missing Codes			Guaranteed by Test
FSE	Full Scale Error		±10		mV	F.S. = (VRHF - VRLF)x0.97
ZSE	Zero Scale Error		5		mV	Single Ended Mode
ANALOG INPUT						
INVR	Input Voltage Range	0		VRHFx0.97	V	VRLF Grounded
INRES	Input Resistance		20		KOhms	
INCAP	Input Capacitance		5		pF	
INBW	Input Bandwidth		400		MHz	-1dB Small Signal
REFERENCE INPUT, INTERNAL BANDGAP REFERENCE AND REFERENCE BUFFER						
RLAD	Ladder Resistance	100	125	150	Ohms	
RLADTCO	Ladder Resistance Tempco		+0.8		Ohms/°C	
VBG	Bandgap Output Voltage Range		1.25		V	
VBGTC	Bandgap Reference Tempco		30		ppm/°C	
VRLF		0.0		2.0	V	
VRHF		VRLF+1.0		AVdd-0.6	V	Internal Reference Buffer
VRHF External Reference		VRLF+1.0		AVdd	V	External
VRHF PSRR Internal Reference Buffer			6		mV/V	
CONVERSION and TIMING CHARACTERISTICS (C_L = 10pF)						
MAXCON	Maximum Conversion Rate	50	60		MSPS	
MINCON	Minimum Conversion Rate		100		KSPS	
PDEL	Pipeline Delay(Latency)			17	CLK	Clock Cycles Digital Data Delay
t_{ad}	Aperture Delay Time		4		ns	
APJT	Aperture Jitter Time		12		ps	Peak-to Peak
t_r	Digital Output Rise Time		3		ns	
t_f	Digital Output Fall Time		3		ns	
t_{pd}	Output Data Propagation Delay		6	14	ns	Guaranteed by Design
t_{den}	Output Data Enable Delay		6	14	ns	Guaranteed by Design
t_{dis}	Output Data Disable Delay		5		ns	
CLKDC	Clock Duty Cycle	40	50	60	%	Guaranteed by Design

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Test Conditions (Unless Otherwise Specified)

T_A = 25°C AV_{DD} = DV_{DD} = +3.3V, VIN = GND to +2.5V, V_{RLF} = GND, V_{RHF} = +2.5V, 50% Duty Cycle, Differential Input Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions/Comments
DYNAMIC PERFORMANCE Fs = 40MHz						
SNR	Signal-to-Noise Ratio					Not Including Harmonics
	Fin = 1.0 MHz		60		dB	
	fin = 4.0 MHz		60		dB	
SINAD	Signal-to Noise and Distortion					
	fin = 1.0 MHz		58		dB	
	fin = 4.0 MHz		58		dB	
	fin = 12.5 MHz		57		dB	
ENOB	Effective Number of Bits					
	fin = 1.0 MHz		9.5		Bit	
	fin = 4.0 MHz		9.5		Bit	
	fin = 12.5 MHz		9.3		Bit	
SFDR	Spurious Free Dynamic Range					
SFDR	fin = 4.0 MHz	70			dB	
Crosstalk	fin = 4.0 MHz	75			dB	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Test Conditions (Unless Otherwise Specified)

T_A = 25°C AV_{DD} = DV_{DD} = +3.3V, VIN = GND to +2.5V, V_{RLF} = GND, V_{RHF} = +2.5V, 50% Duty Cycle, Differential Input Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions/Comments
DYNAMIC PERFORMANCE Fs = 50MHz						
SNR	Signal-to-Noise Ratio					Not Including Harmonics
	Fin = 1.0 MHz	56	58		dB	
	fin = 4.0 MHz	56	58		dB	
SINAD	Signal-to Noise and Distortion					
	fin = 1.0 MHz	55	57		dB	
	fin = 4.0 MHz	54	57		dB	
	fin = 12.5 MHz	54	56		dB	
ENOB	Effective Number of Bits					
	fin = 1.0 MHz	9.0	9.3		Bit	
	fin = 4.0 MHz	9.0	9.3		Bit	
	fin = 12.5 MHz	8.8	9.1		Bit	
SFDR	Spurious Free Dynamic Range					
SFDR	fin = 4.0 MHz	70			dB	
Crosstalk	fin = 4.0 MHz	75			dB	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Test Conditions (Unless Otherwise Specified)

T_A = 25°C AV_{DD} = DV_{DD} = +3.3V, VIN = GND to +2.5V, V_{RLF} = GND, V_{RHF} = +2.5V and Fs = 50 MSPS, 50% Duty Cycle, Differential Input Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions/Comments
DIGITAL INPUTS						
DVINH	Digital Input High Voltage	2.5			V	
DVINL	Digital Input Low Voltage			0.5	V	
DIINH	Digital Input High Current (The DIFF input has an internal pull-up resistor, TRI_A and TRI_B have internal pull-down resistors					
CKIN	Clock Input	-5.0	0.05	5.0	nA	
DIFF	Differential/Single-Ended Input	-1.0	-0.25	1.0	uA	
TRI_A/TRI_B	A/B Channel Tri-State	-125.0	-90.0	-50.0	uA	
DIINL	Digital Input Low Current (The DIFF input has an internal pull-up resistor, TRI_A and TRI_B have internal pull-down resistors					
CKIN	Clock Input	-5.0	0.05	5.0	nA	
DIFF	Differential/Single-Ended Input	50.0	90.0	125.0	uA	
TRI_A/TRI_B	A/B Channel Tri-State	-1.0	0.25	1.0	uA	
DINC	Digital Input Capacitance		5	8	pF	
DIGITAL OUTPUTS (CL = 10 pF)						
DOHV	Digital Output High Voltage	DVdd -0.4V	DVdd-0.3V		V	IOH = 1.5 mA
DOLV	Digital Output Low Voltage		0.3	0.4	V	IOL = 1.5 mA
IOZ	High-Z Leakage	-20	0.2	20	nA	
POWER SUPPLIES						
AV_{DD}	Analog Power Supply Voltage	3.0	3.3	3.6	V	
DV_{DD}	Digital Power Supply Range		AV_{DD}		V	DV_{DD} = AV_{DD}
Fs = 40 MHz, AVdd = DVdd = 3.0V, CL = 10pF, Fin = 10MHz						
AIDD	Analog Supply Current		37		mA	
DIDD	Digital Supply Current		15		mA	
DOIDD	Output Driver Current		15		mA	
VRHF	Top Voltage Ref Force Current		8		mA	VRHF/125, VRHF = 1.0V
PDISS	Power Dissipation		225		mW	
Fs = 50 MHz, AVdd = DVdd = 3.0V, CL = 10pF, Fin = 10MHz						
AIDD	Analog Supply Current		38		mA	
DIDD	Digital Supply Current		19		mA	
DOIDD	Output Driver Current		18		mA	
VRHF	Top Voltage Ref Force Current		8		mA	VRHF/125, VRHF = 1.0V
PDISS	Power Dissipation		250		mW	

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND	+7.0V
V_{RT} & V_{RB}	V_{DD} +0.5 to GND -0.5V
V_{IN}	V_{DD} +0.5 to GND -0.5V
All Inputs	V_{DD} +0.5 to GND -0.5V
All Outputs	V_{DD} +0.5 to GND -0.5V
Storage Temperature	-65°C to 150°C
Lead Temperature (Soldering 10 seconds)	300°C
Maximum Junction Temperature	150°C
Package Power Dissipation Ratings (T_A = +70°C)	
SSOP	θ_{JA} = 89.4°C/W
ESD	2000V min

Notes:

1 *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*

2 *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100ms.*

3 *V_{DD} refers to AV_{DD} and DV^{DD}. GND refers to AGND and DGND*

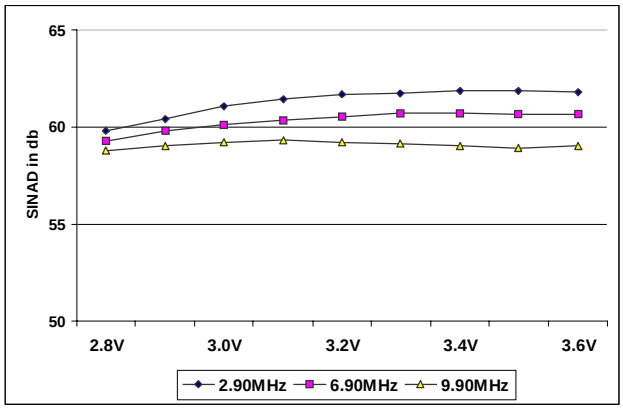


Figure 2 - SINAD vs. Fin and Vdd @Fc = 40.0MHz, DIFFERENTIAL INPUT MODE

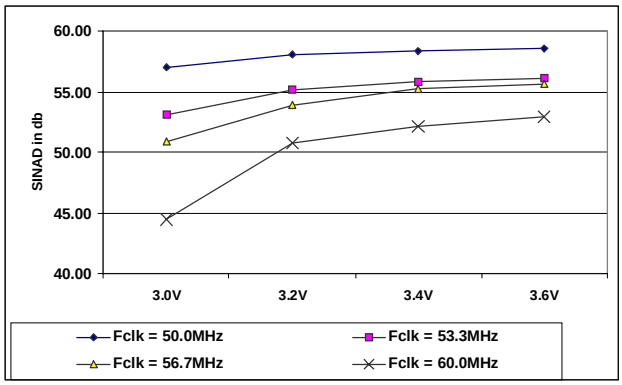


Figure 3 - SINAD vs. Fclock and Vdd DIFFERENTIAL INPUT MODE

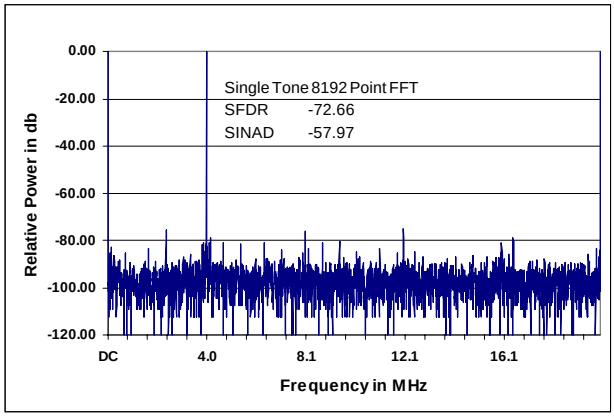


Figure 4 - FFT Spectrum @Fclock = 40.0MHz, Fin = 4.0MHz, DIFFERENTIAL INPUT MODE

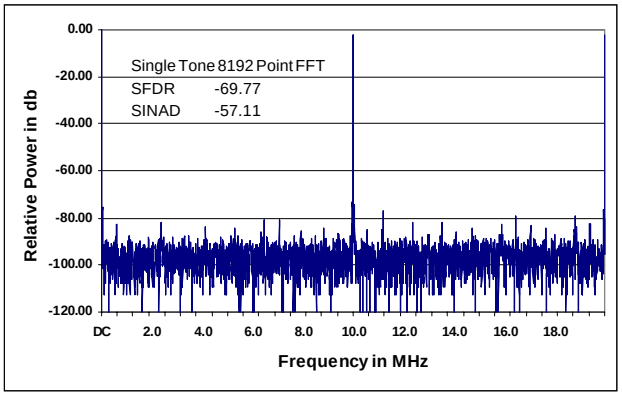


Figure 5 - FFT Spectrum @Fclock = 40.0MHz, Fin = 10.0MHz, DIFFERENTIAL INPUT MODE

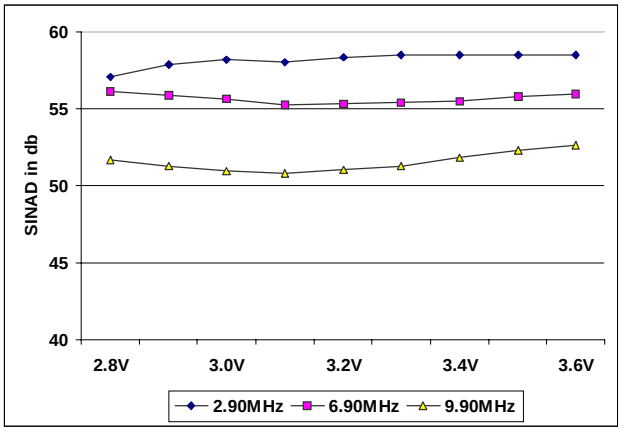


Figure 6 - SINAD vs. Fin and Vdd @Fc = 40.0MHz, SINGLE-ENDED INPUT MODE

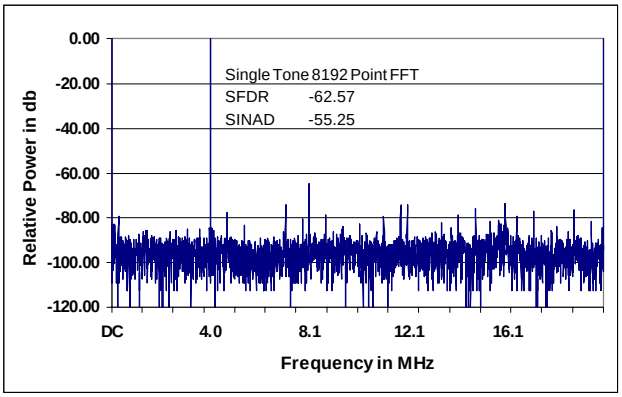


Figure 7 - FFT Spectrum @Fclock = 40.0MHz, Fin = 4.0MHz, Single-ended INPUT MODE

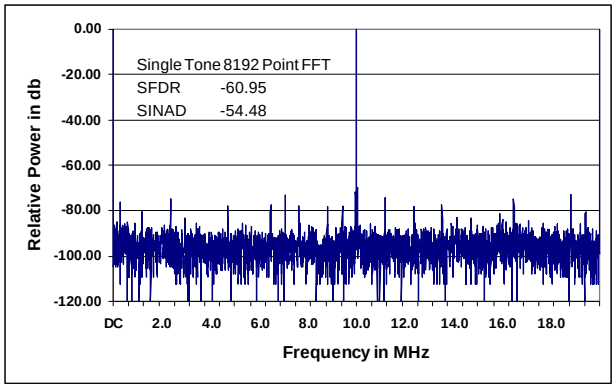


Figure 8 - FFT Spectrum @Fclock = 40.0MHz, Fin = 10.0MHz, Single-ended INPUT MODE

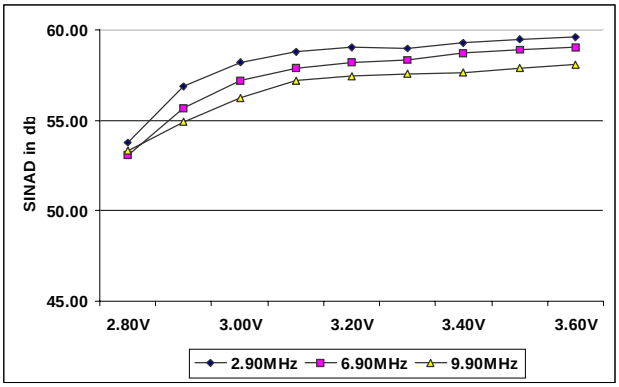


Figure 9 - SINAD vs. Fin and Vdd @Fc = 50.0MHz, DIFFERENTIAL INPUT MODE

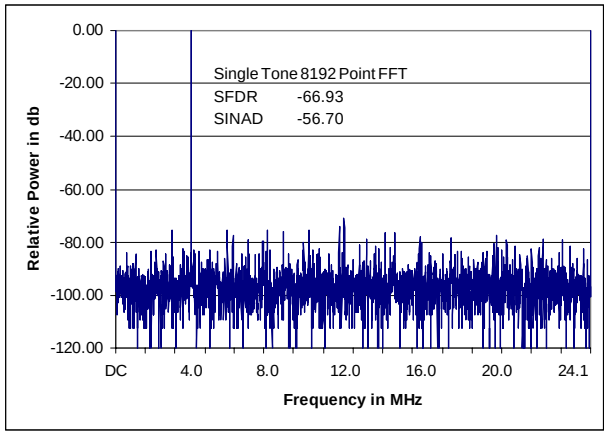


Figure 10 - FFT Spectrum @Fclock = 50.0MHz, Fin = 4.0MHz, DIFFERENTIAL INPUT MODE

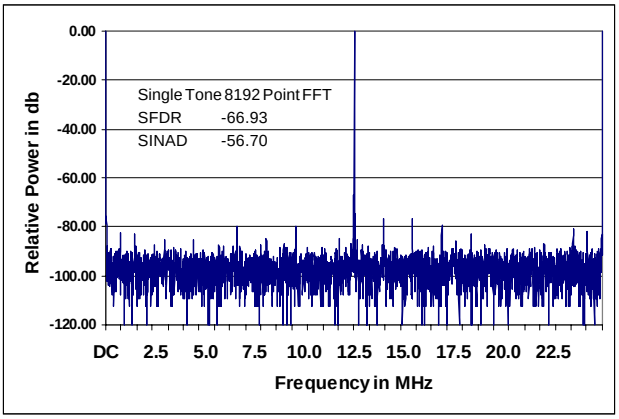


Figure 11 - SINAD @Fclock = 50.0MHz, Fin = 12.5MHz, DIFFERENTIAL INPUT MODE

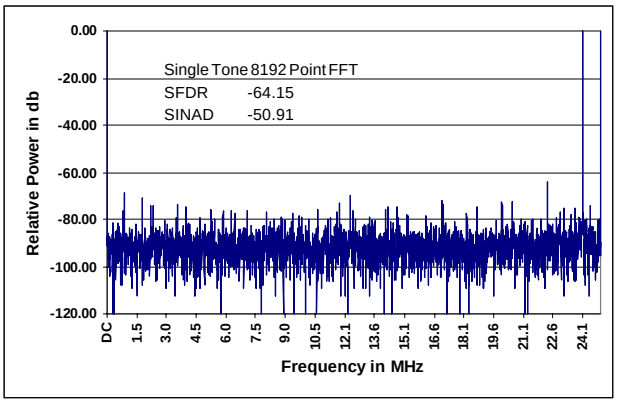


Figure 12 - FFT Spectrum @Fclock = 50.0MHz, Fin = 24.1MHz, DIFFERENTIAL INPUT MODE

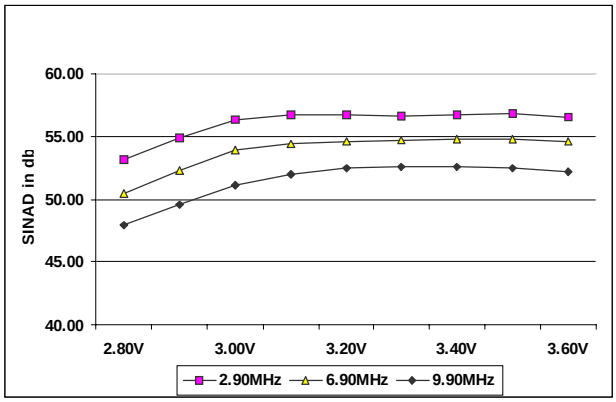


Figure 13 - SINAD vs. Fin and Vdd @Fc = 50.0MHz, SINGLE-ENDED INPUT MODE

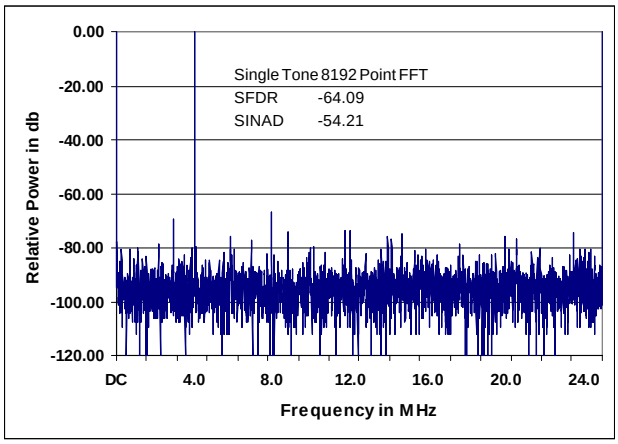


Figure 14 - SINAD @Fclock = 50.0MHz, Fin = 4.0MHz, SINGLE-ENDED INPUT MODE

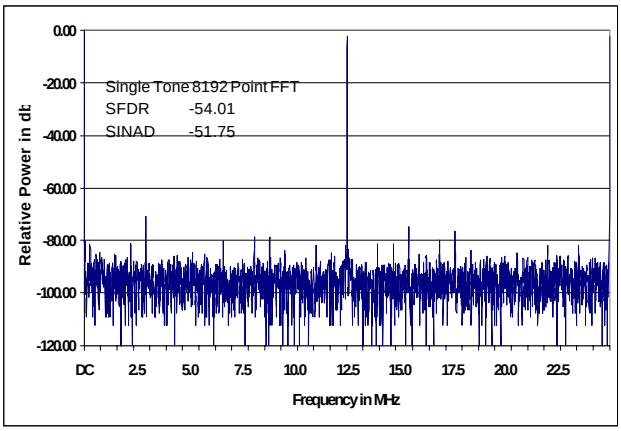


Figure 15 - FFT SPECTRUM @Fclock = 50.0MHz, Fin = 12.5MHz, SINGLE-ENDED INPUT MODE

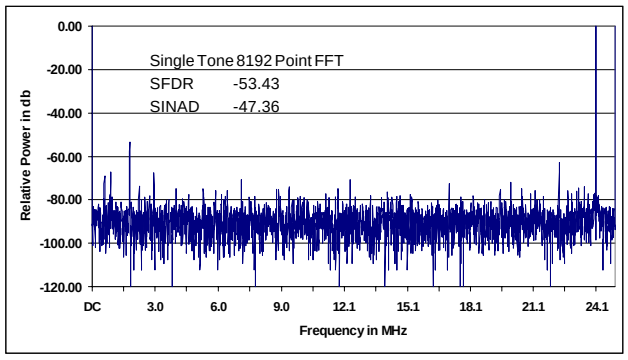


Figure 16 - SINAD @Fclock = 50.0MHz, Fin = 24.1MHz, SINGLE-ENDED INPUT MODE

Notes

NOTICE

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