XRD8785

CMOS 8-Bit High Speed Analog-to-Digital Converter

April 2002

FEATURES

- 8-Bit Resolution
- Up to 20 MHz Sampling Rate
- Internal S/H Function
- Single Supply: 5V
- VIN DC Range: 0V to V_{DD}
- VREF DC Range: 1V to V_{DD}
- Low Power: 75mW typ. (excluding reference)
- Latch-Up Free
- ESD Protection: 2000V Minimum
- 20-Pin Package Available: XRD8775
- 3V Version: XRD87L85

APPLICATIONS

- Digital Color Copiers
- Cellular Telephones
- CCDs and Scanners
- Video Capture Boards

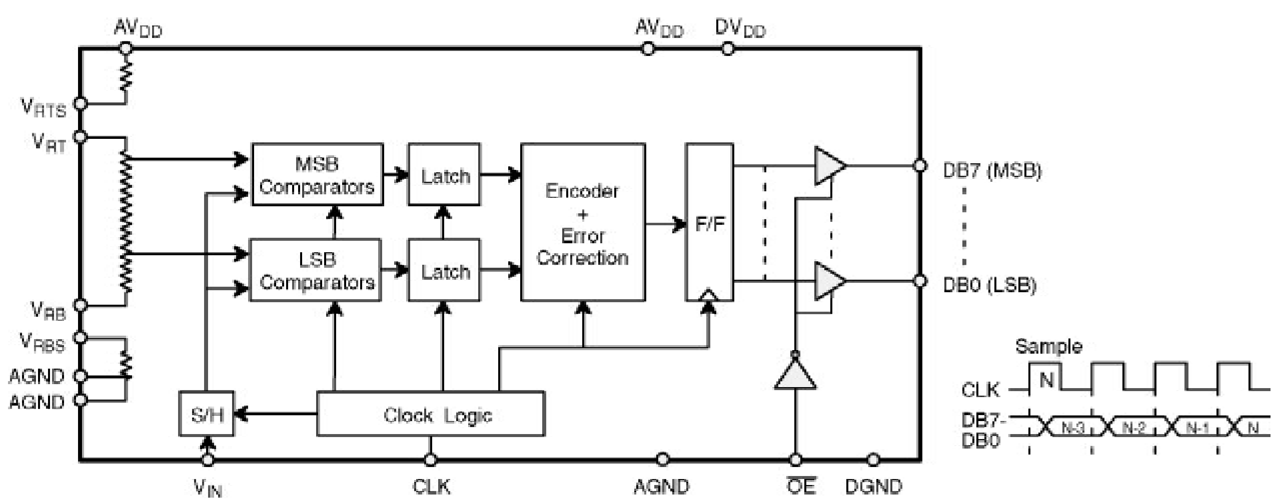
GENERAL DESCRIPTION

The XRD8785 is an 8-bit Analog-to-Digital Converter. Designed using an advanced 5V CMOS process, this part offers excellent performance, low power consumption, and latch-up free operation.

This device uses a two-step flash architecture to maintain low power consumption at high conversion rates. The input circuitry of the XRD8785 includes an on-chip S/H function which allows the user to digitize analog input signals between AGND and AV_{DD}. Careful design and chip layout have achieved a low analog input capacitance. This reduces “kickback” and eases the requirements of the buffer/amplifier used to drive the XRD8785. The designer can choose the internally generated reference voltages by connecting V_{RB} to V_{RBS} and V_{RT} to V_{RTS}, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 0.6V at V_{RB} and 2.6 V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between AGND and AV_{DD}. This also allows the system to adjust these voltages to cancel zero scale and full scale errors, or to change the input range as needed.

The device operates from a single +5V supply. Power consumption is 75mW at FS = 15MHz. Specified for operation over the commercial/industrial (–40 to +85°C) temperature range, the XRD8785 is available in Plastic Dual-in-line (PDIP), Surface Mount (SOIC) and Small Outline (SOP) packages in EIAJ and JEDEC.

SIMPLIFIED BLOCK AND TIMING DIAGRAM



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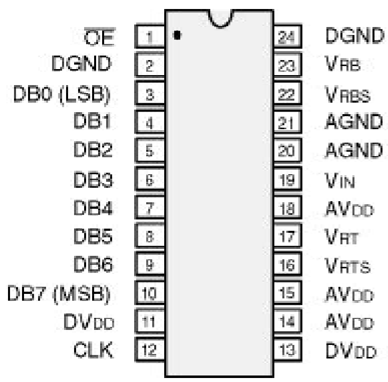
ORDERING INFORMATION

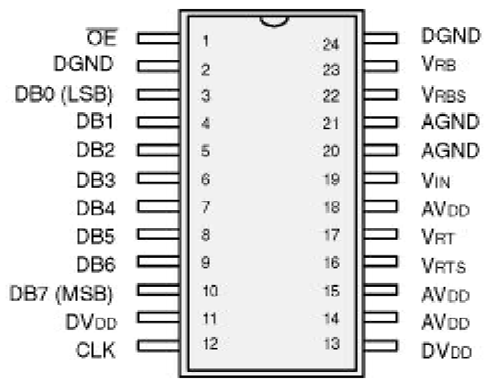
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC (Jedec)	–40 to +85°C	XRD8785AID	+/- 0.75	+/-1.5
SOP (EIAJ)	–40 to +85°C	XRD8785AIK	+/- 0.75	+/-1.5
Plastic Dip (300MIL)	–40 to +85°C	XRD8785AIP	+/- 0.75	+/-1.5

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24-Pin PDIP (300 MIL) - P24



24-Pin SOP (EIAJ, 5.4mm) – K24
24-Pin SOIC (Jedec, 300 MIL) – D24

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION	PIN NO.	NAME	DESCRIPTION
1	$\overline{OE}$	Output Enable	13	DV_{DD}	Digital Power Supply
2	DGND	Digital Ground	14	AV_{DD}	Analog Power Supply
3	DB0	Data Output Bit 0 (LSB)	15	AV_{DD}	Analog Power Supply
4	DB1	Data Output Bit 1	16	V_{RTS}	Generates 2.6 V if tied to V_{RT}
5	DB2	Data Output Bit 2	17	V_{RT}	Top Reference
6	DB3	Data Output Bit 3	18	AV_{DD}	Analog Power Supply
7	DB4	Data Output Bit 4	19	VIN	Analog Input
8	DB5	Data Output Bit 5	20	AGND	Analog Ground
9	DB6	Data Output Bit 6	21	AGND	Analog Ground
10	DB7	Data Output Bit 7 (MSB)	22	V_{RBS}	Generates 0.6 V if tied to V_{RB}
11	DV_{DD}	Digital Power Supply	23	V_{RB}	Bottom Reference
12	CLK	Sampling Clock Input	24	DGND	Digital Ground

ELECTRICAL CHARACTERISTICS TABLE
UNLESS OTHERWISE SPECIFIED: AV_{DD} = DV_{DD} = 5V, FS = 15MHZ (50% DUTY CYCLE), V_{RT} = 2.6V, V_{RB} = 0.6V, T_A = 25°C

			25°C			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions/Comments**
KEY FEATURES						
Resolution		8			Bits	
Sampling Rate	FS	0.1	15	20	MHz	
ACCURACY						
Differential Non-Linearity	DNL			+/-0.75	LSB	@ 15MHz
Differential Non-Linearity	DNL		+/-0.5		LSB	@ 10MHz
Integral Non-Linearity	INL			+/-1.5	LSB	Best Fit Line (Max INL – Min INL)/2
Zero Scale Error	EZS		+3		LSB	
Full Scale Error	EFS		-2		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage	V_{RT}		2.6	AV_{DD}	V	
Negative Ref. Voltage	V_{RB}	AGND	0.6		V	
Differential Ref. Voltage[3]	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} - V_{RB}$
Ladder Resistance	R_L	245	350	550	Ω	
Ladder Temp. Coefficient	R_{TCO}		2000		ppm/°C	
Self Bias 1						
Short V_{RB} and V_{RBS}	V_{RB}		0.6		V	
Short V_{RT} and V_{RTS}	V_{RT}-V_{RB}		2		V	
Self Bias 2						
V_{RB} = AGND, Short V_{RT} and V_{RTS}	V_{RT}		2.3		V	
ANALOG INPUT						
Input Bandwidth (–1 dB)[2, 4]	BW		50		MHz	
Input Voltage Range	V_{IN}	V_{RB}		V_{RT}	V	
Input Capacitance [5]	C_{IN}		16		pF	
Aperture Delay[2]	t_{AP}		3		ns	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	4.0			V	
Logical "0" Voltage	V_{IL}			1.0	V	
DC Leakage Currents [6]	I_{IN}					V_{IN} =DGND to DV_{DD}
CLK			5		µA	
$\overline{OE}$			5		µA	
Input Capacitance			5		pF	
Clock Timing (See Figure 1.)[7]						
Clock Period	1/FS	50	66.7		ns	
High Pulse Width	t_{PWH}	25	33.3		ns	
Low Pulse Width	t_{PWL}	25	33.3		ns	
DIGITAL OUTPUTS						**C_{OUT} =15 pF**
Logical "1" Voltage	V_{OH}	4.5			V	I_{LOAD} = 4 mA
Logical "0" Voltage	V_{OL}			0.4	V	I_{LOAD} = 4 mA
3-state Leakage	I_{OZ}		10		µA	V_{OUT} =DGND to DV_{DD}
Data Valid Delay [8]	t_{DL}		10		ns	
Data Enable Delay	t_{DEN}		5		ns	
Data 3-state Delay	t_{DHZ}		5		ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)
UNLESS OTHERWISE SPECIFIED: $AV_{DD} = DV_{DD}$ = 5V, FS = 15MHZ (50% DUTY CYCLE), V_{RT} = 2.6V, V_{RB} = 0.6V, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
AC PARAMETERS						
Differential Gain Error	dg		2		%	FS = 4 x NTSC
Differential Phase Error	d_{ph}		1		Degree	FS = 4 x NTSC
POWER SUPPLIES						
Operating Voltage (AV_{DD}, DV_{DD})[9]	V_{DD}	4.5	5	5.5	V	
Current (AGND + DGND)	I_{DD}		15	25	mA	Does not include ref. current

NOTES

1. The difference between the measured and the ideal code width (V_{REF}/256) is the DNL error (Figure 3). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (Figure 4). Accuracy is a function of the sampling rate (FS).
2. Guaranteed, not tested
3. Specified values guarantee functionality. Refer to other parameters for accuracy.
4. –1dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.
5. See V_{IN} input equivalent circuit (Figure 5). Switched capacitor analog input requires driver with low output resistance.
6. All inputs have diodes to DV_{DD} and DGND. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.
7. t_R, t_F should be limited to >5ns for best results.
8. Depends on the RC load connected to the output pin.
9. AGND & DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND 7V
V_{RT} & V RB .... V_{DD} +0.5 to GND –0.5V
V_{IN} .... V_{DD} +0.5 to GND –0.5V
All Inputs .... V_{DD} +0.5 to GND –0.5V
All Outputs .... V_{DD} +0.5 to GND –0.5V

Storage Temperature ....–65 to +150°C
Lead Temperature (Soldering 10 seconds) ... +300°C
Package Power Dissipation Rating @ 75°C
PDIP, SOIC, SOP 675mW
Derates above 75°C .... 12mW/°C

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100ms.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

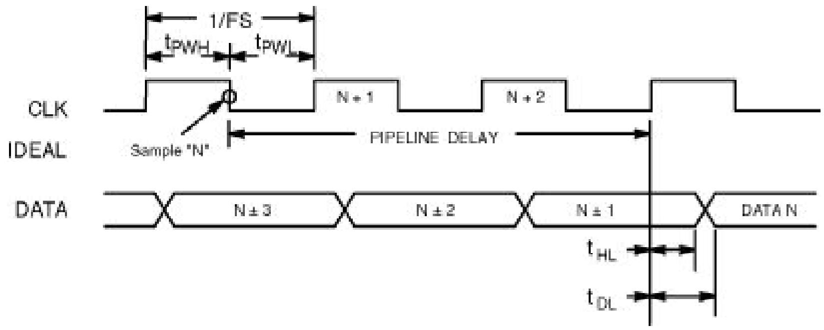


Figure 1. XRD8785 Timing Diagram

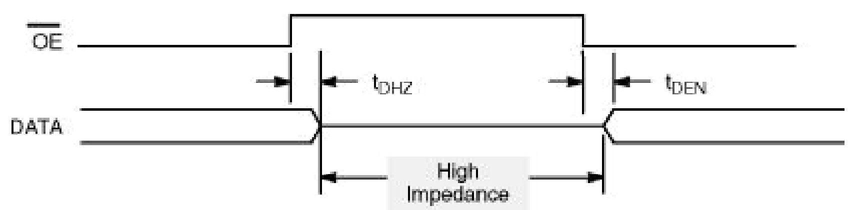


Figure 2. Output Enable/Disable Timing Diagram

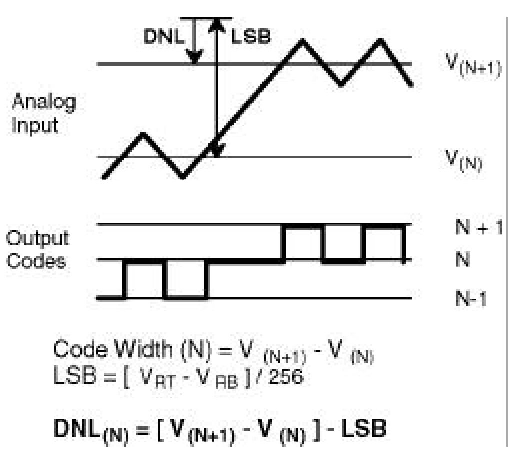


Figure 3. DNL Measurement

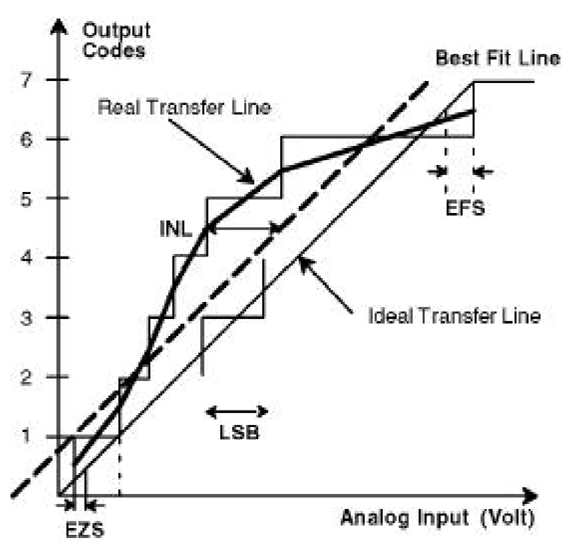


Figure 4. INL Error Calculation

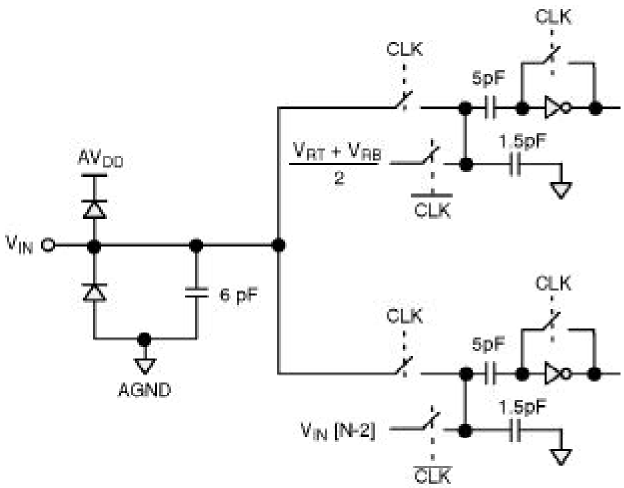


Figure 5. Equivalent Input Circuit

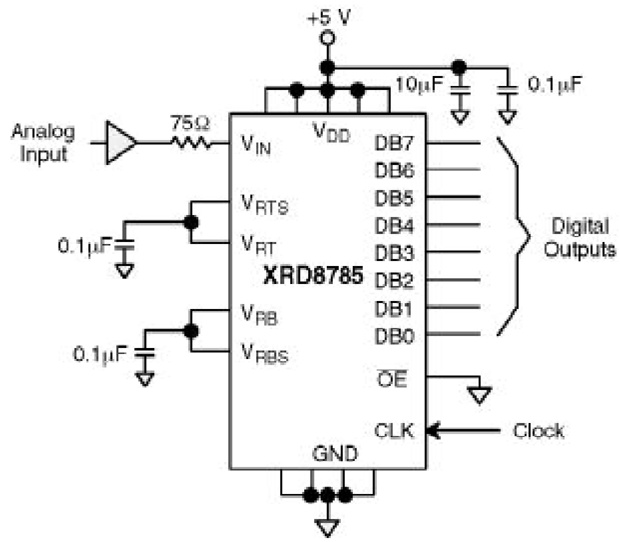


Figure 6. Typical Circuit Connections

APPLICATION NOTES

Signals should not exceed V_{DD} +0.5V or go below GND –0.5V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGND and DGND pins are connected internally through the P-substrate. DC voltage differences between GND pins will cause undesirable internal substrate currents.

The power supply (V_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

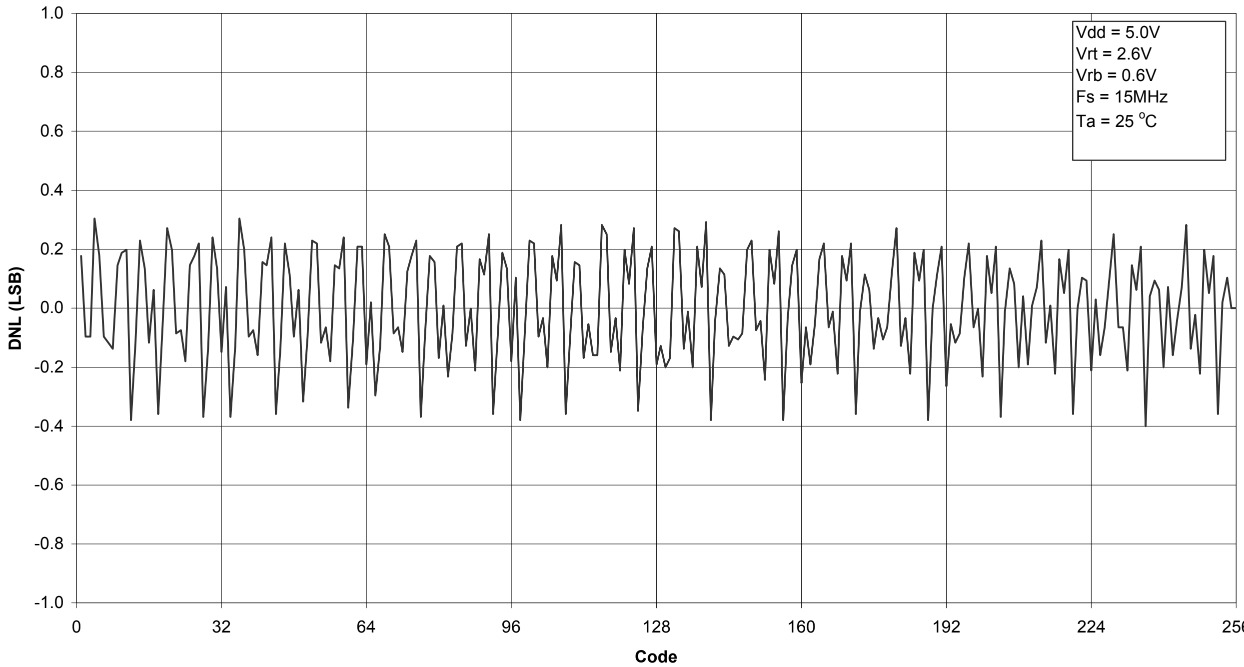
To avoid timing errors, use the rising edge of the sample clock (CLK) to latch data from the XRD8785 to other parts of the system.

The reference can be biased internally by shorting V_{RT} to V_{RTS} and V_{RB} to V_{RBS}. This will generate 0.6V at V_{RB} and 2.6V at V_{RT} (see Figure 5).

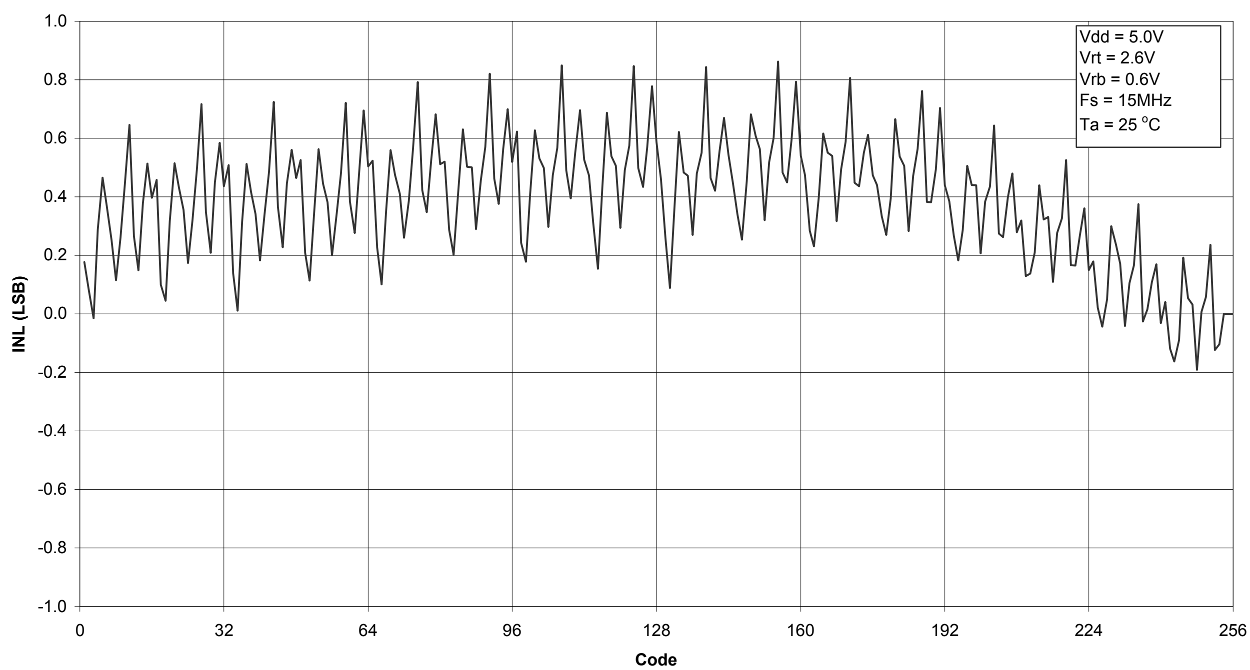
If the internal reference pins V_{RTS} and/or V_{RBS} are not used, they should be left unconnected.

The output enable pin ($\overline{OE}$) should not be left unconnected. If not controlled by an active signal then it must be tied to a logic low value.

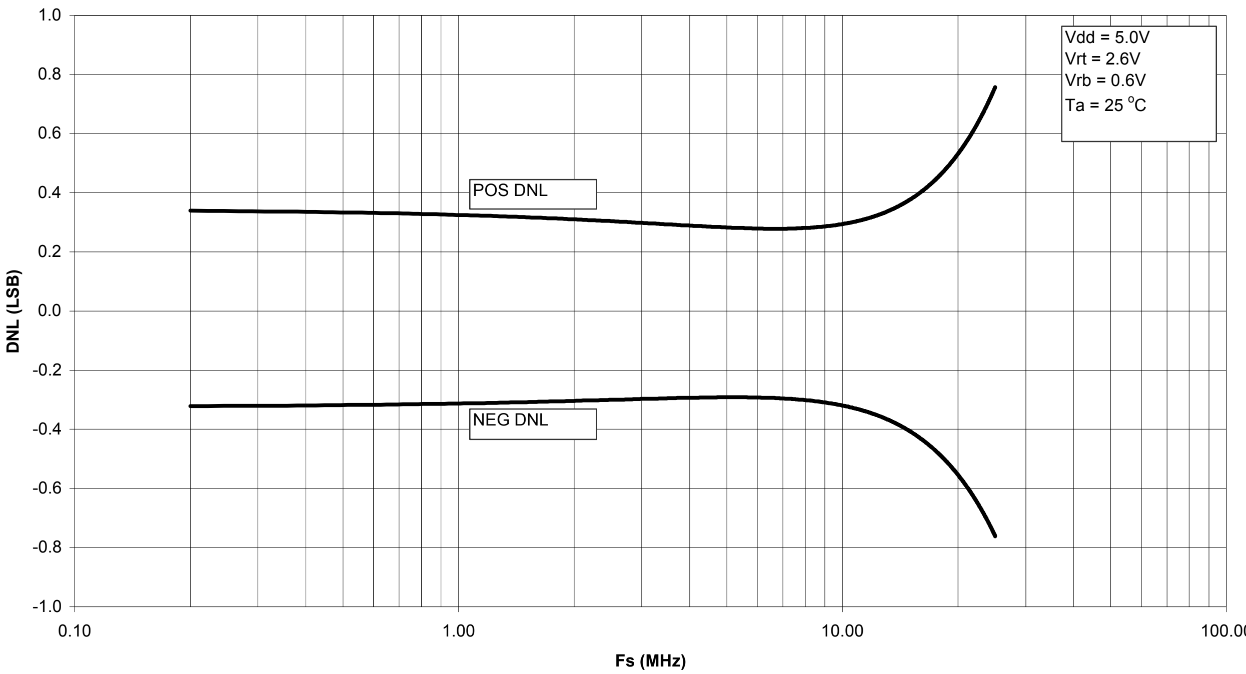
PERFORMANCE CHARACTERISTICS



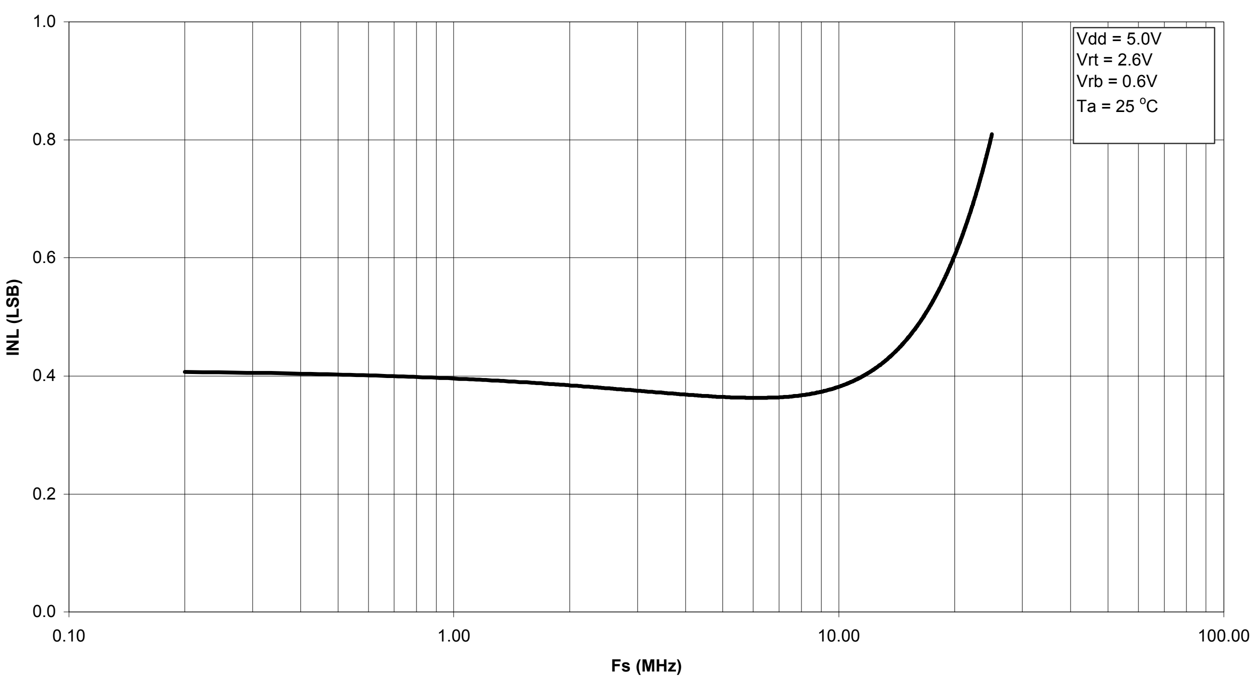
Graph 1. DNL vs. Code



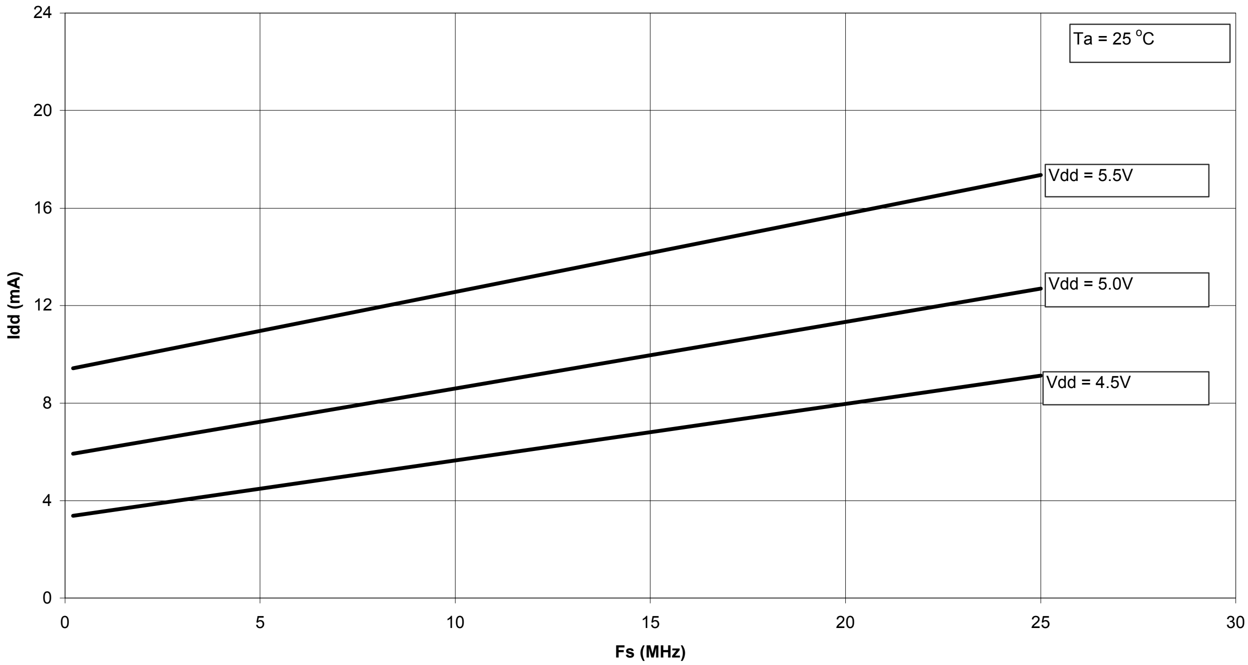
Graph 2. INL vs. Code



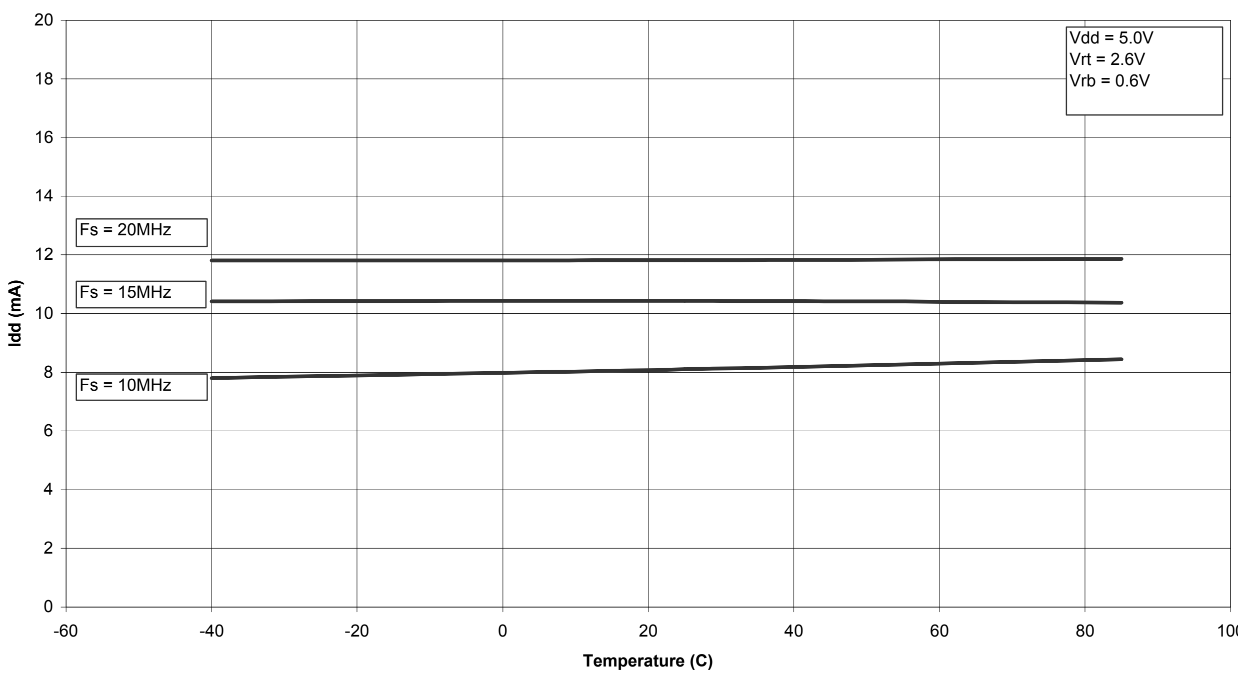
Graph 3. DNL vs. Sampling Frequency



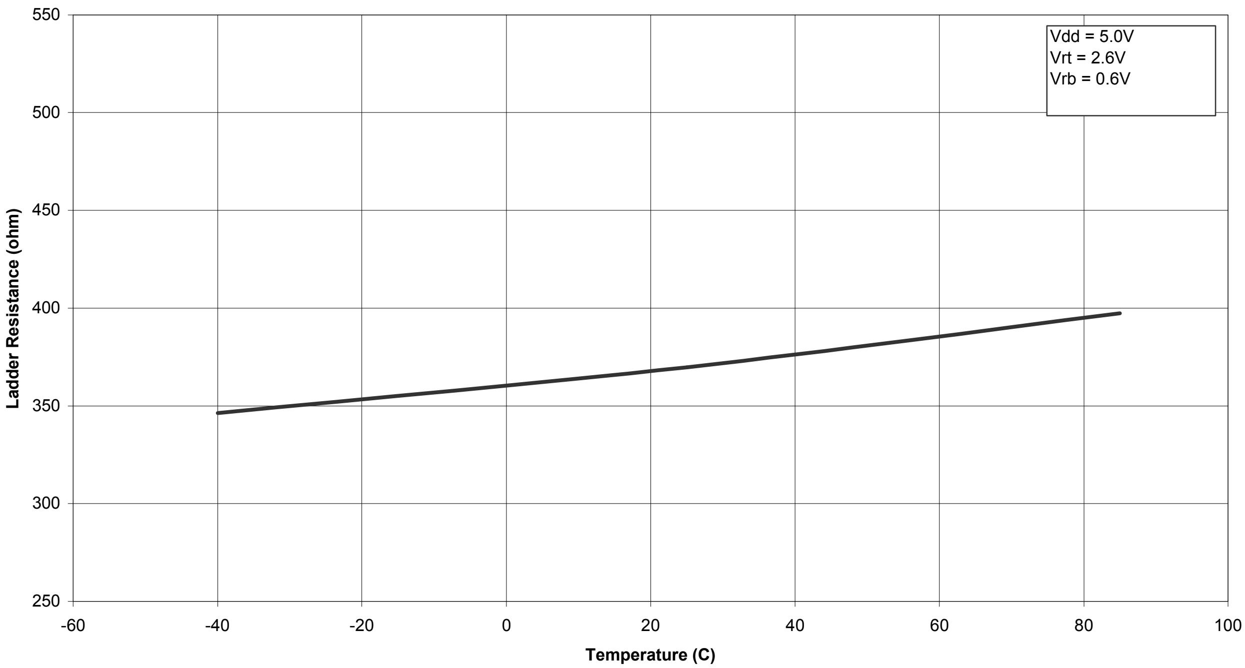
Graph 4. Best Fit INL vs. Sampling Frequency



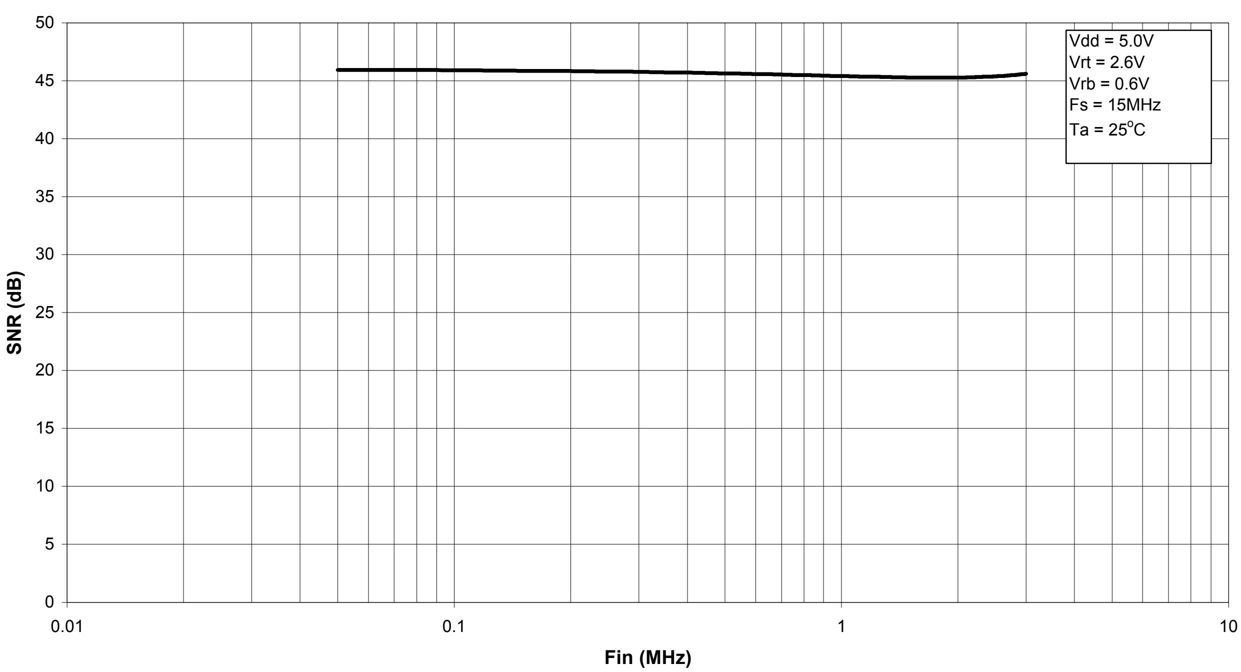
Graph 5. IDD vs. Sampling Frequency



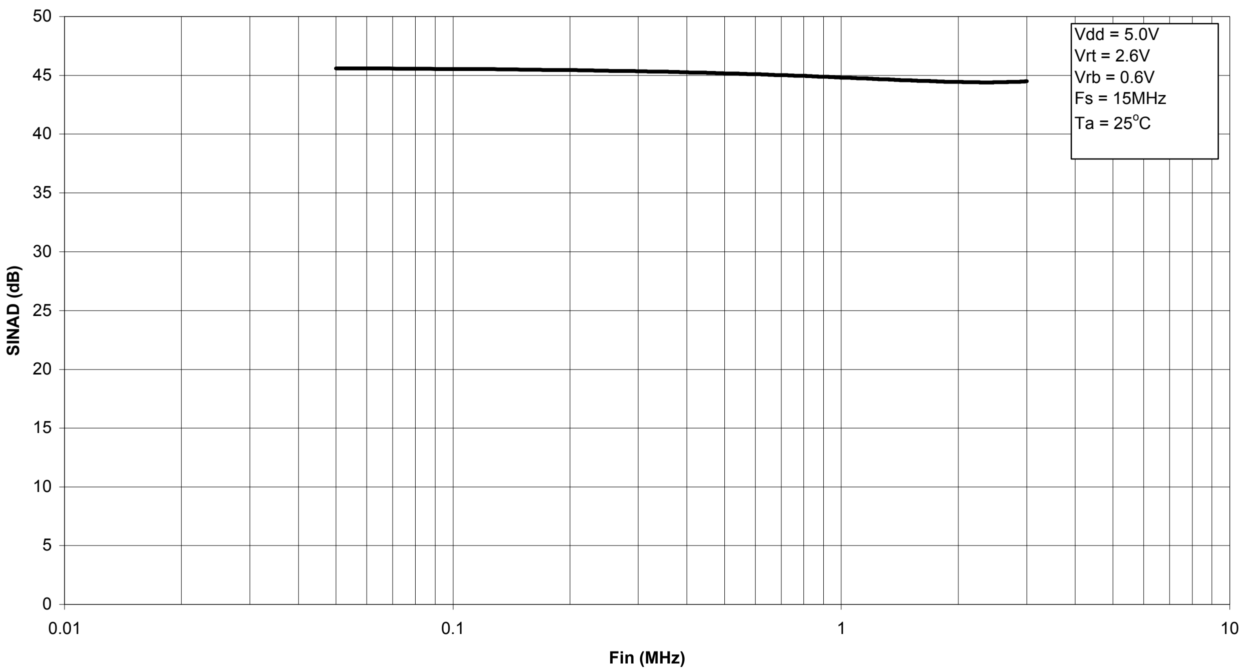
Graph 6. Supply Current vs. Temperature



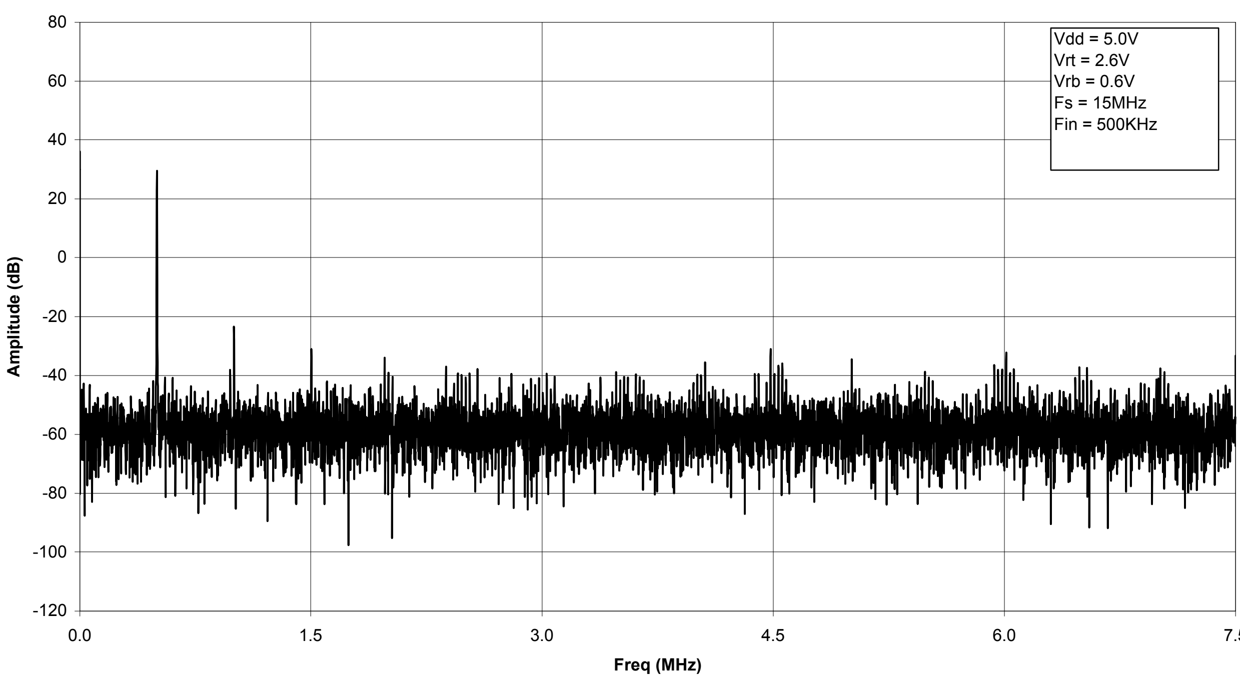
Graph 7. Ladder Resistance vs. Temperature



Graph 8. SNR vs. Input Frequency

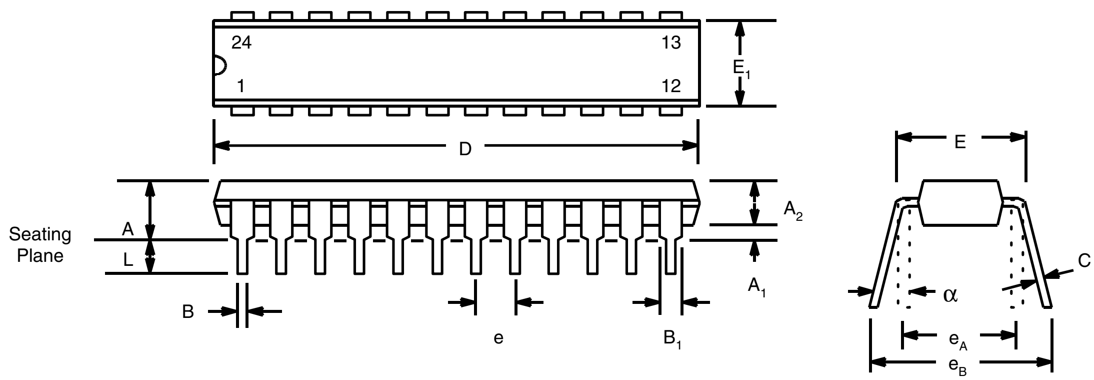


Graph 9. SINAD vs. Input Frequency



Graph 10. FFT Plot

24 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
REV. 1.00

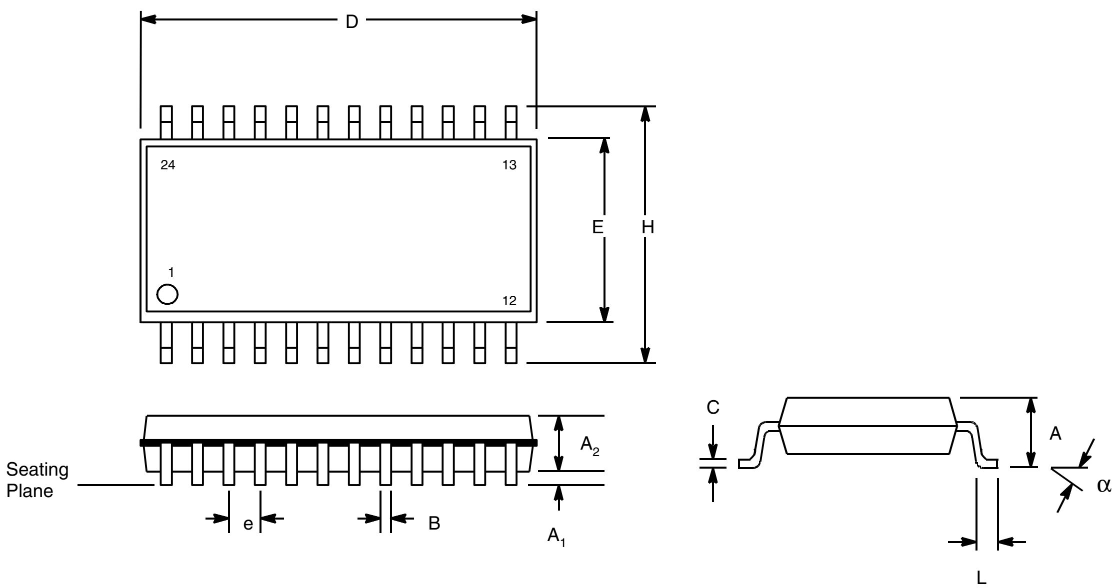


Note: The control dimension is the inch column

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.145	0.210	3.68	5.33
A1	0.015	0.070	0.38	1.78
A2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	1.125	1.275	28.58	32.39
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eA	0.300 BSC		7.62 BSC	
eB	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	5.08
a	0°	15°	0°	15°

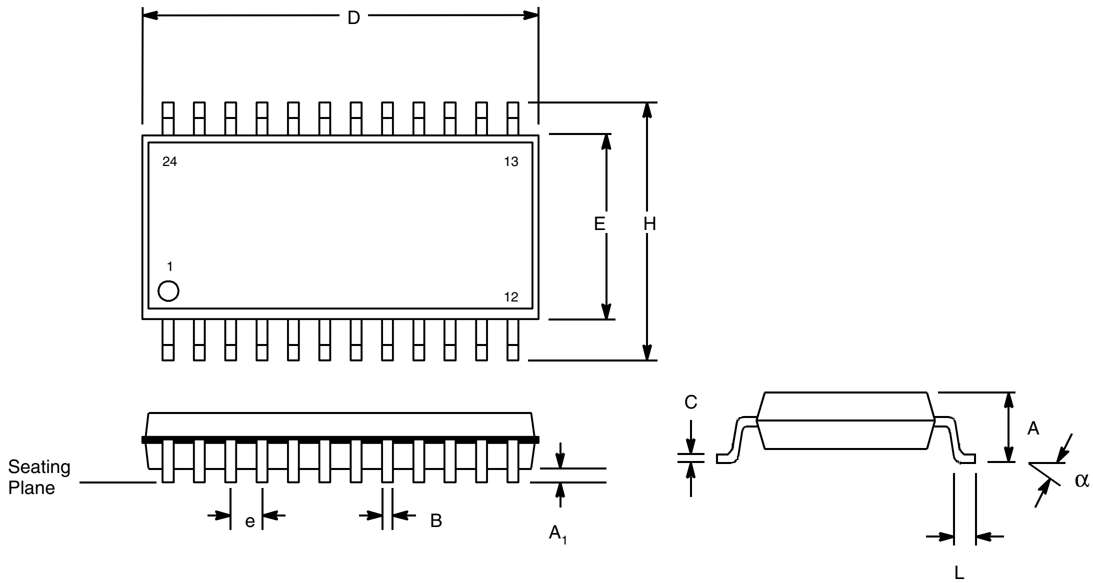
24 LEAD EIAJ SMALL OUTLINE
(5.4 mm EIAJ SOP)

REV. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.069	0.083	1.75	2.10
A1	0.002	0.008	0.05	0.20
A2	0.067	0.075	1.70	1.90
B	0.012	0.020	0.30	0.50
C	0.004	0.008	0.10	0.20
D	0.587	0.594	14.90	15.10
E	0.209	0.217	5.30	5.50
e	0.050 BSC		1.27 BSC	
H	0.299	0.315	7.60	8.00
L	0.012	0.030	0.30	0.76
a	0°	10°	0°	10°

24 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
REV. 1.00



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.598	0.614	15.20	15.60
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
a	0°	8°	0°	8°

NOTICE

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