

LOW POWER, 2 MSPS, 10-BIT, A/D CONVERTER WITH 8-CHANNEL MUX

FEBRUARY 2001

REV. 1.0.0

FEATURES

- 10-Bit Resolution
- 8-Channel Mux
- Sampling Rate - < 1kHz - 2MHz
- Low Power CMOS - 24 mW (typ)
- Power Down; Lower Consumption - 0.1 mW (typ)
- Input Range between GND and V_{DD}
- No S/H Required for Analog Signals less than 100kHz
- No S/H Required for CCD Signals less than 2MHz
- Single Power Supply (2.7 to 3.6V)
- Latch-Up Free
- ESD Protection: 2000 Volts Minimum

APPLICATIONS

- μ P/DSP Interface and Control Application
- High Resolution Imaging - Scanners & Copiers
- Wireless Digital Communications
- Multiplexed Data Acquisition

BENEFITS

- Reduced Board Space (Small Package)
- Reduced External Parts, No Sample/Hold Needed
- Suitable for Battery & Power Critical Applications
- Designer can Adapt Input Range & Scaling

GENERAL DESCRIPTION

The XRD87L99 is a flexible, easy to use, precision 10-bit analog-to-digital converter with 8-channel mux that operates over a wide range of input and sampling conditions. The XRD87L99 can operate with pulsed "on demand" conversion operation or continuous "pipeline" operation for sampling rates up to 2MHz. The elimination of the S/H requirements, very low power, and small package size offer the designer a low cost solution. No sample and hold is required for CCD applications up to 2MHz, or multiplexed input applications when the signal source bandwidth is limited to 100kHz. The input architecture of the XRD87L99 allows direct interface to any analog input range between AGND and AV_{DD} . The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

Scaled reference resistor taps @ 1/4 R, 1/2 R and 3/4 R allow for customizing the transfer curve as well as providing a 1/2 span reference voltage. Digital outputs are CMOS and TTL compatible.

The XRD87L99 uses a two-step flash technique. The first segment converts the 5 MSBs and consists of autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 5 LSBs.

When the power down input is "high", the data outputs DB9 to DB0 hold the current values and $V_{REF(-)}$ is disconnected from $V_{REF1(-)}$. The power consumption during the power down mode is 0.1mW.

ORDERING INFORMATION

| PART NUMBER | PACKAGE | OPERATING TEMPERATURE RANGE |
|-------------|---------|-----------------------------|
| XRD87L99AIQ | PQFP | -40°C to +85°C |

FIGURE 1. SIMPLIFIED BLOCK DIAGRAM AND TIMING

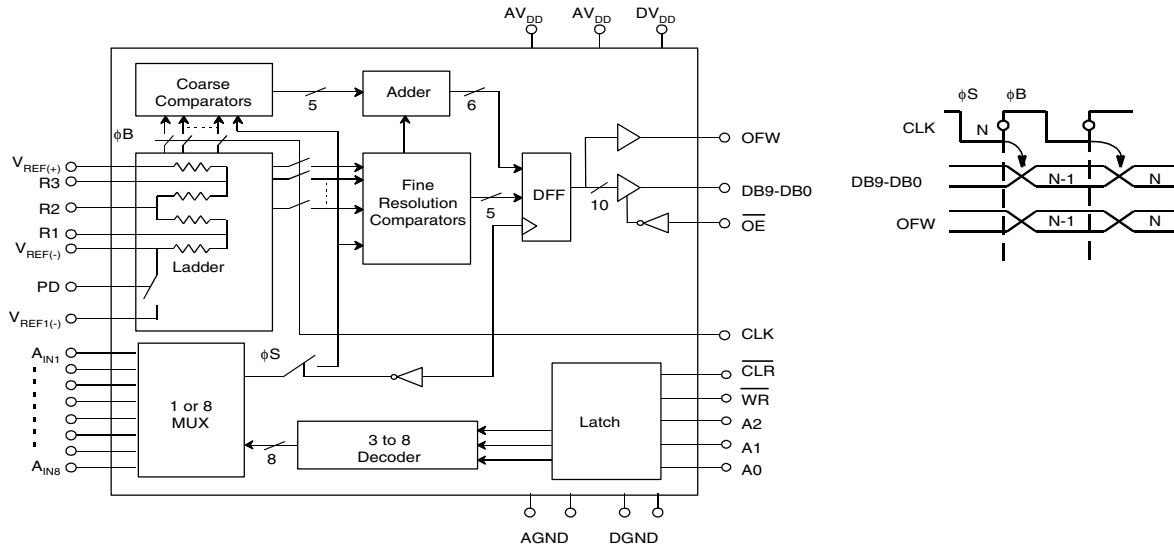
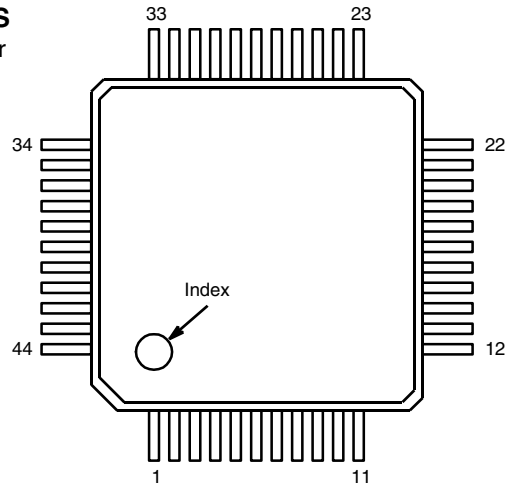


FIGURE 2. PIN OUT OF THE XRD87L99

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



44-Pin PQFP (10mm x 10mm)

PIN DESCRIPTIONS

| PIN # | NAME | DESCRIPTION |
|-------|-------------------------|----------------------------|
| 1 | DB6 | Data Output Bit 6 |
| 2 | DB7 | Data Output Bit 7 |
| 3 | DGND | Digital Ground |
| 4 | DGND | Digital Ground |
| 5 | DV _{DD} | Digital V _{DD} |
| 6 | $\overline{\text{CLR}}$ | Clear (Active Low) |
| 7 | $\overline{\text{WR}}$ | Write (Active Low) |
| 8 | A2 | Address 2 |
| 9 | A1 | Address 1 |
| 10 | A0 | Address 0 |
| 11 | CLK | Clock Input |
| 12 | $\overline{\text{OE}}$ | Output Enable (Active Low) |
| 13 | N/C | No Connect |
| 14 | DB8 | Data Output Bit 8 |
| 15 | DB9 | Data Output Bit 9 (MSB) |
| 16 | OFW | Overflow Output |
| 17 | V _{REF(+)} | Upper Reference Voltage |
| 18 | V _{REF(-)} | Lower Reference Voltage |
| 19 | V _{REF1(-)} | Lower Reference Voltage |
| 20 | R1 | Reference Ladder Tap |
| 21 | R2 | Reference Ladder Tap |
| 22 | A _{IN8} | Analog Signal Input 8 |

| PIN # | NAME | DESCRIPTION |
|-------|------------------|-------------------------|
| 23 | R3 | Reference Ladder Tap |
| 24 | N/C | No Connect |
| 25 | A _{IN1} | Analog Signal Input 1 |
| 26 | A _{IN2} | Analog Signal Input 2 |
| 27 | A _{IN3} | Analog Signal Input 3 |
| 28 | A _{IN4} | Analog Signal Input 4 |
| 29 | A _{IN5} | Analog Signal Input 5 |
| 30 | AGND | Analog Ground |
| 31 | AV _{DD} | Analog V _{DD} |
| 32 | AV _{DD} | Analog V _{DD} |
| 33 | A _{IN6} | Analog Signal Input 6 |
| 34 | AGND | Analog Ground |
| 35 | PD | Power Down |
| 36 | A _{IN7} | Analog Signal Input 7 |
| 37 | DB0 | Data Output Bit 0 (LSB) |
| 38 | DB1 | Data Output Bit 1 |
| 39 | DB2 | Data Output Bit 2 |
| 40 | DB3 | Data Output Bit 3 |
| 41 | DB4 | Data Output Bit 4 |
| 42 | DB5 | Data Output Bit 5 |
| 43 | N/C | No Connect |
| 44 | N/C | No Connect |

TABLE 1: TRUTH TABLE FOR INPUT CHANNEL SELECTION

| \overline{CLR} | WR | A2 | A1 | A0 | Selected Analog Input |
|------------------|----|----|----|----|-----------------------|
| L | X | X | X | X | A_{IN1} |
| H | L | L | L | L | A_{IN1} |
| H | L | L | L | H | A_{IN2} |
| H | L | L | H | L | A_{IN3} |
| H | L | L | H | H | A_{IN4} |
| H | L | H | L | L | A_{IN5} |
| H | L | H | L | H | A_{IN6} |
| H | L | H | H | L | A_{IN7} |
| H | L | H | H | H | A_{IN8} |
| H | H | X | X | X | Previous Selection |

NOTE: \overline{CLR} , \overline{WR} , A2, A1, A0 are internally connected to ground through 500k Ω resistance.

ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS $AV_{DD} = DV_{DD} = 3\text{ V}$, $F_S = 2\text{ MHz}$ (50% DUTY CYCLE), $V_{REF(+)} = 2.6$, $V_{REF(-)} = \text{AGND}$, $T_A = 25^\circ\text{C}$, UNLESS OTHERWISE SPECIFIED

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | TEST CONDITIONS/COMMENTS |
|---|--------------|--------------|-----------|---------------|---------------|---|
| KEY FEATURES | | | | | | |
| Resolution | | | | 10 | Bits | |
| Sampling Rate | FS | .001 | | 2.0 | MHz | For Rated Performance |
| ACCURACY (A GRADE)² | | | | | | |
| Differential Non-Linearity | DNL | -1 | ± 0.3 | 1 | LSB | |
| Integral Non-Linearity | INL | | 1 | 2 | LSB | Best Fit Line (Max INL - Min INL)/2 |
| Zero Scale Error | EZS | 0 | 50 | 100 | mV | |
| Full Scale Error | EFS | 0 | 30 | 60 | mV | |
| REFERENCE VOLTAGES | | | | | | |
| Positive Ref. Voltage ⁵ | $V_{REF(+)}$ | 1.0 | 3.0 | AV_{DD} | V | |
| Negative Ref. Voltage ⁵ | $V_{REF(-)}$ | AGND | 1.0 | $AV_{DD} - 1$ | V | |
| Differential Ref. Voltage ⁵ | V_{REF} | 1.0 | 2.0 | AV_{DD} | V | |
| Ladder Resistance | RL | 500 | 1200 | 2000 | W | |
| ANALOG INPUT¹ | | | | | | |
| Input Bandwidth (-1dB) | | 1.0 | | 4.0 | MHz | 1-Channel |
| Input Bandwidth (-1dB) | | 0.125 | | 0.5 | MHz | 8-Channel |
| Input Voltage Range ⁷ | V_{IN} | $V_{REF(-)}$ | | $V_{REF(+)}$ | V | |
| Input Capacitance ³ | C_{IN} | | 20 | | pF | |
| Aperture Delay ¹ | t_{AP} | | 8 | | ns | |
| DIGITAL INPUTS | | | | | | |
| Logical "1" Voltage | V_{IH} | 2.0 | | | V | |
| Logical "0" Voltage | V_{IL} | | | 0.8 | V | |
| Leakage Currents | I_{IN} | | | | | $V_{IN} = \text{DGND to } DV_{DD}$ |
| CLK | | -1 | | 1 | μA | |
| $\overline{\text{CLR}}$, $\overline{\text{WR}}$, A2, A1, A0, PD, $\overline{\text{OE}}$ | | -5 | | 30 | μA | These input pins have 500k Ω internal resistors to GND |
| Input Capacitance | | | 5 | | pF | |

ELECTRICAL CHARACTERISTICS $AV_{DD} = DV_{DD} = 3\text{ V}$, $F_S = 2\text{ MHz}$ (50% DUTY CYCLE), $V_{REF(+)} = 2.6$, $V_{REF(-)} = \text{AGND}$, $T_A = 25^\circ\text{C}$, UNLESS OTHERWISE SPECIFIED

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | TEST CONDITIONS/COMMENTS |
|--|--------------|---------------|-----|-----------|---------------|--|
| Clock Timing | | | | | | |
| Clock Period | T_S | 500 | | 1,000,000 | ns | |
| Rise & Fall Time ⁴ | t_R, t_F | | | 10 | ns | |
| "High" Time | t_B | 125 | 250 | 500,000 | ns | |
| "Low" Time | t_S | 125 | 250 | 500,000 | ns | |
| DIGITAL OUTPUTS | | | | | | $C_{OUT}=15\text{ pF}$ |
| Logical "1" Voltage | V_{OH} | $DV_{DD}-0.5$ | | | V | $I_{LOAD} = 2\text{ mA}$ |
| Logical "0" Voltage | V_{OL} | | | 0.5 | V | $I_{LOAD} = 2\text{ mA}$ |
| Tristate Leakage | I_{OZ} | -1 | | 1 | μA | $V_{OUT} = 0\text{ to }DV_{DD}$ |
| Data Hold Time ¹ | t_{HLD} | | 12 | | ns | |
| Data Valid Delay ¹ | t_{DL} | | 30 | 35 | ns | |
| Write Pulse Width ¹ | t_{WR} | 40 | | | ns | |
| Multiplexer Address Setup Time ¹ | t_{AS} | 80 | | | ns | |
| Multiplexer Address Hold Time ¹ | t_{AH} | 0 | | | ns | |
| Delay from \overline{WR} to Multiplexer ¹ | | | | | | |
| Enable | t_{MUXEN1} | | | 80 | ns | |
| Clock to PD Setup Time | t_{CLKS1} | | | 400 | ns | |
| Clock to UR Setup Time | t_{CLKS2} | 0 | | | ns | |
| Clock to PD Hold Time | t_{CLKH1} | | | 600 | ns | |

ELECTRICAL CHARACTERISTICS $AV_{DD} = DV_{DD} = 3\text{ V}$, $F_S = 2\text{ MHz}$ (50% DUTY CYCLE), $V_{REF(+)} = 2.6$, $V_{REF(-)} = \text{AGND}$, $T_A = 25^\circ\text{C}$, UNLESS OTHERWISE SPECIFIED

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | TEST CONDITIONS/COMMENTS |
|---|--------------------|-----|------|------|--------|--|
| Clock to $\overline{\text{WR}}$ Hold Time | t_{CLKH2} | 0 | | | ns | |
| Power Down Time ¹ | t_{PD} | | | 300 | ns | |
| Power Up Time ¹ | t_{PU} | | | 200 | ns | |
| Data Enable Delay | t_{DEN} | | 14 | 16 | ns | |
| Data High Z Delay | t_{DHZ} | | 4 | 6 | ns | |
| Pipeline Delay (Latency) | | | 1.5 | | cycles | |
| POWER SUPPLIES ⁸ | | | | | | |
| Power Down (I_{DD}) | $I_{\text{PD-DD}}$ | | 0.01 | 0.10 | mA | PD=High, CLK High or Low |
| Operating Voltage (AV_{DD} , DV_{DD}) | V_{DD} | 2.7 | 3.0 | 3.6 | V | |
| Current ($AV_{\text{DD}} + DV_{\text{DD}}$) | I_{DD} | | 7 | 10 | mA | PD=Low (Normal Mode) $V_{\text{DD}} = 3\text{ V}$ |

NOTES:

- 1 Guaranteed. Not tested.
- 2 Tester measures code transition voltages by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value ($V_{\text{REF}}/1024$) is the DNL error. The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage.
- 3 See V_{IN} input equivalent circuit.
- 4 Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.
- 5 Specified values guarantee functional device. Refer to other parameters for accuracy.
- 6 System can clock the XRD87L99 with any duty cycle as long as all timing conditions are met.
- 7 Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.
- 8 DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package.

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

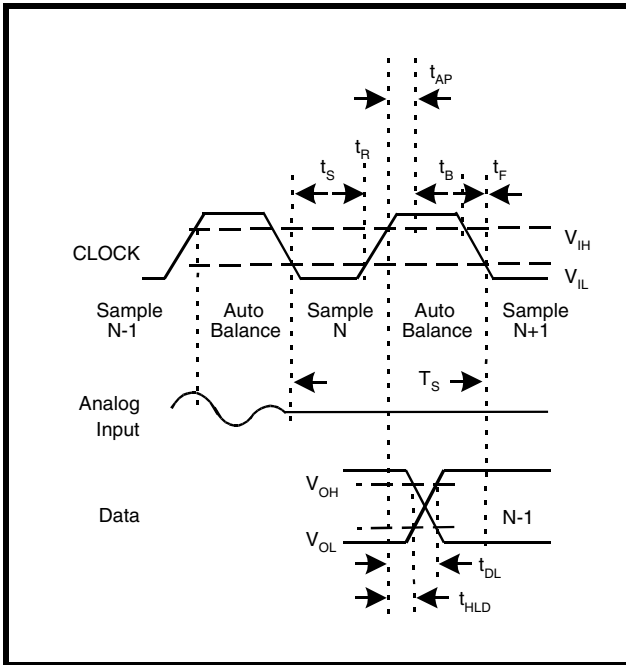
ABSOLUTE MAXIMUM RATINGS: ($T_A = +25^\circ\text{C}$ UNLESS OTHERWISE NOTED)^{1, 2, 3}

| | |
|--|------------------------------|
| V_{DD} (to GND) | +7 V |
| $V_{REF(+)}$, $V_{REF(-)}$, $V_{REF(-)}$ | GND -0.5 to $V_{DD} + 0.5$ V |
| All A_{INs} | GND -0.5 to $V_{DD} + 0.5$ V |
| All Inputs | GND -0.5 to $V_{DD} + 0.5$ V |
| All Outputs | GND -0.5 to $V_{DD} + 0.5$ V |
| Storage Temperature | -65 to +150°C |
| Lead Temperature (Soldering 10 seconds) | +300°C |
| Package Power Dissipation Rating to 75°C | |
| PQFP | 450mW |
| Derates above 75°C | 14mW/°C |

NOTE:

- 1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- 2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps(HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100ns.
- 3 V_{DD} refers to AV_{DD} and DV_{DD} . GND refers to AGND and DGND.

FIGURE 3. XRD87L99 TIMING DIAGRAM



THEORY OF OPERATION

1.0 ANALOG-TO-DIGITAL CONVERSION

The XRD87L99 converts analog voltages into 1024 digital codes by encoding the outputs of coarse and fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 2 clock periods.

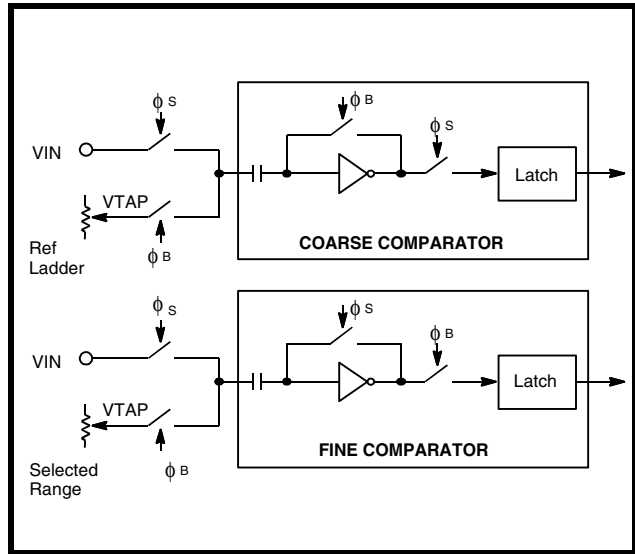
The reference resistance ladder is a series of resistors. The fine comparators use a patented interpolation circuit to generate the equivalent of 1024 evenly spaced reference voltages between $V_{REF(-)}$ and $V_{REF(+)}$.

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (See Figure 1). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S

disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and selects a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.

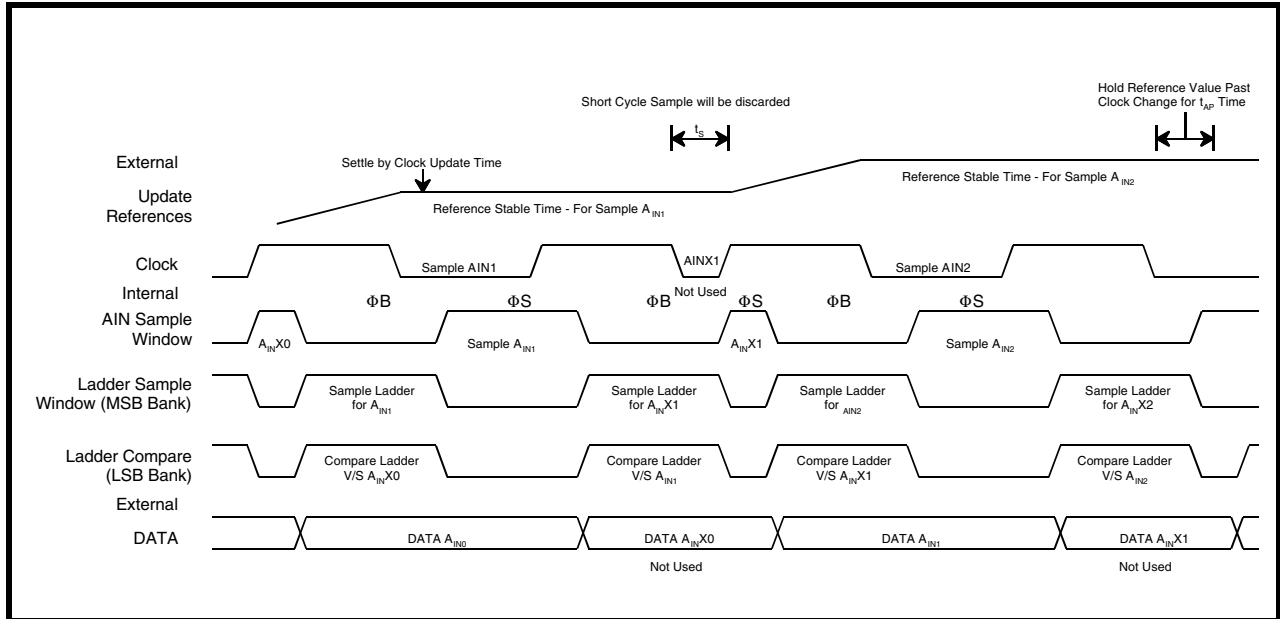
FIGURE 4. XRD87L99 COMPARATORS



A_{IN} Sampling, Ladder Sampling, and Conversion Timing

Figure 3 shows this relationship as a timing chart. A_{IN} sampling, ladder sampling and output data relationships are shown for the general case where the levels which drive the ladder need to change for each sampled A_{IN} time point. The ladder is referenced for both last A_{IN} sample and next A_{IN} sample at the same time. If the ladder's levels change by more than 1 LSB, one of the samples must be discarded. Also note that the clock low period for the discarded A_{IN} can be reduced to the minimum t_S time.

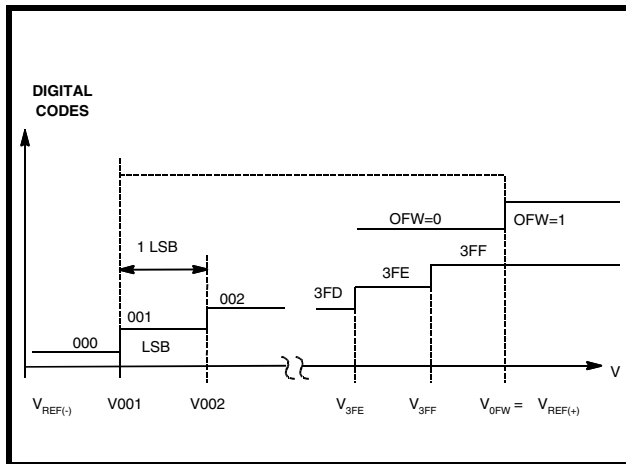
FIGURE 5. XRD87L99 COMPARATORS WITH CHANGING REFERENCE VOLTAGE



1.1 ACCURACY OF CONVERSION: DNL AND INL

The transfer function for an ideal A/D converter is shown in Figure 6.

FIGURE 6. IDEAL A/D TRANSFER FUNCTION



The overflow transition (VOFW) takes place at:

$$V_{IN} = V_{OFW} = V_{REF(+)}$$

The first and the last transitions for the data bits take place at:

$$V_{IN} = V_{001} = V_{REF(-)} + 1.0 * LSB$$

$$V_{IN} = V_{3FF} = V_{REF(-)} - 1.0 * LSB$$

$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$

$$LSB = V_{REF} / 1024 = (V_{3FF} - V_{001}) / 1022$$

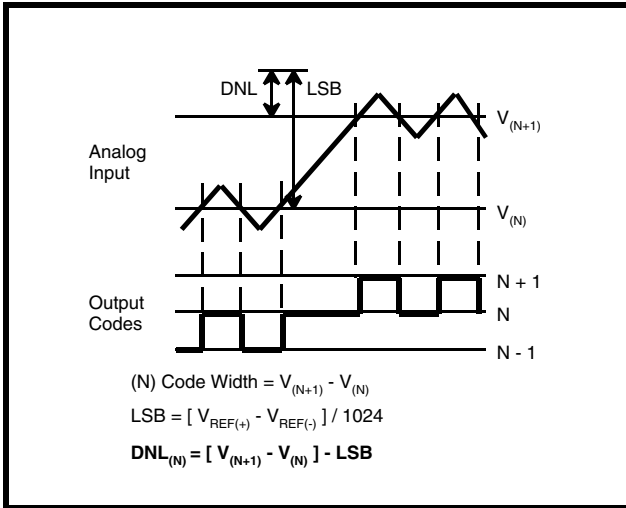
NOTE: The overflow transition is a flag and has no impact on the data bits.

In a "real" converter the code-to-code transitions don't fall exactly every $V_{REF}/1024$ volts.

A positive DNL (Differential Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSBs.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ± 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If $V_{REF} = 2.56$ V then 1 LSB = 2.5 mV and every code width is within 1.25 and 3.75 mV.

FIGURE 7. DNL MEASUREMENT ON PRODUCTION TESTER



The formulas for Differential Non-Linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (EVS, EFS) are:

$$DNL(001) = V002 - V001 - LSB$$

$$\vdots$$

$$DNL(3FE) = V3FF - V3FE - LSB$$

$$EFS \text{ (full scale error)} = V3FF - [V_{REF(+)} - 1.5 * LSB]$$

$$EVS \text{ (zero scale error)} = V001 - [V_{REF(-)} + 0.5 * LSB]$$

FIGURE 8. REAL A/D TRANSFER CURVE

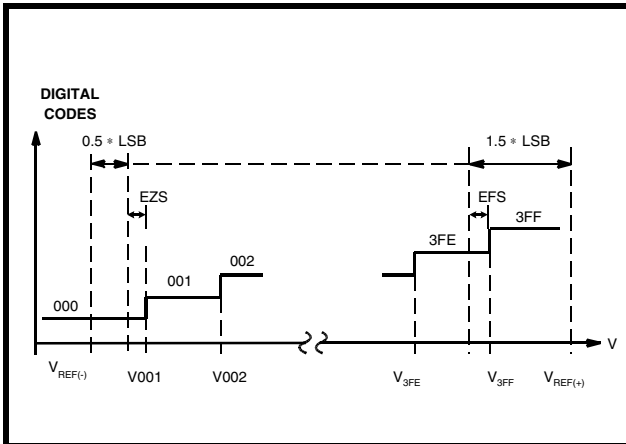
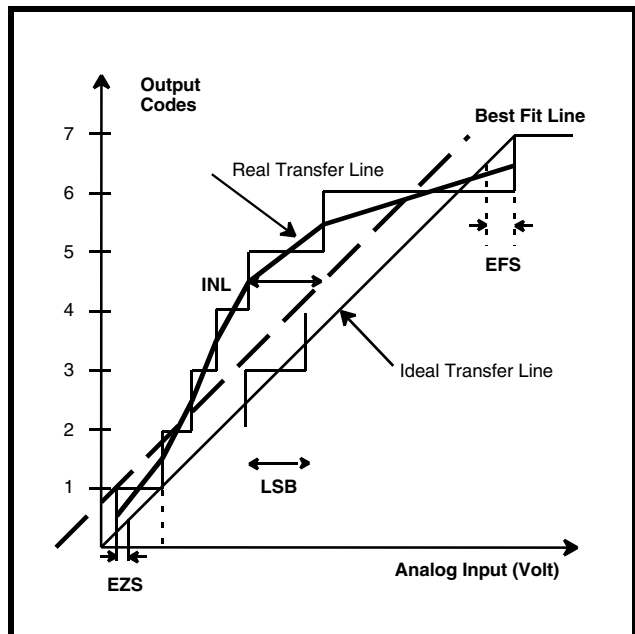


Figure 8 shows the zero scale and full scale error terms.

Figure 9 gives a visual definition of the INL error. The chart shows a 3-bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition the best fit line makes equal the positive and the negative INL errors. For example, an INL error of -1 to +2 LSB's relative to the Ideal Line would be ± 1.5 LSB's relative to the best fit line.

FIGURE 9. INL ERROR CALCULATION



1.2 CLOCK AND CONVERSION TIMING

A system will clock the XRD87L99 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of Figure 10a shows normal operation, while the timing of Figure 10b keeps the XRD87L99 in balance and ready to sample the analog input.

FIGURE 10. RELATIONSHIP OF DATA TO CLOCK

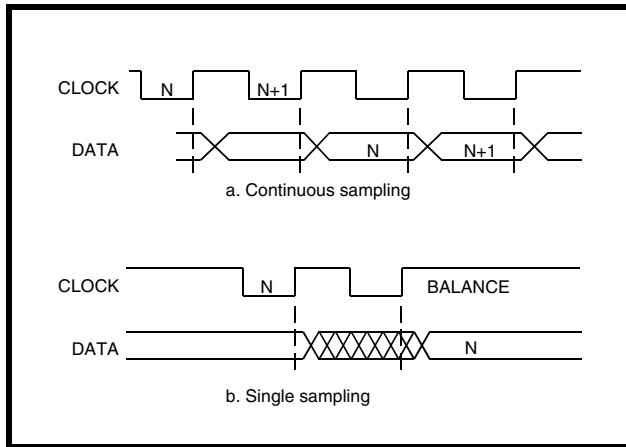
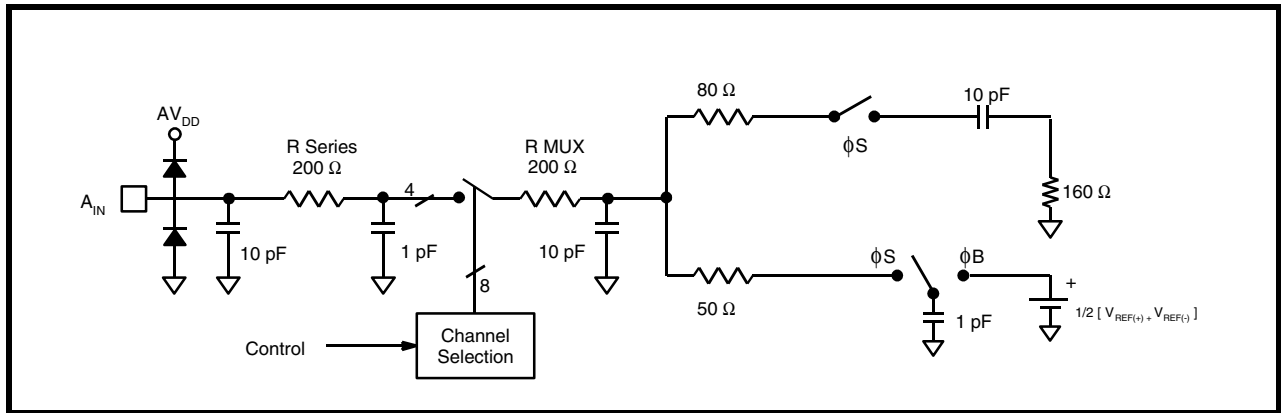


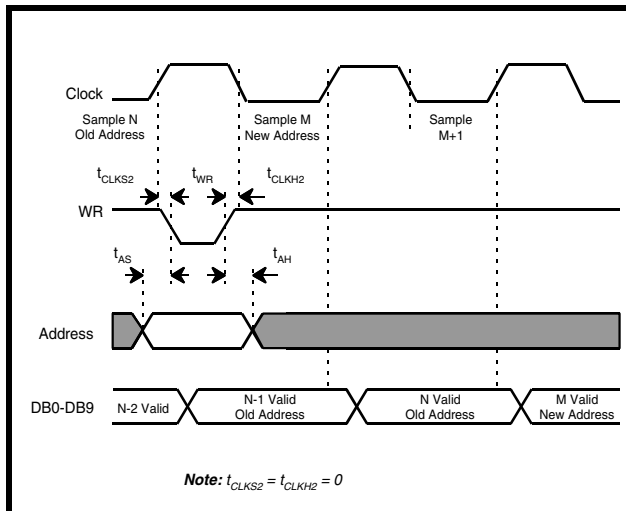
FIGURE 11. ANALOG INPUT EQUIVALENT CIRCUIT



1.4 ANALOG INPUT MULTIPLEXER

The XRD87L99 includes a 8-Channel analog input multiplexer. The relationship between the clock, the multiplexer address, the \overline{WR} and the output data is shown in Figure 12.

FIGURE 12. MUX ADDRESS TIMING



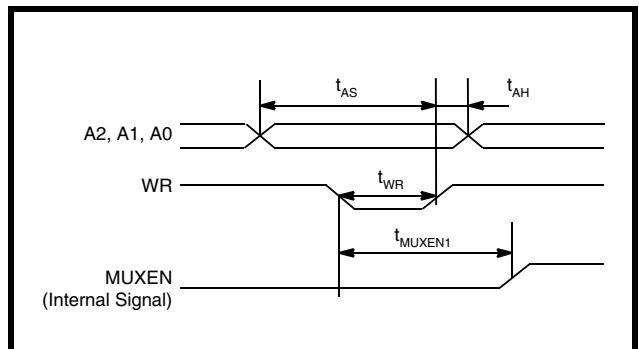
1.3 ANALOG INPUT

The XRD87L99 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then vary the input DC and AC levels to match the VREF range. Another method is to first design the analog input circuitry and then adjust the reference voltages for the analog input range.

One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds.

The XRD87L99's performance is optimized by using analog input circuitry that is capable of driving the A_{IN} input. Figure 11 shows the equivalent circuit for A_{IN} .

FIGURE 13. ANALOG MUX TIMING



1.5 REFERENCE VOLTAGES

The input/output relationship is a function of V_{REF} :

$$A_{IN} = V_{IN} - V_{REF(-)}$$

$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$

$$DATA = 1024 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}

1.6 DIGITAL INTERFACES

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output.

The functional equivalent of the XRD87L99 (Figure 14) is composed of:

1. Delay stage (t_{AP}) from the clock to the sampling phase (f_S).
2. An ideal analog switch which samples V_{IN} .
3. An ideal A/D which tracks and converts V_{IN} with no delay.
4. A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP} , t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.

1.7 POWER DOWN

Figure 15 shows the relationship between the clock, sampled V_{IN} to output data relationship and the effect of power down.

FIGURE 14. XRD87L99 FUNCTIONAL EQUIVALENT CIRCUIT AND INTERFACE TIMING

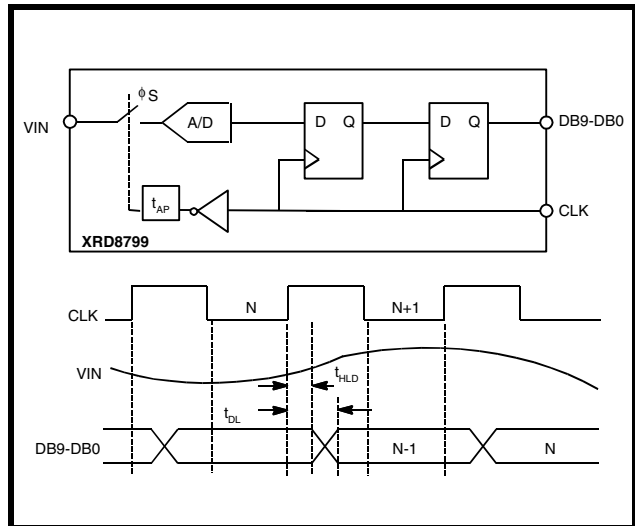
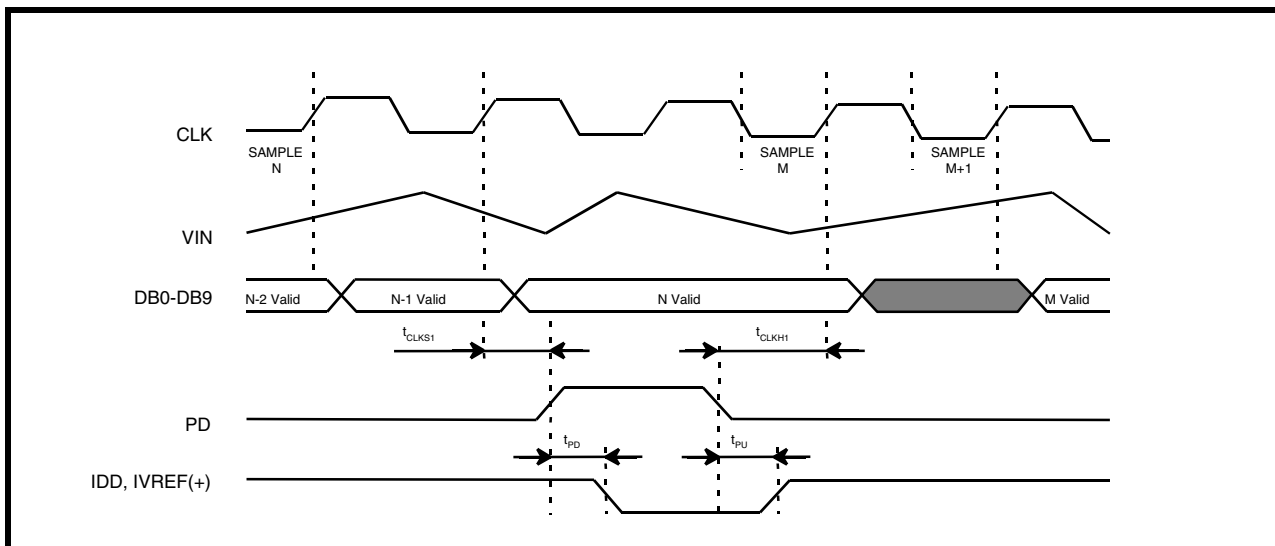
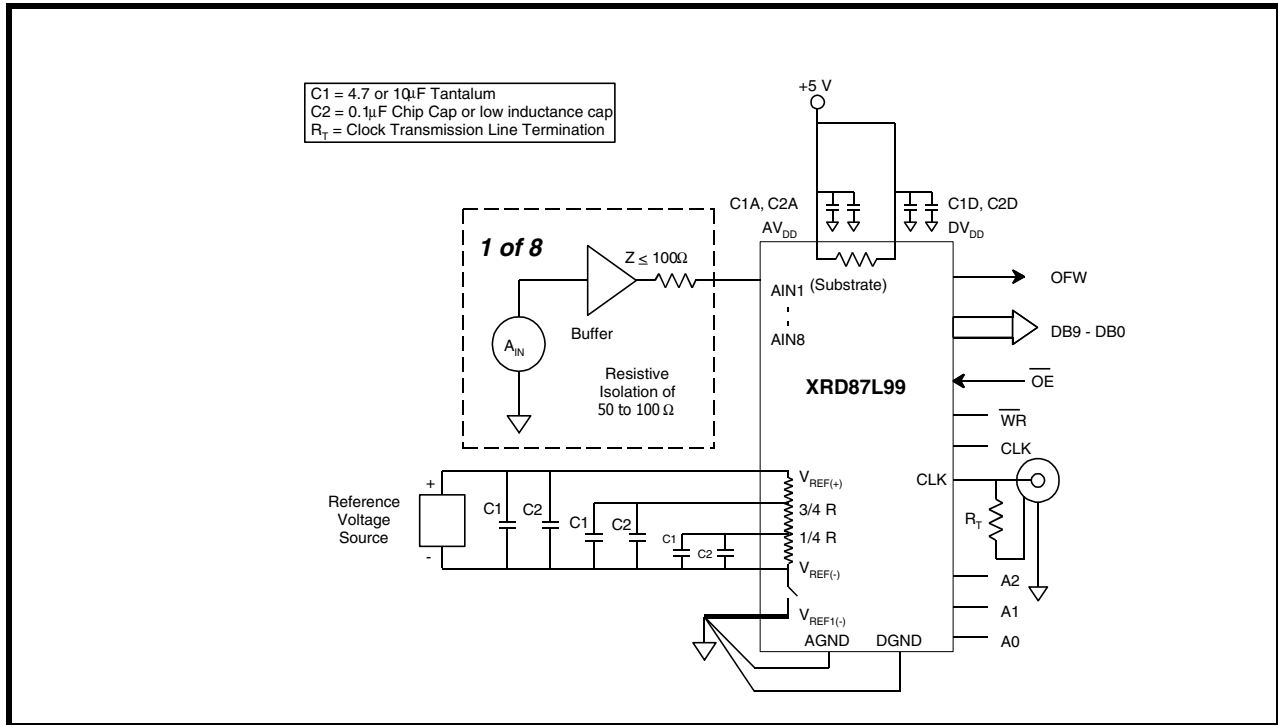


FIGURE 15. POWER DOWN TIMING DIAGRAM



2.0 APPLICATION NOTES

FIGURE 16. TYPICAL CIRCUIT CONNECTIONS



The following information will be useful in maximizing the performance of the XRD87L99.

1. All signals should not exceed AV_{DD} +0.5 V or AGND -0.5 V or DV_{DD} +0.5 V or DGND -0.5 V.
2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND -0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All XRD87L99 inputs have input protection diodes which will protect the device from short transients outside the supply ranges.
3. The design of a PC board will affect the accuracy of XRD87L99. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the XRD87L99.
7. DV_{DD} should not be shared with other digital circuitry to avoid conversion errors caused by digital supply transients. DV_{DD} for the XRD87L99 should be connected to AV_{DD} next to the XRD87L99.
8. DV_{DD} and AV_{DD} are connected inside the XRD87L99. DGND and AGND are connected internally.
9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used. 100Ω resistors in series with the digital outputs in some applications reduces the digital output disruption of A_{IN}.

FIGURE 17. EXAMPLE OF A REFERENCE VOLTAGE SOURCE

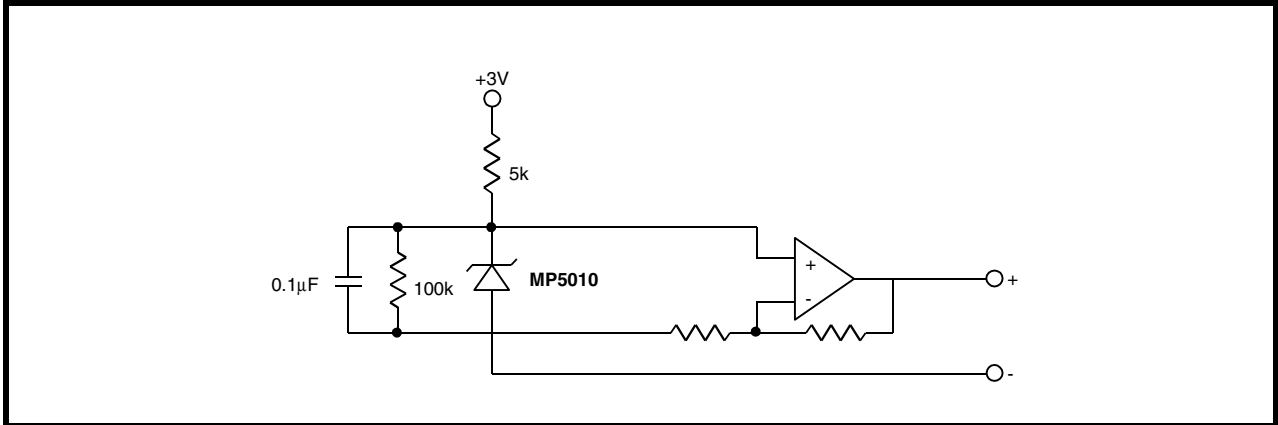
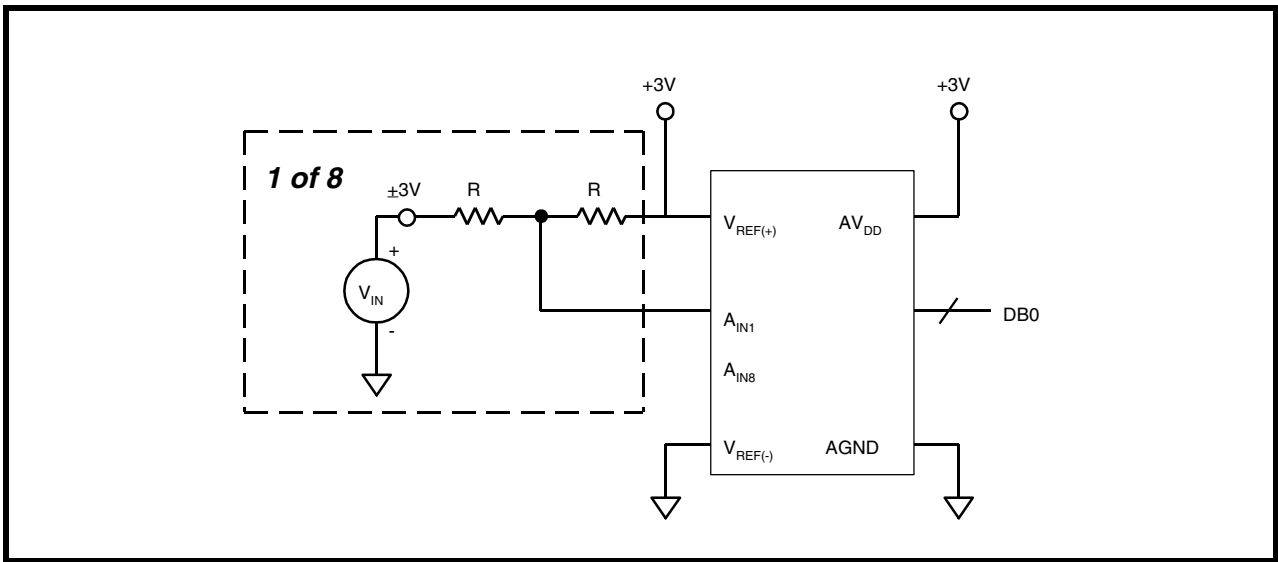


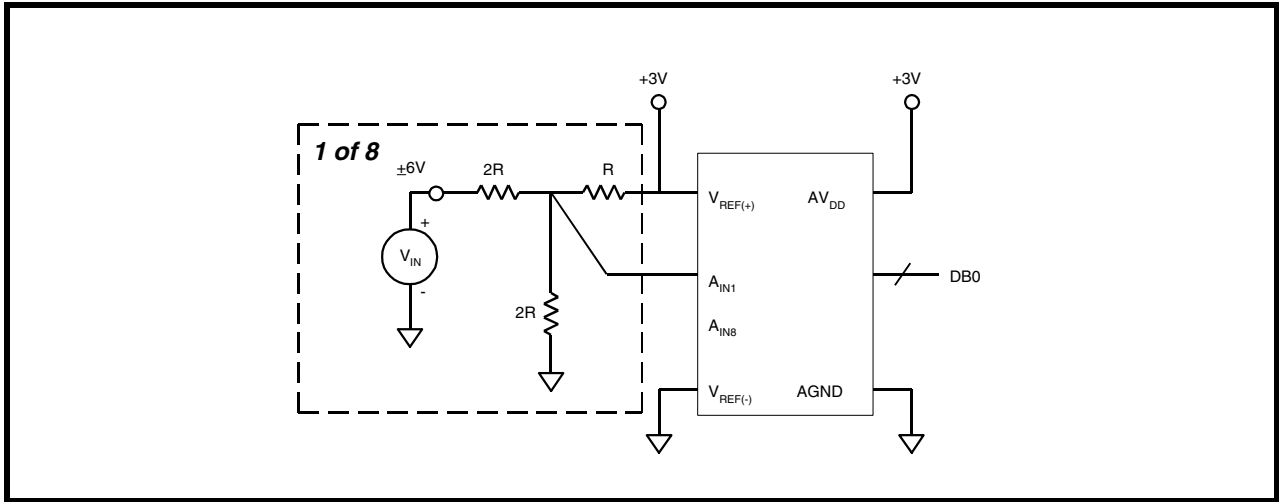
FIGURE 18. ±3V ANALOG INPUT



For $R = 5k$ use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the $(R * C_{IN})$ of ADC time constant. Therefore, for different applications the R value needs to be selected as a trade-off between A_{IN} settling time and power dissipation.

FIGURE 19. $\pm 6V$ ANALOG INPUT



For $R = 5k$ use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the $(R * C_{IN}$ of ADC) time constant. Therefore, for different applications the R value needs to be selected as a trade-off between A_{IN} settling time and power dissipation.

FIGURE 20. A/D LADDER AND A_{IN} WITH PROGRAMMED CONTROL (OF $V_{REF(+)}$, $V_{REF(-)}$, 1/4 AND 3/4 TAP.)

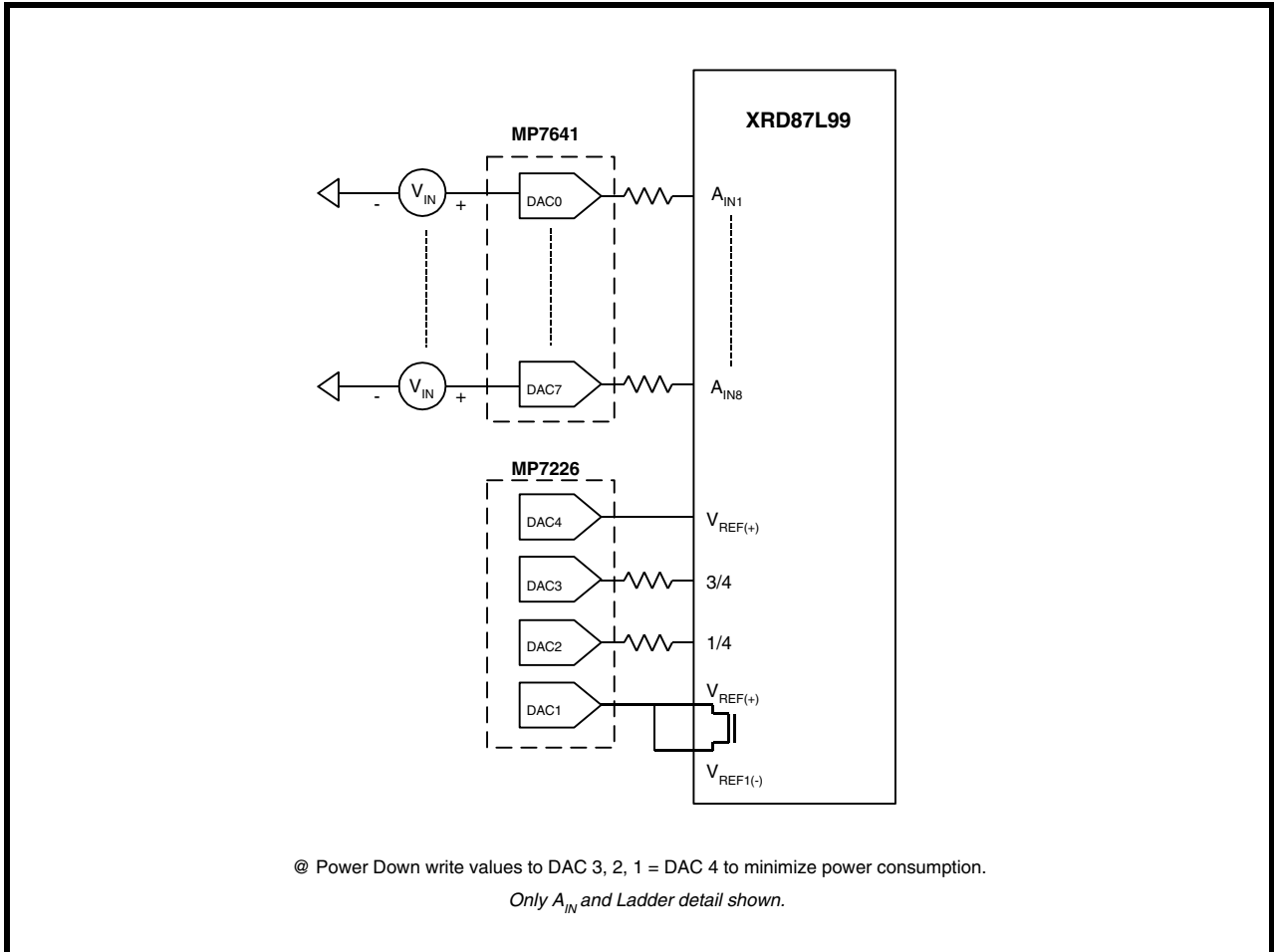


FIGURE 21. DNL vs. SAMPLING FREQUENCY

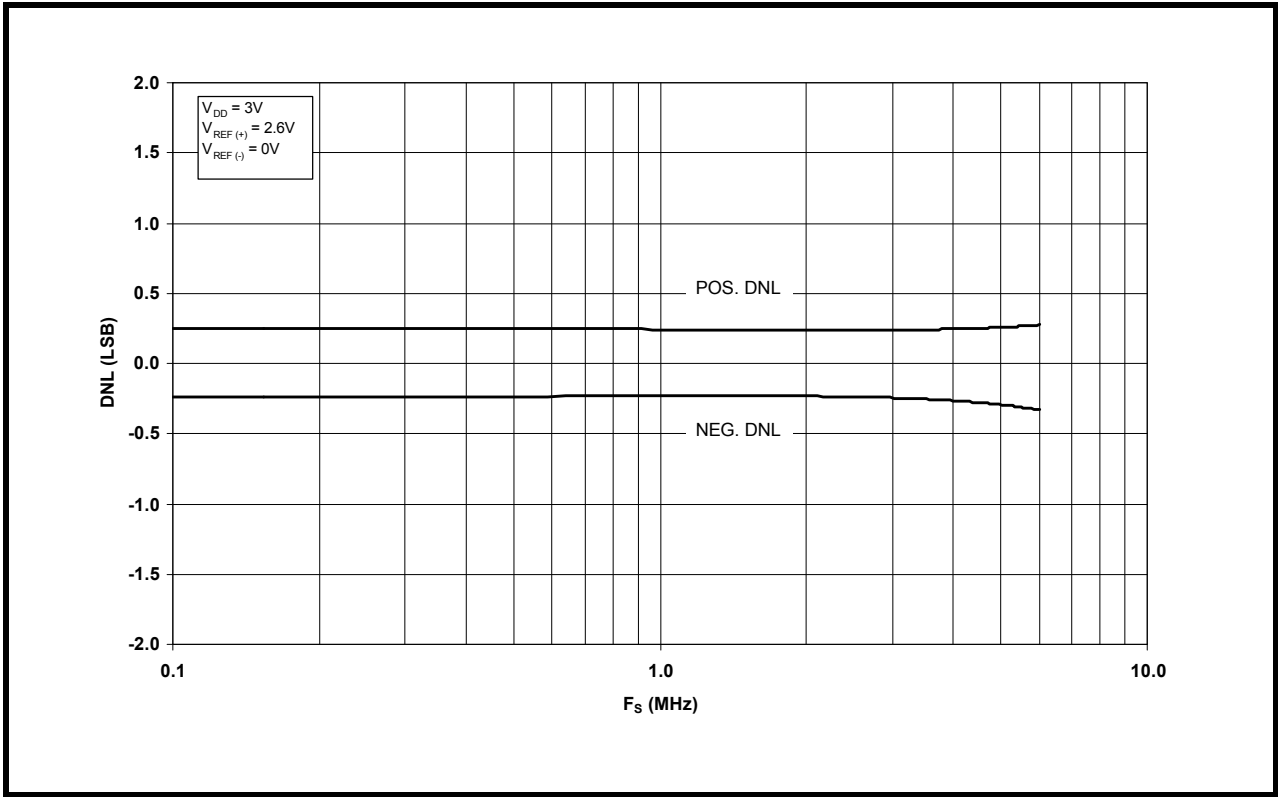


FIGURE 22. INL vs. SAMPLING FREQUENCY

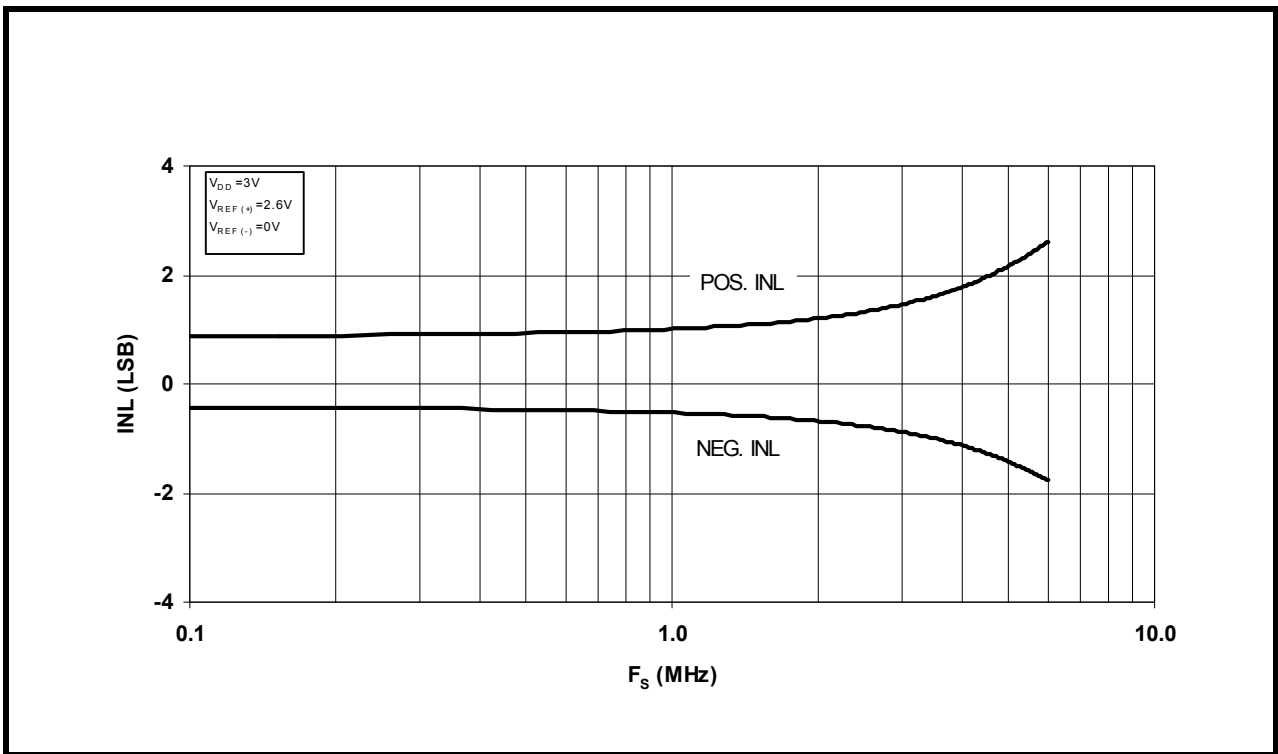


FIGURE 23. SUPPLY CURRENT VS. SAMPLING FREQUENCY

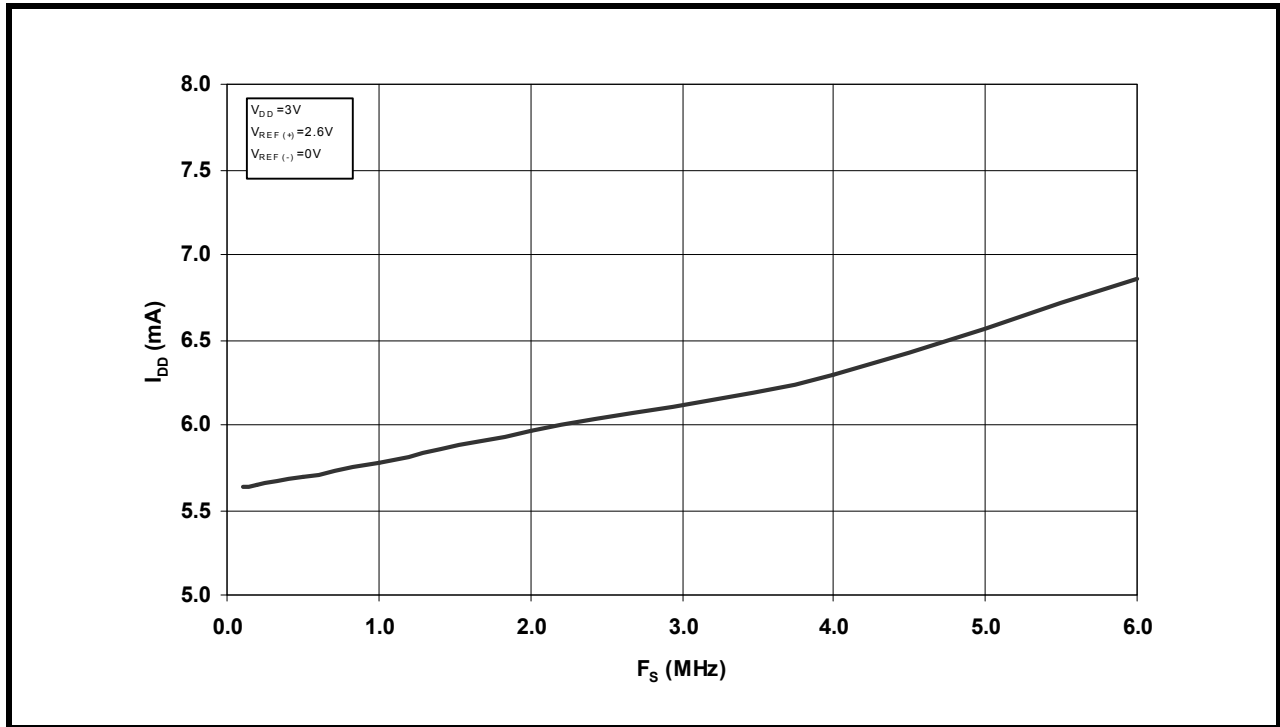


FIGURE 24. BEST FIT INL VS. REFERENCE VOLTAGE

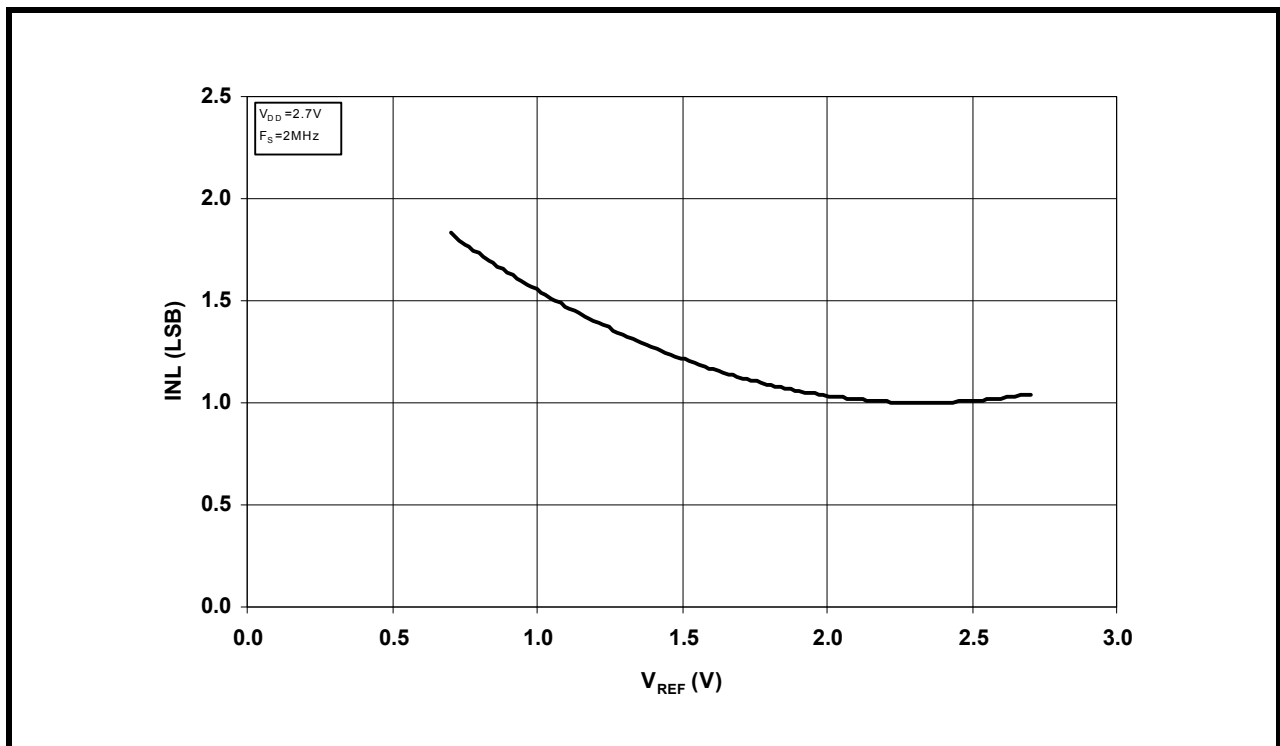


FIGURE 25. DNL VS. REFERENCE VOLTAGE

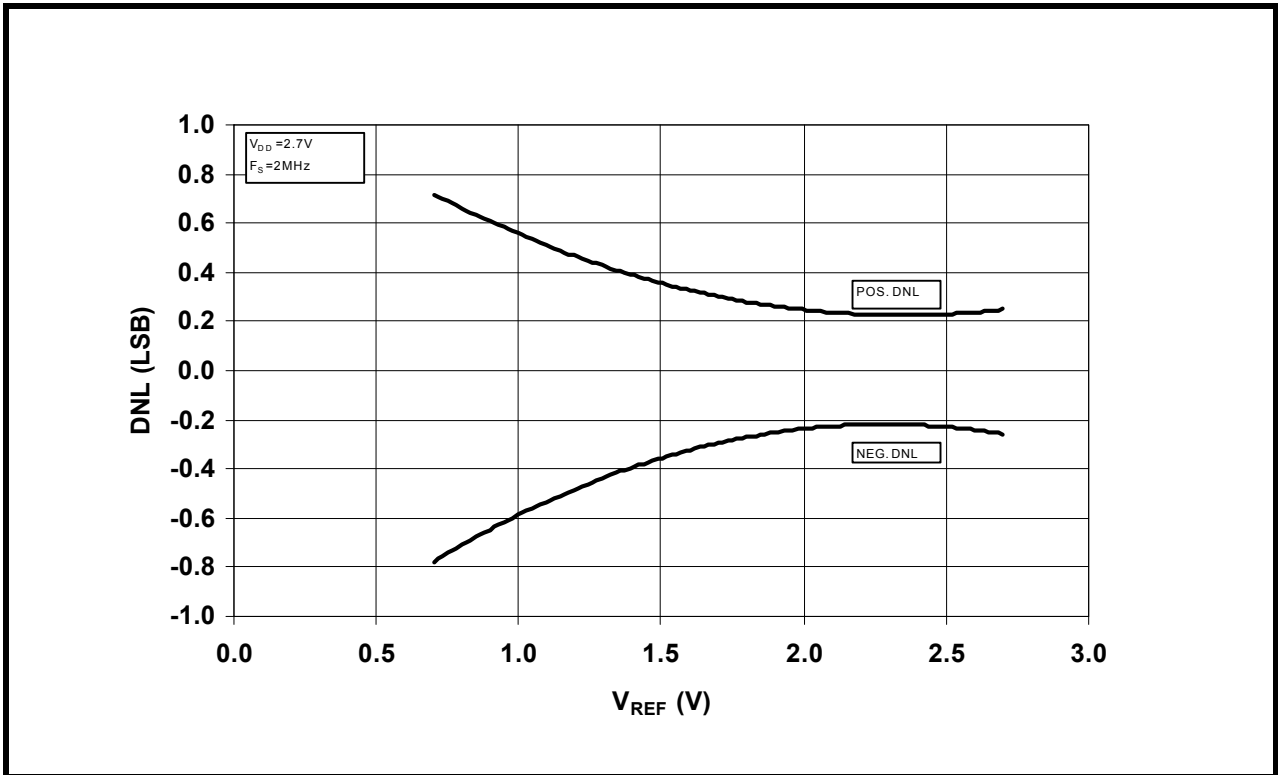


FIGURE 26. SUPPLY CURRENT VS. TEMPERATURE

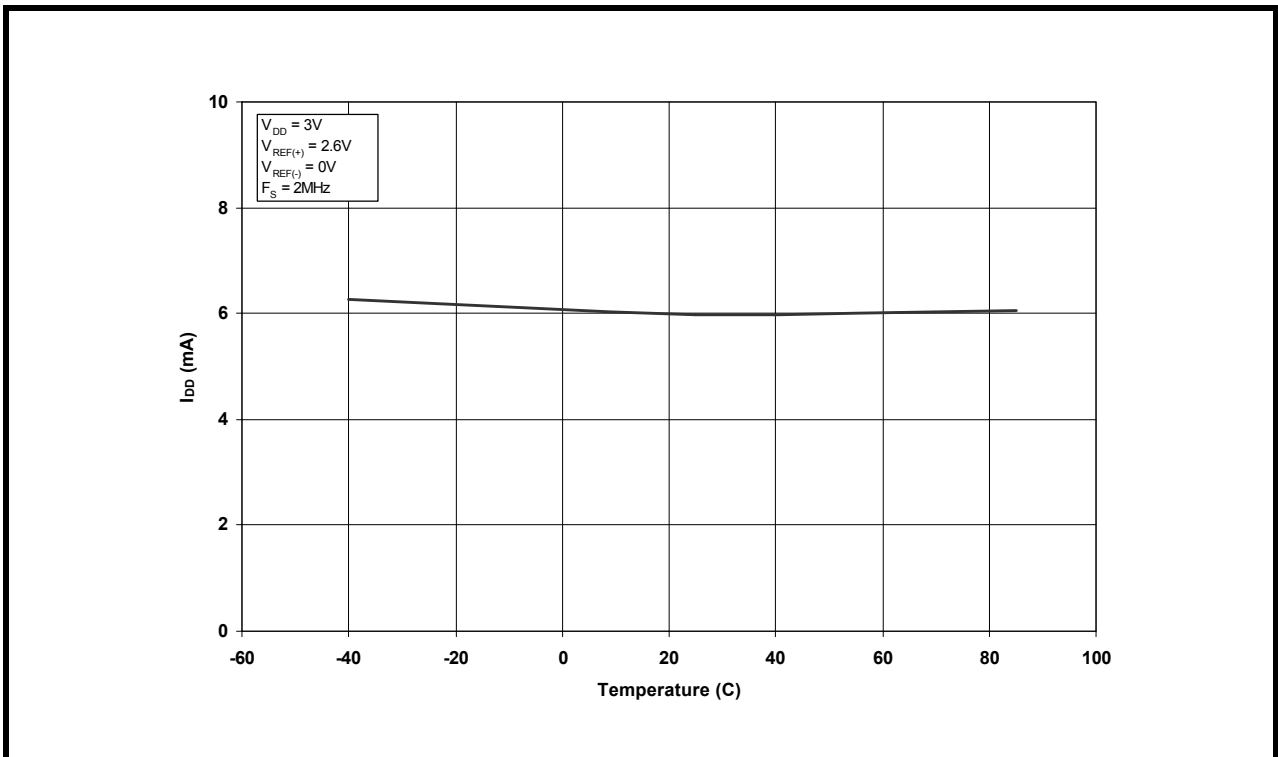


FIGURE 27. DNL VS. TEMPERATURE

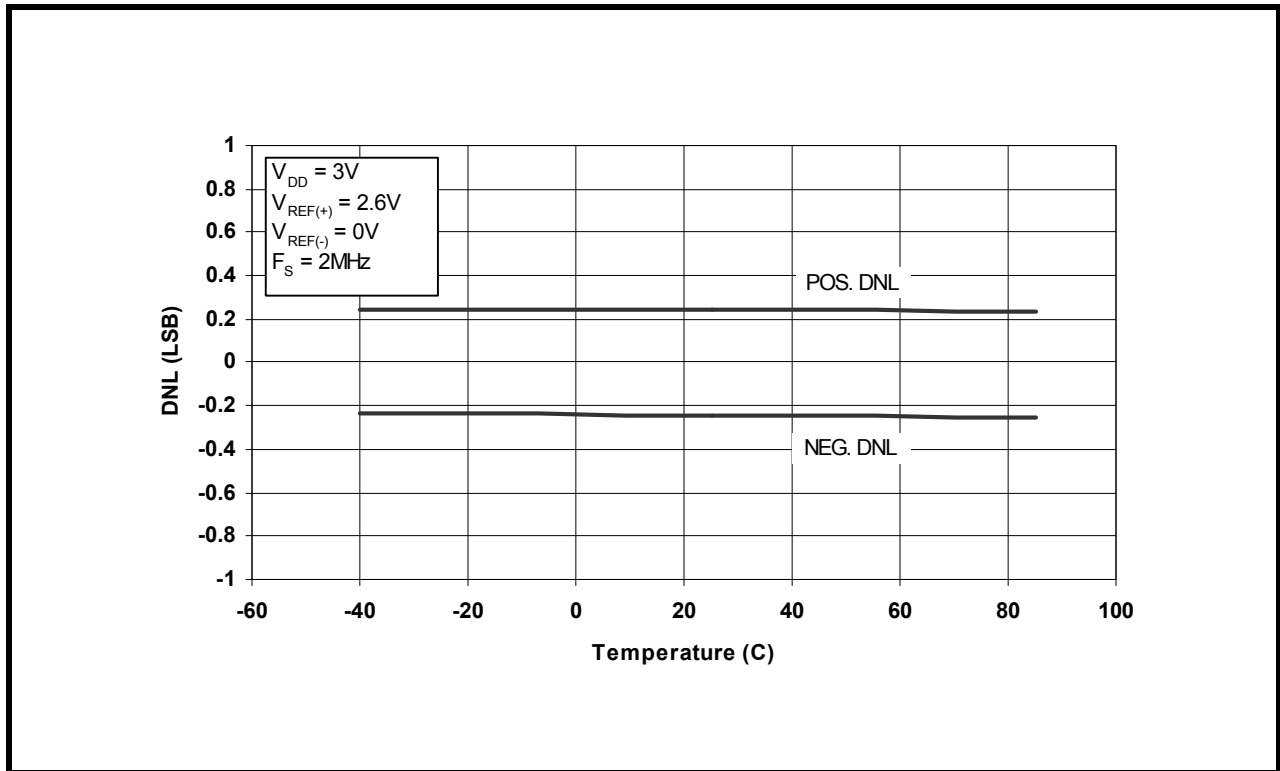


FIGURE 28. REFERENCE RESISTANCE VS. TEMPERATURE

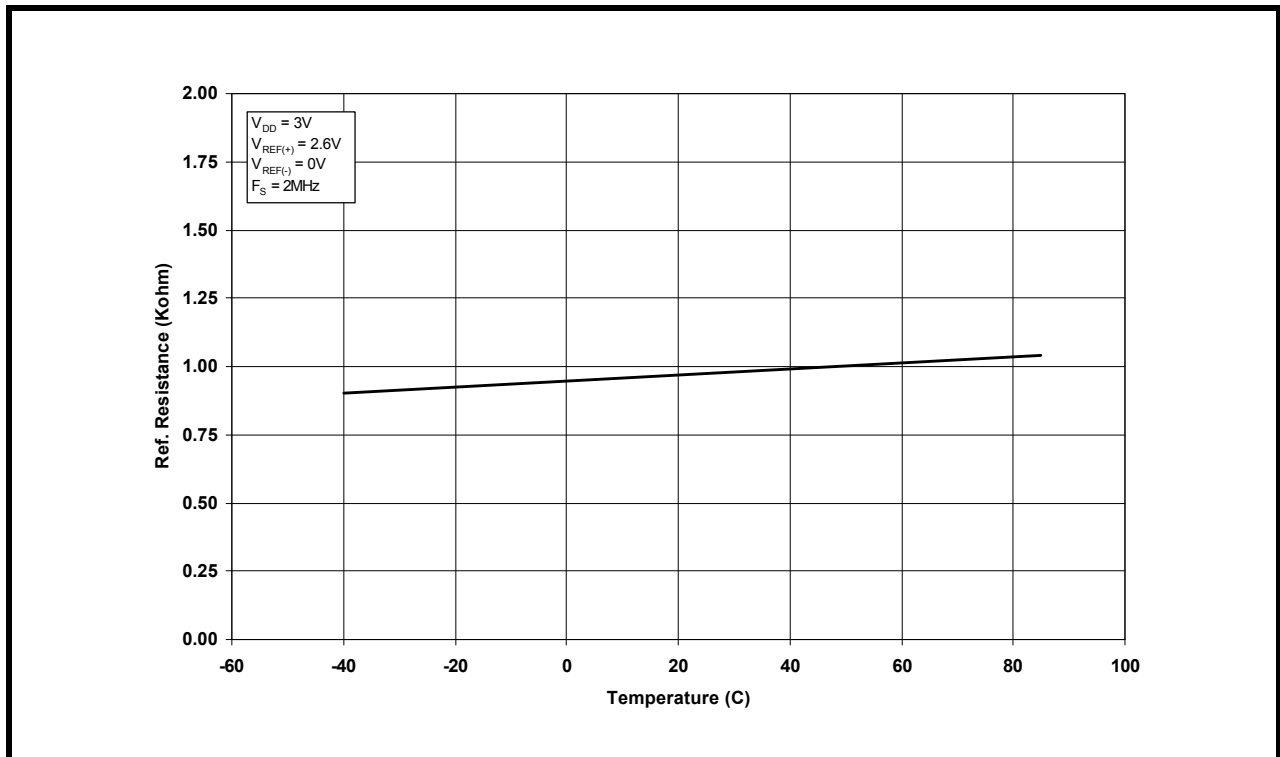


FIGURE 29. I_{DD} vs. V_{DD}

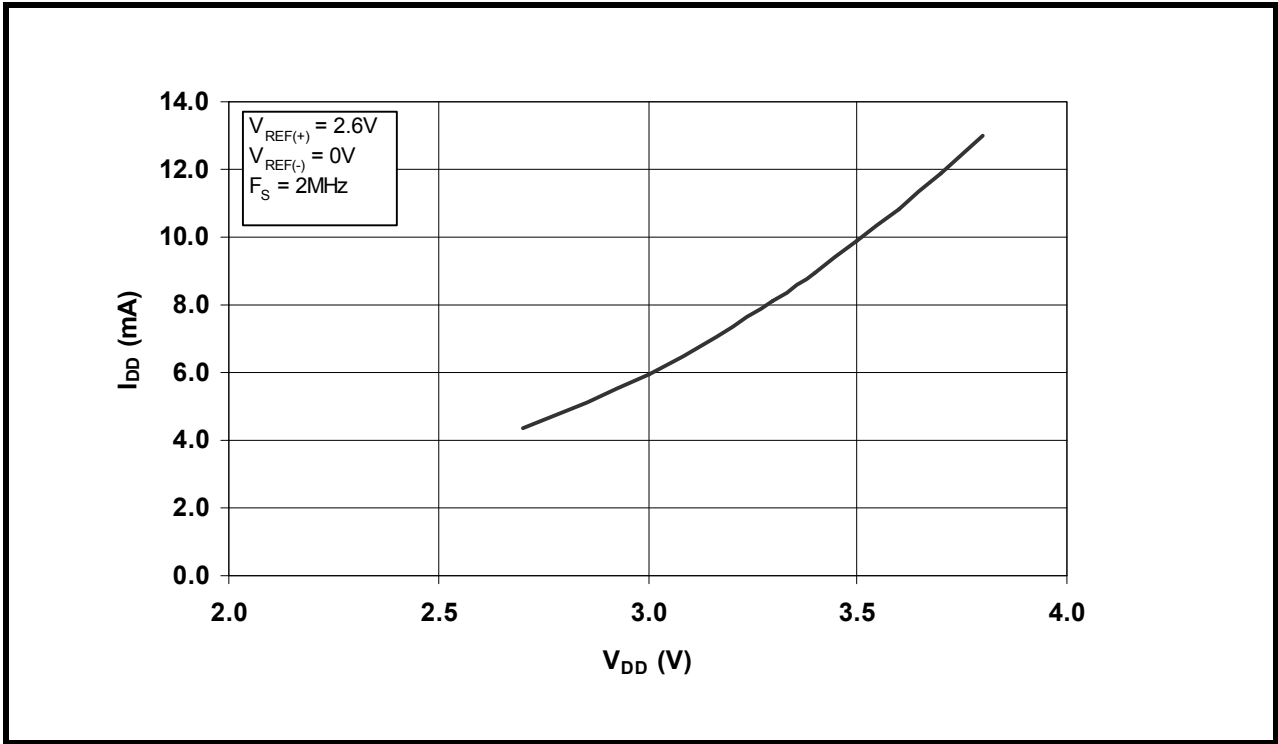
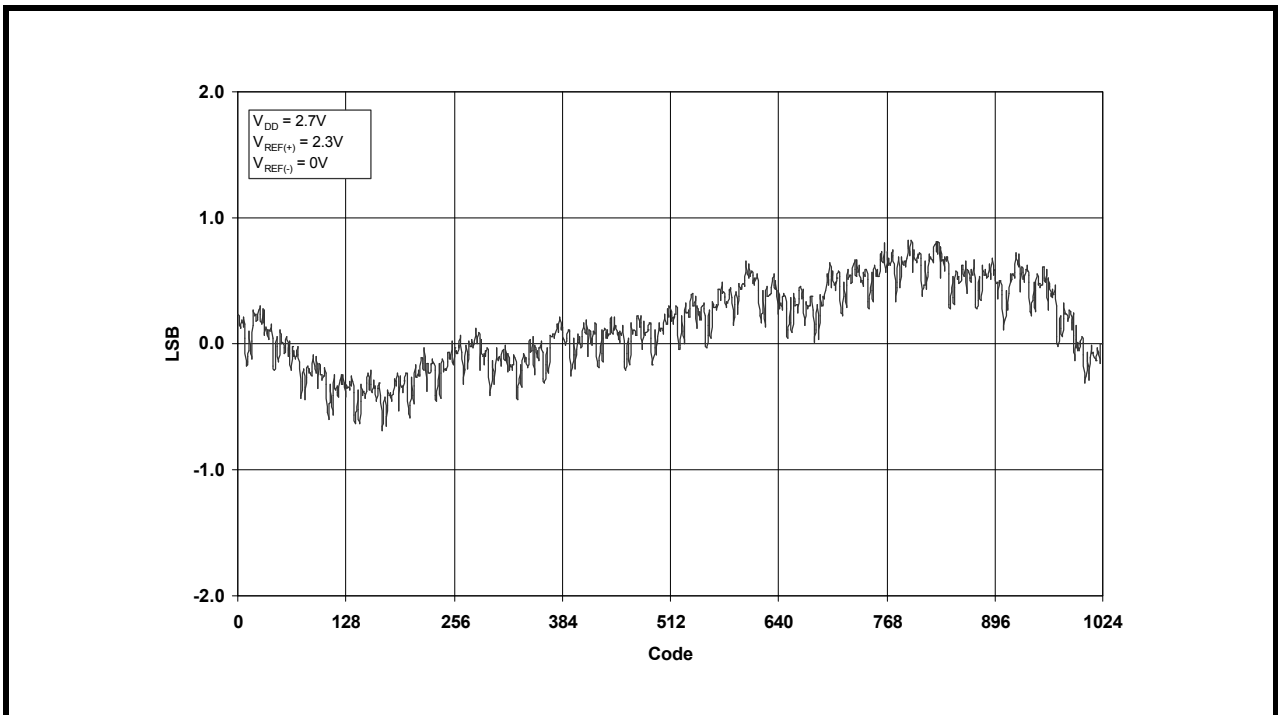


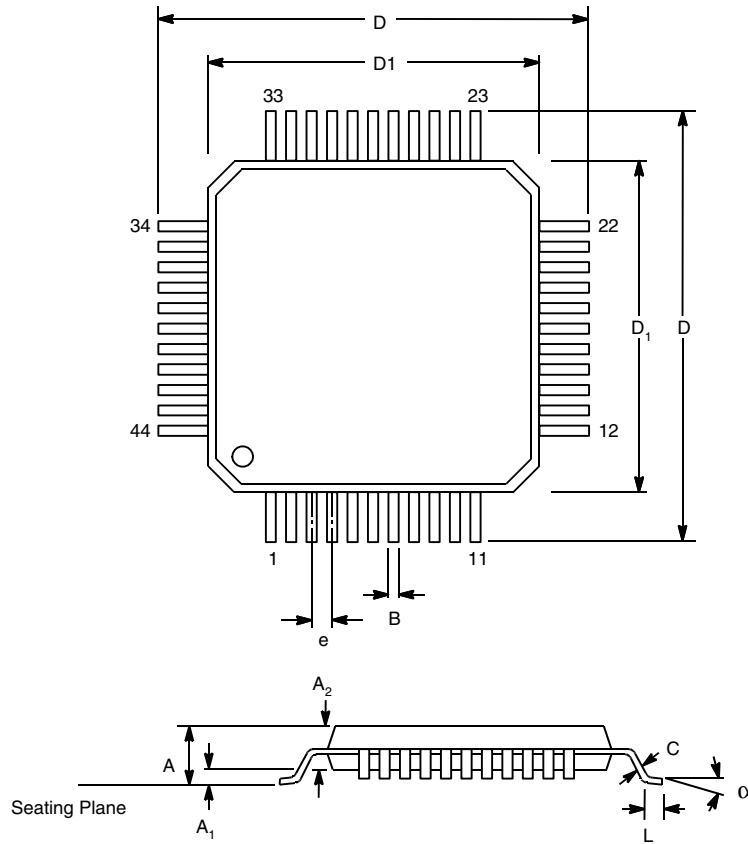
FIGURE 30. INL @ 2MSPS



44 LEAD PLASTIC QUAD FLAT PACK

(10 mm x 10 mm QFP, 1.60 mm Form)

REV. 2.00



Note: The control dimension is the millimeter column

| SYMBOL | INCHES | | MILLIMETERS | |
|----------------|------------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.072 | 0.093 | 1.82 | 2.45 |
| A ₁ | 0.001 | 0.010 | 0.02 | 0.25 |
| A ₂ | 0.071 | 0.087 | 1.80 | 2.20 |
| B | 0.011 | 0.018 | 0.29 | 0.45 |
| C | 0.004 | 0.009 | 0.11 | 0.23 |
| D | 0.510 | 0.530 | 12.95 | 13.45 |
| D ₁ | 0.390 | 0.398 | 9.90 | 10.10 |
| e | 0.0315 BSC | | 0.80 BSC | |
| L | 0.029 | 0.040 | 0.73 | 1.03 |
| α | 0° | 7° | 0° | 7° |

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