Introduction

EXAR's family of high resolution, high speed current output digital-to-analog converters are often used in applications where speed is critical. Since applying these devices requires interfacing with an op amp, the DACs code dependent output capacitance becomes important. Capacitance from the input of the op amp to ground adversely affects transient and overshoot characteristics. Solutions to this problem are addressed below.

Capacitive loading of the output amplifier can also cause a ringing problem and circuit considerations to minimize these effects are discussed.

The Effect of DAC Output Capacitance

Below (*Figure 1.)* is the classical connection for creating a voltage output from a CMOS current output D/A converter. *Figure 2.* shows the equivalent AC circuit at Full Scale output.

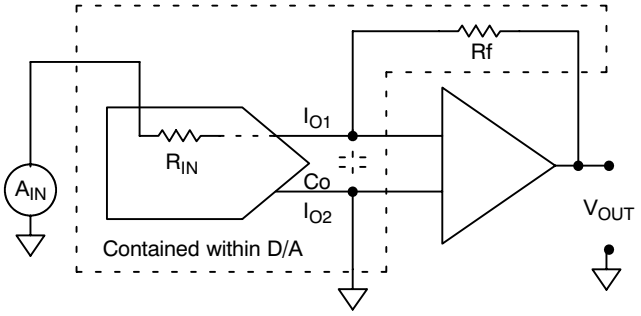

Figure 1. Typical Configuration CMOS I_{OUT} DAC with External Op Amp forming Voltage Output Configuration

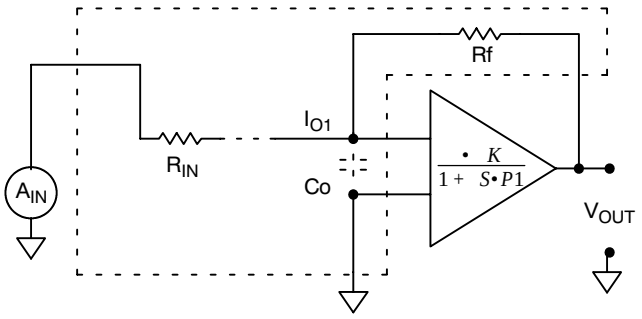

Figure 2. Equivalent Circuit at Full Scale for AC Analysis

By inspecting the linear systems characteristics of this circuit (in the form of the classical Bode plots and root locus plot, *Figures 3, 4 and 5.*), it is evident that this circuit will exhibit an under damped response, which could be unacceptable in some wide bandwidth applications. This non ideal response is due to the Co parasitic of the D/A.

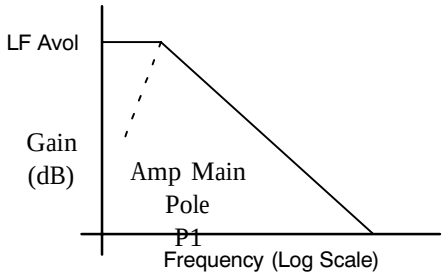

Figure 3. Op Amp Open Loop Characteristics

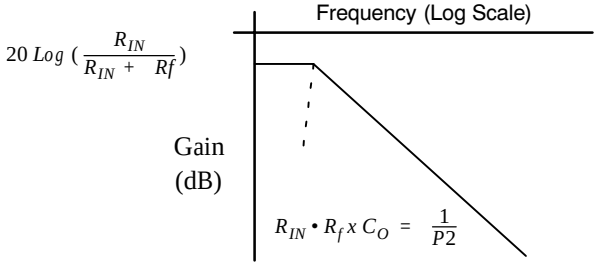

Figure 4. Feedback Signal Path Transfer Characteristics

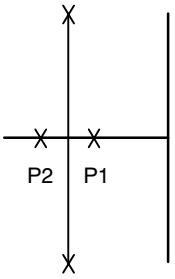

Figure 5. Root Locus

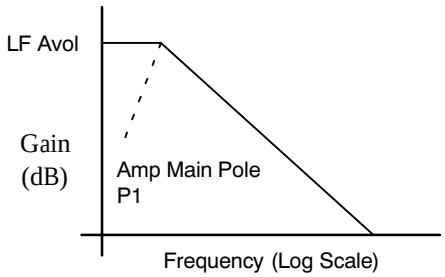

Figure 8. Op Amp Open Loop Characteristics

Most manufacturers propose the solution of inserting a Zero (a capacitor) in the feedback loop to compensate for this Co generated pole *(Figure 6. and Figure 7.)* The resulting linear systems plots (Figures 8, 9, and 10*)* show what is expected.

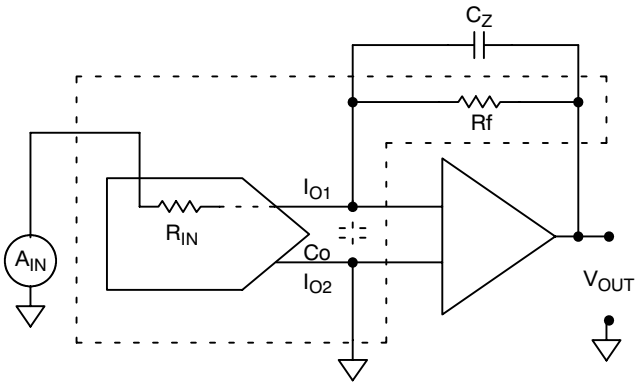

Figure 6. Typical Zero Compensation of Co General Pole

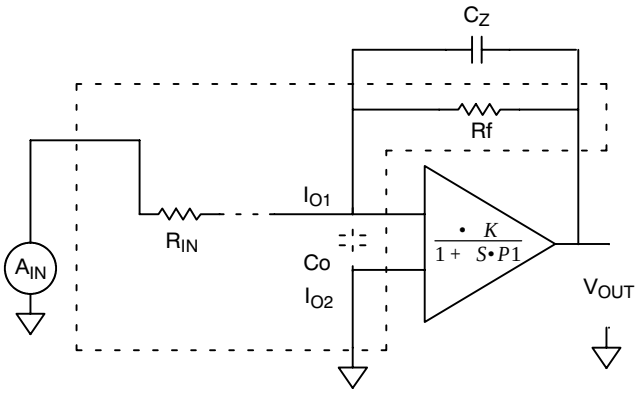

Figure 7. Equivalent Circuit at Full Scale for AC Analysis

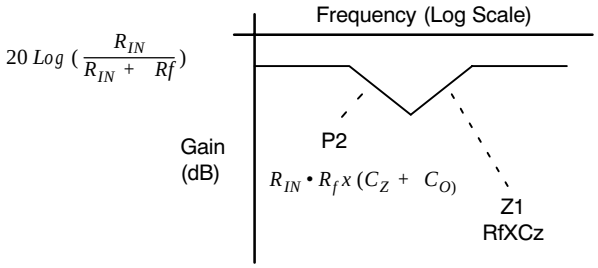

Figure 9. Feedback Signal Path Transfer Characteristics

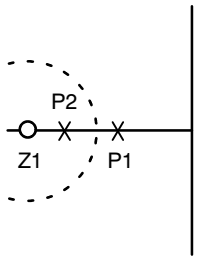

Figure 10. Root Locus

By adding Ra across Co *(Figure 11. and Figure 12.)*, 4 improvements are obtained :

1) The loop gain of the circuit is lowered, making the response more damped *(Figures 13, 14, and 15)*.
2) The Co X R is decreased, separating the Amp pole from the parasitic Co pole.
3) The Resistance at the Co node is made more constant versus DAC code, minimizing variations due to code changes. (The Co still will change versus code, so this circuit is still not perfect.)
4) Cz can be made smaller, which increases the DAC frequency response.

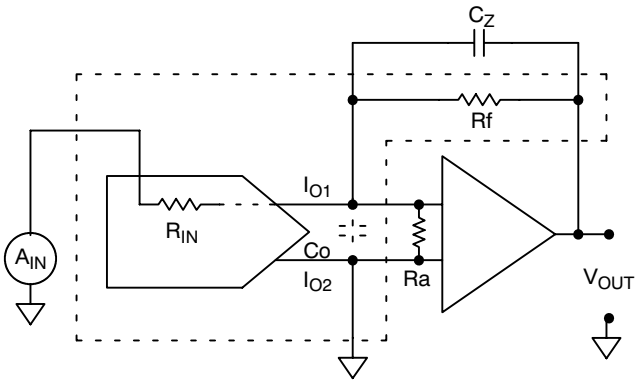

Figure 11. Typical Zero Compensation of Co General Pole

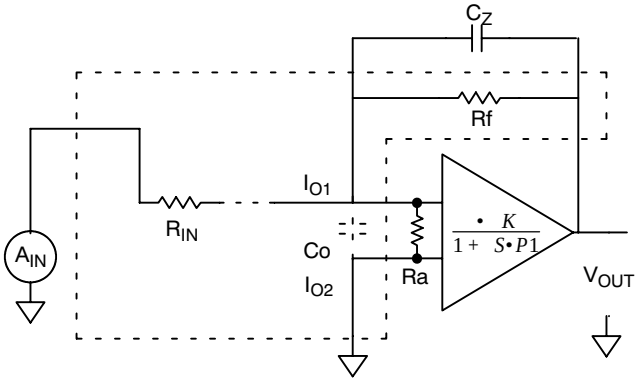

Figure 12. Equivalent Circuit at Full Scale for AC Analysis

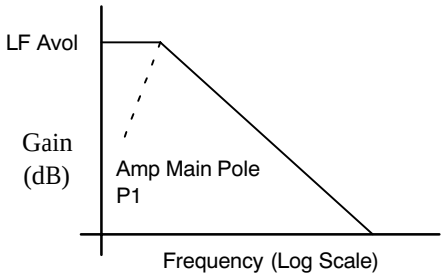

Figure 13. Op Amp Open Loop Characteristics

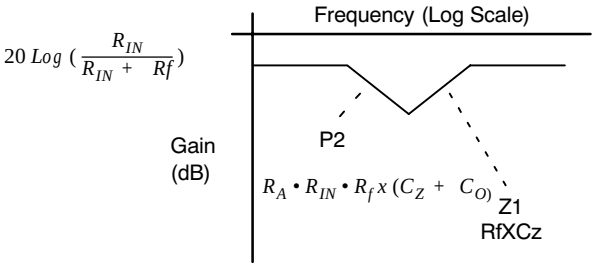

Figure 14. Feedback Signal Path Transfer Characteristics

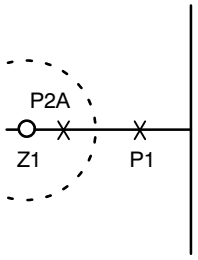

Figure 15. Root Locus

The best way to characterize the various alternatives is to do both a step or impulse response and a frequency / phase plot for the A_{IN} to V_{OUT} transfer function.

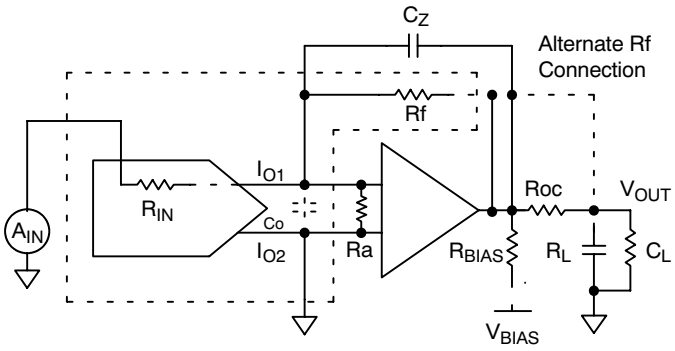

Figure 16. Typical Zero Compensation of Co General Pole

Output Loading Effects

Finally, the last area to be addressed is the characteristic of the op amp output stage itself *(Figure 16.)*

Where high frequency impulse current loads are experienced, like at the input of most modern high speed A/D converters, the output stage itself will overshoot. Even if this seems to be at very high frequencies and very short duration, this overshoot will degrade the A/D linearity in most cases. The overshoot is due to the Inductive tendency of the output emitter followers at very high frequencies.

Most manufacturers recommend 25 to 50Ω in series with their op amp output when driving capacitive loads to alleviate this problem. The only drawback of this configuration is the DC error generated by the insertion of Roc. The addition of R_{BIAS} – from the amp output to a minus supply in some cases provides enough additional current in the output NPN to give adequate response without this series Roc.

Finally, the alternate connection shown for Rf may in some cases give satisfactory AC results while compensating the loop for the DC error generated by the Roc – R_L voltage divider. This connection is possible only because Cz provides feedback for high frequencies. The best configuration is determined by experimentation and depends upon the op amp being used.

One last trick for applications which can tolerate a shifted Ground: By connecting the Op Amp and I_{O2} to a voltage of 0.3 to 0.6 volts above the CMOS D/A ground, The Co will be reduced by over 30 % due to the “Body Back Bias” effect on the D/A switches.

A Practical Example

Now, specifically for the MP7529A or B versus the PM7628: The MP7529A or B Co is 120 pF. The PM7628 Co is 60 pF. By adding the Ra = 2kΩ, to the application, the MP7529A or B will actually settle faster since the data path to the analog current steering switches is about 30 to 60 nS faster than the PM7628. Without the Ra, the MP7529A or B will have overshoot when in a circuit “tuned for the PM7628”.