GENERAL DESCRIPTION

FUNCTIONAL DESCRIPTION

Offered in both 16 pin SOIC and TSSOP packages, XRK32309 is a low cost 3.3V zero delay buffer. It is designed to distribute high speed clocks by taking one reference input and driving nine output clocks. The feedback of its on-chip PLL is internally connected to the FB output. XRK32309 devices operate over 10-100 MHz frequency range with 30 pF loads and up to 120MHz with lower loads (10 pF). The -1H version has higher drive strength than the base -1 version, featuring faster rise and fall time.

The XRK32309 has two banks each with four outputs. These outputs are controlled by two select input lines according to the Table 2, “Select Input Decoding,” on page 3. In cases where not all outputs are needed, bank B can be tri-stated. The select lines also enable putting the device in a bypass mode where the input is directly applied to the outputs. This feature is useful for chip and testing purposes.

Some applications may require distributing the clock to several destinations. In such situations, multiple XRK32309 devices can be connected to accept the same input clock and generate several clock signals. In this case, the skew between the outputs of two devices is guaranteed to be less than 700 ps.

The available versions of XRK32309 are shown in Table 12, “Ordering Information,” on page 10. The XRK32309-1 is the base part.

FEATURES

- 10-MHz to 120-MHz operating range, compatible with CPU and PCI bus frequencies
- Zero input-output propagation delay
- Multiple low-skew outputs
  - Output-output skew less than 250 ps
  - Device-device skew less than 700 ps
  - One input drives nine outputs, grouped as 4 + 4 + 1
- Less than 200 ps cycle-cycle jitter, compatible with Pentium®-based systems
- Test Mode to bypass phase-locked loop (PLL) (see “Select Input Decoding” on page 2)
- Available in space-saving 16-pin 150-mil SOIC or 4.4-mm TSSOP packages
- 3.3V operation
- Industrial and commercial temperature available

FIGURE 1. BLOCK DIAGRAM OF THE XRK32309

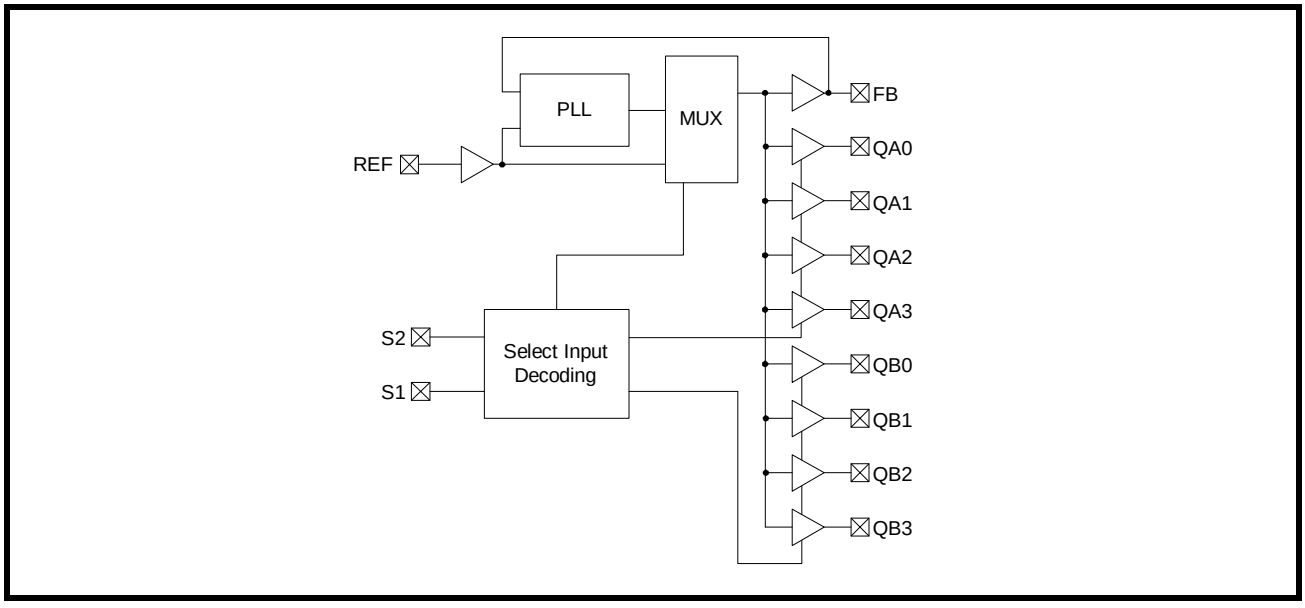


FIGURE 2. PIN OUT OF THE XRK32309

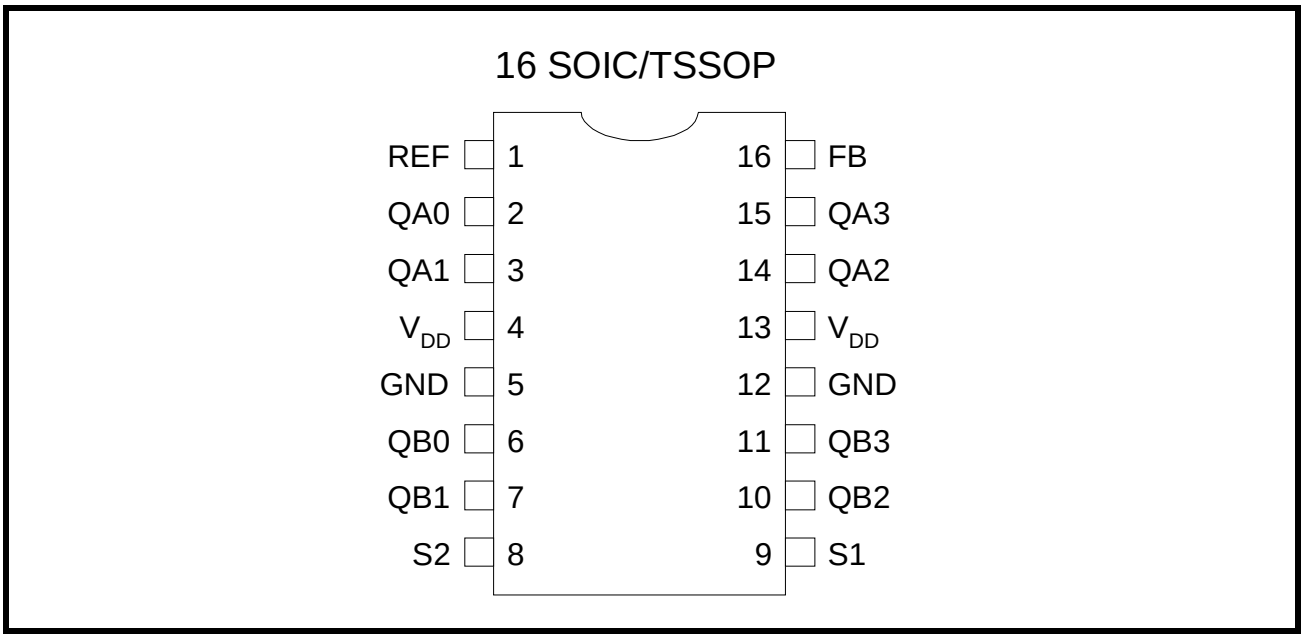


TABLE 1: PIN DESCRIPTION FOR XRK32309

PIN	SIGNAL	DESCRIPTION
1	REF[1]	Input reference frequency.
2	QA0[2]	Buffered clock output, Bank A
3	QA1[2]	Buffered clock output, Bank A
4	V_{DD}	3.3V supply
5	GND	Ground
6	QB0[2]	Buffered clock output, Bank B
7	QB1[2]	Buffered clock output, Bank B
8	S2[3]	Select input, bit 2
9	S1[3]	Select input, bit 1
10	QB2[2]	Buffered clock output, Bank B
11	QB3[2]	Buffered clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3V supply
14	QA2[2]	Buffered clock output, Bank A
15	QA3[2]	Buffered clock output, Bank A
16	FB[2]	Buffered output, internal feedback on this pin

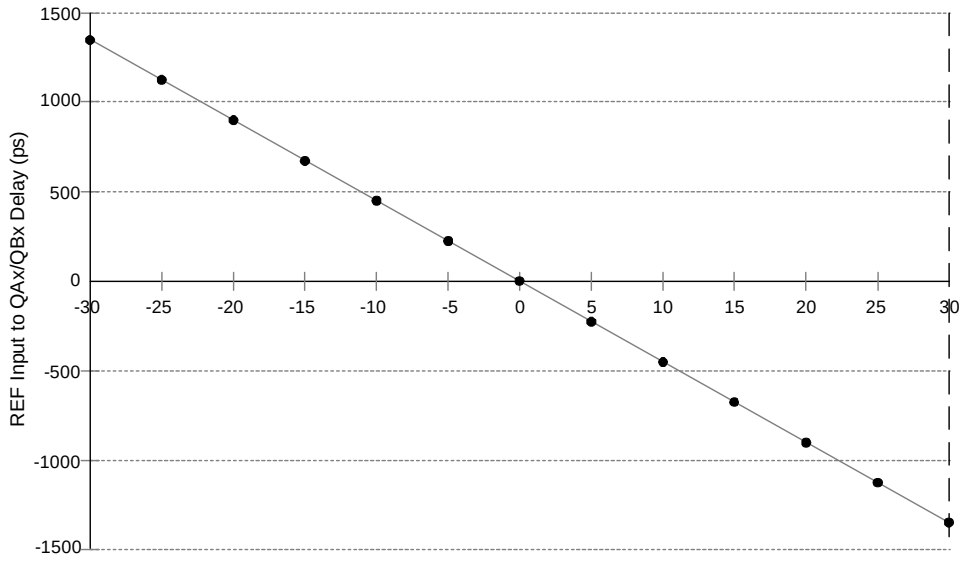
TABLE 2: SELECT INPUT DECODING

S2	S1	QA0-QA3	QB0-QB3	FB[4]	OUTPUT SOURCE
0	0	Tri-Stated	Tri-Stated	Driven	PLL
0	1	Driven	Tri-Stated	Driven	PLL
1	0	Driven	Driven	Driven	Reference
1	1	Driven	Driven	Driven	PLL

NOTES:

1. *Weak pull-down.*
2. *Weak pull-down on all outputs.*
3. *Weak pull-ups on these inputs.*
4. *This output has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.*

FIGURE 3. REF. INPUT TO QAX/QBX DELAY VS. LOADING DIFFERENCE BETWEEN FB AND QAX/QBX PINS



Note: Target only, actual characterization curve may be slightly different.

ZERO DELAY AND SKEW CONTROL

In order to achieve Zero Delay between the input reference and the output, all outputs, including FB, must be equally loaded even when the FB output is not being used.

Being internally connected as the PLL feedback, the FB output's capacitive loading relative to the other outputs can adjust the input to output delay according to the characteristic shown in Figure 3. This figure provides a tool for mapping the required delay to the capacitive load difference required between the FB and the Clock output of interest.

For zero output to output skew, the outputs have to be loaded equally as well.

TABLE 3: ABSOLUTE MAXIMUM RATINGS

PARAMETER	RANGE
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage (Except REF)	-0.5V to V_{DD} +0.5V
DC Input Voltage REF	-0.5 to 7V
Storage Temperature	-65°C to +150°C
Junction Temperature	150°C
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2000V

TABLE 4: OPERATING CONDITIONS FOR XRK32309SC-XX COMMERCIAL TEMPERATURE DEVICES

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance, below 100MHz	-	30	pF
	Load Capacitance, from 100MHz to 120MHz	-	10	pF
C_{IN}	Input Capacitance	-	7	pF
t_{PU}	Power-up time for all V_{DD}'s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

TABLE 5: ELECTRICAL CHARACTERISTICS FOR XRK32309SC-XX COMMERCIAL TEMPERATURE DEVICES

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNIT
V_{IL}	Input Low Voltage[5]		-	0.8	V
V_{IH}	Input High Voltage[5]		2.0	-	V
I_{IL}	Input Low Current	V_{IN}=0V	-	50.0	µA
I_{IH}	Input High Current	V_{IN}=V_{DD}	-	100.0	µA
V_{OL}	Output Low Voltage[6]	I_{OL}= 8mA (-1) I_{OL}= 12mA (-1H)	-	0.4	V
V_{OH}	Output High Voltage[6]	I_{OH}= -8mA (-1) I_{OH}= -12mA (-1H)	2.4	-	V
I_{DD}	Supply Current	Unloaded outputs at 66.67MHz, SEL inputs at V_{DD}	-	32.0	mA

TABLE 6: SWITCHING CHARACTERISTICS FOR XRK32309SC-1 COMMERCIAL TEMPERATURE DEVICES[7]

PARAMETER	NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Output Frequency	30-pF load 10-pF load	10 10	-	100 120	MHz MHz
DC	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{OUT}=66.67MHz	40.0	50.0	60.0	%
t_3	Rise Time[6]	Measured between 0.8V and 2.0V	-	-	2.50	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V	-	-	2.50	ns
t_5	Output to Output Skew[6]	All outputs equally loaded	-	-	250	ps
t_{6A}	Delay, REF Rising Edge to FB Rising Edge[6]	Measured at $V_{DD}/2$	-	0	±350	ps
t_{6B}	Delay, REF Rising Edge to FB Rising Edge[6]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode	1	5	8.7	ns
t_7	Device to Device Skew[6]	Measured at $V_{DD}/2$ on the FB pins of devices	-	0	700	ps
t_J	Cycle to Cycle Jitter[6]	Measured at 66.67MHz, loaded outputs	-	-	200	ps
t_{LOCK}	PLL Lock Time[6]	Stable power suppy, valid clock presented on REF pin	-	-	1.0	ms

NOTES:

5. *REF input has a threshold voltage of $V_{DD}/2$.*
6. *Parameter is guaranteed by design and characterization. Not 100% tested in production.*
7. *All parameters specified with loaded outputs.*

TABLE 7: SWITCHING CHARACTERISTICS FOR XRK32309SC-1H COMMERCIAL TEMPERATURE DEVICES[7]

PARAMETER	NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Output Frequency	30-pF load 10-pF load	10 10	-	100 120	MHz MHz
DC	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{OUT}=66.67MHz	40.0	50.0	60.0	%
		Measured at 1.4V, F_{OUT}<50.0MHz	45.0	50.0	55.0	%
t_3	Rise Time[6]	Measured between 0.8V and 2.0V	-	-	1.50	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V	-	-	1.50	ns
t_5	Output to Output Skew[6]	All outputs equally loaded	-	-	250	ps
t_{6A}	Delay, REF Rising Edge to FB Rising Edge[6]	Measured at $V_{DD}/2$	-	0	±350	ps
t_{6B}	Delay, REF Rising Edge to FB Rising Edge[6]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode	1	5	8.7	ns
t_7	Device to Device Skew[6]	Measured at $V_{DD}/2$ on the FB pins of devices	-	0	700	ps
t_8	Output Slew Rate[6]	Measured between 0.8V and 2.0V using Test Circuit #2	1	-	-	V/ns
t_J	Cycle to Cycle Jitter[6]	Measured at 66.67MHz, loaded outputs	-	-	200	ps
t_{LOCK}	PLL Lock Time[6]	Stable power suppy, valid clock presented on REF pin	-	-	1.0	ms

TABLE 8: OPERATING CONDITIONS FOR XRK32309SI-XX INDUSTRIAL TEMPERATURE DEVICES

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	-40	85	°C
C_L	Load Capacitance, below 100MHz	-	30	pF
	Load Capacitance, from 100MHz to 120MHz	-	10	pF
C_{IN}	Input Capacitance	-	7	pF
t_{PU}	Power-up time for all V_{DD}'s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

TABLE 9: ELECTRICAL CHARACTERISTICS FOR XRK32309SI-XX INDUSTRIAL TEMPERATURE DEVICES

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNIT
V_{IL}	Input Low Voltage[5]		-	0.8	V
V_{IH}	Input High Voltage[5]		2.0	-	V
I_{IL}	Input Low Current	V_{IN}=0V	-	50.0	µA
I_{IH}	Input High Current	V_{IN}=V_{DD}	-	100.0	µA
V_{OL}	Output Low Voltage[6]	I_{OL}= 8mA (-1) I_{OL}= 12mA (-1H)	-	0.4	V
V_{OH}	Output High Voltage[6]	I_{OH}= -8mA (-1) I_{OH}= -12mA (-1H)	2.4	-	V
I_{DD}	Supply Current	Unloaded outputs at 66.67MHz REF, SEL inputs at V_{DD}	-	35.0	mA

TABLE 10: SWITCHING CHARACTERISTICS FOR XRK32309SI-1 INDUSTRIAL TEMPERATURE DEVICES[7]

PARAMETER	NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Output Frequency	30-pF load 10-pF load	10 10	-	100 120	MHz MHz
DC	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{OUT}=66.67MHz	40.0	50.0	60.0	%
t_3	Rise Time[6]	Measured between 0.8V and 2.0V	-	-	2.50	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V	-	-	2.50	ns
t_5	Output to Output Skew[6]	All outputs equally loaded	-	-	250	ps
t_{6A}	Delay, REF Rising Edge to FB Rising Edge[6]	Measured at $V_{DD}/2$	-	0	±350	ps
t_{6B}	Delay, REF Rising Edge to FB Rising Edge[6]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode	1	5	8.7	ns
t_7	Device to Device Skew[6]	Measured at $V_{DD}/2$ on the FB pins of devices	-	0	700	ps
t_J	Cycle to Cycle Jitter[6]	Measured at 66.67MHz, loaded outputs	-	-	200	ps
t_{LOCK}	PLL Lock Time[6]	Stable power suppy, valid clock presented on REF pin	-	-	1.0	ms

TABLE 11: SWITCHING CHARACTERISTICS FOR XRK32309SI-1H INDUSTRIAL TEMPERATURE DEVICES[7]

PARAMETER	NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Output Frequency	30-pF load 10-pF load	10 10	-	100 120	MHz MHz
DC	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{OUT}=66.67MHz	40.0	50.0	60.0	%
		Measured at 1.4V, F_{OUT}<50.0MHz	45.0	50.0	55.0	%
t_3	Rise Time[6]	Measured between 0.8V and 2.0V	-	-	1.50	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V	-	-	1.50	ns
t_5	Output to Output Skew[6]	All outputs equally loaded	-	-	250	ps
t_{6A}	Delay, REF Rising Edge to FB Rising Edge[6]	Measured at $V_{DD}/2$	-	0	±350	ps
t_{6B}	Delay, REF Rising Edge to FB Rising Edge[6]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode	1	5	8.7	ns
t_7	Device to Device Skew[6]	Measured at $V_{DD}/2$ on the FB pins of devices	-	0	700	ps
t_8	Output Slew Rate[6]	Measured between 0.8V and 2.0V using Test Circuit #2	1	-	-	v/ns

TABLE 11: SWITCHING CHARACTERISTICS FOR XRK32309SI-1H INDUSTRIAL TEMPERATURE DEVICES[7]

PARAMETER	NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_J	Cycle to Cycle Jitter[6]	Measured at 66.67MHz, loaded outputs	-	-	200	ps
t_{LOCK}	PLL Lock Time[6]	Stable power suppy, valid clock presented on REF pin	-	-	1.0	ms

FIGURE 4. SWITCHING WAVEFORMS

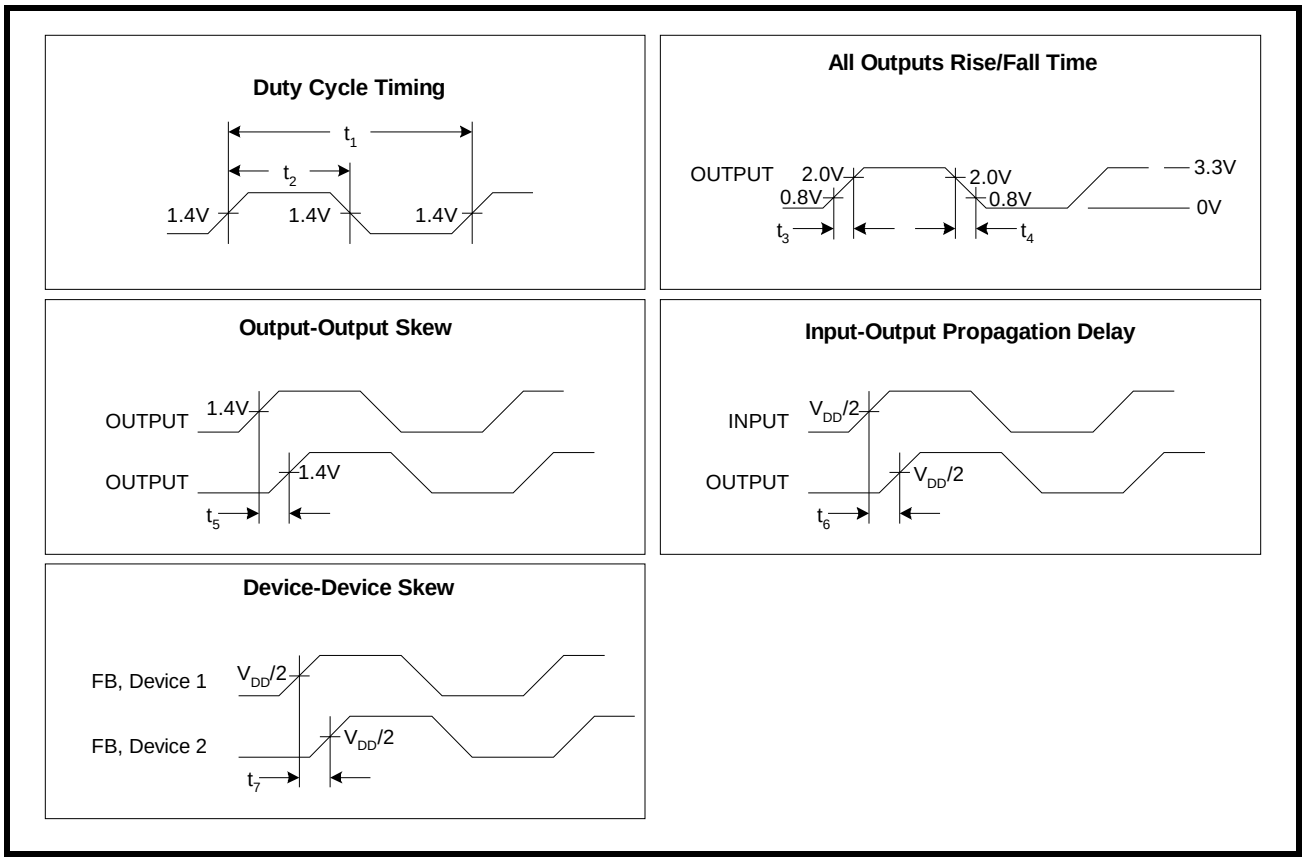
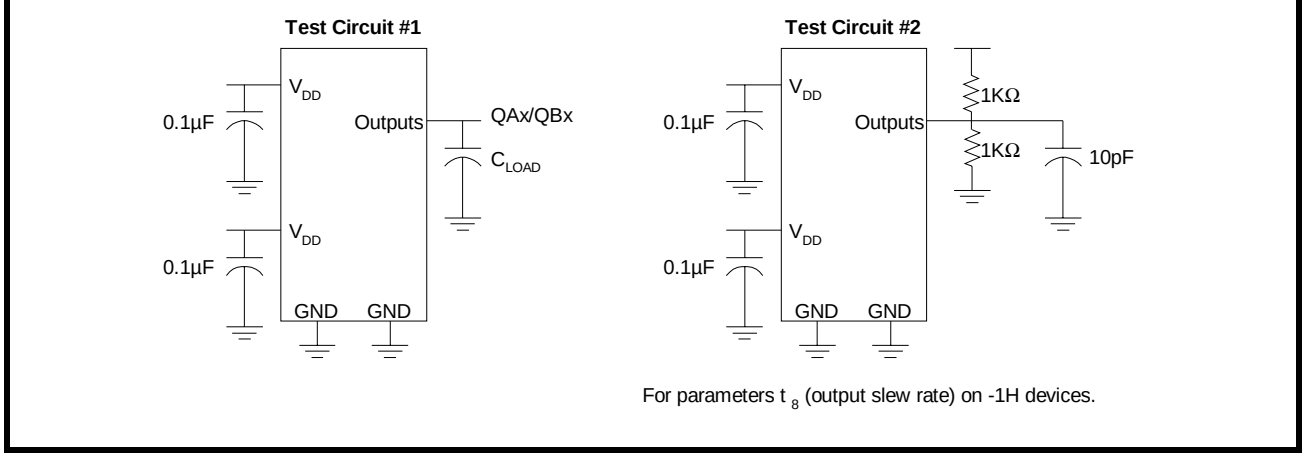


FIGURE 5. TEST CIRCUIT



For parameters t_8 (output slew rate) on -1H devices.

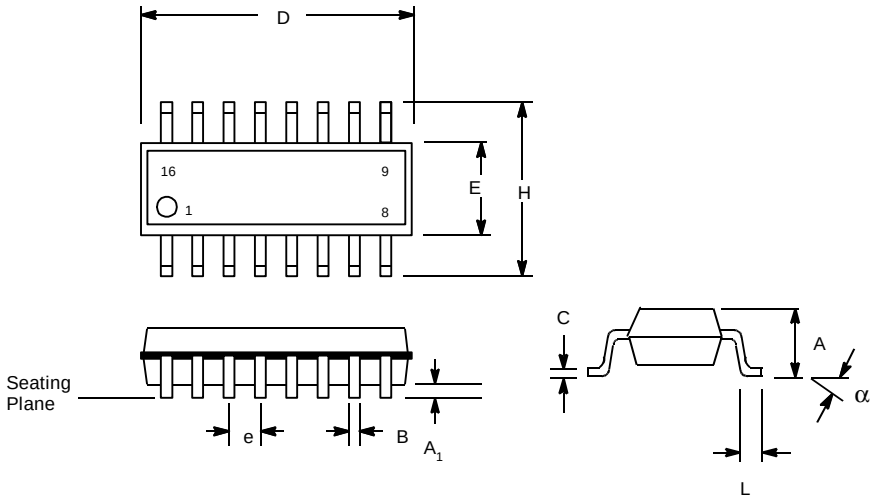
TABLE 12: ORDERING INFORMATION

PART ORDERING NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRK32309CD-1	16 PIN SOIC	0° TO +70°
XRK32309CDTR-1	16 PIN SOIC	0° TO +70°
XRK32309ID-1	16 Pin SOIC	-40° to +85°
XRK32309IDTR-1	16 Pin SOIC	-40° to +85°
XRK32309CD-1H	16 Pin SOIC	0° TO +70°
XRK32309CDTR-1H	16 Pin SOIC	0° TO +70°
XRK32309ID-1H	16 Pin SOIC	-40° to +85°
XRK32309IDTR-1H	16 Pin SOIC	-40° to +85°
XRK32309CG-1H	16 Pin TSSOP	0° TO +70°
XRK32309CGTR-1H	16 Pin TSSOP	0° TO +70°
XRK32309IG-1H	16 Pin TSSOP	-40° to +85°
XRK32309IGTR-1H	16 Pin TSSOP	-40° to +85°

PACKAGE DRAWINGS AND DIMENSIONS

FIGURE 6. XRK32309 PACKAGE DRAWING - 16 LEAD SMALL OUTLINE

16 LEAD SMALL OUTLINE
(150 MIL JEDEC SOIC)

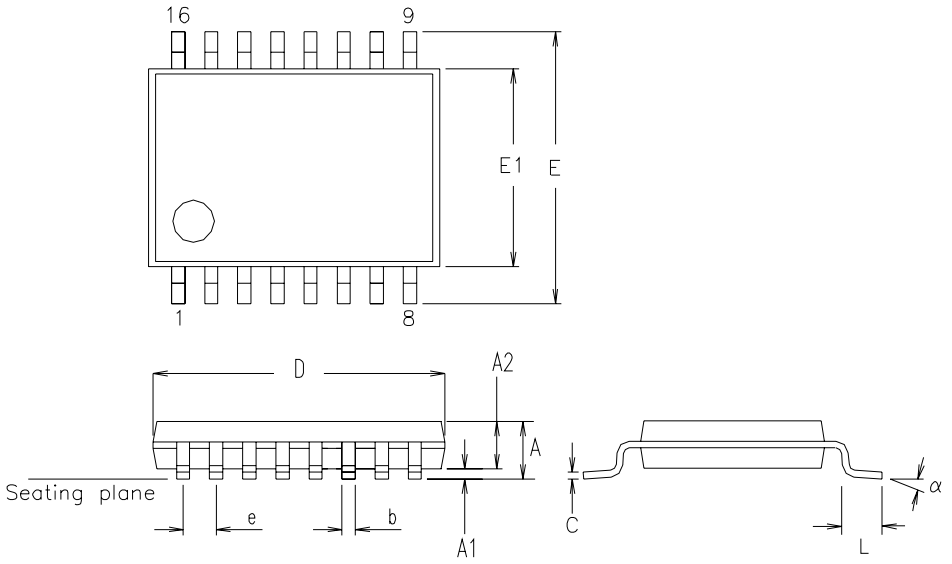


Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A_1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.386	0.394	9.80	10.00
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

FIGURE 7. XRK32309 PACKAGE DRAWING - 16 LEAD THIN SHRINK SMALL OUTLINE

16 LEAD TSSOP THIN SHRINK SMALL OUTLINE
(4.4mm TSSOP)



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.031	0.043	0.80	1.10
A1	0.002	0.006	0.05	0.15
A2	0.031	0.037	0.80	0.95
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.193	0.201	4.90	5.10
E	0.248	0.260	6.30	6.60
E1	0.169	0.177	4.30	4.50
e	0.0256 BSC		0.65 BSC	
L	0.018	0.030	0.45	0.75
α	0°	8°	0°	8°

REVISIONS

REV. #	DATE	DESCRIPTION OF CHANGES
P1.0.0	04/05/06	Initial release.
P1.0.1	05/12/06	Operating range changed to 10MHz to 120MHz - edit all references of this.

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Datasheet May 2006.

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