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REV. P1.0.0

### XRK39653 GENERAL DESCRIPTION

The XRK39653 is a low voltage high performance PLL based zero delay buffer/clock generator designed for high speed clock distribution applications. It provides 9 low skew, low jitter outputs ideal for networking, computing and telecom applications.

The PLL based design allows the 9 outputs (8 clock outputs and 1 feedback output) to be phase aligned to the input reference clock. The outputs source LVCMOS compatible levels and can drive 50Ω transmission lines. If series termination is used, each output can drive up to 2 lines providing effectively a fanout of 1:16. The XRK39653's reference input accepts a LVPECL clock source.

For normal operation (PLL used to source the outputs), the feedback output (QFB) is connected to the feedback input (FB\_IN). The VCO range of operation is 200 to 500MHz.

This means that the input/output ranges are determined by the divider setting. If ÷4 is used, the input/output range is 50 to 125MHz (high range), if ÷8 is used the input/output range is 25 to 62.5MHz (low range).

For testing purposes two PLL bypass modes are provided.

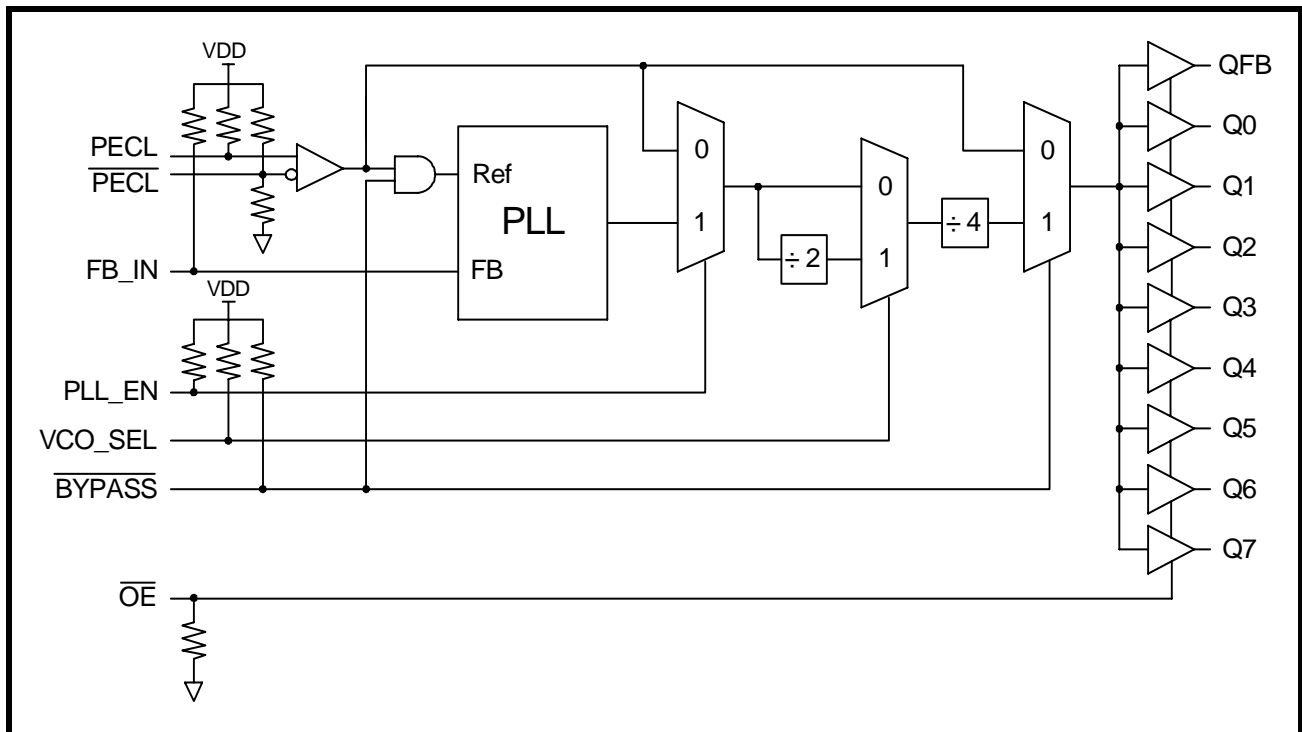
The first simply replaces the PLL output with the reference clock (PLL\_EN=0,  $\overline{\text{BYPASS}}$ =1). The dividers are still in

use. The second is a full bypass mode that has the PLL and divider operation removed ( $\overline{\text{BYPASS}}$ =0). In this mode the reference clock directly sources the outputs drivers.

### FEATURES

- 8 LVCMOS Clock Outputs
- 1 Feedback Output
- LVPECL reference clock input
- 25-200 MHz input/output frequency range
  - Input/Output range (÷4): 50-125MHz
  - Input/Output range (÷8): 25-62.5MHz
- 150ps max output to output skew
- Two bypass test mode options
- Fully Integrated PLL
- 3.3V Operation
- Pin compatible with MPC9353
- Industrial temp range: -40°C to +85°C
- 32-Lead TQFP Packaging

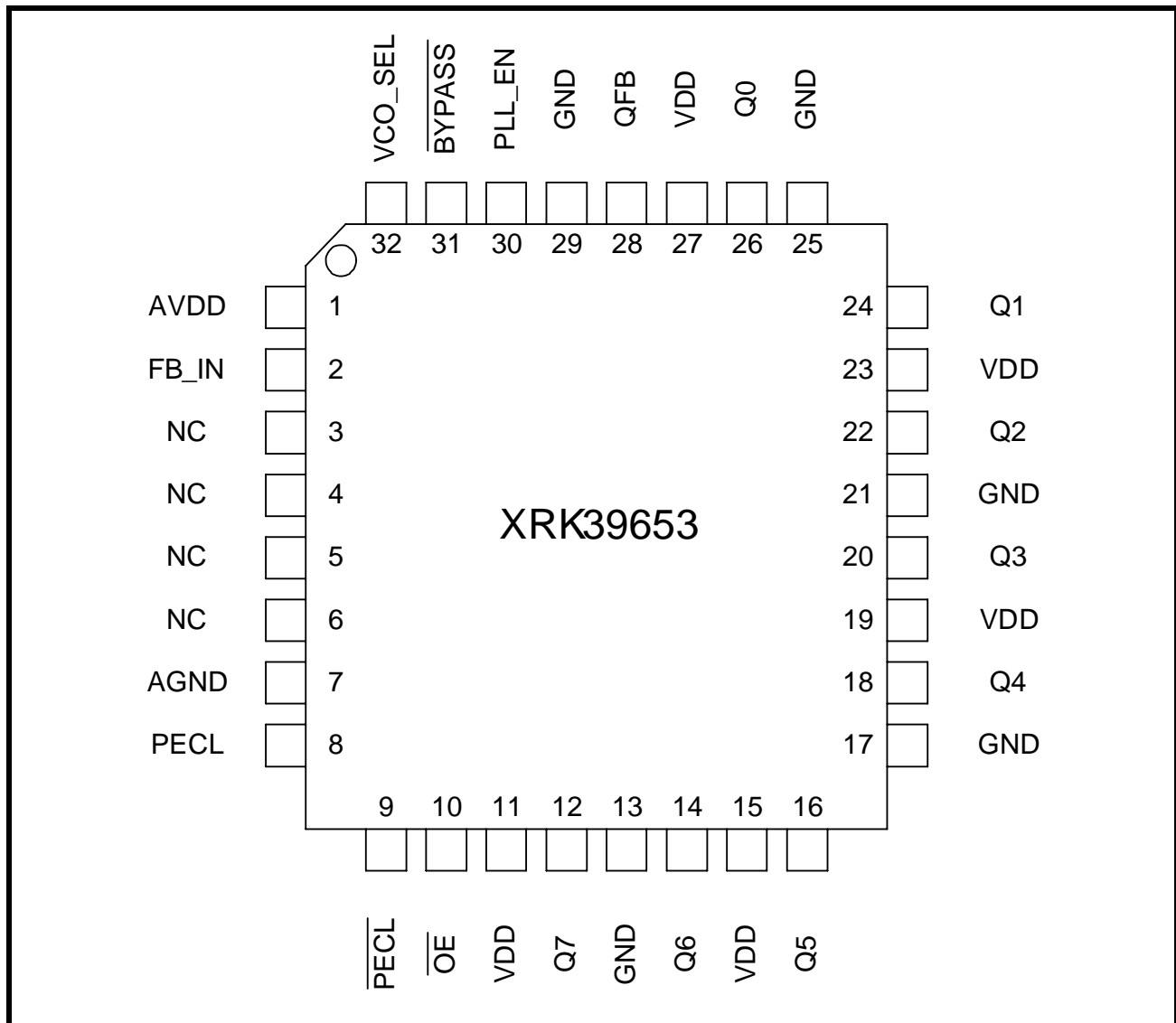
FIGURE 1. BLOCK DIAGRAM OF THE XRK39653



**PRODUCT ORDERING INFORMATION**

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRK39653IQ	32-Lead TQFP	-40°C to +85°C
XRK39653IQ-F	32-Lead TQFP "Lead Free"	-40°C to +85°C

**FIGURE 2. PIN OUT OF THE XRK39653**



**PIN DESCRIPTIONS**

NUMBER	NAME	TYPE		DESCRIPTION
1	AVDD	Power		Power supply for PLL
2	FB_IN	Input	pull-up	External PLL feedback clock input
3, 4, 5, 6	NC			
7	AGND	Power		PLL ground
8	PECL	Input		LVPECL - pos differential reference clock
9	$\overline{\text{PECL}}$	Input		LVPECL - neg differential reference clock
10	$\overline{\text{OE}}$	Input	pull-down	Output enable/disable and device reset
11,15, 19, 23, 27,	VDD	Power		Power supply
12, 14, 16, 18, 20, 22, 24, 26	Q[7:0]	Output		Clock outputs
13, 17, 21, 25, 29	GND	Power		Ground
28	QFB	Output		Feedback output for PLL
30	PLL_EN	Input	pull-up	PLL enable/disable select
31	$\overline{\text{BYPASS}}$	Input	pull-up	PLL and output divider bypass select
32	VCO_SEL	Input	pull-up	VCO divider select

**TABLE 1: CONTROL INPUT FUNCTION TABLE**

Pin Name	0	1	Default
VCO_SEL	System Divide = 4 of VCO output	System Divide = 8 of VCO output	1
PLL_EN	PLL is bypassed and disabled. The PECL clock reference source drives the outputs through the divider blocks	PLL enabled. Normal operation. VCO output drives the outputs through the divider blocks	1
$\overline{\text{BYPASS}}$	Complete bypass of the PLL and divider blocks. PECL reference clocks the outputs.	Normal operation. Dividers selected.	1
$\overline{\text{OE}}$	Outputs enabled	Outputs tri-stated and device reset. VCO running at minimum frequency	0

DC CHARACTERISTICS ( $V_{CC}= 3.3 \pm 5\%$ ,  $T_A= -40^{\circ}\text{C TO } +85^{\circ}\text{C}$ )

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNIT	CONDITION
$V_{CMR}^a$	PECL Clock inputs common mode range	1.0		$V_{DD}-0.6$	V	LVPECL
$V_{PP}$	PECL Clock peak-to-peak input voltage	300		1000	mV	LVPECL
$V_{IH}$	Input voltage high	2.0		$V_{DD}+0.3$	V	LVC MOS
$V_{IL}$	Input voltage low			0.8	V	LVC MOS
$V_{OH}$	Output High Voltage <sup>a</sup>	2.4			V	$I_{OH}=-24\text{mA}$
$V_{OL}$	Output Low Voltage <sup>a</sup>			0.55 0.30	V	$I_{OL}=24\text{mA}$ $I_{OL}=12\text{mA}$
$Z_{OUT}$	Output Impedance		14-17		$\Omega$	
$I_{IN}$	Input leakage current			$\pm 200$	$\mu\text{A}$	$V_{IN}=V_{DD}$ or $V_{IN}=\text{GND}$
$I_{CC\_PLL}$	Maximum PLL supply current		5.0	10.0	mA	$\overline{AV}_{DD}$ pin
$I_{CCQ}$	Maximum Quiescent supply current			10.0	mA	All $V_{DD}$ pins, $\overline{OE}=1$
$V_{TT}$	Output Termination Voltage		$V_{CC}\pm 2$		V	

a.  $V_{CMR}$  is the cross point of the differential input signal.

AC CHARACTERISTICS ( $V_{CC}= 3.3 \pm 5\%$ ,  $T_A= -40^{\circ}\text{C TO } +85^{\circ}\text{C}$ )<sup>a</sup>

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
$f_{VCO}$	VCO Frequency	200		500	MHz	
$f_{ref}$	Input Reference Frequency	$\div 4$ feedback $\div 8$ feedback PLL Bypass	50 25 0	125 62.5 200	MHz	PLL locked PLL locked bypass mode
$f_{MAX}$	Max Output Frequency	$\div 4$ feedback $\div 8$ feedback	50 25	125 62.5	MHz	PLL locked PLL locked
$V_{PP}$	PECL Clock peak-to-peak input voltage	450		1000	mV	LVPECL
$V_{CMR}$	PECL input Common Mode range	1.2		$V_{DD}-0.75$	V	LVPECL
$t_{PW\ Min}$	Input Reference Clock Minimum Pulse Width	2			ns	
$t_{SPO}$	Propagation Delay - Static Phase Offset (PECL to FB_IN)	-75		125	ps	PLL locked
$t_{PD}$	Propagation Delay - PLL Bypassed					
	Bypass mode 1 ( $\overline{BYPASS} = 0$ )	1.2		3.3	ns	
	Bypass mode 2, ( $\overline{BYPASS} = 1$ , $\overline{PLL\_EN} = 0$ )	3.0		7.0	ns	
$t_{skew(O)}$	Output-to-Output Skew			150	ps	
$t_{skew(PP)}$	Part to Part Skew (bypass PLL & divider)			1.5	ns	$\overline{BYPASS}=0$
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter			100	ps	

**AC CHARACTERISTICS ( $V_{CC}= 3.3 \pm 5\%$ ,  $T_A= -40^{\circ}\text{C}$  TO  $+85^{\circ}\text{C}$ )<sup>a</sup>**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
$t_{\text{JIT(PER)}}$	Period Jitter			100	ps	
$t_{\text{JIT(I/O)}}$	I/O Phase Jitter (RMS)			25	ps	
BW	PLL bandwidth ÷4 feedback ÷8 feedback			0.8 - 4 0.5 - 1.3	MHz MHz	
DC	Output duty cycle	45	50	55	%	PLL locked
$t_{\text{LOCK}}$	Maximum PLL Lock Time			10.0	ms	
$t_{\text{or}}/t_{\text{of}}$	Output Rise/Fall time	100		1000	ps	0.55 to 2.4V
$t_{\text{PLZ,HZ}}$	Output Disable Time			7	ns	
$t_{\text{PHZ,LZ}}$	Output Enable Time			6	ns	

a. AC characteristics apply for parallel output termination of 50Ω to  $V_{\text{TT}}$ .

**MAXIMUM RATINGS<sup>a</sup>**

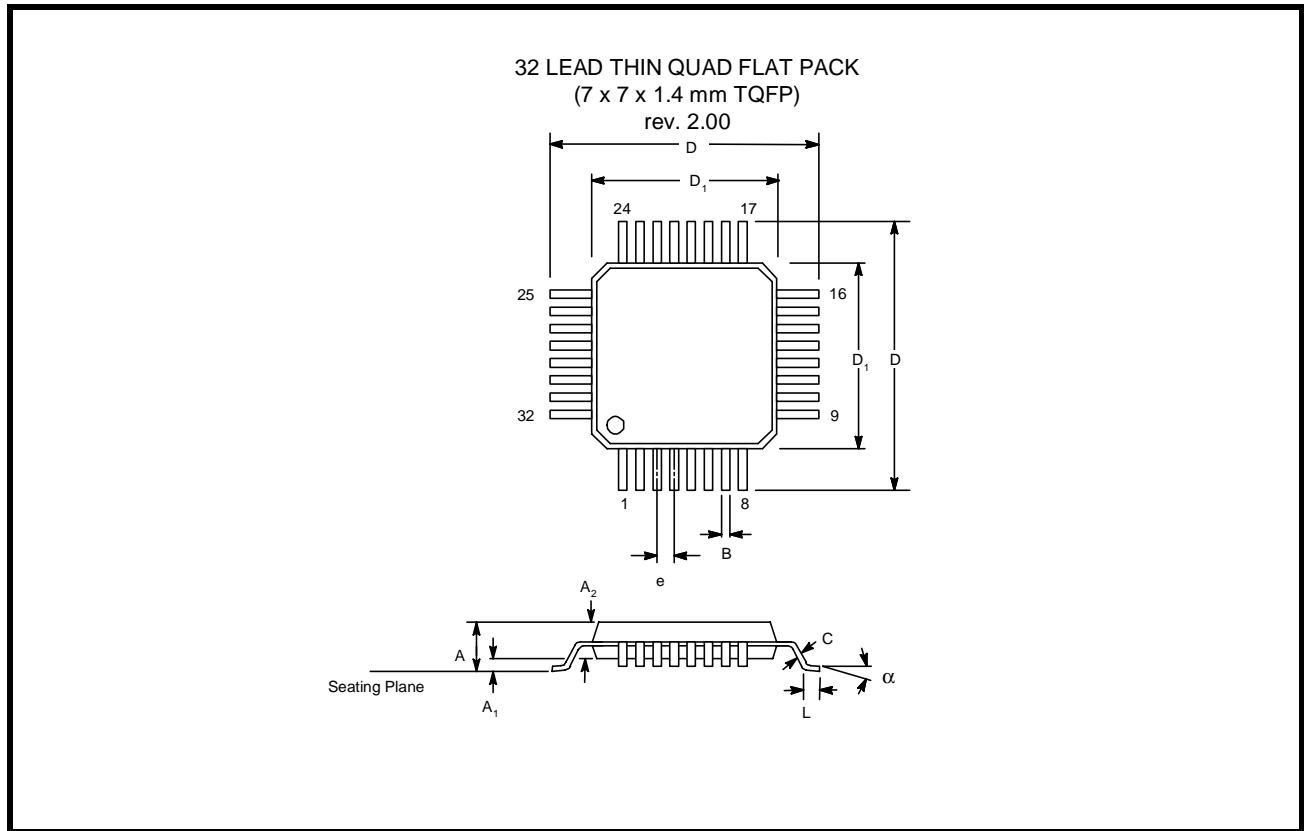
SYMBOL	CHARACTERISTICS	MIN	MAX	UNIT	CONDITION
$V_{\text{DD}}$	Supply Voltage	-0.3	3.9	V	
$V_{\text{IN}}$	DC Input Voltage	-0.3	$V_{\text{DD}}+0.3$	V	
$V_{\text{OUT}}$	DC Output Voltage	-0.3	$V_{\text{DD}}+0.3$	V	
$I_{\text{IN}}$	DC Input Current		±20	mA	
$I_{\text{OUT}}$	DC Output Current		±50	mA	
$T_{\text{S}}$	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability.

**GENERAL SPECIFICATIONS**

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNIT	CONDITION
$V_{\text{TT}}$	Output termination voltage		$V_{\text{CC}}\div 2$		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
LU	Latch-up immunity	200			mA	
$C_{\text{IN}}$	Input Capacitance		4.0		pF	Inputs

**PACKAGE DIMENSIONS**



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A <sub>1</sub>	0.002	0.006	0.05	0.15
A <sub>2</sub>	0.053	0.057	1.35	1.45
B	0.012	0.018	0.30	0.45
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D <sub>1</sub>	0.272	0.280	6.90	7.10
e	0.0315 BSC		0.80 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

**REVISION HISTORY**

REVISION #	DATE	DESCRIPTION
P1.0.0	February 2006	Initial release.

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