

FEBRUARY 2005

REV. P1.0.2

FUNCTIONAL DESCRIPTION

The XRK4991A 3.3V High-Speed Low-Voltage Programmable Skew Clock Buffer offers user selectable control over system clock functions to optimize the timing of high-performance computer systems. Eight individual drivers, arranged as four pairs of user-controllable outputs, can each drive terminated transmission lines with impedances as low as 50 Ω while delivering minimal and specified output skews and full-swing logic levels (LVTTTL).

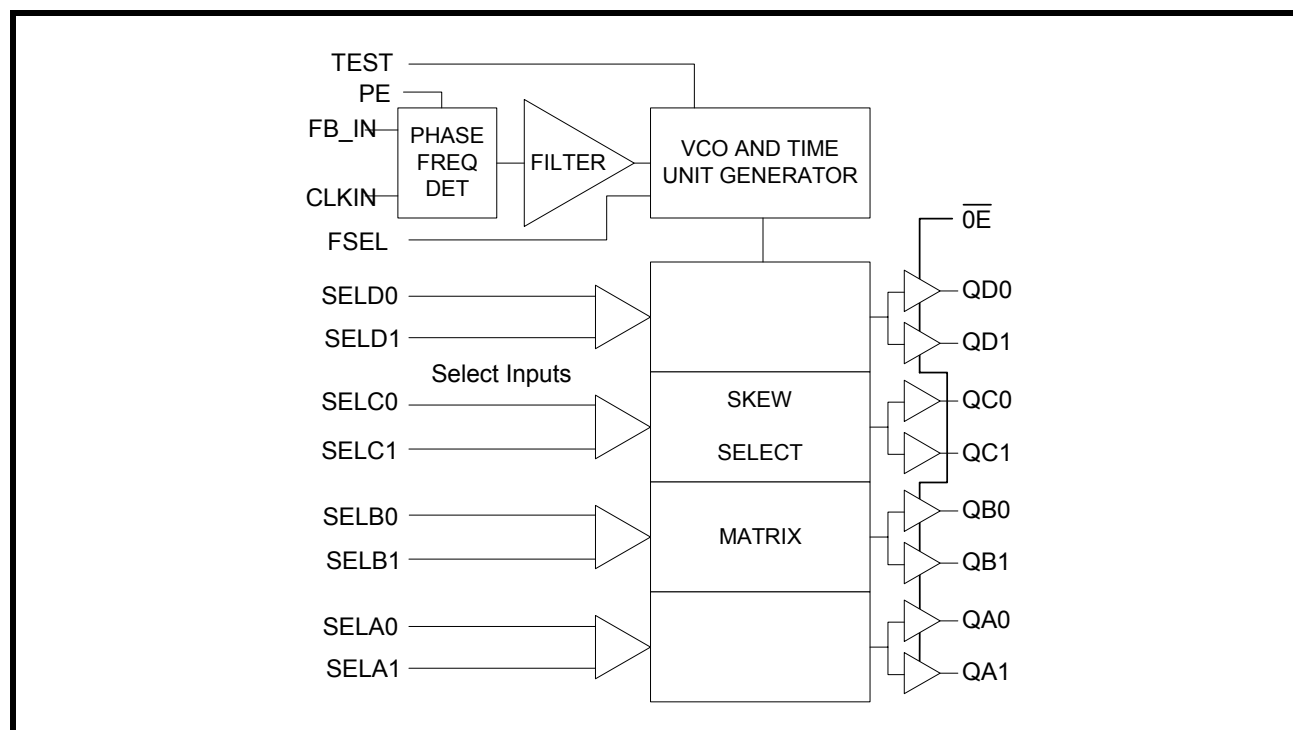
Each output can be hardwired to one of nine delay or function configurations. Delay increments of 0.7 to 1.5 ns are determined by the operating frequency with outputs able to skew up to ± 6 time units from their nominal “zero” skew position. The completely integrated PLL allows external load and transmission line delay effects to be canceled. When this “zero delay” capability is combined with the selectable output skew functions, the user can create output-to-output delays of up to ± 12 time units.

Divide-by-two and divide-by-four output functions are provided for additional flexibility in designing complex clock systems. When combined with the internal PLL, these divide functions allow distribution of a low-frequency clock that can be multiplied by two or four

at the clock destination. This feature minimizes clock distribution difficulty while allowing maximum system clock speed and flexibility.

FEATURES

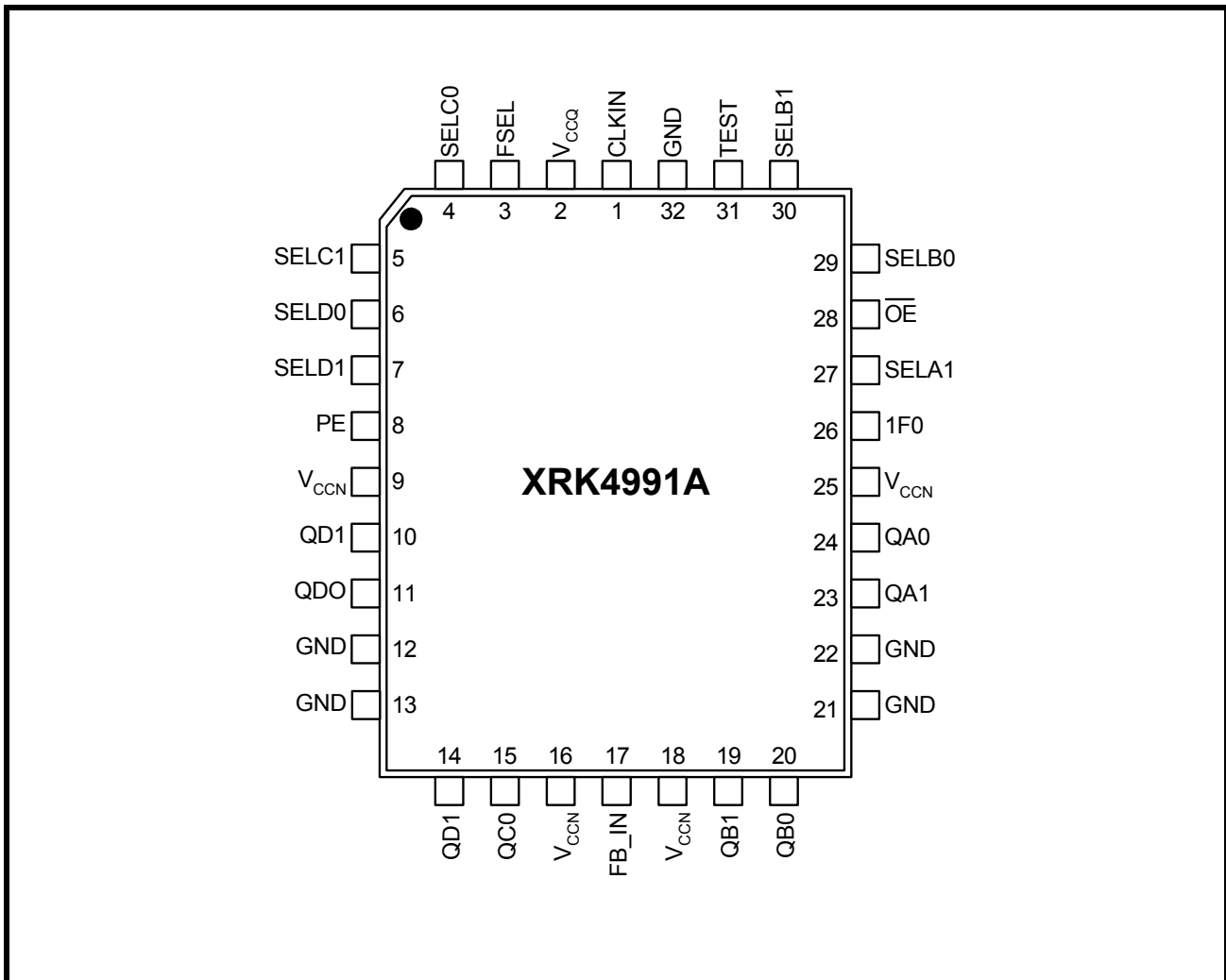
- Ref input is 5V tolerant
- 3 pairs of programmable skew outputs
- Low skew: 200ps same pair, 250ps all outputs
- Selectable positive or negative edge synchronization: Excellent for DSP applications
- Synchronous output enable
- Output frequency: 3.75MHz to 85MHz
- 2x, 4x, 1/2, and 1/4 outputs
- 2 skew grades
- 3-level inputs for skew and PLL range control
- PLL bypass for DC testing
- External feedback, internal loop filter
- 12mA balanced drive outputs
- 32-pin PLCC package
- Jitter < 200 ps peak-to-peak (< 25 ps RMS)
- Green packaging

FIGURE 1. BLOCK DIAGRAM OF THE XRK4991A

PRODUCT ORDERING INFORMATION

| PRODUCT NUMBER | ACCURACY | OPERATING TEMPERATURE RANGE |
|----------------|----------|-----------------------------|
| XRK4991AIJ-5 | 500 ps | -40°C to +85°C |
| XRK4991ACJ-5 | 500 ps | 0°C to +70°C |
| XRK4991ACJ-7 | 750 ps | 0°C to +70°C |
| XRK4991AIJ-7 | 750 ps | -40°C to +85°C |

FIGURE 2. PIN OUT OF THE XRK4991



PIN DESCRIPTIONS

| PIN NAME | PIN # | TYPE | DESCRIPTION |
|------------------|----------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLKIN | 1 | I | Reference frequency input. This input supplies the frequency and timing against which all functional variation is measured. |
| FB_IN | 17 | I | PLL feedback input (typically connected to one of the eight outputs). |
| FSEL | 3 | I | Three-level frequency range select. Set Table 2. |
| SELA0 SELA1 | 26 27 | I | Three-level function selects inputs for output pair 1 (QA0, QA1). Table 3. |
| SELB0 SELB1 | 29 30 | I | Three-level function selects inputs for output pair 2 (QB0, QB1). Table 3. |
| SELC0 SELC1 | 4 5 | I | Three-level function selects inputs for output pair 3 (QC0, QC1). See Table 3. |
| SELD0 SELD1 | 7 1 | I | Three-level function selects inputs for output pair 4 (QD0, QD1). See Table 3. |
| TEST | 31 | I | Three-level select. See test mode section under the block diagram descriptions. |
| \overline{OE} | 28 | I | Synchronous Output Enable. When HIGH, it stops clock outputs (except QC[1:0]) in a "Low" state - QC[1:0] may be used as the feedback signal to maintain phase lock. When TEST is held at MID level and \overline{OE} is "High", the nF[1:0] pins act as output disable controls for individual banks when nF[1:0] = LL. Set \overline{OE} "Low" for normal operation. |
| PE | 8 | I | Selectable positive or negative edge control. When "Low"/"High" the outputs are synchronized with the negative/positive edge of the reference clock. |
| QA0 QA1 | 24 23 | O | Output pair 1. See Table 2. |
| QB0 QB1 | 20 19 | O | Output pair 2. See Table 2. |
| QC0 QC1 | 15 14 | O | Output pair 3. See Table 2. |
| QD0 QD1 | 11 10 | O | Output pair 4. See Table 2. |
| V _{CCN} | 9 16 18 25 | PWR | Power supply for output drivers. |
| V _{CCQ} | 2 | PWR | Power supply for internal circuitry. |
| GND | 12 13 21 22 32 | PWR | Ground. |

EXTERNAL FEEDBACK

By providing external feedback, the XRK4991A gives users flexibility with regard to skew adjustment. The FB_IN signal is compared with the input CLKIN signal at the phase detector in order to drive the VCO. Phase differences cause the VCO to adjust upwards or downwards accordingly. An internal loop filter moderates the response of the VCO to the phase detector. The loop filter transfer function has been chosen to provide minimal jitter (or frequency variation) while still providing accurate responses to input frequency changes.

TABLE 1: PLL PROGRAMMABLE SKEW RANGE AND RESOLUTION TABLE

| | FSEL = LOW | FSEL = MID | FSEL = HIGH | COMMENTS |
|---------------------------------------------------------|-------------------------|-------------------------|-------------------------|-----------------|
| Timing Unit Calculation (t_U) | $1/(44 \times F_{NOM})$ | $1/(26 \times F_{NOM})$ | $1/(16 \times F_{NOM})$ | |
| VCO Frequency Range (F_{NOM}) ^(1,2) | 15 to 35MHz | 25 to 60MHz | 40 to 100MHz | |
| Skew Adjustment Range ⁽³⁾ Max Adjustment: | $\pm 9.09ns$ | $\pm 9.23ns$ | $\pm 9.38ns$ | ns |
| | $\pm 49^\circ$ | $\pm 83^\circ$ | $\pm 135^\circ$ | Phase Degrees |
| | $\pm 14\%$ | $\pm 23\%$ | $\pm 37\%$ | % of Cycle Time |
| Example 1, $F_{NOM} = 15MHz$ | $t_U = 1.52ns$ | | | |
| Example 2, $F_{NOM} = 25MHz$ | $t_U = 0.91ns$ | $t_U = 1.54ns$ | | |
| Example 3, $F_{NOM} = 30MHz$ | $t_U = 0.76ns$ | $t_U = 1.28ns$ | | |
| Example 4, $F_{NOM} = 40MHz$ | | $t_U = 0.96ns$ | $t_U = 1.56ns$ | |
| Example 5, $F_{NOM} = 50MHz$ | | $t_U = 0.77ns$ | $t_U = 1.25ns$ | |
| Example 6, $F_{NOM} = 80MHz$ | | | $t_U = 0.78ns$ | |

NOTES:

1. The device may be operated outside recommended frequency ranges without damage, but functional operation is not guaranteed. Selecting the appropriate FSEL value based on input frequency range allows the PLL to operate in its 'sweet spot' where jitter is lowest.
2. The level to be set on FSEL is determined by the nominal operating frequency of the VCO and Time Unit Generator. The VCO frequency always appears at QA[1:0], QB[1:0] and the higher outputs when they are operated in their undivided modes. The frequency appearing at the CLKIN and FB_IN inputs will be the same as the VCO when the output connected to FB_IN is undivided. The frequency of the CLKIN and FB_IN inputs will be 1/2 or 1/4 the VCO frequency when the part is configured for a frequency multiplication by using a divided output as the FB_IN input.
3. Skew adjustment range assumes that a zero skew output is used for feedback. If a skewed Q output is used for feedback, then adjustment range will be greater. For example if a $4t_U$ skewed output is used for feedback, all other outputs will be skewed $-4t_U$ in addition to whatever skew value is programmed for those outputs. 'Max adjustment' range applies to output pairs 3 and 4 where $\pm 6t_U$ skew adjustment is possible and at the lowest FNOM value.

TABLE 2: FREQUENCY RANGE SELECT AND t_U CALCULATION ^[1]

| FSEL ^[2,3] | f_{NOM} (MHz) | | $t_U = 1 / f_{NOM} \times N$ WHERE N = | APPROXIMATE FREQUENCY (MHz) AT WHICH $t_U = 1.0ns$ |
|-----------------------|-----------------|-----|-------------------------------------------|----------------------------------------------------------|
| | MIN | MAX | | |
| LOW | 15 | 30 | 44 | 22.7 |
| MID | 25 | 50 | 26 | 38.5 |
| HIGH | 40 | 85 | 16 | 62.5 |

SKEW SELECT MATRIX

The skew select matrix is comprised of four independent sections. Each section has two low-skew, high-fanout drivers (Qx[0:1]), and two corresponding three-level function select (SELx[0:1]) inputs. Table 2 below shows the nine possible output functions for each section as determined by the function select inputs. All times are measured with respect to the CLKIN input assuming that the output connected to the FB_IN input has 0t_U selected.

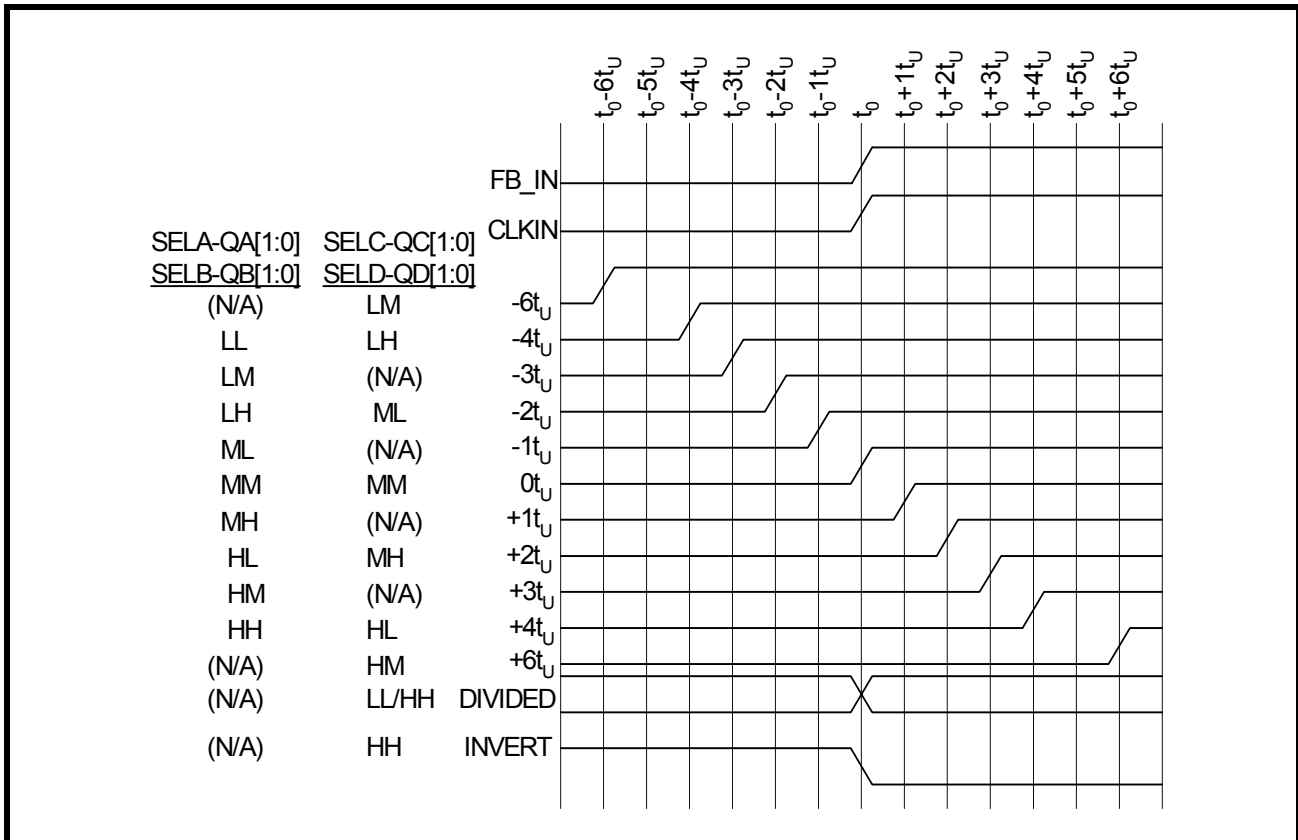
TABLE 3: PROGRAMMABLE SKEW CONFIGURATIONS ^[1]

| FUNCTION SELECTS | | OUTPUT FUNCTIONS | | |
|------------------|-------|------------------|------------------|------------------|
| SELx1 | SELx0 | QA[1:0], QB[1:0] | QC[1:0] | QD[1:0] |
| LOW | LOW | -4t _U | Divide by 2 | Divide by 2 |
| LOW | MID | -3t _U | -6t _U | -6t _U |
| LOW | HIGH | -2t _U | -4t _U | -4t _U |
| MID | LOW | -1t _U | -2t _U | -2t _U |
| MID | MID | 0t _U | 0t _U | 0t _U |
| MID | HIGH | +1t _U | +2t _U | +2t _U |
| HIGH | LOW | +2t _U | +4t _U | +4t _U |
| HIGH | MID | +3t _U | +6t _U | +6t _U |
| HIGH | HIGH | +4t _U | Divide by 4 | Inverted |

NOTES:

1. For all three-state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to V_{CC}/2.
2. The level to be set on FSEL is determined by the “normal” operating frequency (f_{NOM}) of the V_{CO} and Time Unit Generator (see Logic Block Diagram). Nominal frequency (f_{NOM}) always appears at QA0 and the other outputs when they are operated in their undivided modes (see Table 2). The frequency appearing at the CLKIN and FB_IN inputs will be f_{NOM} when the output connected to FB_IN is undivided. The frequency of the CLKIN and FB_IN inputs will be f_{NOM}/2 or f_{NOM}/4 when the part is configured for a frequency multiplication by using a divided output as the FB_IN input.
3. When the FSEL pin is selected HIGH, the CLKIN input must not transition upon power-up until V_{CC} has reached 2.8V.

FIGURE 3. TYPICAL OUTPUTS WITH FB_IN CONNECTED TO A ZERO-SKEW OUTPUT [4]



NOTES:

4. FB_IN connected to an output selected for "zero" skew (i.e. SELx1 = SELx0 = MID).

TEST MODE

The TEST input is a three-level input. In normal system operation, this pin is connected to ground, allowing the XRK4991 to operate as explained briefly above (for testing purposes, any of the three-level inputs can have a removable jumper to ground, or be tied LOW through a 100Ω resistor. This will allow an external tester to change the state of these pins.)

If the TEST input is forced to its MID or HIGH state, the device will operate with its internal phase locked loop disconnected, and input levels supplied to CLKIN will directly control all outputs. Relative output to output functions are the same as in normal mode.

In contrast with normal operation (TEST tied LOW). All outputs will function based only on the connection of their own function select inputs (SELx[1:0]) and the waveform characteristics.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS ⁽⁵⁾

| | |
|---------------------------------------------------------|-----------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature with Power Applied | -55°C to +125°C |
| Supply Voltage to Ground | -0.5V to +7.0V |
| DC Input Voltage | -0.5V to +7.0V |
| Output Current into Outputs (LOW) | 64 mA |
| Static Discharge Voltage (per MIL-STD-883, Method 3015) | >2001V |
| Latch-Up Current. | >200 mA |

NOTES:

5. Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

TABLE 4: DC ELECTRICAL CHARACTERISTICS OVER THE 3.3V ± 10% OPERATING RANGE

| SYMBOL | DESCRIPTION | MIN | MAX | UNIT | CONDITION | |
|------------------|------------------------------------------------------------|------------------------|------------------------|------|---------------------------------------------------------------------------|------------|
| V _{IH} | Input HIGH Voltage (CLKIN, FB_IN, \overline{OE} , PE) | 2.0 | V _{CC} | V | Guaranteed Logic HIGH (CLKIN, FB_IN, \overline{OE} , PE Inputs Only) | |
| V _{IL} | Input LOW Voltage (CLKIN, FB_IN, \overline{OE} , PE) | | 0.8 | V | Guaranteed Logic LOW (CLKIN, FB_IN, \overline{OE} , PE Inputs Only) | |
| V _{IHH} | Three-Level Input HIGH Voltage ^[6] | V _{CC} -0.6 | V _{CC} | V | 3-Level Inputs Only | |
| V _{IMM} | Three-Level Input MID Voltage ^[6] | V _{CC} /2-0.3 | V _{CC} /2+0.3 | V | 3-Level Inputs Only | |
| V _{ILL} | Three-Level Input LOW Voltage ^[6] | | 0.6 | V | 3-Level Inputs Only | |
| I _{IN} | Input Leakage Current (CLKIN and FB_IN inputs only) | | ± 5 | μA | V _{CC} = Max. V _{IN} = V _{CC} or GND | |
| I ₃ | 3-Level Input DC Current (TEST, FSEL) | | ±200 | μA | V _{IN} = V _{CC} | HIGH Level |
| | | | ±50 | μA | V _{IN} = V _{CC} /2 | MID Level |
| | | | ±200 | μA | V _{IN} = GND | LOW Level |
| I _{IPU} | Input Pull-Up Current (PE) | | ±100 | μA | V _{CC} = Max V _{IN} = GND | |
| I _{IPD} | Input Pull-Down Current (\overline{OE}) | | ±100 | μA | V _{CC} = Max V _{IN} = V _{CC} | |
| V _{OH} | Output HIGH Voltage | 2.4 | | V | V _{CC} = Min., I _{OH} = -12mA | |
| V _{OL} | Output LOW Voltage | | 0.55 | V | V _{CC} = Min., I _{OL} = 12mA | |

NOTES:

6. These inputs are normally wired to VCC, GND, or unconnected. Internal termination resistors bias unconnected inputs to V_{CC}/2. If these inputs are switched (during operation), the function and timing of the outputs may be glitched, and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.

TABLE 5: POWER REQUIREMENTS ($V_{CC} = 3.3V \pm 10\%$ OPERATING RANGE)

| SYMBOL | PARAMETER | TEST CONDITIONS | TYP | MAX. | UNIT |
|-----------------|-----------------------------------------|----------------------------------------------------------------------------------------------------------------|-----|------|-------------|
| I_{CCQ} | Quiescent Power Supply Current | $V_{CC} = \text{Max.}$, TEST=MID, CLKIN=LOW PE=LOW, $\overline{OE} = \text{LOW}$, All outputs unloaded | 8 | 25 | mA |
| ΔI_{CC} | Power Supply Current per Input HIGH | $V_{CC} = \text{Max.}$, $V_{IN} = 3V$ | 1 | 30 | μA |
| I_{CCD} | Dynamic Power Supply Current per Output | $V_{CC} = \text{Max.}$, $C_L = 0pF$ | 55 | 90 | $\mu A/MHz$ |
| I_{TOT} | Total Power Supply Current | $V_{CC} = 3.3V$, $F_{CLKIN} = 20MHz$, $C_L = 160pF^{(1)}$ | 29 | | mA |
| | | $V_{CC} = 3.3V$, $F_{CLKIN} = 33MHz$, $C_L = 160pF^{(1)}$ | 42 | | |
| | | $V_{CC} = 3.3V$, $F_{CLKIN} = 66MHz$, $C_L = 160pF^{(1)}$ | 76 | | |

NOTE: (1) For eight outputs, each loaded with 20pF.

TABLE 6: INPUT TIMING REQUIREMENTS

| SYMBOL | DESCRIPTION ⁽¹⁾ | MIN. | MAX. | UNIT |
|------------|-----------------------------------------------|------|------|------|
| t_R, t_F | Maximum input rise and fall times, 0.8V to 2V | | 10 | ns/V |
| t_{PWC} | Input clock pulse, HIGH or LOW | 3 | | ns |
| D_H | Input duty cycle | 10 | 90 | % |
| CLKIN | Reference Clock Input | 3.75 | 85 | MHz |

NOTE: (1) Where pulse width implied by D_H is less than t_{PWC} limit, t_{PWC} limit applies.

TABLE 7: SWITCHING CHARACTERISTICS (3.3V ± 10% OPERATING RANGE)

| SYMBOL | PARAMETER | XRK4991A-2 | | | XRK4991A-5 | | | XRK4991A-7 | | | UNIT |
|----------------------|--------------------------------------------------------------------|------------------------------------------------------|------|------|------------|------|------|------------|-----|------|------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| F _{NOM} | VCO Frequency Range | See PLL Programmable Skew Range and Resolution Table | | | | | | | | | |
| t _{RPWH} | CLKIN Pulse Width HIGH ⁽¹¹⁾ | 3 | | | 3 | | | 3 | | | ns |
| t _{RPWL} | CLKIN Pulse Width LOW ⁽¹¹⁾ | 3 | | | 3 | | | 3 | | | ns |
| t _U | Programmable Skew Time Unit | See Control Summary Table | | | | | | | | | |
| t _{SKREWPR} | Zero Output Matched-Pair Skew (Qx[1:0]) [1,2,3] | | 0.05 | 0.2 | | 0.1 | 0.25 | | 0.1 | 0.25 | ns |
| t _{SKREW0} | Zero Output Skew (All Outputs) [1, 4] | | 0.1 | 0.25 | | 0.25 | 0.5 | | 0.3 | 0.75 | ns |
| t _{SKREW1} | Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs) [1, 6] | | 0.25 | 0.5 | | 0.6 | 0.7 | | 0.6 | 1 | ns |
| t _{SKREW2} | Output Skew (Rise-Fall, Divided-Divided) [1, 6] | | 0.3 | 1.2 | | 0.5 | 1.2 | | 1 | 1.5 | ns |
| t _{SKREW3} | Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs) [1, 6] | | 0.25 | 0.5 | | 0.5 | 0.7 | | 0.7 | 1.2 | ns |
| t _{SKREW4} | Output Skew (Rise-Fall, Nominal-Divided, [1, 2]) | | 0.5 | 0.9 | | 0.5 | 1 | | 1.2 | 1.7 | ns |
| t _{DEV} | Device-to-Device Skew [1, 2, 7] | | | 0.75 | | | 1.25 | | | 1.65 | ns |
| t _{PD} | CLKIN Input to FB_IN Propagation Delay [1, 9] | -0.25 | 0 | 0.25 | -0.5 | 0 | 0.5 | -0.7 | 0 | 0.7 | ns |
| t _{ODCV} | Output Duty Cycle Variation from 50% [1] | -1.2 | 0 | 1.2 | -1.2 | 0 | 1.2 | -1.2 | 0 | 1.2 | ns |
| t _{PWH} | Output HIGH Time Deviation from 50% [1, 10] | | | 2 | | | 2.5 | | | 3 | ns |
| t _{PWL} | Output LOW Time Deviation from 50% [1,11] | | | 1.5 | | | 3 | | | 3.5 | ns |
| t _{ORISE} | Output Rise Time [1] | 0.15 | 1 | 1.2 | 0.15 | 1 | 1.8 | 0.15 | 1.5 | 2.5 | ns |
| t _{OFALL} | Output Fall Time [1] | 0.15 | 1 | 1.2 | 0.15 | 1 | 1.8 | 0.15 | 1.5 | 2.5 | ns |
| t _{LOCK} | PLL Lock Time [1,8] | | | 0.5 | | | 0.5 | | | 0.5 | ns |
| t _{JR} | Cycle-to-Cycle Output Jitter [1] | RMS | | 25 | | | 25 | | | 25 | ps |
| | | Peak-to-Peak | | 200 | | | 200 | | | 200 | |

NOTES:

1. All timing and jitter tolerances apply for F_{NOM} > 25MHz.
2. Skew is the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with the specified load.
3. t_{SKREWPR} is the skew between a pair of outputs (Qx[1:0]) when all eight outputs are selected for 0t_U.
4. t_{SKREW0} is the skew between outputs when they are selected for 0t_U.

5. For XRK4993-2 t_{SKEW0} is measured with $C_L = 0pF$; for $C_L = 20pF$, $t_{SKEW0} = 0.35ns$ Max.
6. There are 2 classes of outputs: Nominal (multiple of t_U delay), and Divided (QC[1:0] only in Divide-by-2 or Divide-by-4 mode).
7. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{CC} , ambient temperature, air flow, etc.)
8. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at CLKIN or FB_IN until tPD is within specified limits.
9. t_{PD} is measured with CLKIN input rise and fall times (from 0.8V to 2V) of 1ns.
10. Measured at 2V.
11. Measured at 0.8V.

FIGURE 4. AC TEST LOADS AND WAVEFORMS

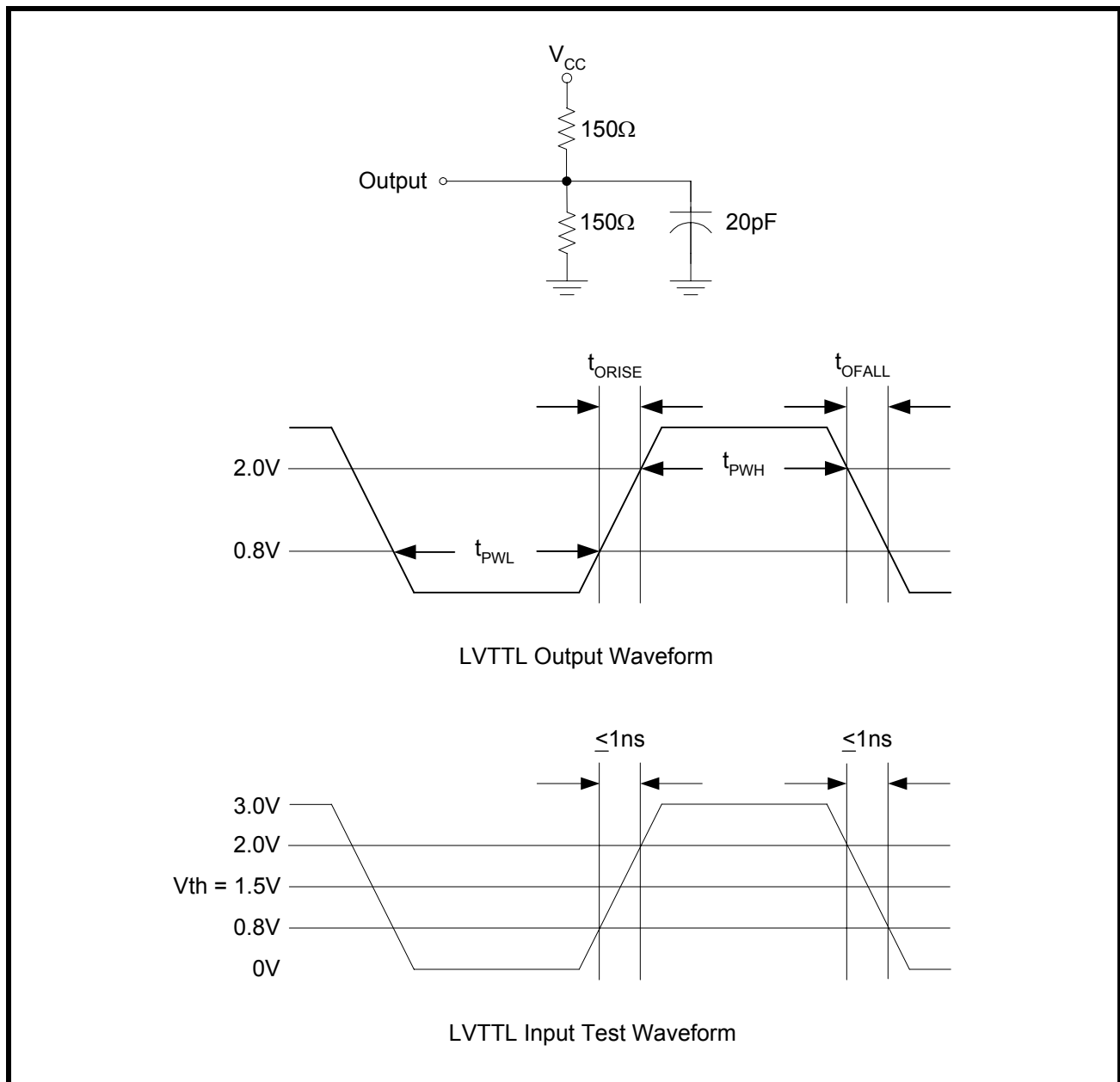
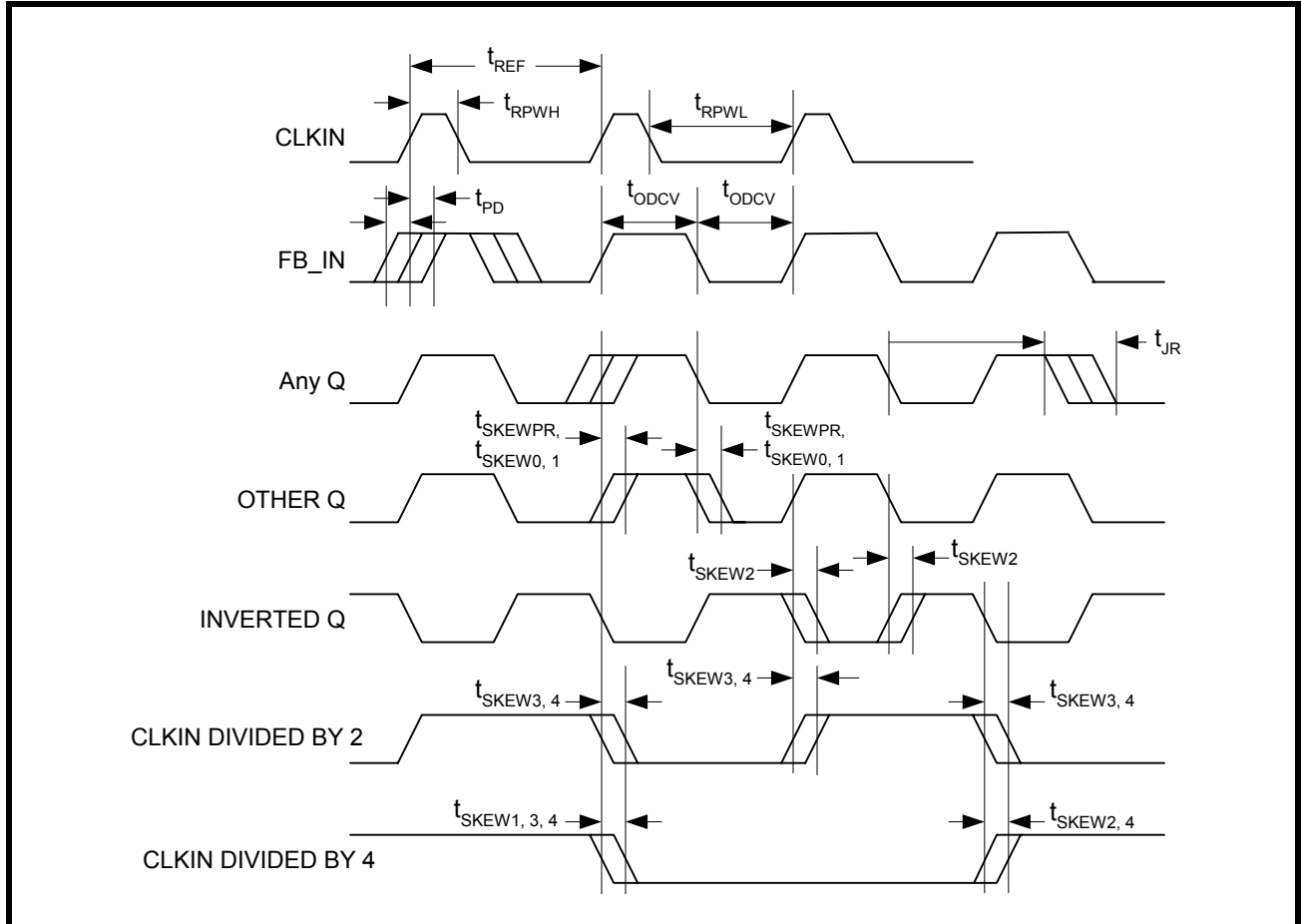


FIGURE 5. AC TIMING DIAGRAM

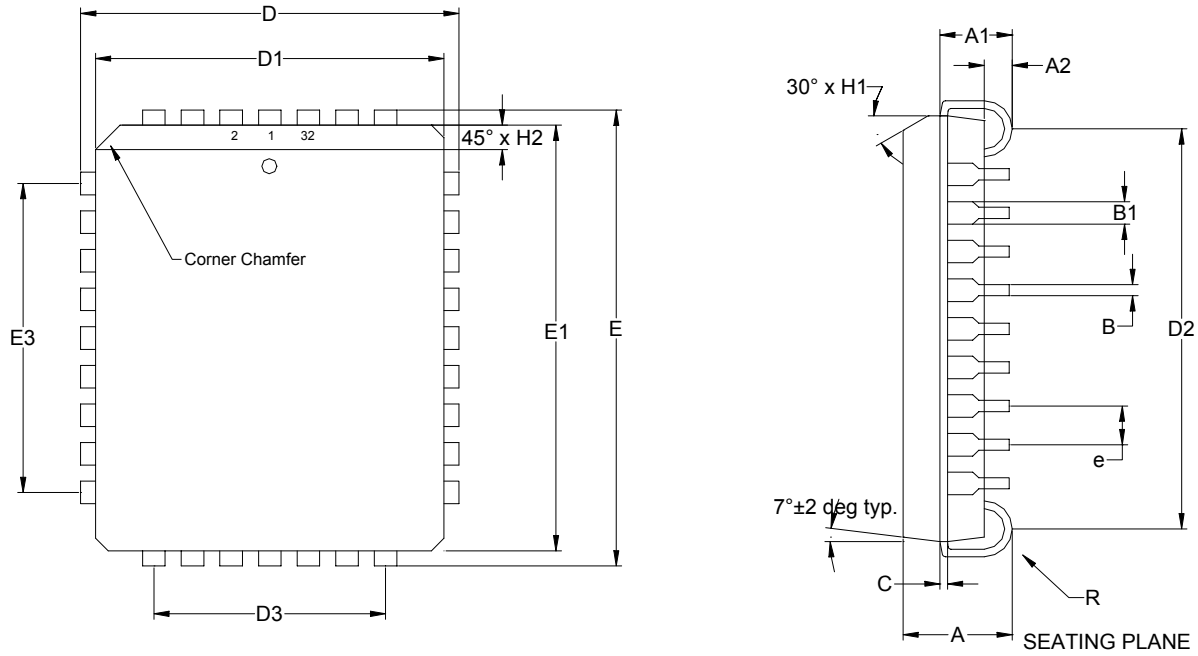


NOTES:

1. PE: The AC Timing Diagram applies to $PE=V_{CC}$. For $PE=GND$, the negative edge of FB_IN aligns with the negative edge of CLKIN, divided outputs change on the negative edge of CLKIN, and the positive edges of the divide-by-2 and the divide-by-4 signals align.
2. Skew: The time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with 20pF and terminated with 75Ω to $V_{CC}/2$.
3. t_{SKEWPR} : The skew between a pair of outputs (Qx[1:0]) when all eight outputs are selected for $0t_U$.
4. t_{SKEW0} : The skew between outputs when they are selected for $0t_U$.
5. t_{DEV} : The output-to-output skew between any two devices operating under the same conditions (V_{CC} , ambient temperature, air flow, etc.)
6. t_{ODCV} : The deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.
7. t_{PWH} is measured at 2V.
8. t_{PWL} is measured at 0.8V.
9. t_{ORISE} and t_{OFALL} are measured between 0.8V and 2V.
10. t_{LOCK} : The time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at CLKIN or FB_IN until t_{PD} is within specified limits.

PACKAGE DIMENSIONS

**32 LEAD PLASTIC LEADED CHIP CARRIER
 (PLCC)
 Rev. 1.00**



| SYMBOL | INCHES | | MILLIMETERS | |
|--------|------------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.120 | 0.140 | 3.05 | 3.56 |
| A1 | 0.075 | 0.095 | 1.91 | 2.41 |
| A2 | 0.020 | --- | 0.51 | --- |
| B | 0.013 | 0.021 | 0.33 | 0.53 |
| B1 | 0.026 | 0.032 | 0.66 | 0.81 |
| C | 0.008 | 0.013 | 0.19 | 0.32 |
| D | 0.485 | 0.495 | 12.33 | 12.58 |
| D1 | 0.448 | 0.454 | 11.39 | 11.54 |
| D2 | 0.400 | 0.440 | 10.17 | 11.18 |
| D3 | 0.300 typ. | | 7.62 typ. | |
| E | 0.585 | 0.595 | 14.87 | 15.11 |
| E1 | 0.545 | 0.557 | 13.85 | 14.15 |
| E2 | 0.500 | 0.540 | 12.71 | 13.72 |
| E3 | 0.400 typ. | | 10.16 typ. | |
| e | 0.050 BSC | | 1.27 BSC | |
| H1 | 0.023 | 0.029 | 0.58 | 0.74 |
| H2 | 0.042 | 0.048 | 1.07 | 1.22 |
| R | 0.025 | 0.045 | 0.64 | 1.14 |

Note: The control dimension is in inches.

REVISION HISTORY

| REVISION # | DATE | DESCRIPTION |
|------------|---------------|--------------------------------------------------------------------------------------------|
| P1.0.0 | February 2004 | Initial release |
| P1.0.1 | July 2004 | Update block diagram. |
| P1.0.2 | February 2005 | Renamed pins to Exar convention., removed reference to 2.5V operation. Made edits to text. |
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