

## GENERAL DESCRIPTION

The XRK69772 is a PLL based LVCMOS Clock Generator targeted for high performance and low skew clock distribution applications. The XRK69772 can select between one of three reference inputs and provides 14 LVCMOS outputs -12 outputs (3 banks of 4) for clock distribution, 1 for feedback and 1 for synchronization.

The XRK69772 is a highly flexible device. It can be configured to accept either a crystal oscillator input or one of two LVCMOS compatible inputs for use as the input reference clock source. To support clock redundancy, two LVCMOS inputs are provided. Switching the internal reference clock is controlled by the control input, CLK\_SEL.

The XRK69772 uses PLL technology to frequency lock its outputs to the input reference clock. The divider in the feedback path will determine the frequency of the VCO. Each of the separate output banks can individually divide down the VCO output frequency. This allows the XRK69772 to generate a multitude of different bank frequency ratios and output-to-input frequency ratios.

The outputs of the XRK69772 can individually be immobilized, in the low state, by use of the stop clock feature. All outputs except QC0 and QFB can be immobilized through a 2 pin serial interface. Global output disabling and reset can be achieved the control input MR/OE.

The XRK69772 also has a QSYNC output which can be used for system synchronization purposes. It monitors Bank A and Bank C outputs and goes low one period of the faster clock prior to coincident rising edges of Bank A and

Bank C clocks. QSYNC then goes high again when the coincident rising edges of Bank A and Bank C occur. This feature is used primarily in applications where Bank A and Bank C are running at different frequencies, and is particularly useful when they are running at non-integer multiples of one another.

The XRK69772 has an output frequency range of 8.33MHz to 125MHz and an input frequency range of 5MHz to 120MHz.

## FEATURES

- Fully Integrated PLL
- Selectable crystal oscillator or LVCMOS inputs for reference clock source
- 14 LVCMOS outputs
  - 3 banks with 4 outputs each. Frequencies can be individually controlled by bank
  - 1 dedicated feedback with frequency control
  - 1 Sync
- VCO Range 200MHz to 480MHz
- Output freq. range: 5MHz to 240MHz
- Max Output Skew of 250ps
- Cycle-to-cycle jitter: 150ps (typ)

## APPLICATIONS

- System Clock generator
- Zero Delay Buffer

## PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRK69772CR	52-LEAD LQFP	0°C to +70°C
XRK69772IR	52-LEAD LQFP	-40°C to +85°C

1:12 LVCMOS PLL CLOCK GENERATOR

FIGURE 1. BLOCK DIAGRAM OF THE XRK69772

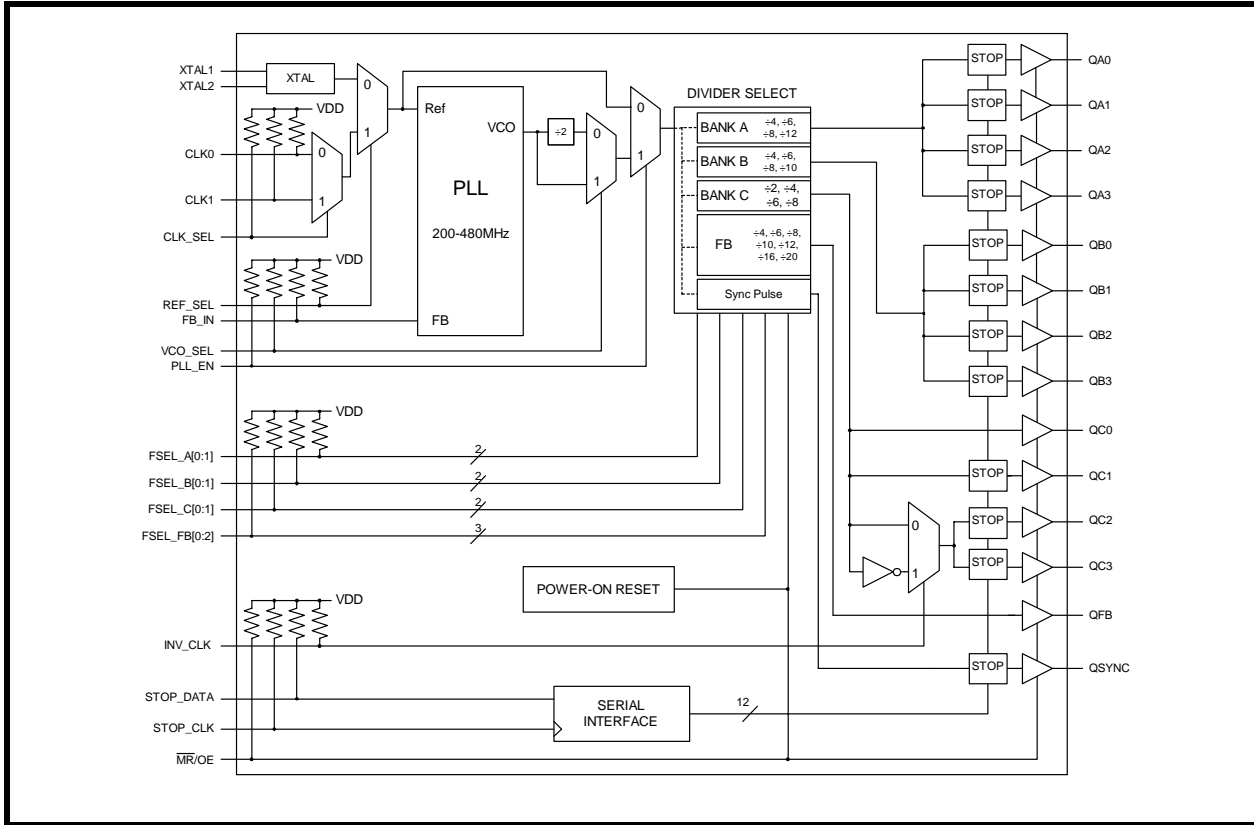
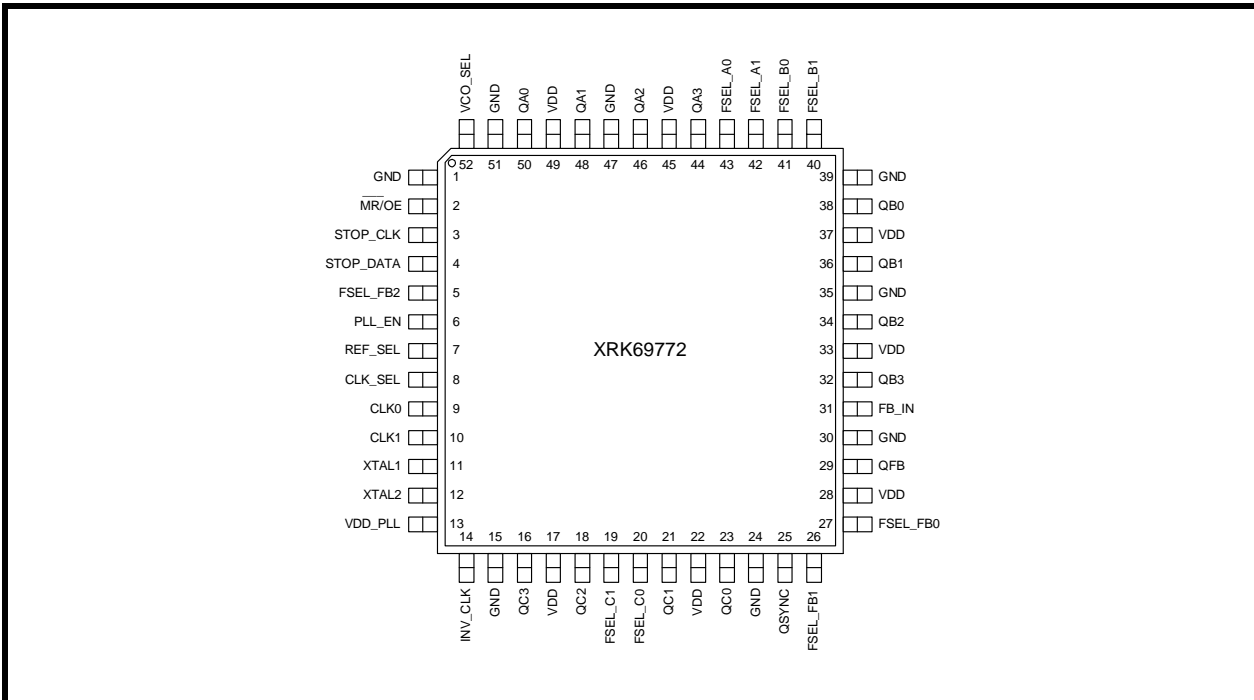


FIGURE 2. PIN OUT OF THE XRK69772



## PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
1, 15, 24, 30, 35, 39, 47, 51	GND	POWER	Power supply ground
2	$\overline{\text{MR/OE}}$	INPUT*	Master reset and output enable. High = output enabled, Low = device reset & outputs tri-stated
3	STOP_CLK	INPUT*	Clock input for serial control.
4	STOP_DATA	INPUT*	Data input for serial control
5, 26, 27	FSEL_FB[2:0]	INPUT*	Select inputs for control of feedback divide value.
6	PLL_EN	INPUT*	PLL bypass. High = PLL, Low = PLL bypass
7	REF_SEL	INPUT*	Xtal or CLKx select. High = Xtal input selected, Low = CLK0 or CLK1 selected
8	CLK_SEL	INPUT*	CLK0 or CLK1 Select. High = CLK1selected, Low = CLK0 selected
9,10	CLK0, CLK1	INPUT*	Reference clock inputs.
11	XTAL1	INPUT	Crystal oscillator input
12	XTAL2	OUTPUT	Crystal oscillator output
13	VDD_PLL	POWER	Analog supply for PLL
14	INV_CLK	INPUT*	Invert clock select for QC3 & QC2. High = invert, Low = normal operation
16, 18, 21, 23	QC[3:0]	OUTPUT	Clock outputs (Bank C)
17, 22, 33, 37, 45, 49	VDD	POWER	Power supply for outputs.
19, 20	FSEL_C[1:0]	INPUT*	Bank C divide select pins.
25	QSYNC	OUTPUT	Synchronization output for Bank A and Bank C.
28	VDD	POWER	Power supply for core.
29	QFB	OUTPUT	Feedback clock output
31	FB_IN	INPUT*	Feedback input
32, 34, 36, 38	QB[3:0]	OUTPUT	Clock outputs (Bank B)
40, 41	FSEL_B[1:0]	INPUT*	Bank B divide select pins.
42, 43	FSEL_A[1:0]	INPUT*	Bank A divide select pins.
44, 46, 48, 50	QA[3:0]	OUTPUT	Clock outputs (Bank A)
52	VCO_SEL	INPUT*	VCO select. High = VCO/1, Low = VCO/2.

\* 25K $\Omega$  pull-up resistor

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## 1.0 DEVICE SPECIFICATIONS

TABLE 1: GENERAL SPECIFICATIONS

SYMBOL	CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNIT
$V_{TT}$	Output Termination Voltage			$V_{DD} \div 2$		V
$ESD_{MM}$	ESD Protection (Machine model)		200			V
$ESD_{HBM}$	ESD Protection (Human body model)		2000			V
LU	Latch-up Immunity		200			mA
$C_{IN}$	Input capacitance	per input		4		pf

TABLE 2: ABSOLUTE MAXIMUM RATINGS

SYMBOL	CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNIT
$V_{DD}$	Supply Voltage		-0.3		3.9	V
$V_{IN}$	DC Input Voltage		-0.3		$V_{DD} + 0.3$	V
$V_{OUT}$	DC Output Voltage		-0.3		$V_{DD} + 0.3$	V
$I_{IN}$	DC Input Current				+/-20	mA
$I_{OUT}$	DC Output Current				+/-50	mA
$T_S$	Storage Temperature		-65		125	C

TABLE 3: DC CHARACTERISTICS ( $V_{DD} = 3.3V \pm 5\%$ )

SYMBOL	CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNIT
$V_{DD\_PLL}$	PLL Supply Voltage		3.0		$V_{DD}$	V
$V_{IH}$	Input High Voltage		2.0		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage				0.8	V
$V_{OH}$	Output High Voltage	$I_{OH} = -24mA$	2.4			V
$V_{OL}$	Output Low Voltage	$I_{OL} = 24mA$ $I_{OL} = 12mA$			0.55 0.30	V
$Z_{OUT}$	Output Impedance			14 -17		$\Omega$
$I_{PU}$	Input Current	$V_{IN} = GND$ or $V_{DD}$	-100		200	$\mu A$
$I_{DD\_PLL}$	PLL Supply Current	@ $V_{DD\_PLL}$ Pin		8	13.5	mA
$I_{DDQ}$	Quiescent Supply Current	All $V_{DD}$ pins			35	mA

TABLE 4: AC CHARACTERISTICS ( $V_{DD} = 3.3V \pm 5\%$ )

SYMBOL	CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNIT
$f_{REF}$	Input reference frequency <sup>a</sup>	÷4 feedback	50.0		120	MHz
		÷6 feedback	33.3		80.0	MHz
		÷8 feedback	25.0		60.0	MHz
		÷10 feedback	20.0		48.0	MHz
		÷12 feedback	16.6		40.0	MHz
		÷16 feedback	12.5		30.0	MHz
		÷20 feedback	10.0		24.0	MHz
		÷24 feedback	8.33		20.0	MHz
		÷32 feedback	6.25		15.0	MHz
		÷40 feedback	5.00		12.0	MHz
	PLL bypass mode			250	MHz	
$f_{VCO}$	VCO frequency range		200		480	MHz
$f_{XTAL}$	Crystal input frequency range		10		25	MHz
$f_{MAX}$	Output frequency <sup>a</sup>	÷2 output	100.0		240.0	MHz
		÷4 output	50.0		120.0	MHz
		÷6 output	33.3		80.0	MHz
		÷8 output	25.0		60.0	MHz
		÷10 output	20.0		48.0	MHz
		÷12 output	16.6		40.0	MHz
		÷16 output	12.5		30.0	MHz
		÷20 output	10.0		24.0	MHz
÷24 output	8.33		20.0	MHz		
$f_{STOP\_CLK}$	Serial interface max. frequency				20.0	MHz
$t_{PW}$	CLKx pulse min. width		2.0			ns
$t_{tR}, t_{tF}$	Input CLKx Rise/Fall time	0.8V to 2.0V			1.0	ns
$t_{(\phi)}$	Propagation Delay (static phase offset) CLKx to FB_IN <sup>b</sup>	$6.25MHz < f_{REF} < 65.0MHz$	-3		+3	°
		$65.0MHz < f_{REF} < 125MHz$	-4		+4	°
		$f_{REF} = 50MHz \& FB = \div 8$	-166		+166	ps
$t_{SK(O)}$	Output to output skew <sup>c</sup>	Bank A (QAx to QAy)			100	ps
		Bank B (QBx to QBy)			100	ps
		Bank C (QCx to QCy)			100	ps
		all outputs (QXy to QWz)			250	ps
DC	Output duty cycle <sup>d</sup>		(T÷2)-200	T÷2	(T÷2)+200	ps
$O_{tR}, O_{tF}$	Output Rise/Fall time	0.55V to 2.4V	0.1		1.0	ns

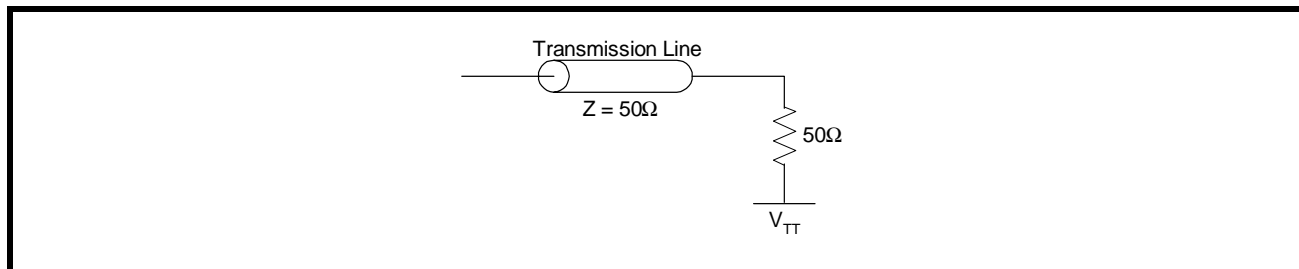
TABLE 5: AC CHARACTERISTICS (CON'T) ( $V_{DD} = 3.3V \pm 5\%$ )

SYMBOL	CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNIT
$t_{PLZ}, t_{PHZ}$	Output Disable Time				8	ns
$t_{PZL}, t_{PZH}$	Output Enable Time				8	ns
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	All outputs in same divider configuration		150	200	ps
$t_{JIT(PER)}$	Period Jitter	All outputs in same divider configuration			150	ps
$t_{JIT(I/O)RMS}$	I/O Jitter (RMS) VCO @ 400MHz	÷4 feedback ÷6 feedback ÷8 feedback ÷10 feedback ÷12 feedback ÷16 feedback ÷20 feedback ÷24 feedback ÷32 feedback ÷40 feedback			11 86 13 88 16 19 21 22 27 30	ps ps ps ps ps ps ps ps ps ps
BW	PLL closed loop bandwidth	÷4 feedback ÷6 feedback ÷8 feedback ÷10 feedback ÷12 feedback ÷16 feedback ÷20 feedback ÷24 feedback ÷32 feedback ÷40 feedback		1.20-3.5 0.70-2.50 0.50-1.80 0.45-1.20 0.30-1.00 0.25-0.70 0.20-0.55 0.17-0.40 0.12-0.30 0.11-0.28		MHz MHz MHz MHz MHz MHz MHz MHz MHz MHz
$t_{LOCK}$	Max PLL Lock Time				10	ns

**NOTES:**

- a. PLL locked, except when configured in bypass mode.
- b.  $t_{(\emptyset)}[s] = t_{(\emptyset)}[^\circ] \div (\text{fref} \times 360^\circ)$
- c. Not including Qsync output
- d. T is the output period.

FIGURE 3. TEST LOAD



**2.0 CONFIGURATION TABLES**

**TABLE 6: FUNCTION CONTROLS**

CONTROL PIN	Logic 0	Logic 1
MR/OE	Resets the output divide circuitry and serial interface, tri-states all outputs	Enables all outputs - normal operation
PLL_SEL	PLL bypass mode enabled. This is a test mode in which the reference clock is provided to the output dividers in place of the VCO.	PLL enabled - normal operation
REF_SEL	CLKx selected as ref source to PLL	Crystal Oscillator selected as ref source to PLL.
CLK_SEL	CLK0 selected	CLK1 selected
INV_CLK	QC2 & QC3 are in phase with QC1 & QC4	QC2 & QC3 are 180° out of phase with QC1 & QC4
VCO_SEL	VCO ÷ 2	no divide of VCO

**TABLE 7: BANK OUTPUT DIVIDER CONTROLS**

INPUT		OUTPUT	INPUT		OUTPUT	INPUT		OUTPUT
FSEL_A1	FSEL_A0	QA	FSEL_B1	FSEL_B0	QB	FSEL_C1	FSEL_C0	QC
0	0	÷4	0	0	÷4	0	0	÷2
0	1	÷6	0	1	÷6	0	1	÷4
1	0	÷8	1	0	÷8	1	0	÷6
1	1	÷12	1	1	÷10	1	1	÷8

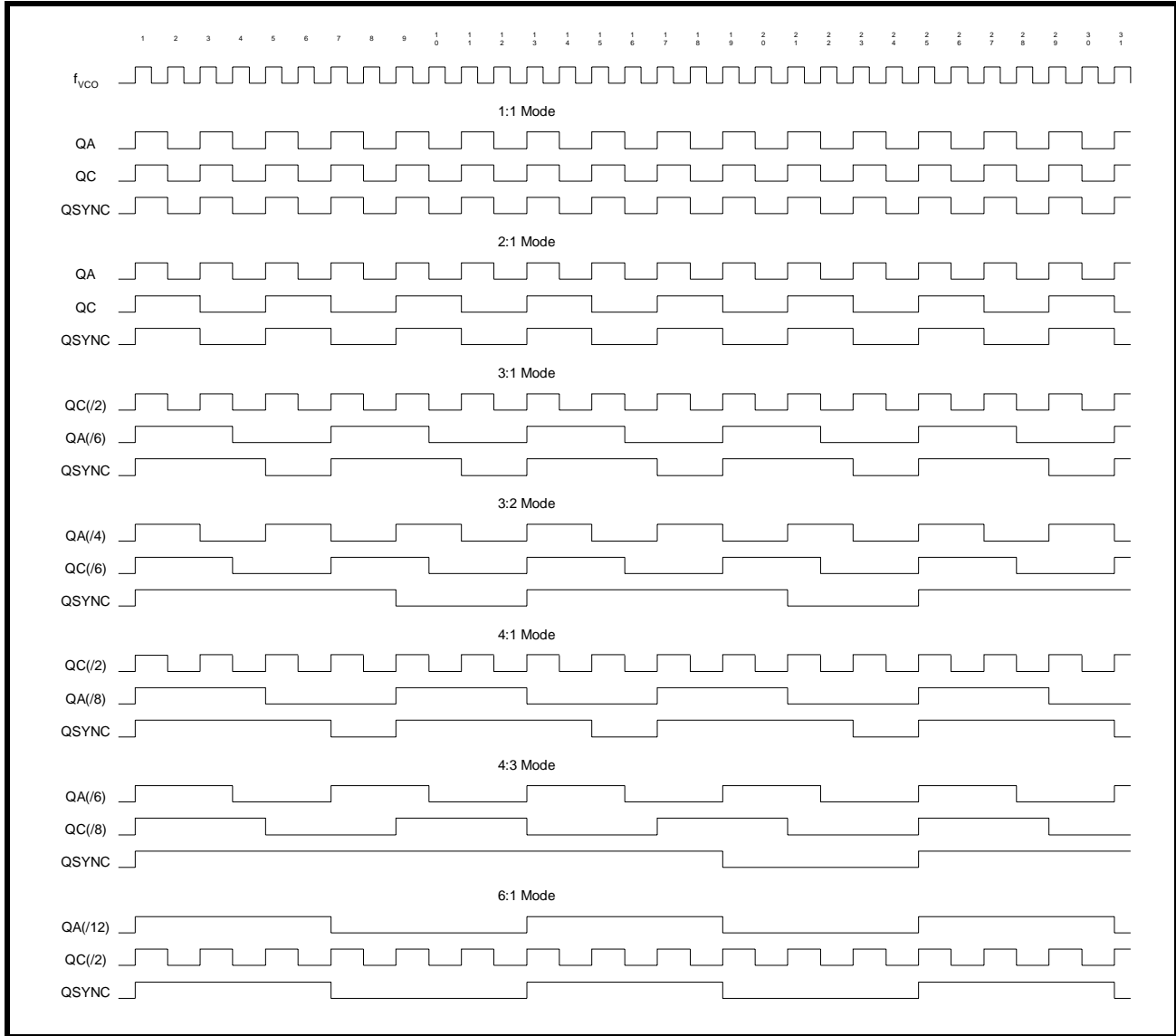
**TABLE 8: FEEDBACK DIVIDER CONTROL**

FSEL_FB2	FSEL_FB1	FSEL_FB0	QFB
0	0	0	÷4
0	0	1	÷6
0	1	0	÷8
0	1	1	÷10
1	0	0	÷8
1	0	1	÷12
1	1	0	÷16
1	1	1	÷20

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3.0 QSYNC TIMING

FIGURE 4. QSYNC TIMING DIAGRAM



XRK69772 INDIVIDUAL OUTPUT DISABLE (STOP CLOCK ) CIRCUITRY

The user can write to the serial input register through the STOP\_DATA input by supplying a logic '0' start bit followed serially by 12 NRZ disable/enable bits. The period of each STOP\_DATA bit equals the period of the free-running STOP\_CLK signal. The STOP\_DATA serial transmission should be timed so the XRK69772 can sample each STOP\_DATA bit with the rising edge of the free-running STOP\_CLK signal. A logic "0" to any stop bit location will disable the corresponding device output while a logic "1" will enable. All outputs are by default, enabled.

FIGURE 5. STOP CLOCK CIRCUIT PROGRAMMING

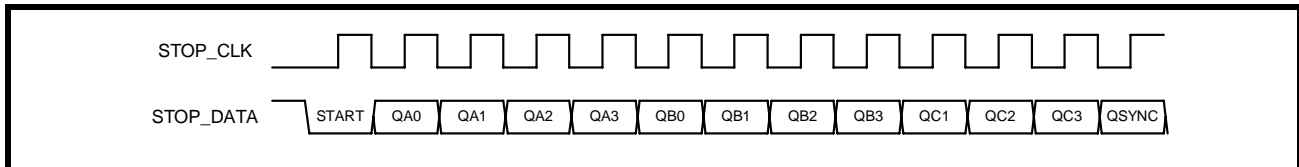




FIGURE 6. OUTPUT-TO-OUTPUT SKEW  $t_{SK(O)}$

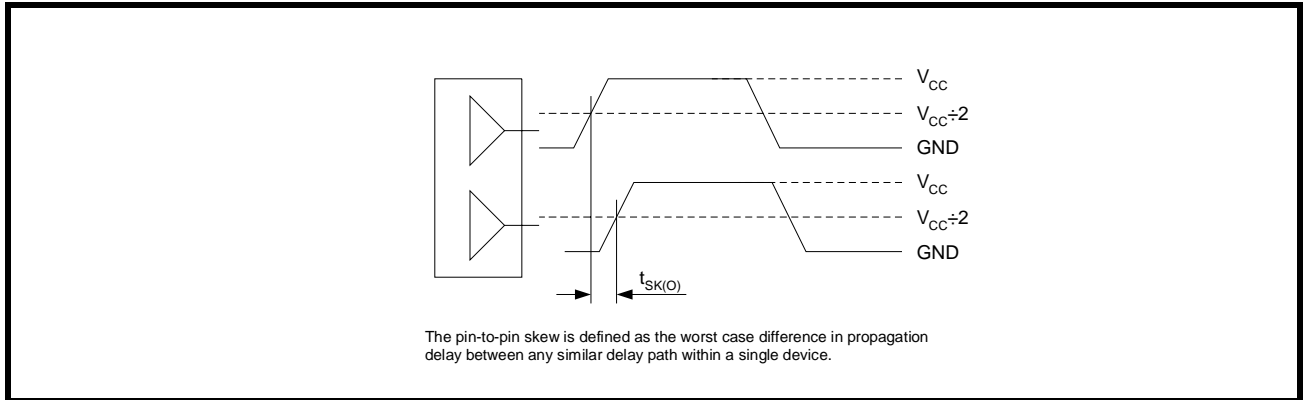


FIGURE 7. PROPOGATION DELAY ( $t_{\phi}$ ), STATIC PHASE OFFSET) TEST REFERENCE

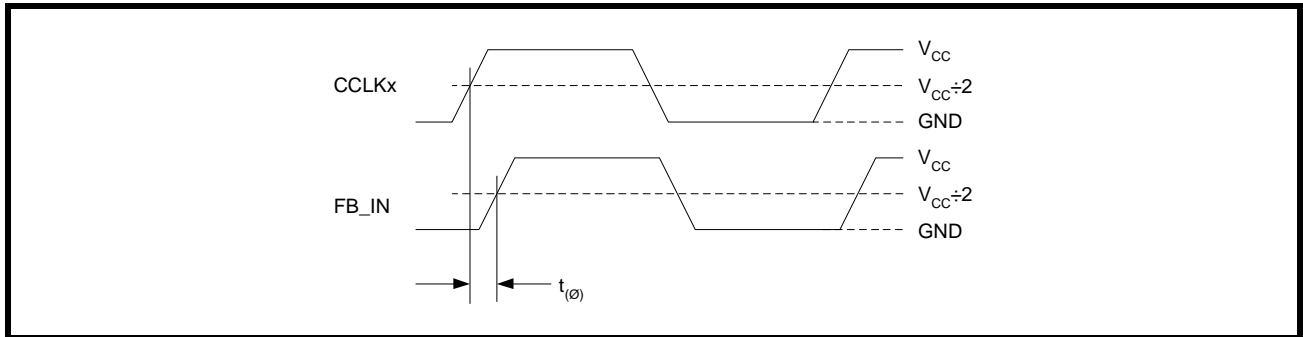


FIGURE 8. OUTPUT DUTY CYCLE (DC)

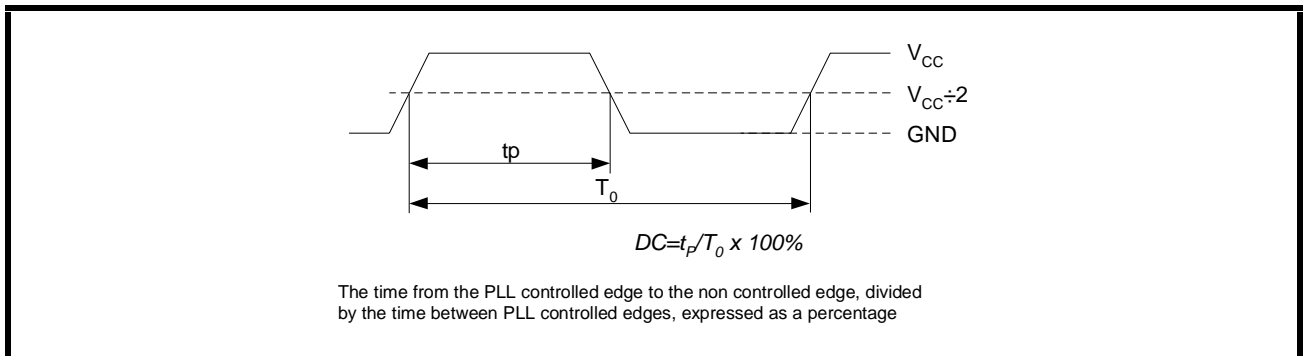
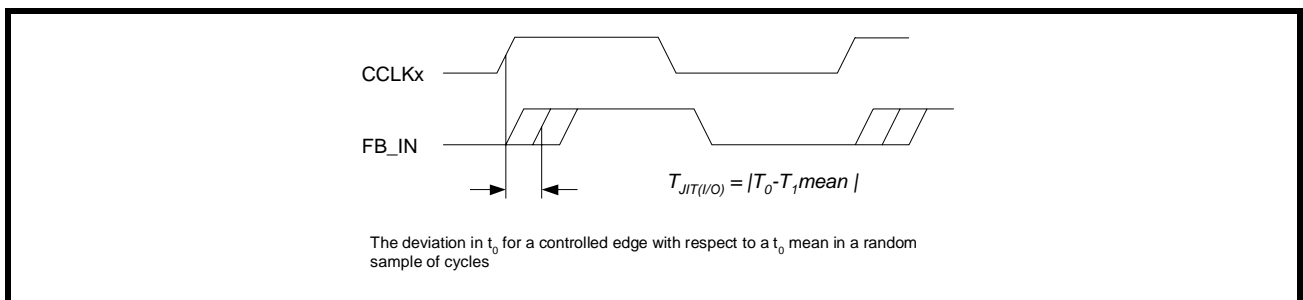


FIGURE 9. I/O JITTER



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FIGURE 10. CYCLE-TO-CYCLE JITTER

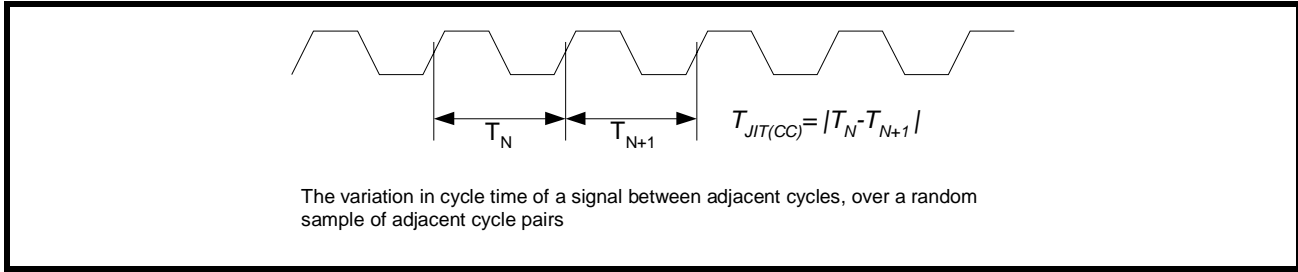


FIGURE 11. PERIOD JITTER

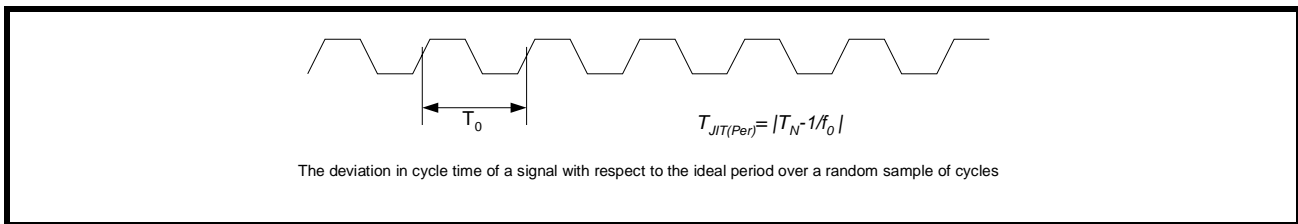
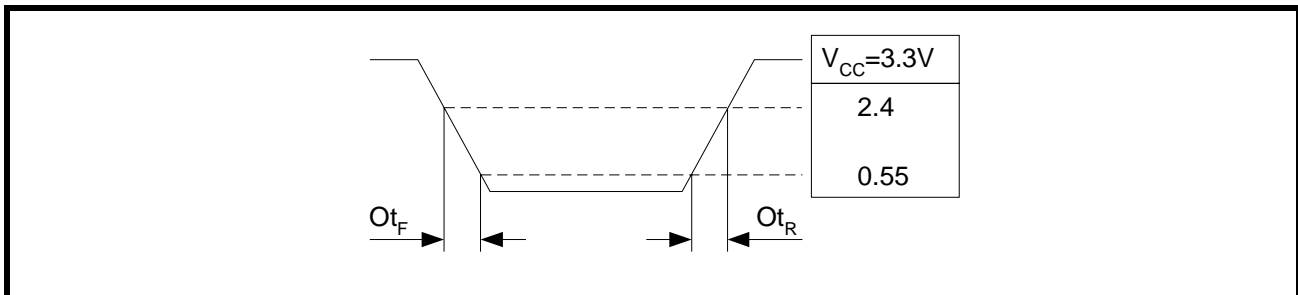


FIGURE 12. OUTPUT TRANSITION TIME TEST REFERENCE



**PACKAGE DIMENSIONS**

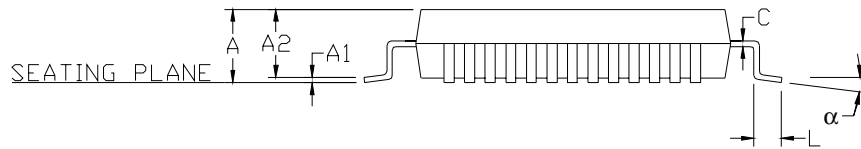
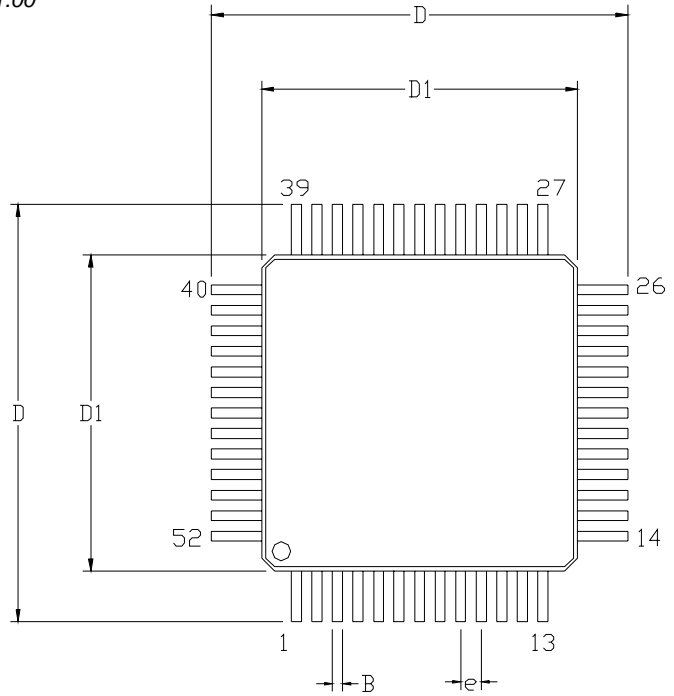


52 LEAD LOW-PROFILE QUAD FLAT PACK  
(10 mm x 10 mm X 1.4 mm LQFP, 1.0 mm Form)

Rev. 1.00

Note: The control dimension is in millimeters.

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.010	0.014	0.25	0.35
C	0.004	0.009	0.11	0.23
D	0.465	0.480	11.80	12.20
D1	0.390	0.398	9.90	10.10
e	0.0256 BSC		0.65 BSC	
L	0.029	0.041	0.73	1.03
$\alpha$	0°	7°	0°	7°



**REVISION HISTORY**

REVISION #	DATE	DESCRIPTION
P1.0.0	April 6, 2006	Initial release.

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