

MARCH 2005

REV. P1.0.1

**GENERAL DESCRIPTION**

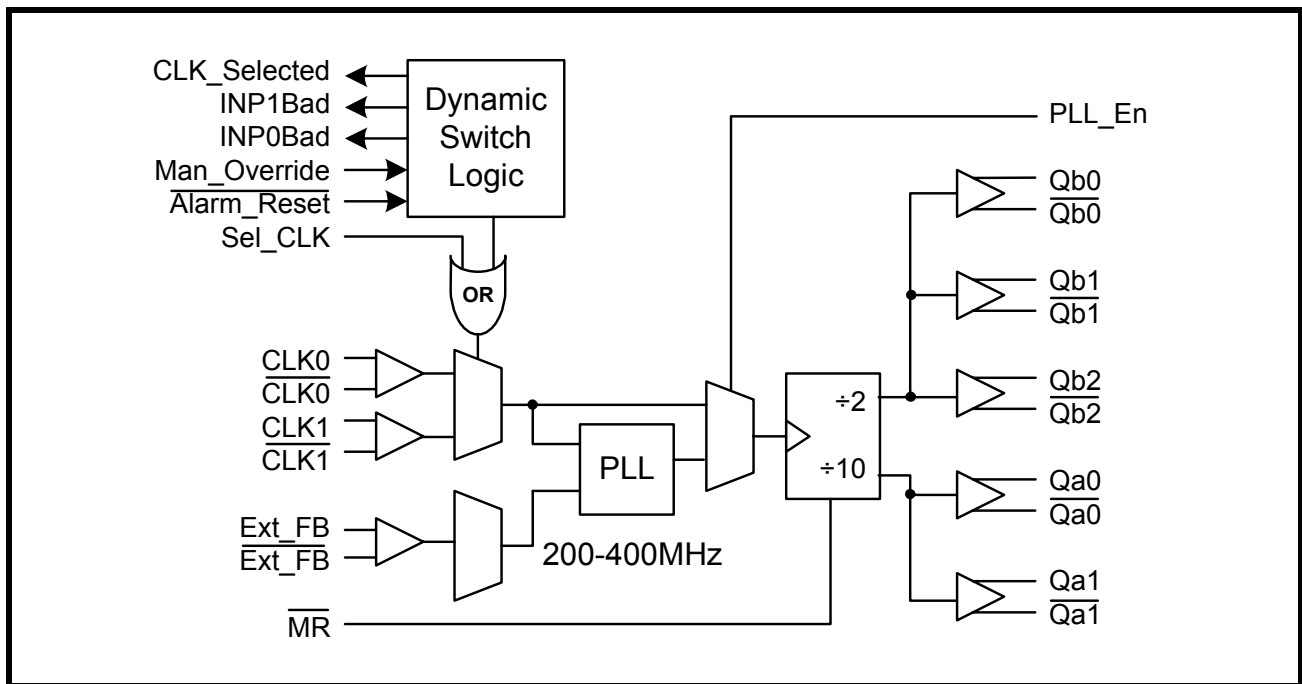
The XRK7955 is a PLL clock driver designed specifically for redundant clock tree designs. The device receives two differential LVPECL clock signals from which it generates 5 new differential LVPECL clock outputs. Two of the output pairs regenerate the input signals frequency and phase while the other three pairs generate 5x, phase aligned clock outputs. External PLL feedback is used to also provide zero delay buffer performance.

The XRK7955 Intelligent Dynamic Clock Switch circuit continuously monitors both input CLK signals. Upon detection of a failure (CLK stuck HIGH or LOW for at least 1 period), the INP\_BAD for that CLK will

be latched (H). If that CLK is the primary clock, the device will switch to the good secondary clock and phase/frequency alignment will occur with minimal output phase disturbance. The typical phase bump caused by a failed clock is eliminated.

**FEATURES**

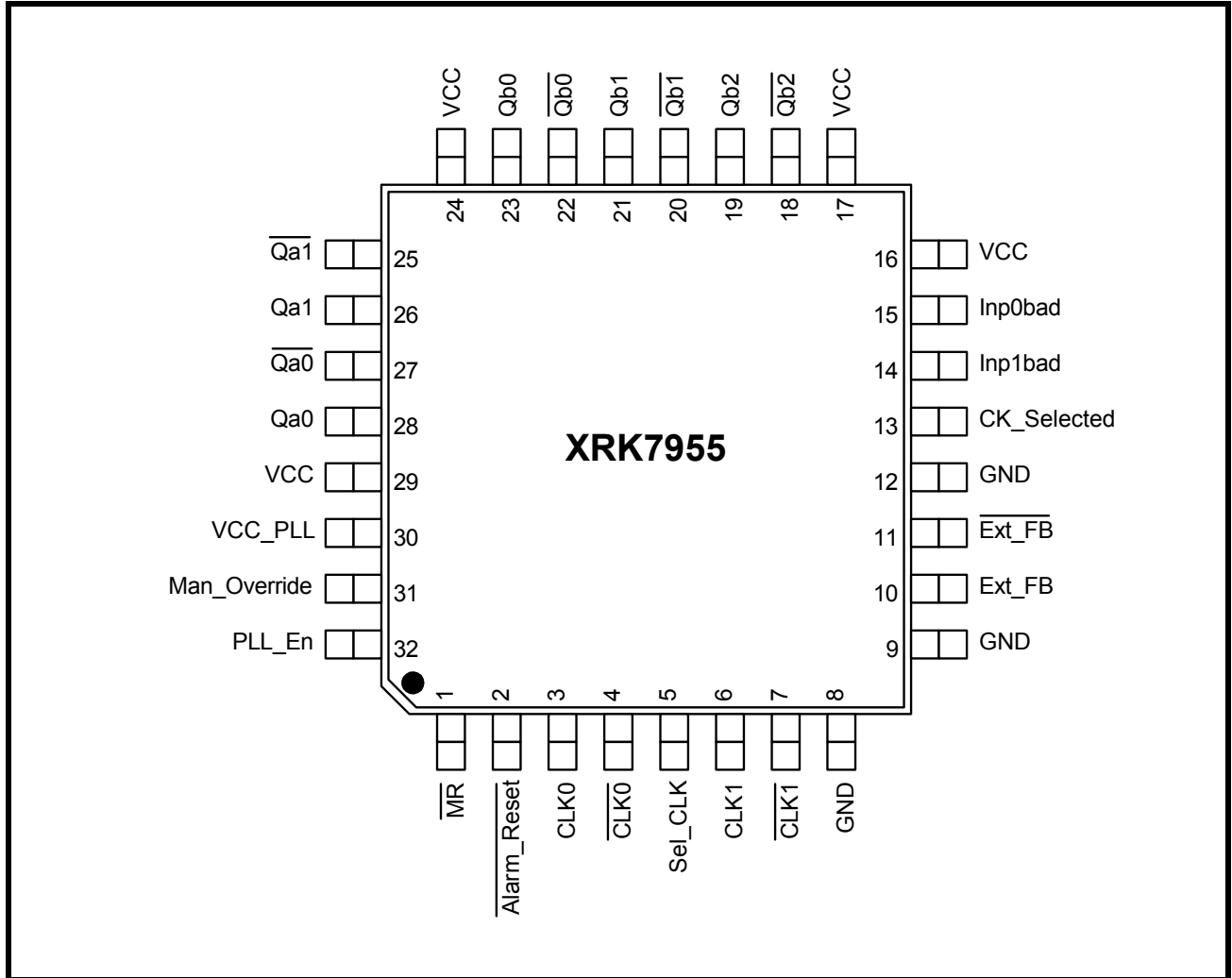
- Fully Integrated PLL
- Intelligent Dynamic Clock Switch
- LVPECL Clock Outputs
- LVCMOS Control I/O
- 3.3V Operation
- 32-Lead LQFP Packaging

**FIGURE 1. BLOCK DIAGRAM OF THE XRK7955**

**PRODUCT ORDERING INFORMATION**

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRK7955	32-Lead LQFP	-40°C to +85°C

**FIGURE 2. PIN OUT OF THE XRK7955**



**PIN DESCRIPTIONS**

PIN NAME	TYPE	DESCRIPTION
CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$	LVPECL Input LVPECL Input	Differential PLL clock reference (CLK0 pulldown, $\overline{\text{CLK0}}$ pullup) Differential PLL clock reference (CLK1 pulldown, $\overline{\text{CLK1}}$ pullup)
Ext_FB, $\overline{\text{Ext\_FB}}$	LVPECL Input	Differential PLL feedback clock (Ext_FB pulldown, $\overline{\text{Ext\_FB}}$ pullup)
Qa[1:0], $\overline{\text{Qa[1:0]}}$	LVPECL Output	Differential 1x output pairs
Qb[2:0], $\overline{\text{Qb[2:0]}}$	LVPECL Output	Differential 5x output pairs
Inp0bad	LVC MOS Output	Indicates detection of a bad input reference clock 0 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted.
Inp1bad	LVC MOS Output	Indicates detection of a bad input reference clock 1 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted.
Clk_Selected	LVC MOS Output	0 - if clock 0 is selected 1 - if clock 1 is selected
$\overline{\text{Alarm\_Reset}}$	LVC MOS Input	0 - will reset the input bad flags and align Clk_Selected with Sel_Clk. The input is one-shotted (50K $\Omega$ pullup).
Sel_Clk	LVC MOS Input	0 - selects CLK0 1 - selects CLK1 (40k $\Omega$ pulldown)
Manual_Override	LVC MOS Input	1 - disables internal clock switch circuitry (40K $\Omega$ pulldown).
PLL_En	LVC MOS Input	0 - bypasses selected input reference around the phase-locked loop (50K $\Omega$ pullup).
$\overline{\text{MR}}$	LVC MOS Input	0 - resets the internal dividers forcing Q outputs LOW. Asynchronous to the clock (50K $\Omega$ pullup).
VCCA	Power Supply	PLL power supply
VCC	Power Supply	Digital power supply
GND A	Power Supply	PLL Ground
GND	Power Supply	Digital Ground

**ABSOLUTE MAXIMUM RATINGS<sup>a</sup>**

SYMBOL	CHARACTERISTICS	MIN	MAX	UNIT	CONDITION
V <sub>CC</sub>	Supply Voltage	-0.3	3.6	V	
V <sub>IN</sub>	DC Input Voltage	-0.3	V <sub>CC</sub> +0.3	V	
V <sub>OUT</sub>	DC Output Voltage	-0.3	V <sub>CC</sub> +0.3	V	
I <sub>IN</sub>	DC Input Current		±20	mA	
I <sub>OUT</sub>	DC Output Current		±50	mA	
T <sub>S</sub>	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**GENERAL SPECIFICATIONS**

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNIT	CONDITION
V <sub>TT</sub>	Output termination voltage		V <sub>CC</sub> -2		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
LU	Latch-up immunity	200			mA	
C <sub>IN</sub>	Input Capacitance		4.0		pF	Inputs
θ <sub>JA</sub>	Thermal resistance junction to ambient JESD 51-3, single layer test board			62.0	°C/W	Natural convection
	JESD 51-6, 2S2P multilayer test board			47.0	°C/W	Natural convection
θ <sub>JC</sub>	Thermal resistance junction to case			14	°C/W	
	Operating junction temperature			115	°C	

DC CHARACTERISTICS ( $V_{CC} = 3.3 \pm 5\%$ ,  $T_A = -40^{\circ}\text{C}$  TO  $+85^{\circ}\text{C}$ )

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNIT	CONDITION
<b>LVCMOS control inputs (MR, PLL_En, Sel_CLK, Man_Override, Alarm_Reset)</b>						
$V_{IH}$	Input voltage high	2.0		$V_{CC}+0.3$	V	
$V_{IL}$	Input voltage low			0.8	V	
$I_{IN}$	Input current <sup>a</sup>	100		-150	$\mu\text{A}$	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$
<b>LVCMOS Control Outputs</b>						
$V_{OH}$	Output High Voltage	2.0			V	$I_{OH} = -10\text{mA}$
$V_{OL}$	Output Low Voltage			0.55	V	$I_{OL} = 10\text{mA}$
<b>LVPECL clock inputs (CLK, <math>\overline{\text{CLK}}</math>)<sup>b</sup></b>						
$I_{IN}$	Input current			$\pm 100$	$\mu\text{A}$	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$
<b>LVPECL clock outputs (Qa[1:0], <math>\overline{\text{Qa}}</math>[1:0], Qb[2:0], <math>\overline{\text{Qb}}</math>[2:0])</b>						
$V_{OH}$	Output high voltage	$V_{CC}-1.2$		$V_{CC}-0.7$	V	Termination $50\Omega$ to $V_{TT}$
$V_{OL}$	Output low voltage	$V_{CC}-1.9$		$V_{CC}-1.45$	V	Termination $50\Omega$ to $V_{TT}$
<b>Supply Current</b>						
$I_{GND}$	Maximum ground supply current - gnd pins			180	mA	GND pins
$I_{CCPLL}$	Maximum PLL power supply - VCC_PLL pin			15	mA	$V_{CCPLL}$ pin

- a. Inputs have internal pullup/pulldown resistors which affect the input current.
- b. Clock inputs driven by LVPECL compatible signals.

**AC CHARACTERISTICS ( $V_{CC} = 3.3 \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $+85^\circ\text{C}$ ) (NOTE 5) <sup>f</sup>**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
$f_{ref}$	Input Reference Frequency $\div 10$ feedback	20		40	MHz	Locked
$f_{VCO}$	PLL VCO Lock Range	200		400	MHz	Qa Output used for feedback
$f_{MAX}$	Output Frequency Qa[1:0] Qa[1:0]	20 100		40 200	MHz	
$f_{refDC}$	Reference Input Duty Cycle	25		75	%	
$t_{pd}$	Propagation Delay CLKn to Ext_FB (SPO) <sup>c</sup> CLKn to Q (Bypass)	-150		150 5	ps ns	PLL_EN = 1 PLL_EN = 0
$V_{PP}$	Differential input voltage (peak-to-peak)	0.25		1.3	V	
$V_{CMR}$	Differential input crosspoint voltage	$V_{CC}-1.7$		$V_{CC}-0.3$	V	
$t_{skew}$	Output Skew Within Qa[1:0] or Qb[2:0] All outputs			50 80	ps ps	
$\Delta_{per/cycle}$	Rate of change of periods Qa[1:0] <sup>d</sup> Qb[2:0] <sup>d</sup> Qa[1:0] <sup>e</sup> Qb[2:0] <sup>e</sup>			50 25 400 200	ps/cycle	
$t_{pw}$	Output duty cycle	45		55	%	
$t_{jitter}$	Cycle-to-cycle jitter, Standard deviation (RMS)			40	ps	@ $f_{ref} = 30\text{MHz}$
$t_{lock}$	Maximum PLL lock time			10	ms	
$t_r/t_f$	Output Rise/Fall time	50		700	ps	

- c. Static phase offset between the selected reference clock and the feedback signal.
- d. Specification holds for a clock switch between two signals no greater than 400ps out of phase. Delta period change per cycle is averaged over the clock switch excursion. (See Applications Information section for more detail)
- e. Specification holds for a clock switch between two signals no greater than  $\pm\pi$  out of phase. Delta period change per cycle is averaged over the clock switch excursion.
- f. PECL output termination is 50 ohms to  $V_{CC} - 2.0V$ .
- g.  $V_{PP}$  is the minimum differential input voltage swing required to maintain AC characteristic including SPO, device and part-to-part skew. Applicable to CLK0, CLK1 and Ext\_FB.
- h.  $V_{CMR}$  is the crosspoint of the differential input signal. Normal operation is obtained when the crosspoint is within the  $V_{CMR}$  range and the input swing lies within the  $V_{PP}$  specification. Violation of  $V_{CMR}$  or  $V_{PP}$  impacts the SPO, device and part-to-part skew. Applicable to CLK0, CLK1 and Ext\_FB.

## APPLICATIONS INFORMATION

The XRK7955 is a dual clock PLL with on-chip Intelligent Dynamic Clock Switch circuitry.

### DEFINITIONS

*primary clock*: The input CLK selected by Sel\_Clk.

*secondary clock*: The input CLK NOT selected by Sel\_Clk.

*PLL reference signal*: The CLK selected as the PLL reference signal by Sel\_Clk or the Intelligent Dynamic Clock Switch. The Intelligent Dynamic Clock Switch can override Sel\_Clk.

### STATUS FUNCTIONS

*Clk\_Selected*: Clk\_Selected (L) indicates CLK0 is selected as the PLL reference signal. Clk\_Selected (H) indicates CLK1 is selected as the PLL reference signal.

*Inp0bad, Inp1bad*: Inp0bad is latched (H) when CLK0 is stuck (H) or (L) for at least one Ext\_FB period, or if one of the inputs CLK0 or CLK0 is floating. Inp1bad is latched (H) when CLK1 is stuck (H) or (L) for at least one Ext\_FB period, or if one of the inputs CLK1 or CLK1 is floating. Both Inp0bad and Inp1bad are latched (H) when Ext\_FB is stuck (H) or (L) for at least one Qa period, or if one of the inputs Ext\_FB or Ext\_FB is floating. Both Inp0bad and Inp1bad are cleared (L) on assertion of Alarm\_Reset. The status functions Inp0bad and Inp1bad are active for Man\_Override (H) or (L).

### CONTROL FUNCTIONS

*Sel\_Clk*: Sel\_Clk (L) selects CLK0 as the primary clock. Sel\_Clk (H) selects CLK1 as the primary clock.

*Alarm\_Reset*: Asserted by a negative edge. Generates a one-shot reset pulse that clears INPUT\_BAD latches and Clk\_Selected latch.

*PLL\_En*: While (L), the PLL reference signal is substituted for the VCO output.

*MR*: While (L), internal dividers are held in reset which holds all Q outputs LOW.

### MAN OVERRIDE (H)

(IDCS is disabled, PLL functions normally). PLL reference signal (as indicated by Clk\_Selected) will always be the CLK selected by Sel\_Clk. If Ext\_FB misses at least one pulse, Qa and Qb outputs will drop to a minimum frequency (~20MHz) for 1- $\mu$ S, or until Ext\_FB shows any activity, whichever is longer. This prevents the Qa and Qb frequencies from rising due the PLL incorrectly interpreting an intermittent Ext\_FB as a VCO running too slow.

### MAN OVERRIDE (L)

Intelligent Dynamic Clock Switch is enabled. The first CLK to fail will latch it's INP\_BAD (H) status flag and select the other input as the Clk\_Selected for the PLL reference clock. Once latched, the Clk\_Selected and INP\_BAD remain latched until assertion of Alarm\_Reset which clears all latches (INP\_BADs are cleared and Clk\_Selected = Sel\_Clk).

If both Inp0bad and Inp1bad are (H), either due to both CLK0 and CLK1 having missed at least 1 pulse each or Ext\_FB having missed at least 1 pulse, then Qa and Qb outputs will drop to a minimum frequency (~20MHz) until such time as Alarm\_Reset\_b is asserted.

**NOTE:** *If both CLKs are bad when Alarm\_Reset is asserted, both INP\_BADs will be latched (H) after one Ext\_FB period and Clk\_Selected will be latched (L) indicating CLK0 is the PLL reference signal. While neither INP\_BAD is latched (H), the Clk\_Selected can be freely changed with Sel\_Clk. Whenever a CLK switch occurs, (manually or by the Intelligent Dynamic Clock Switch), following the next negative edge of the newly selected PLL reference signal, the next positive edge pair of Ext\_FB and the newly selected PLL reference signal will slew to alignment.*

To calculate the overall uncertainty between the input CLKs and the outputs from multiple XRK7955's, the following procedure should be used. Assuming that the input CLKs to all XRK7955's are exactly in phase, the total uncertainty will be the sum of the static phase offset, max I/O jitter, and output to output skew.

During a dynamic switch, the output phase between two devices may be increased for a short period of time. If the two input CLKs are 400ps out of phase, a dynamic switch of an XRK7955 will result in an instantaneous phase change of 400ps to the PLL reference signal without a corresponding change in the output phase (due to the limited response of the PLL). As a result, the I/O phase of a device, undergoing this switch, will initially

be 400ps and diminish as the PLL slews to its new phase alignment. This transient timing issue should be considered when analyzing the overall skew budget of a system.

**HOT INSERTION AND WITHDRAWAL**

In PECL applications, a powered up driver will experience a low impedance path through an XRK7955 input to its powered down VCC pins. In this case, a 100 ohm series resistance should be used in front of the input pins to limit the driver current. The resistor will have minimal impact on the rise and fall times of the input signals.

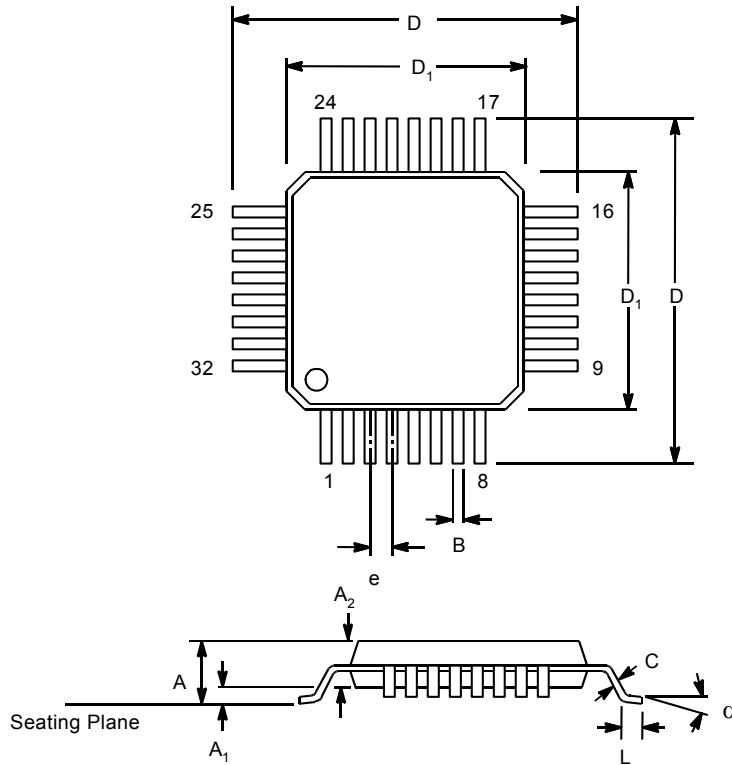
**ACQUIRING FREQUENCY LOCK**

1. While the XRK7955 is receiving a valid CLK signal, assert Man\_Override HIGH.
2. The PLL will phase and frequency lock within the specified lock time.
3. Apply a HIGH to LOW transition to Alarm\_Reset to reset Input Bad flags.
4. De-assert Man\_Override LOW to enable Intelligent Dynamic Clock Switch mode.



PACKAGE DIMENSIONS

32 LEAD THIN QUAD FLAT PACK  
 (7 x 7 x 1.4 mm TQFP)  
 rev. 2.00



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A <sub>1</sub>	0.002	0.006	0.05	0.15
A <sub>2</sub>	0.053	0.057	1.35	1.45
B	0.012	0.018	0.30	0.45
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D <sub>1</sub>	0.272	0.280	6.90	7.10
e	0.0315 BSC		0.80 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

**REVISION HISTORY**

REVISION #	DATE	DESCRIPTION
A1.0.0	August 2004	Initial release.
P1.0.0	January 2005	Revised Electrical characteristics, Application Section, changed to Preliminary.
P1.0.1	March 2005	Minor style edits.

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