GENERAL DESCRIPTION

The XRP2997 is a Double Data Rate (DDR) termination voltage regulator supporting all power requirements of DDR I, II, III and IV memories and is capable of sinking or sourcing 2A continuously.

Tightly regulating its output voltage within ±20mV, the XRP2997 converts input voltages as low as 1.1V while the output voltage is adjustable through an external resistor divider or by forcing the V_{REF} pin voltage. It maintains a fast line and load transient response and only requires an output capacitance of 22µF to operate. An enable function via an external MOSFET and a soft start feature allow for a controlled implementation of power-up sequencing.

Built-in source/sink overcurrent, over-temperature and under-voltage lockout protections insure safe operation under abnormal operating conditions.

The XRP2997 meets JEDEC SSTL-2, SSTL-18, HSTL, SCSI-1 and SCSI-3 specifications for DDR SDRAM memories.

The XRP2997 is offered in a RoHS compliant, "green"/halogen free 8-pin Exposed Pad SOIC package.

APPLICATIONS

- **DDR I / II / III / IV Memory Termination**
- **Active Termination Buses**
- **Audio-Video Equipments**
- **Video-Graphics Cards**

FEATURES

- **DDR1, DDR2, DDR3 and DDR4 Support**
  - $0.75V_{TT}$ Generation
  - ±20mV Output Voltage Offset
- **2 Amps Continuous Current Sourcing & Sinking**
  - 1.1V to 5.5V Wide Input Voltage Range
- **Adjustable Output Voltage**
- **Suspend to RAM(STR), Enable & Soft Start Functions**
- **Stable with 22µF Ceramic Capacitor**
- **UVLO, Over Temperature and Over Current Protections**
- **Minimal External Components**
- **Pin / Function Compatible with SP2996B**
- **RoHS Compliant "Green" / Halogen Free 8-Pin SOIC Package**

TYPICAL APPLICATION DIAGRAM

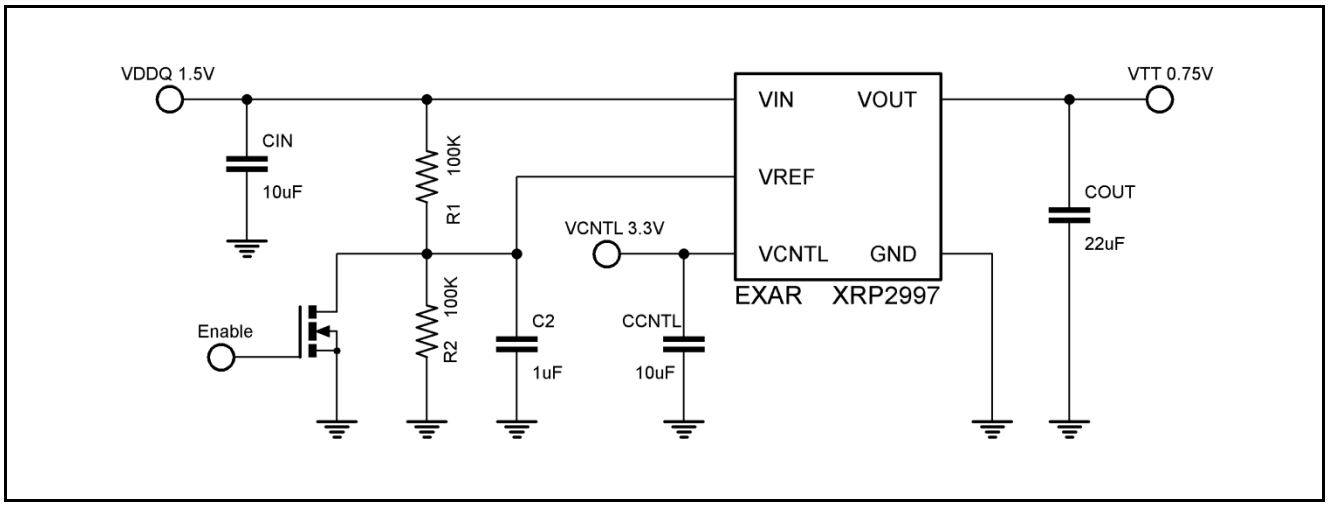


Fig. 1: XRP2997 DDRIII V_{TT} Application Diagram

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{IN}, V_{REF}, V_{CNTL} ..... -0.3V to 6.0V
Junction Temperature Range..... -40°C to +150°C
Storage Temperature..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING RATINGS

Operating Temperature Range..... -40°C to +85°C
Thermal Resistance θ_{JA} ..... 60°C/W
Thermal Resistance θ_{JC} ..... 16°C/W

ELECTRICAL SPECIFICATIONS

Specifications are for an Operating Ambient Temperature of T_A = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN} = 1.8V/1.5V, V_{CNTL} = 3.3V, V_{REF} = 0.5xV_{IN}, C_{OUT} = 22µF (ceramic), T_A= 25°C.

Parameter	Min.	Typ.	Max.	Units		Conditions
V_{IN}, Input Voltage Range	1.1	1.8/1.5	5.5	V		Keep $V_{CNTL} \geq V_{IN}$ during power on and power off sequences (note 4)
V_{CNTL}, Input Voltage Range	2.375	3.3	5.5	V		Keep $V_{CNTL} \geq V_{IN}$ during power on and power off sequences (note 4)
V_{OUT}, Output Voltage		V_{REF}		V		I_{OUT} = 0mA
V_{OS}, Output Voltage Offset	-20		+20	mV		I_{OUT} = 0mA (note 1)
ΔV_{LOR}, Load Regulation	-20		+20	mV		I_{OUT} = 0.1mA to +2A
	-20		+20	mV		I_{OUT} = 0.1mA to -2A
I_Q, Quiescent Current		2	90	µA		V_{REF} < 0.2V, V_{OUT} = OFF
I_{CNTL}, Operating Current of V_{CNTL}		1	2.5	mA		I_{OUT} = 0mA
I_{REF}, Bias Current of V_{REF}	0		1	µA		V_{REF} = 1.25V
I_{IL}, Current Limit	2.4	3		A		Source: V_{OUT}=0.33xV_{REF} Sink: V_{OUT}=0.95xV_{IN} (note 3)
R_{DSCHG}, Output Discharge Resistance		18	25	Ω		V_{REF}=0V, V_{OUT}=0.3V
Thermal Protection						
T_{SD}, Thermal Shutdown Temperature		160		°C		3.3V ≤ V_{CNTL} ≤ 5V, guaranteed by design (note 4)
Thermal Shutdown Hysteresis		30		°C		Guaranteed by design
Shutdown Specifications						
$V_{TRIGGER}$, Shutdown Threshold	0.6			V		Output ON V_{REF} = 0V → 1.25V
			0.2			Output OFF V_{REF} = 1.25V → 0V

Note 1: V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REF}.
Note 2: Load regulation is measured at constant junction temperature, using pulse testing with a short ON time.
Note 3: Current limit is measured by applying a short duration current pulse.
Note 4: In order to safely operate yo2ur system, V_{CNTL} must be > V_{IN}.

BLOCK DIAGRAM

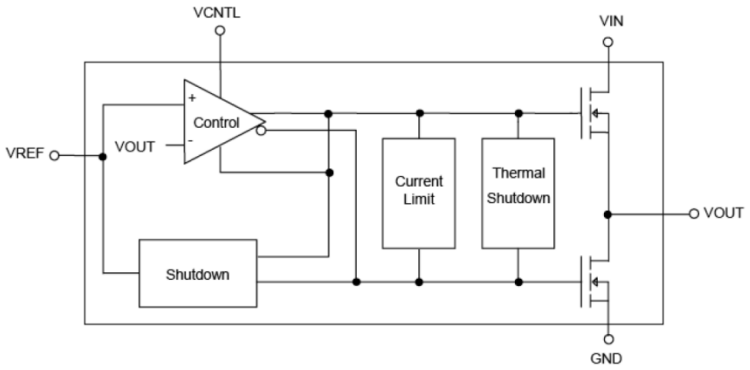


Fig. 2: XRP2997 Block Diagram

PIN ASSIGNMENT

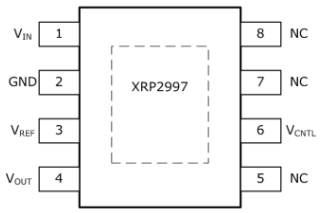


Fig. 3: XRP2997 Pin Assignment

PIN DESCRIPTION

Name	Pin Number	Description
V_{IN}	1	Power Input Voltage
GND	2 Exposed Pad	Ground Signal
V_{REF}	3	Reference Input Voltage. This input can also be used as an enable signal; pulling this pin low shuts down the XRP2997. Refer to typical application circuit.
V_{OUT}	4	Output Voltage
NC	5, 7, 8	NC
V_{CNTL}	6	Voltage for the driver circuit and all analog blocks

ORDERING INFORMATION(1)

Part Number	Operating Temperature Range	Lead-Free	Package	Packing Method
XRP2997IDBTR-F	-40°C≤T_A≤+85°C	Yes (2)	Exposed pad HSOIC-8 Option 1	Tape & Reel

NOTE:

1. Refer to www.exar.com/XRP2997 for most up-to-date Ordering Information
2. Visit www.exar.com for additional information on Environmental Rating.

TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at V_{IN} = 1.8V/1.5V, V_{CNTL} = 3.3V, V_{REF} = 0.5xV_{IN}, C_{OUT} = 22µF (ceramic), T_A= 25°C, unless otherwise specified - Schematic and BOM from Application Information section of this datasheet.

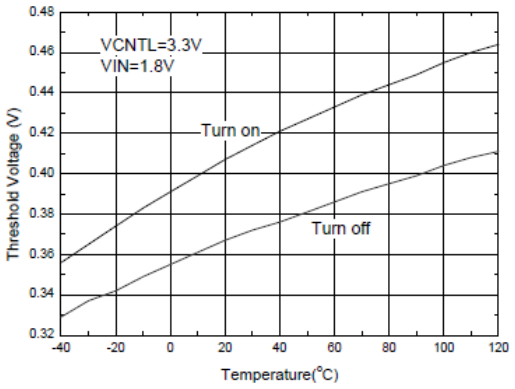


Fig. 4: Turn on and turn off vs. Temperature

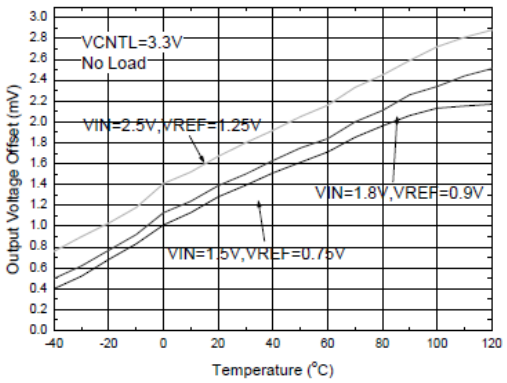


Fig. 5: Output Voltage vs. Temperature

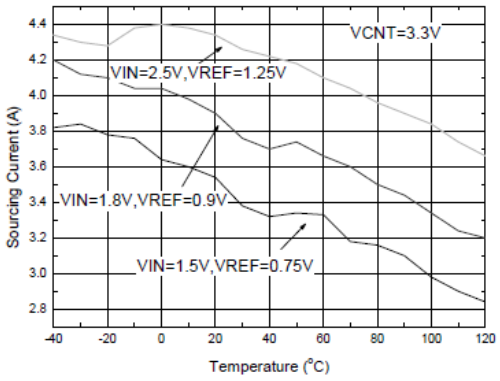


Fig. 6: Current limit (sourcing) vs. Temperature

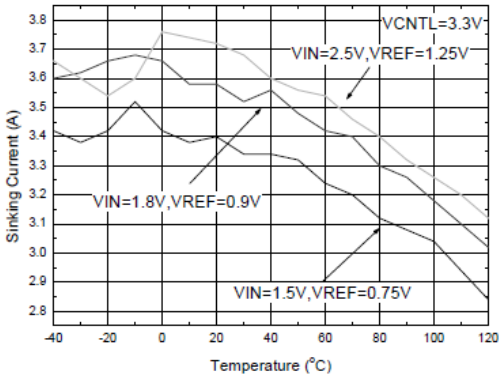


Fig. 7: Current limit (sinking) vs. Temperature

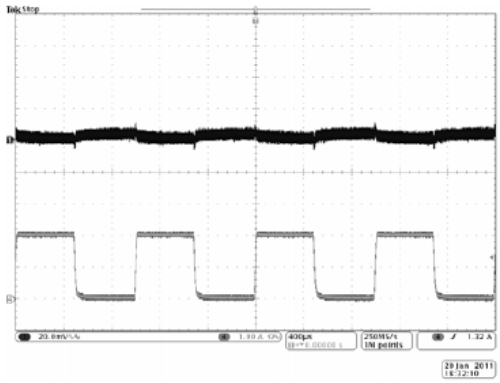


Fig. 8: V_{IN}=1.5V, V_{REF}=0.75V source response

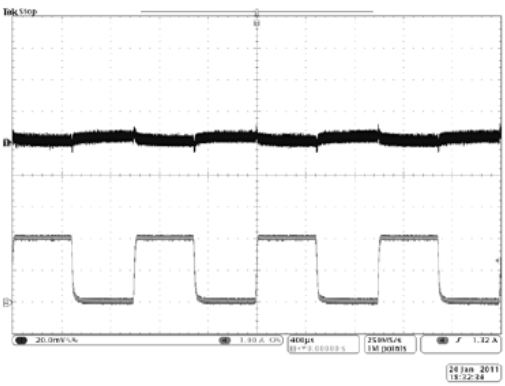


Fig. 9: V_{IN}=1.8V, V_{REF}=0.9V source response

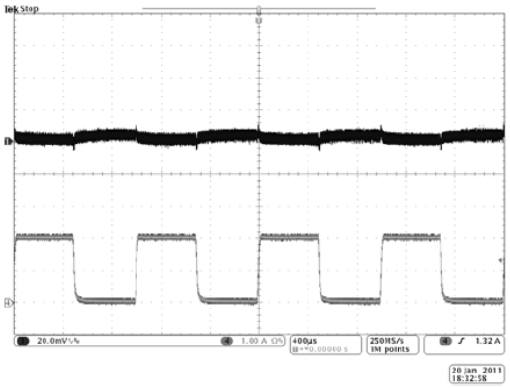


Fig. 10: V_{IN}=2.5V, V_{REF}=1.25V source response

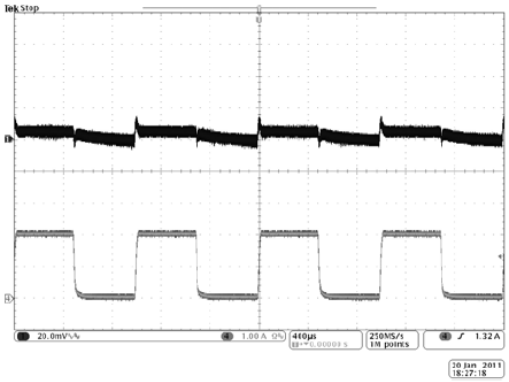


Fig. 11: V_{IN}=1.5V, V_{REF}=0.75V sink response

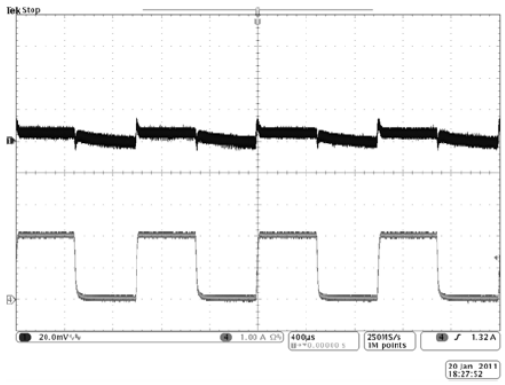


Fig. 9: V_{IN}=1.8V, V_{REF}=0.9V sink response

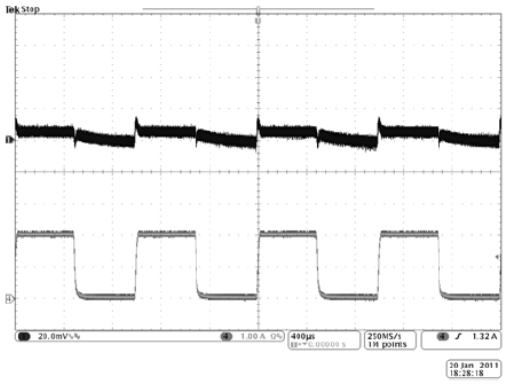


Fig. 10: V_{IN}=2.5V, V_{REF}=1.25V sink response

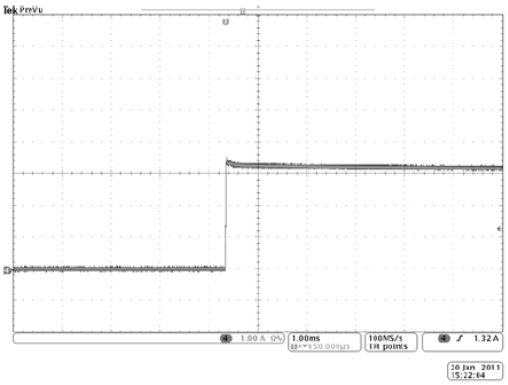


Fig. 14: V_{IN}=1.5V, V_{REF}=0.75V source short circuit

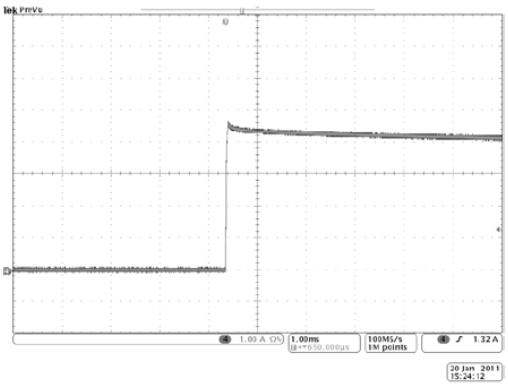


Fig. 15: V_{IN}=1.8V, V_{REF}=0.9V source short circuit

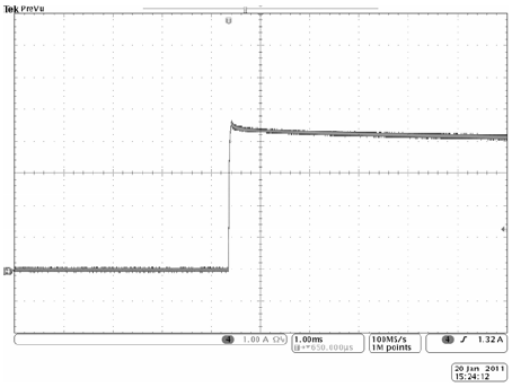


Fig. 11: V_{IN}=2.5V, V_{REF}=1.25V source short circuit

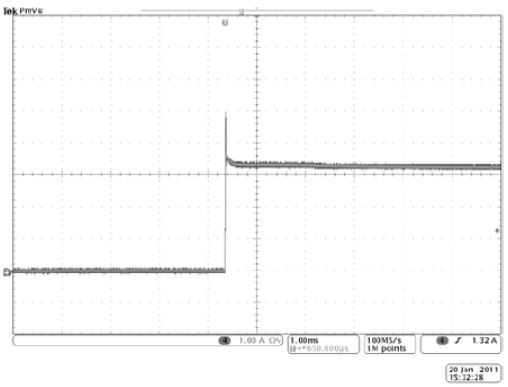


Fig. 12: V_{IN}=1.5V, V_{REF}=0.75V sink short circuit

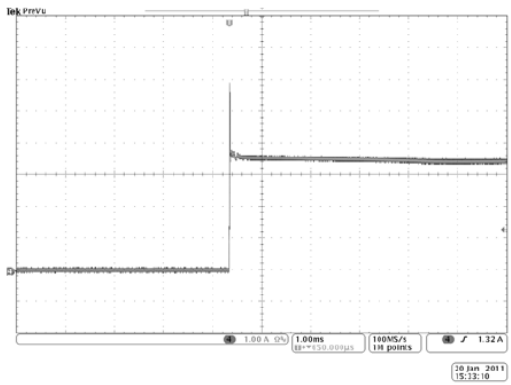


Fig. 13: V_{IN}=1.8V, V_{REF}=0.9V sink short circuit

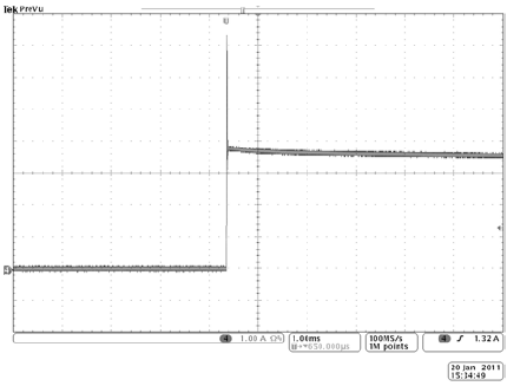


Fig. 14: V_{IN}=2.5V, V_{REF}=1.25V sink short circuit

APPLICATION INFORMATION

INPUT CAPACITOR CIN

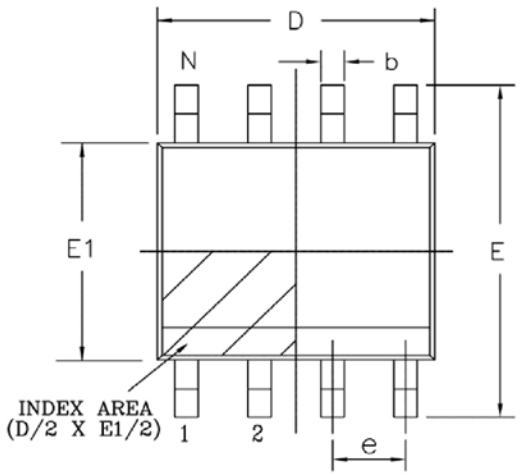
Select the input capacitor CIN for voltage rating, RMS current rating and capacitance. The voltage rating should be at least 50% higher than the regulator's maximum input voltage. The value of this capacitor, its charge, should be selected in order to be able to supply enough current to the XRP2997 in the event of a transient increase of source current required. A minimum value of 10µF is advised while a recommended value of 47µF is recommended for optimum transient response performance.

LAYOUT CONSIDERATIONS

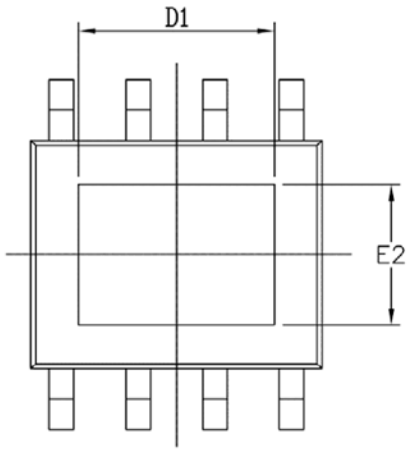
The XRP2997 is offered in the 8-pin exposed-pad SOIC package in order to facilitate power dissipation (heat dissipation). Power dissipation can be maximized by soldering the exposed pad to a large land area on top layer of PCB and by using vias to connect the exposed pad to an interlayer(s) or bottom layer. All capacitors should be placed as close as possible to the respective pins.

PACKAGE SPECIFICATION

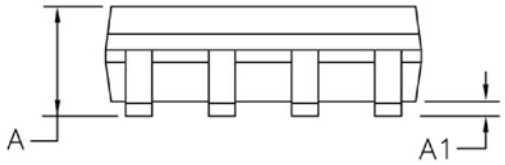
8-PIN HSOIC (EXPOSED PAD) OPTION 1



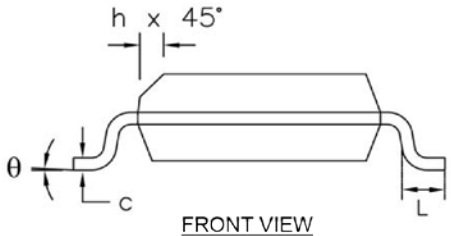
TOP VIEW



BOTTOM VIEW



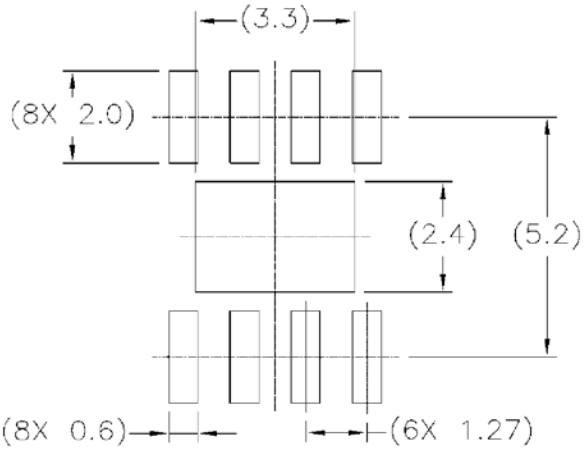
SIDE VIEW



FRONT VIEW

8 Pin HSOICN JEDEC MS-012 Variation BA			
SYMBOLS	DIMENSIONS IN MM		
	MIN	NOM	MAX
A	1.35		1.75
A1	0.00		0.15
b	0.31		0.51
c	0.17		0.25
D	4.80		5.00
D1	1.50		3.50
E	5.80		6.20
E1	3.80		4.00
E2	1.00		2.55
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0°		8°
N	8		

TERMINAL DETAILS



LAND PATTERN RECOMMENDED

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREE

Drawing No. : POD - 00000125
Revision: A

REVISION HISTORY

Revision	Date	Description
1.0.0	07/22/2011	Initial release of datasheet
1.1.0	01/09/2012	Corrected part number in ordering information
1.1.1	03/29/2012	Corrected turn on threshold from 0.8V to 0.6V. Typographical error.
1.2.0	10/29/2012	Reformat of datasheet Updated typical application schematics (figure 1) Addition of CIN selection under Application Information section
1.2.1	8/17/2017	Added DDR IV. Updated to MaxLinear logo. Updated format, ordering information and package drawing.

FOR FURTHER ASSISTANCE

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