1.0 INTRODUCTION

The EXAR XRS10L140 is a Serial ATA port multiplier designed for next generation enterprise class disk array systems that use SATA mid-planes. The device is targeted at low cost storage applications.

This function is used when one active host has to communicate with multiple SATA drives. The XRS10L140 supports up to 4 SATA drives and utilizes the full bandwidth of the host connection.

The upstream ports of XRS10L140 can also be attached to a port selector (XRS10L20) or a Serial ATA Switch to provide redundancy in a more complex topology.

The XRS10L140 includes enhanced features such as staggered HDD spin-up, power management control, hot plug capability and support for legacy software. The XRS10L140 acts as a retimer, maintaining independent signaling domains between the drives themselves and the external interconnect.

The high-speed serial input features selectable equalization adjustment and the high-speed serial output features selectable pre-emphasis to compensate for ISI (Inter-Symbol Interference) and increase maximum cable distances.

XRS10L140 meets tight jitter budgets in SATA applications. Exar's serial I/O technology enables reliable data transmission over 1 meter or more of FR-4 and 15 meters or more of unequalized copper cable.

Host and drive port speeds can be mixed and matched, based upon inherent data rate negotiation present in the SATA II specifications.

The MDIO bus allows simple configuration of the device.

To summarize, the XRT10L24 port multiplier device allows the system designer to increase the number of serial ATA connections in an enclosure that does not have a sufficient number of serial ATA connections for all of the drives in the enclosure.

OVERVIEW OF PORT MULTIPLIER LOGIC

XRS10L140 port multiplier is a multiplexer where one active host connection is multiplexed to multiple device connections. The XRS10L140 is an extensible design that can support up to 4 device connections and utilizes the full bandwidth of the host connection. XRS10L140 uses four bits, known as the PM Port field in all Serial ATA frame types, to route frames between the selected host and the appropriate device. PM ports 0 through 3 are valid device ports within the 4-output XRS10L140, while PM port 15 is designated for communication between the host and the XRS10L140 itself. For host-to-device transactions, the PM Port field is designated by the host in order to specify which device the frame is intended for. For device-to-host transactions, the XRS10L140 fills in the PM Port field with the port address of the device that is transmitting the frame.

STANDARDS COMPLIANCE

The XRS10L140 is compliant with the following industry specifications:

- Serial ATA, Revision 1.0a
- Serial ATA II: Extensions to Serial ATA 1.0a, Revision 1.2
- Serial ATA II PHY Electrical Specifications, Revision 1.0
- Serial ATA II: Port Multiplier, Revision 1.2

APPLICATIONS

- Serial ATA Enclosures
- Other Serial ATA link replicator applications
- Buffers for externally connected links
- High density storage boxes
- RAID Subsystems

FEATURES

GENERAL FEATURES

- Five independent 3/1.5G SATA ports.
- Supports 3/1.5G rate detection/speed negotiation.
- Supports power down modes - Active, partial, slumber and power down.

PORT MULTIPLIER LOGIC FEATURES

- Low latency architecture.
- Supports OOB signaling for SATA applications. Internal OOB detectors for COMSAS, COMRESET/ COMINIT and COMWAKE.

TEST AND CONTROL FEATURES

- Supports MDIO Bus.
- Outputs for various failure modes.
- Built-In self test mode through the MDIO bus.
- Supports various loopback modes.

HIGH SPEED I/O FEATURES

- High speed outputs with selectable pre-emphasis to extend the link budgets.
- High speed input equalization for improved signal integrity.
- Compliant with SATA Gen2i & Gen2 specification.
- Enables reliable data transmission over 1 meter or more of FR-4 and 15 meters or more of unequalized copper cable.
- Supports spread spectrum clocking to reduce EMI.

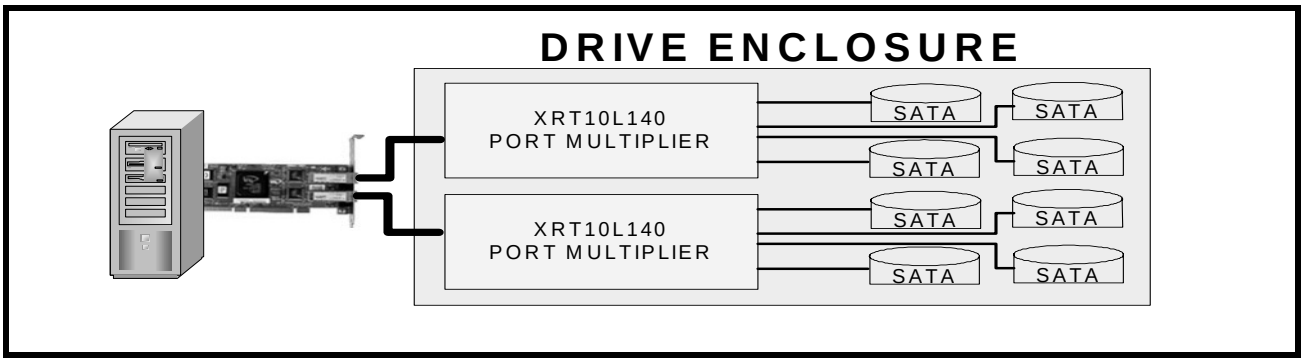
PHYSICAL FEATURES

- CMOS 0.13 Micron Technology
- Single 1.2 V Power Supply
- -40°C to 85°C Industrial Temperature Range
- 2000 V ESD Rating on All Pins
- No heatsink or airflow required
- 100-Pin QFP Package

APPLICATION EXAMPLE

The XRS10L140 is ideally suited for use within an external drive enclosure as a means of providing access to up to four target devices per XRS10L140. This application is shown in **Figure 1**. Other applications for the XRS10L140 include use in fixed-content or network attached storage systems, storage arrays, desktop applications or entry-level servers, RAID storage or disk-to-disk backup.

FIGURE 1. SYSTEM BLOCK DIAGRAM FOR XRS10L140 IN A DRIVE ENCLOSURE APPLICATION



2.0 PIN DESCRIPTIONS

TABLE 1: XRS10L140 PIN DESCRIPTIONS

Pin Name	Pin Number	I/O	DESCRIPTION
DATA INTERFACE			
SOTP0/SOTN0	68, 69	O	Serial ATA Output Transmitters. These ports communicate from the XRS10L140 to downstream devices
SOTP1/SOTN1	57, 56		
SOTP2/SOTN2	8, 7		
SOTP3/SOTN3	19, 20		
SORP0/SORN0	65, 66	I	Serial ATA Input Receivers. These ports receive signals from downstream devices
SORP1/SORN1	60, 59		
SORP2/SORN2	11, 10		
SORP3/SORN3	16, 17		
SITP/SITN	93, 94	O	Serial ATA Output Transmitter. This port communicates from the XRS10L140 to upstream hosts.
SIRP/SIRN	90, 91	I	Serial ATA Input Receiver. This port receives signals from upstream hosts.
CLOCK INTERFACE			
CMU_REFP/ CMU_REFN	46, 47	I	Reference clock input
XOD	43	I	Crystal oscillator input
XOG	44	I	Crystal oscillator input
MDIO INTERFACE SIGNALS			
MDC	3	I	MDIO clock input
MDIO	5	I/O	MDIO data port. Open drain
JTAG INTERFACE SIGNALS			
TCK	96	I	JTAG test clock
TDI	100	I	JTAG test data in
TDO	99	O	JTAG test data out. Open drain
TMS	97	I	JTAG mode select
TRST	1	I	JTAG test reset
GENERAL CONTROL AND CONFIGURATION SIGNALS (CMOS)			
RBIAS	49	I	Connection point for calibration termination resistor.
RESETB	75	I	Active low reset pin.
PWRDNB	52	I	Active low power down signal for chip.
DRACT[3:0]	71, 72, 73, 74	O	Drive activity port for external LED. 1.2V CMOS open drain

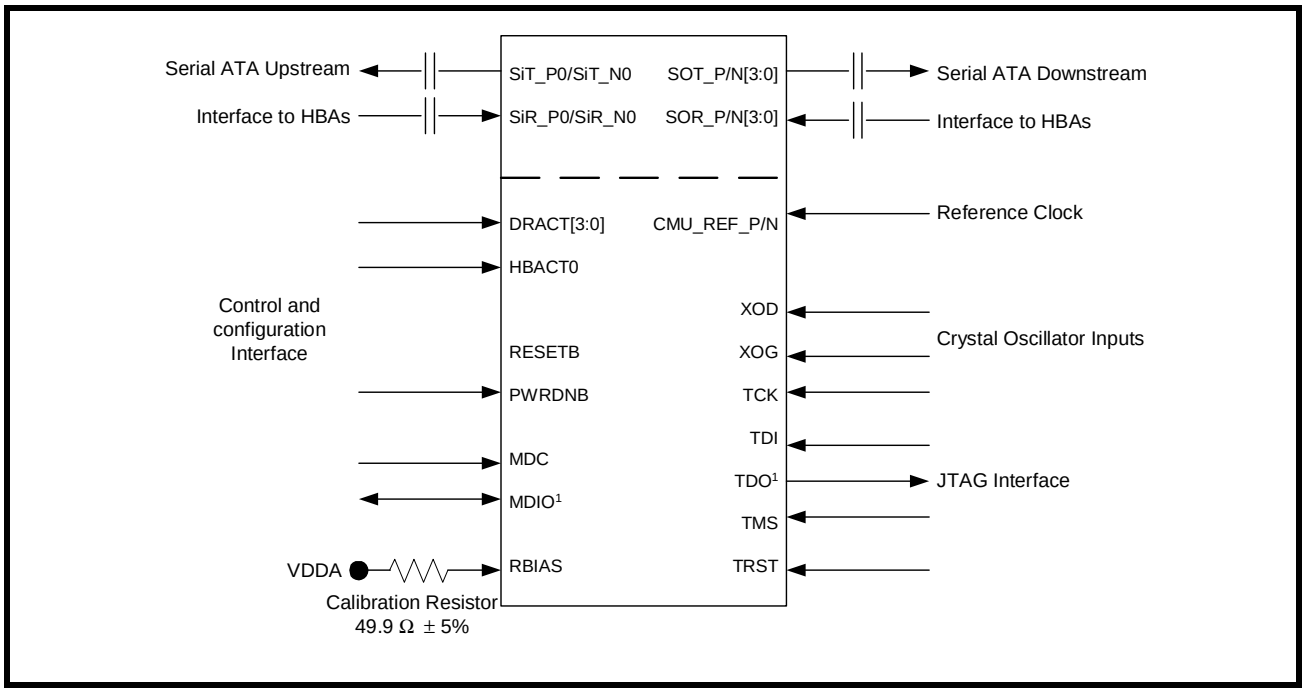
TABLE 1: XRS10L140 PIN DESCRIPTIONS

Pin Name	Pin Number	I/O	DESCRIPTION
HBACT	76	O	Host bus adaptor activity port for external LED. 1.2V CMOS open drain
TEST PIN			
ANTEST	51	O	Analog test pin
PORTSEL	2	I	Ground
CLKSTN/ CLKSTP	24, 25	O	Output clock test pin
RESERVED PINS			
PRP0/PRN0	31, 30	I	Short with a 100 ohms resistor
PRP1/PRN1	36, 37	I	Short with a 100 ohms resistor
PTP0/PTN0	28, 27	O	No Connect
PTP1/PTN1	39, 40	O	No Connect
Reserved	77, 81, 82, 84, 85, 2	-	No Connect
POWER AND GROUND SIGNALS			
VDD	9, 18, 23, 29, 38, 54, 58, 67, 79, 83, 92, 98	I	1.2V supply.
VDDA	14, 34, 45, 50, 62, 87	I	1.2V Analog supply.
VSS	4, 6, 12, 15, 21, 22, 26, 32, 35, 41, 53, 55, 61, 64, 70, 78, 80, 86, 89, 95	I	Ground.
VSSA	13, 33, 42, 48, 63, 88	I	Analog Ground.

3.0 FUNCTIONAL DESCRIPTION

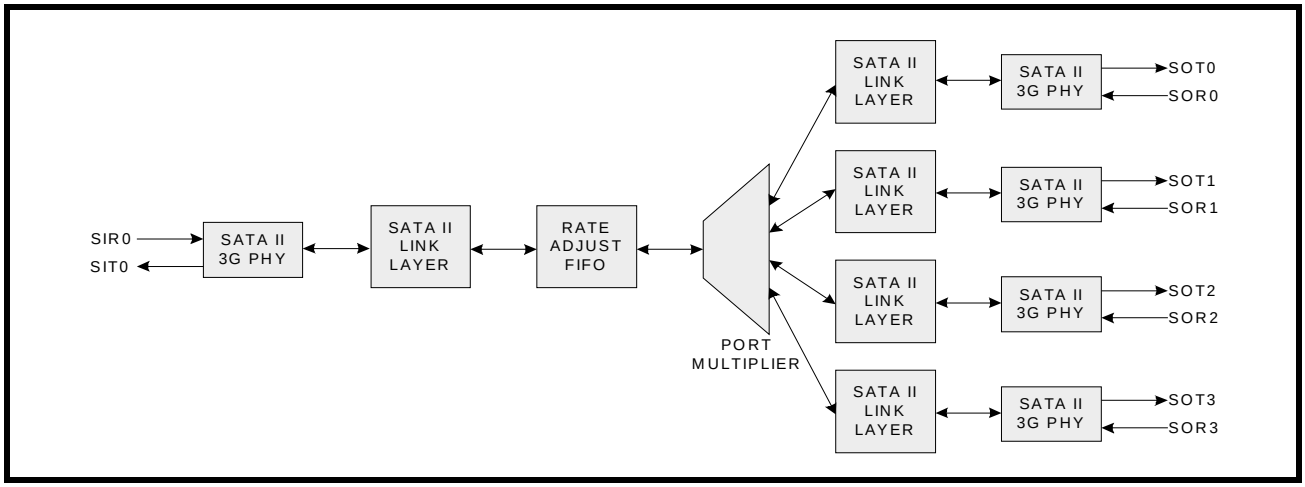
A top-level view of the XRS10L140 is shown in **Figure 2** outlining the interfaces to the device and the required support components. The data path can be seen at the top of the device. This includes the output transmit and input receive path at the top left, providing the upstream interface to the host, and the four output transmit and input receive paths at the top right, providing the downstream interface to the target devices. The clocking, control, and configuration interfaces are shown below the dotted line.

FIGURE 2. XRS10L140 INTERFACES



The XRS10L140 incorporates identical instantiations of a dual-channel Serial ATA II 3 Gbps PHY macro. This common building block provides a uniform implementation with common characteristics and a common register map, but provides a functional implementation of independent PHY blocks. Digital logic implementations of Serial ATA link layer blocks along with port multiplier logic provide the remainder of the data path within the XRS10L140. In addition, management and control interfaces including an MDIO interface for register control, a JTAG interface for boundary scan purposes, and a resistor calibration circuit complete the device. A block diagram of the XRS10L140 is shown in **Figure 3**.

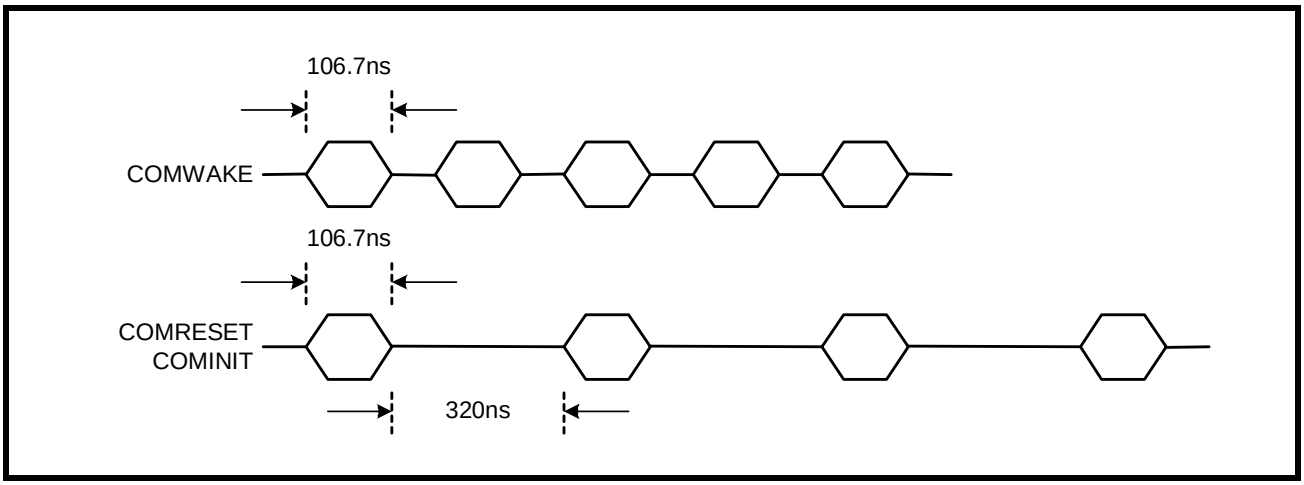
FIGURE 3. XRS10L140 BLOCK DIAGRAM



3.1 Out of Band Feature

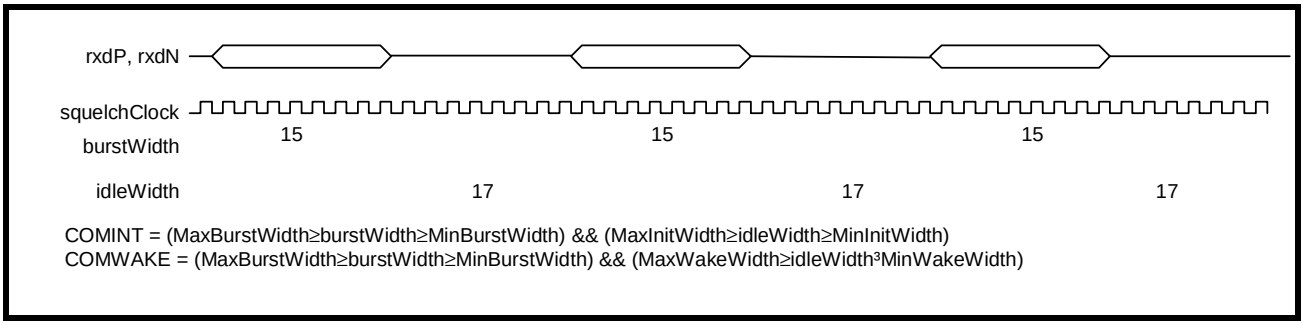
Each Serial ATA link provides full support for the three Out Of Band (OOB) signals supported by Serial ATA: COMRESET, COMINIT and COMWAKE. These sequences must be separated by idle periods as shown in **Figure 4**. The sequences are comprised of 106.7ns bursts of activity that are interleaved with varying length stretches of electrical idle. This alternating sequence must be repeated four times to be recognized.

FIGURE 4. COMWAKE AND COMRESET/COMINIT SEQUENCES



An example OOB sequence and the resulting burst and idle widths are shown in **Figure 5**. If the sequence of burstWidth and idleWidth counts falls within the range specified in the MDIO registers for four consecutive burst/idle sequences, then the link will assert COMINIT or COMWAKE. This OOB signal will remain asserted for as long as the corresponding sequence on the input pins continues.

FIGURE 5. EXAMPLE OOB SEQUENCE



3.2 Power Down Modes

Each Serial ATA link within the XRS10L140 features independent full support for the 3 defined Serial ATA power modes, as follows:

- Active: All parts of the link are active. All power-down signals are de-asserted.
- Partial: In partial mode, the input and output pipelines are shut down, but the PLL and the OOB generation circuits are active.
- Slumber: In slumber mode, the PLL is also shut down, saving additional power but adding latency on exit.

The XRS10L140 also provides full support for power management commands from connected hosts and devices, as outlined by the Serial ATA II port multiplier specifications.

If the PhyRdy signal is not present between the active host and the XRS10L140, the XRS10L140 will power down the PHY connected to that host and squelch the four device transmitters. OOB signals will still be propagated between the host and the XRS10L140.

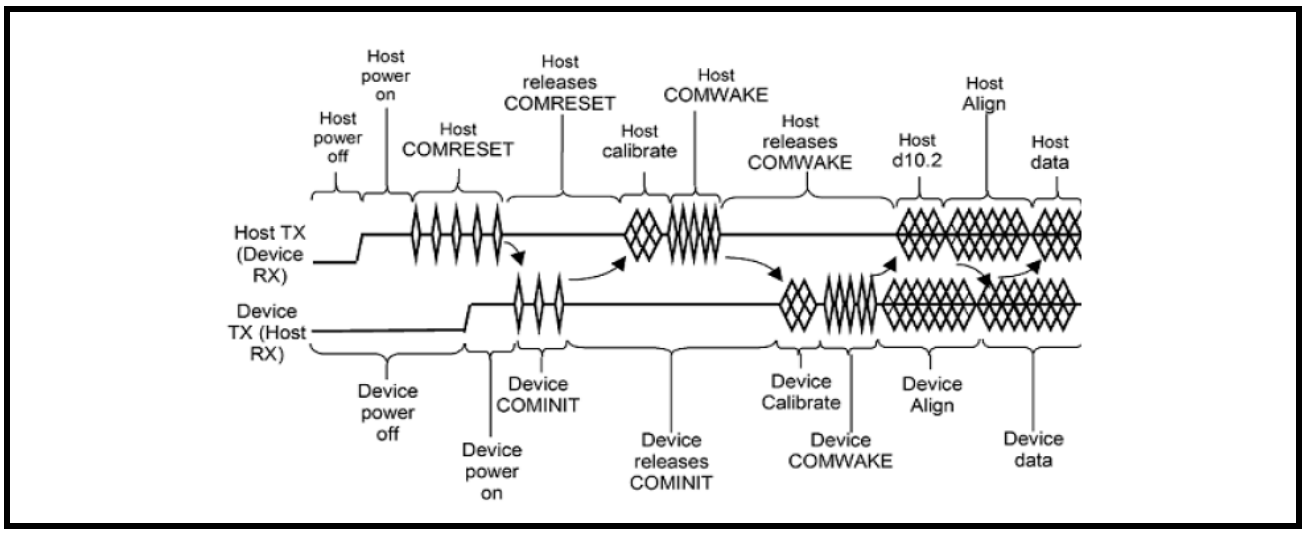
Power management requests from a host port, as specified by a PMREQ primitive, will propagate to all active device ports. In such a condition, the XRS10L140 will respond with a PMACK or PMNAK primitive, appropriately modify the power setting of the link with the host, and then propagate the request to each device that has PhyRdy set. The link within the XRS10L140 to each device that responds with a valid PMACK signal will be appropriately modified to reflect the new power setting.

Power management requests from a device port, as specified by a PMREQ primitive, will only affect the link between that device and the XRS10L140. In such a condition, the XRS10L140 will respond with a PMACK or PMNAK primitive, and modify the link to reflect the requested power state.

3.3 Speed Negotiation

The XRS10L140 will automatically perform speed negotiation with the host and devices in order to verify whether the second generation Serial ATA 3.0 Gbps data rate is available or whether the system will need to fall back upon the first generation Serial ATA 1.5 Gbps data rate. Speed negotiation is performed on an independent basis by each of the dual-channel macros. To perform speed negotiation with a downstream device, the XRS10L140 will first perform a COMRESET/COMINIT handshake with the device and then performs a calibrate/COMWAKE handshake. Following receipt of the device COMWAKE signal, the XRS10L140 will continually send out a D10.2 signal while awaiting receipt of the device ALIGN primitive. Depending on the speed of the ALIGN primitive, the XRS10L140 will be able to determine the PHY generation of the device, and provide the appropriate 1.5 Gbps or 3.0 Gbps ALIGN primitive in return to the device, thus completing speed negotiation. This process is outlined in **Figure 6**.

FIGURE 6. SERIAL ATA SPEED NEGOTIATION



For speed negotiation with an upstream host, after the COMRESET/COMINIT and COMWAKE handshake is complete, the XRS10L140 will initially send out an ALIGN primitive at the 2nd generation 3.0 Gbps data rate. If no confirming 3.0 Gbps ALIGN primitive is received from the host, the XRS10L140 will then step down and attempt negotiation at the lower 1.5 Gbps data rate.

3.4 Port Multiplier Implementation

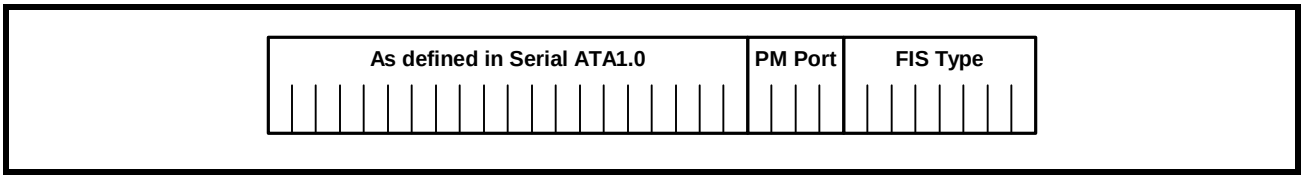
The XRS10L140 provides full support for the functionality outlined in the Serial ATA II Port Multiplier specification.

A Serial ATA II Port Multiplier is a mechanism for a host connection to communicate with multiple devices. A Port Multiplier is conceptually a simple multiplexer in which a host connection is multiplexed to multiple device connections.

The XRS10L140 uses four bits, known as the PM Port field in all Serial ATA frame types, to route frames between the host and the appropriate device. PM ports 0 through 3 are valid device ports within the 4-output XRS10L140, while PM port 15 is designated for communication between the host and the XRS10L140 itself. For host-to-device transactions, the PM Port field is designated by the host in order to specify which device the frame is intended for. For device-to-host transactions, the XRS10L140 fills in the PM Port field with the port address of the device that is transmitting the frame.

The PM Port field is defined in the Serial ATA port multiplier specification to be the first 32-bit Dword in the Frame Information Structure (FIS) for all FIS types, as shown in **Figure 7**.

FIGURE 7. PORT SELECTION SIGNAL - TRANSMITTED COMRESET SIGNALS



3.5 Transmission from a Host to a Device

A host indicates the target device for receipt of a transmitted frame by setting the PM Port field in the frame to the device's port address. When an XRS10L140 receives a frame as selected from the host, it checks the PM Port field in the frame to determine which port address should be used. If the frame is set for transmission to the control port (15), the XRS10L140 receives the frame and performs the command or operation requested. If the frame is designated for a device port, the XRS10L140 obeys the following procedure:

1. The XRS10L140 first determines if the device port is valid. If the device port is not valid, the XRS10L140 will issue a SYNC primitive to the host and terminate reception of the frame.
2. The XRS10L140 determines if the X bit is set in the device port's PSCR[1] (SError) register. If the X bit is set, the XRS10L140 issues a SYNC primitive to the host and terminates reception of the frame.
3. The XRS10L140 determines if a collision has occurred. A collision occurs when a reception is already in progress from the device that the host wants to transmit to. If a collision has occurred, the XRS10L140 will finish receiving the frame from the host and will then issue an R_ERR primitive to the host as the ending status. The XRS10L140 will then discard the frame, but will not return an R_RDY primitive to the host until the frame from the affected device port has been transmitted to the host, thus indicating to the host when it can retry to send the frame. The transmission from the device will proceed as requested, as the device will always take collision precedence over the host.
4. The XRS10L140 initiates a transfer with the device by issuing an X_RDY primitive to the device. A collision may occur as the XRS10L140 is issuing the X_RDY to the device if the device has started transmitting an X_RDY primitive to the XRS10L140, indicating a decision to start a transmission to the host. In this case, the XRS10L140 will finish receiving the frame from the host and then issue an R_ERR primitive to the host to indicate an unsuccessful transmission. The transmission from the device will proceed as requested, as the device will always take collision precedence over the host.
5. After the device issues an R_RDY primitive to the XRS10L140, the XRS10L140 will transmit the frame from the host to the device. The XRS10L140 will not send an R_OK status primitive to the host until the

device has issued an R_OK primitive to indicate successful frame reception. In this way, the R_OK status handshake is interlocked from the device to the host.

If an error is detected during any part of the frame transfer, the XRS10L140 will ensure that the error condition is propagated to the host and the device. If no error occurs during frame transfer, the XRS10L140 will not alter the contents of the frame, or modify the CRC in any way.

3.5.1 Transmission from a Device to a Host

A device indicates a transmit to a host in the same way as would be done if the host and device were attached directly. This transaction obeys the following procedure:

1. After receiving an X_RDY primitive from the device, the XRS10L140 will determine if the X bit is set in the device port's PSCR (SError) register. The XRS10L140 will not issue an R_RDY primitive to the device until this bit is cleared to zero.
2. The XRS10L140 will then receive the frame from the device. The XRS10L140 will fill in the PM Port field with the port address of the transmitting device. The XRS10L140 will then check the CRC received from the device, and if valid, it will recalculate the CRC based upon the new PM Port field. If the CRC calculated from the device is incorrect, the XRS10L140 will corrupt the CRC sent to the host to ensure propagation of the error condition
3. The XRS10L140 will issue an X_RDY primitive to the host to start the transmission of the frame to the host. After the host issues an R_RDY primitive to the XRS10L140, the frame from the device, with the updated CRC, will then be transmitted to the host. The XRS10L140 will not send an R_OK status primitive to the device until the host has issued an R_OK primitive to indicate successful frame reception. In this way, the R_OK status handshake will be interlocked from the device to the host.

If an error is detected during any part of the frame transfer, the XRS10L140 will ensure that the error condition is propagated to the host and the device.

3.6 Clocking

The XRS10L140 allows the use of either an external reference clock or of a low cost crystal oscillator to act as a reference clock. Separate device inputs are available for each approach, with full rate reference clock inputs provided on pins CMU_REFP and CMU_REFN, and crystal oscillator inputs provided on pins XOD and XOG. Supported data rates and their appropriate PLL divide factors are outlined in **Table 2**.

TABLE 2: PLL DIVIDE FACTORS

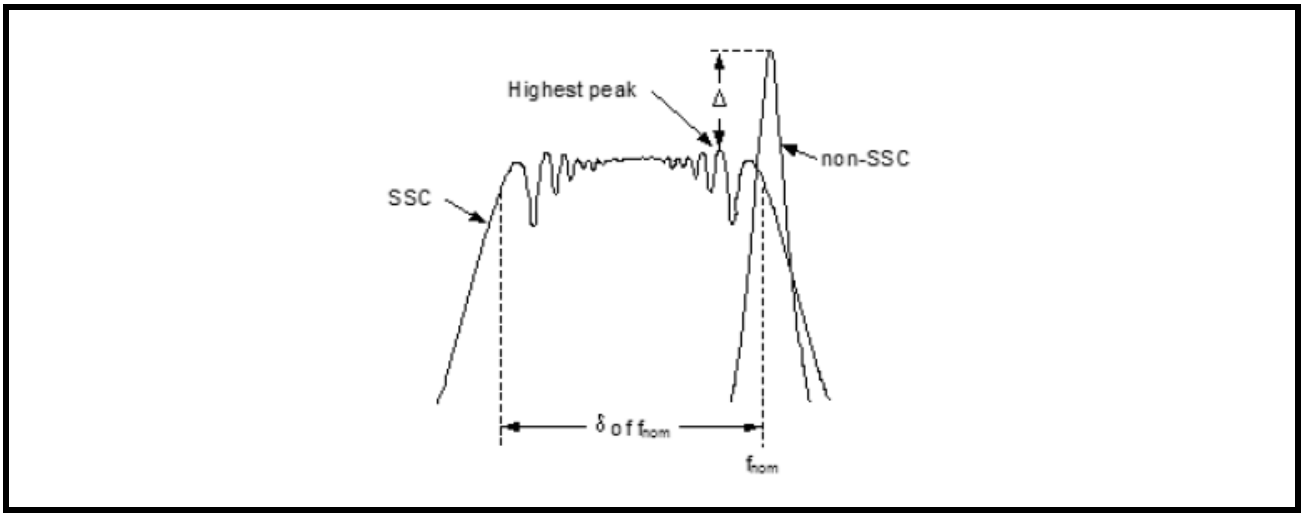
MODE	SYSCLK	/REF	/FB	DINCLK RXCLK	SERIAL CLOCK	DATA RATE
SATA Gen. 1	25MHz	1	30	150MHz	750MHz	1.5Gbps*
SATA Gen. 1	75MHz	1	10	150MHz	750MHz	1.5Gbps*
SATA Gen. 1	100MHz	2	15	150MHz	750MHz	1.5Gbps*
SATA Gen. 1	150MHz	1	5	150MHz	750MHz	1.5Gbps*
SATA Gen. 2	25MHz	1	60	300MHz	1.5GHz	3.0Gbps
SATA Gen. 2	75MHz	1	20	300MHz	1.5GHz	3.0Gbps
SATA Gen. 2	100MHz	2	30	300MHz	1.5GHz	3.0Gbps
SATA Gen. 2	150MHz	1	10	300MHz	1.5GHz	3.0Gbps

NOTE: ** All link start with 3.0Gbps, then negotiate down to 1.5Gbps for SATA Generation 1 devices.*

3.6.1 Spread Spectrum Clocking

The XRS10L140 provides full support for receipt and generation of signals that have been configured for Spread Spectrum Clocking (SSC) support. The spread technique is implemented by down-spreading the data rate by 0.5% as a means of reducing EMI. Generation of the down-spread clock is performed within the XRS10L140. An example of the resultant spectral fundamental frequency before and after SSC can be seen in **Figure 8**.

FIGURE 8. SPREAD SPECTRUM CLOCKING



3.7 Test and Loopback Modes

The XRS10L140 provides for loopback testing on both the host and device interfaces, and incorporates a number of internal testing features, as outlined in the following subsections.

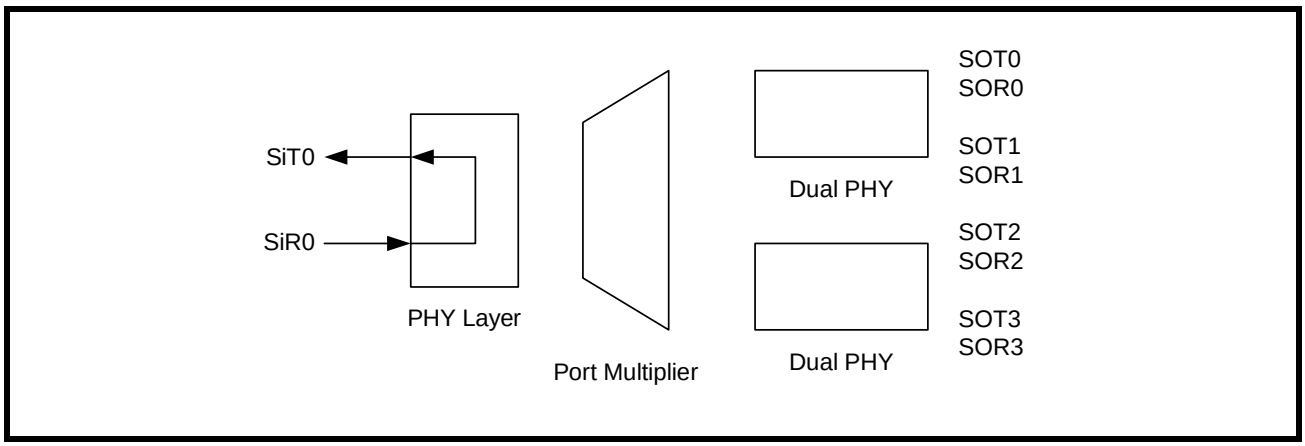
3.7.1 Host Side Loopback Modes

The XRS10L140 supports two forms of host loopback modes: a shallow serial loopback implemented within the host PHY macro, or a deep parallel loopback implemented within the device PHY macros after the port selector and port multiplier functionality.

SHALLOW HOST LOOPBACK MODE

The shallow host loopback mode is shown in **Figure 9**. In this mode, the incoming data stream from the host and embedded clock are recovered by an internal CDR, and the deserialized data is retransmitted serially back to the host, as clocked by the recovered clock. In this implementation, the received data is still transmitted to the internal port selector block and will propagate through to the device side output pins.

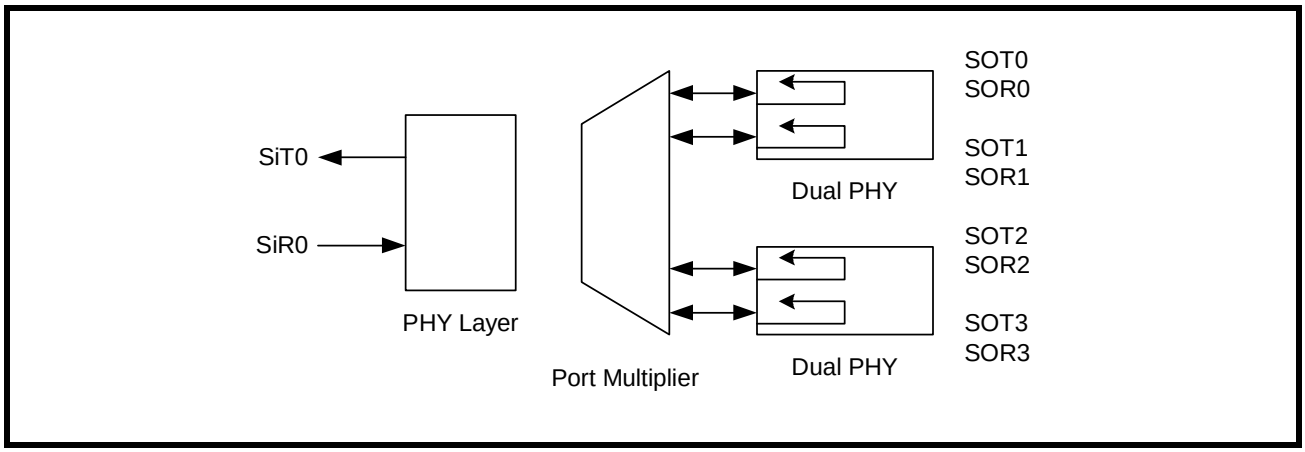
FIGURE 9. SHALLOW HOST LOOPBACK MODE



DEEP HOST LOOPBACK MODE

The deep host loopback mode is shown in **Figure 10**. In this mode, the incoming data stream from the host is transmitted through the digital blocks within the XRS10L140, and the loopback path is implemented at the device-side Serial ATA PHY block. Note that once again, the looped back data is still transmitted on the device-side output pins. The deep host loopback mode is enabled by using the Parallel Loopback registers for the downstream PHYs in Device 2 or 3. This received data must be in the form of valid SATA frames for a deep loopback to be successful, or the internal logic must be bypassed via MDIO register settings.

FIGURE 10. DEEP HOST LOOPBACK MODE



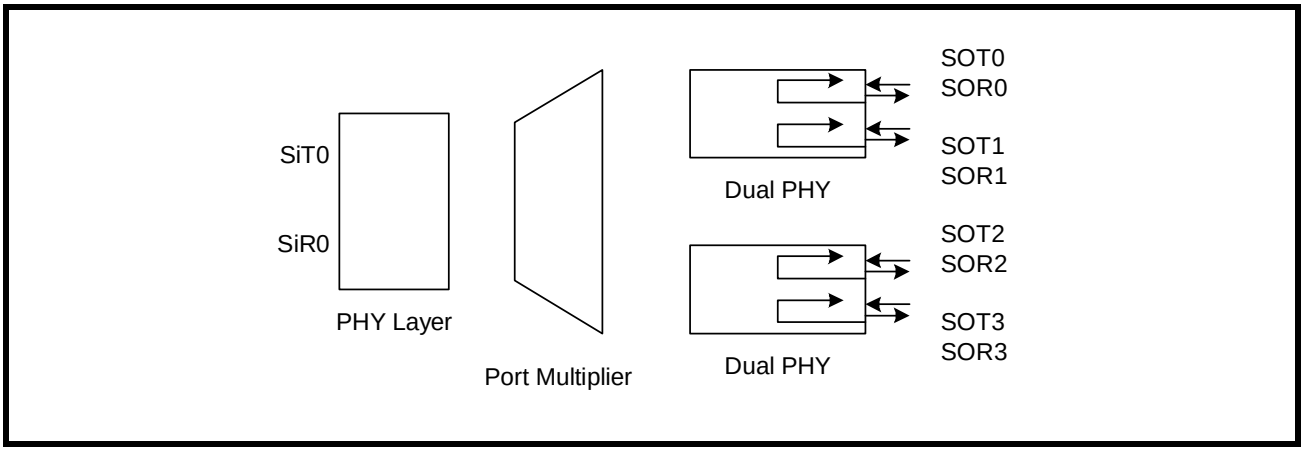
3.7.2 Device Side Loopback Modes

The XRS10L140 supports two forms of device-side loopback modes: a shallow serial loopback implemented within the device-side PHY macros, or a deep parallel loopback implemented within the host PHY macro after the port selector and port multiplier functionality.

SHALLOW DEVICE LOOPBACK MODE

The shallow device loopback mode is shown in **Figure 11**. In this mode, the incoming data stream from the device and embedded clock are recovered by an internal CDR, and the deserialized data is retransmitted serially back to the designated device, as clocked by the recovered clock. In this implementation, the received data is still transmitted to the internal port multiplier block.

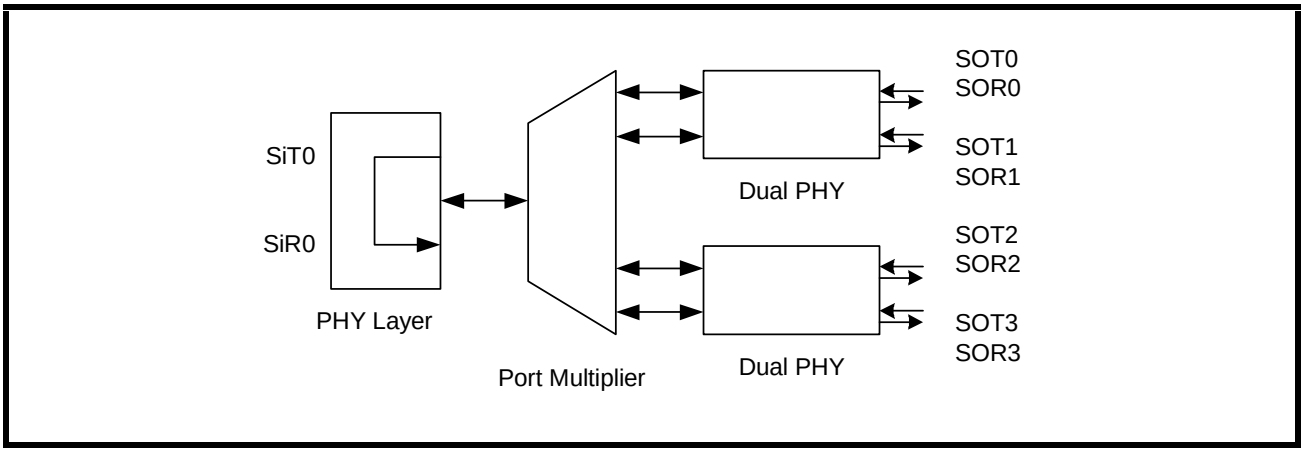
FIGURE 11. SHALLOW DEVICE LOOPBACK MODE



DEEP DEVICE LOOPBACK MODE

The deep device loopback mode is shown in **Figure 12**. In this mode, the incoming data stream from the device is transmitted through the digital blocks within the XRS10L140, and the loopback path is implemented at the host-side Serial ATA PHY block. Note that once again, the looped back data is still transmitted on the host-side output pins.

FIGURE 12. DEEP DEVICE LOOPBACK MODE



4.0 ELECTRICAL SPECIFICATIONS

This section contains the electrical specifications for the XRS10L140.

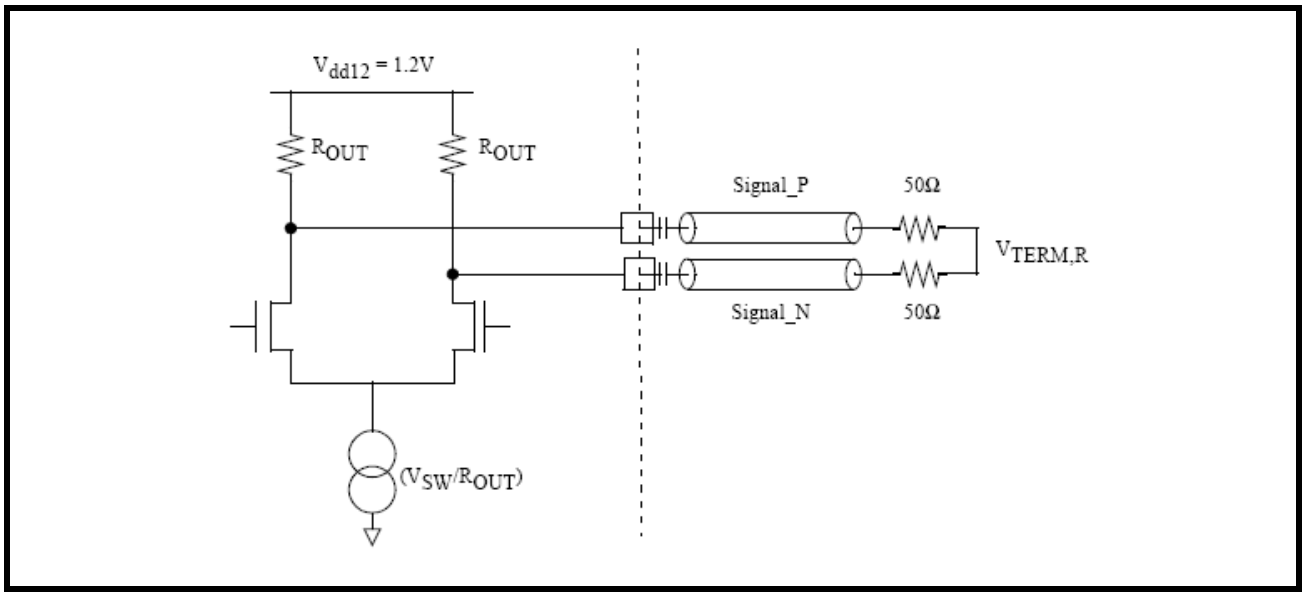
4.1 Serial ATA Specifications

The XRS10L140 electrical transmit and receive specifications are outlined in this section. The XRS10L140 is fully compliant to the Serial ATA II specification for Gen2i, Gen2x, Gen1i, Gen1x and Gen1m variations at 3.0 and 1.5 Gbps.

4.1.1 Serial ATA Transmitter

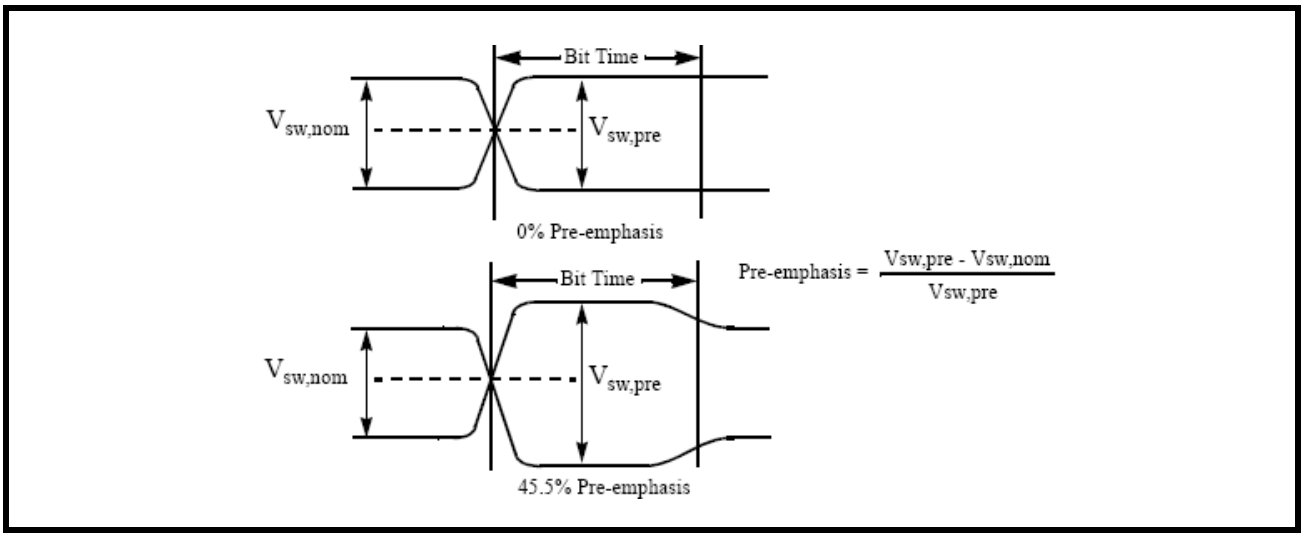
A simplified version of the output circuit and test fixture for each of the 6 Serial ATA transmit outputs on the XRS10L140 is shown in **Figure 13**. The output differential pair is terminated to the supply VDD. The circuit is designed to be AC coupled.

FIGURE 13. SERIAL ATA EQUIVALENT OUTPUT CIRCUIT



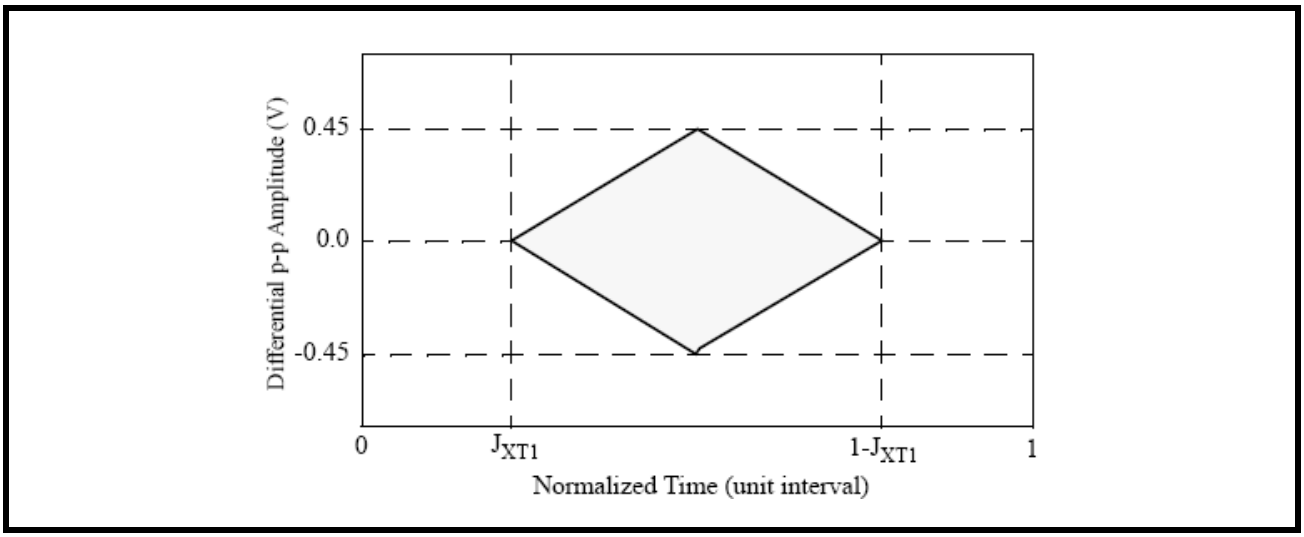
The XRS10L140 Serial ATA outputs include a simple one-tap equalizer, that is useful in driving longer printed circuit traces and is a required component in second generation Serial ATA PHYs. This equalizer pre-emphasizes the output signal whenever there is a data transition. The amount of pre-emphasis can vary between 0 and 45.5%, and is configured via MDIO register settings. Note that pre-emphasis doesn't increase the overall swing, but instead reduces the output amplitude when there is no transition.

FIGURE 14. EFFECTS OF TRANSMIT PRE-EMPHASIS



The overall swing level can also be modified via MDIO register settings. The XRS10L140 transmit mask is shown in **Figure 15**.

FIGURE 15. TRANSMIT EYE MASK FOR SERIAL ATA OUTPUT



SERIAL ATA RECEIVER

An equivalent circuit for the XRS10L140 Serial ATA inputs is shown in **Figure 16**. The device receiver mask is shown in **Figure 17**. This circuit is designed to be AC coupled. Note that the Serial ATA system specification requires the common mode value of the receiver to be near ground; to accomplish this, a high value resistor should be placed on the connector side of the AC coupling capacitor. The termination resistors are not connected during power-up.

FIGURE 16. SERIAL ATA EQUIVALENT INPUT CIRCUIT

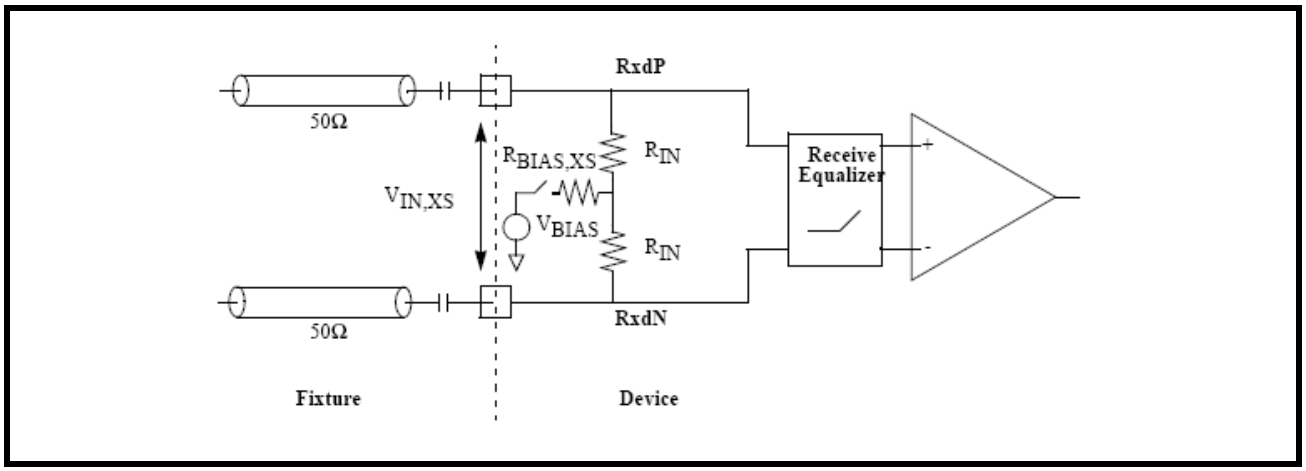


FIGURE 17. RECEIVE EYE MASK FOR SERIAL ATA INPUT

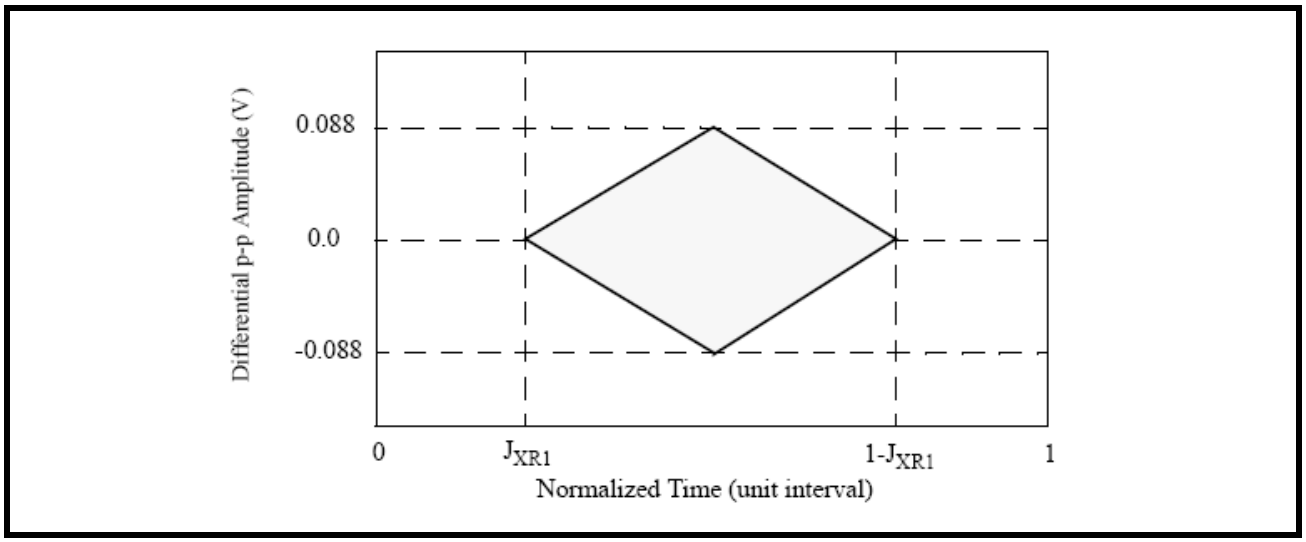


TABLE 3: SERIAL ATA LINK SPECIFICATIONS

NAME	DESCRIPTION	MIN.	NOM	MAX	UNITS
$t_{BIT,XS}$	Bit Time	670	-	333	ps
J_{XR1}	Input Jitter Tolerance Mask at signal crossover	0.32	-	-	UI
$J_{XR1,DJ}$	Deterministic jitter tolerance at signal crossover	0.18	-	-	UI
J_{XT1}	Output jitter mask at signal crossover	-	-	0.15	UI
$J_{XT1,DJ}$	Deterministic output jitter at signal crossover	-	-	0.07	UI
t_R/t_F	Input signal rise/fall times (20% - 80%)	0.2	-	0.46	UI
t_{QR}/t_{QF}	Output signal rise/fall times (20% - 80%)	0.2	-	0.41	UI
$t_{TOL,RX}$[1]	RX to sysclock frequency offset tolerance	-5350	0	350	ppm
V_{IN}	Input swing, differential peak-peak	175	-	1600	mV
V_{SW}[2]	Output swing, differential peak-peak	800	-	1200	mV
$V_{IN,IDLE}$	No swing detection threshold	65	120	155	mV
$R_{IN,DIFF}$	Differential mode input resistance	85	100	115	mV
$R_{IN,CM}$[3]	Common mode input resistance	40	50	60	Ω
$R_{IN,OFF}$	Common mode input resistance, no power	200	-	-	kΩ
$R_{IN,XS}$	Output termination resistance	40	50	60	Ω
$S_{11,IN,DIFF}$	Differential input return loss, 50MHz - 1.5GHz	12	-	-	dB
$S_{11,IN,CM}$	Common mode input return loss 50MHz-1.5GHz	6	-	-	dB
$S_{22,OUT,DIFF}$	Differential output return loss 50MHz-1.5GHz	12	-	-	dB
$S_{22,OUT,CM}$	Common mode output return loss 50MHz-1.5GHz	6	-	-	dB
$t_{S,REG}$	Setup time for register port	1.5	-	-	ns
$t_{H,REG}$	Hold time for register port	1.5	-	-	ns
$t_{Q,REG}$	Clock to Q time for register port	0	-	2	ns
$t_{CYC,REG}$	Register port clock cycle time	10	-	-	ns
$t_{HI,REG}$	R register port clock high time	4	-	-	ns
$t_{LO,REG}$	Register port clock low time	4	-	-	ns
$t_{RF,REG}$	Register port input rise/fall time	-	-	0.5	ns

4.2 CMOS Interface

AC and DC specifications for the CMOS inputs and outputs are listed in **Table 4**. Since all these signals are asychronous, there are no setup or hold times defined. The CMOS pins are defined in the General Control and Configuration portion of **Table 1** in Section 1, "Pin Descriptions".

TABLE 4: CMOS I/O SPECIFICATIONS

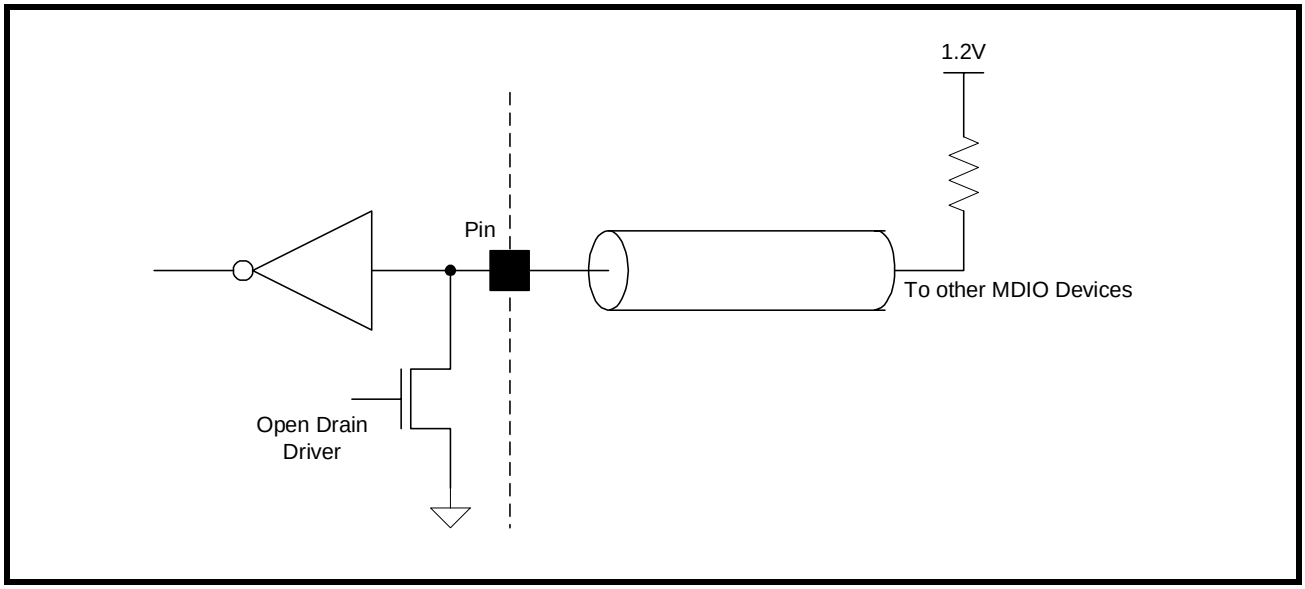
NAME	DESCRIPTION	MIN	NOM	MAX	UNITS
$t_{DR}/t_{DF,CMOS}$	CMOS input signal rise/fall times (20% - 80%)	0.2	-	5	ns
$t_{QR}/t_{QF,CMOS}$1	CMOS output signal rise/fall times (20% - 80%)	0.2	-	5	ns
$V_{IL,CMOS}$	CMOS input low voltage	-0.3	0	0.36	V
$V_{IH,CMOS}$	CMOS input high voltage	0.8	2.5	2.8	V
$I_{OL,CMOS}$	Output current for VOL = 0.2V	4.0	-	20	mA
$dI_{OL}/dt_{,CMOS}$	Output current rate of change	-10	-	10	mA/ns
$L_{I,CMOS}$	CMOS I/O inductance	-	-	8	nH
$C_{I,CMOS}$	CMOS I/O capacitance	-	-	5	pF

.1. This value is measured driving a load of 20pF.

4.3 MDIO Interface

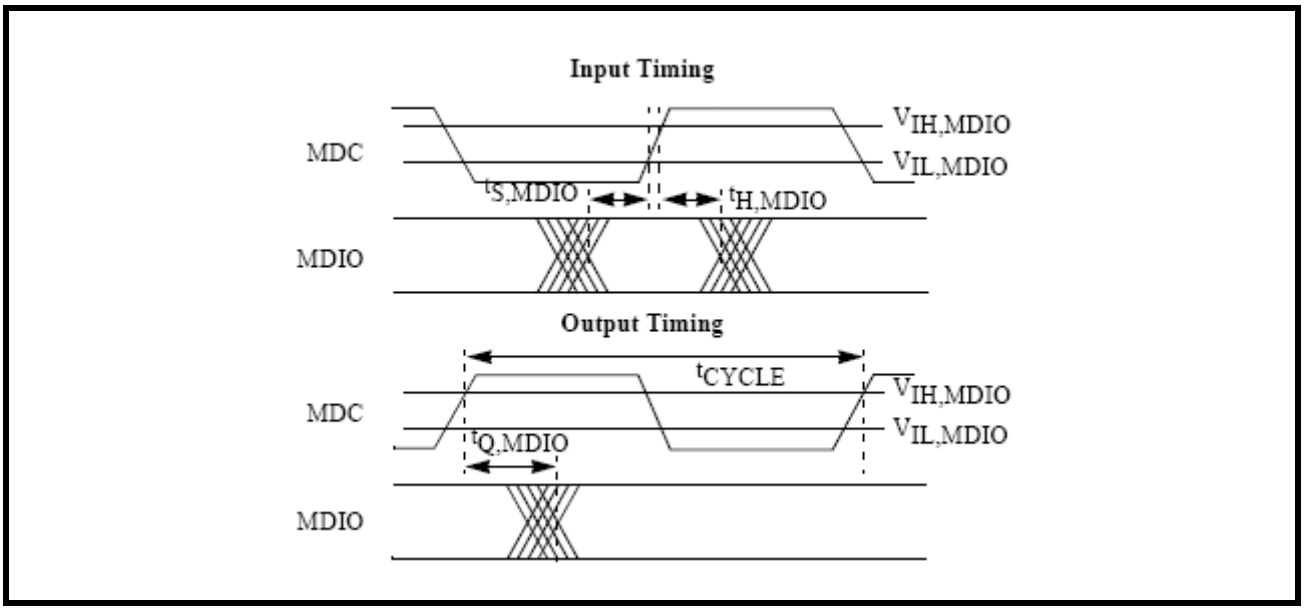
The Management Data Input/Output (MDIO) port complies with Clause 45 of the IEEE 802.3ae specification. A representative MDIO driver/receiver is shown in **Figure 18**. MDIO uses an open drain driver with a pullup resistor to 1.2V.

FIGURE 18. REPRESENTATIVE MDIO CIRCUIT



Representative MDIO Read and Write waveforms are shown in **Figure 19**. The XRS10L140 samples MDIO on the rising edge of MDC for input and drives MDIO after the rising edge of MDC for output. Note that setup, hold, and output timings are defined from the maximum V_{IL} and minimum V_{IH} levels.

FIGURE 19. MDIO INPUT AND OUTPUT WAVEFORMS



Values for MDIO parameters are shown in **Table 5**

TABLE 5: MDIO DC AND AC CHARACTERISTICS

Name	Description	Min	Nom	Max	Units
$t_{CYCLE,MDIO}$	MDC cycle time	400	-	-	ns
$t_{LOW,MDC}$	MDC low time	160	-	-	ns
$t_{HIGH,MDC}$	MDC high time	160	-	-	ns
$t_{S,MDIO}$[1]	MDIO input to MDC setup time	10	-	-	ns
$t_{H,MDIO}$[2]	MDC to MDIO input hold time	10	-	-	ns
$t_{Q,MDIO}$[3]	MDC to MDIO output time	0	-	150	ns
$t_{DR}/t_{DF,MDIO}$	MDIO input signal rise/fall times (20% - 80%)	0.2	-	100	ns
$t_{QR}/t_{QF,MDIO}$[4]	MDIO output signal rise/fall times (20% - 80%)	0.2	-	80	ns
$V_{IL,MDIO}$	MDIO input low voltage	-0.3	0	0.36	V
$V_{IH,MDIO}$	MDIO input high voltage	0.84	1.2	1.5	V
$V_{OL,MDIO}$[4]	MDIO output low voltage	-0.3	0	0.2	V

TABLE 5: MDIO DC AND AC CHARACTERISTICS

$V_{OH,MDIO}$[4]	MDIO output high voltage	1.0	1.2	1.5	V
$I_{OL,MDIO}$	MDIO Output current for VOL = 0.2V	4.0	-	20	mA
$dI_{OL}/dt_{,MDIO}$	MDIO Output current rate of change	-10	-	10	mA/ns
$L_{I,MDIO}$	MDIO input inductance	-	-	8	nH
$C_{I,MDIO}$	MDIO input capacitance	-	-	5	pF

NOTES:

1. *Measured from minimum MDIO VIH to maximum MDC VIL for MDIO rising edge.*
   Measured from maximum MDIO VIL to maximum MDC VIL for MDIO falling edge.
2. *Measured from minimum MDC VIH to maximum MDIO VIL for MDIO rising edge.*
   Measured from minimum MDC VIH to minimum MDIO VIH for MDIO falling edge.
3. *Measured from minimum MDC VIH to maximum MDIO VIL for MDIO rising edge and MDC rising edge.*
   Measured from minimum MDC VIH to minimum MDIO VIH for MDIO falling edge and MDC rising edge.
   Measured from maximum MDC VIL to maximum MDIO VIL for MDIO rising edge and MDC falling edge.
   Measured from maximum MDC VIL to minimum MDIO VIH for MDIO falling edge and MDC falling edge.
4. *Measured driving a load of 470pF.*

TABLE 6: OPERATING CONDITIONS

Name	Description	Min	Nom	Max	Units
T_A	Ambient temperature under bias	0	25	70	^0C
V_{DD}	Core power supply voltage	1.14	1.2	1.26	V
I_{DD}	Core power supply current	-	650	800	mA
V_{ESD}	Electrostatic discharge tolerance, Human Body Model	2000			V
θ_{JA}	Junction-to-ambient thermal resistance		38.5		$^0C/W$

5.0 REGISTERS DESCRIPTION

The XRS10L140 provides a variety of registers for the purpose of device configuration, testing and monitoring. These registers are accessed through the MDIO interface, outlined in **"Section 4.3, MDIO Interface" on page 17**. The entire register set is described in this section.

5.1 Register Overview

The XRS10L140 port address is hardwired to 0; this field should be set to 0 in all packets.The XRS10L140 contains three identical instantiations of a dual Serial ATA PHY macro. A common set of registers exists within each of these macros, and are outlined in **"Section 5.2, Macro Registers" on page 21**. MDIO device designations 1-3 are used for each of these three macros as shown in Table 8. Registers relating to the XRS10L140 as a whole are outlined in **"Section 5.3, XRS10L140 Device Generic Registers" on page 35** and make use of MDIO device 0.

TABLE 7: MDIO DEVICE DESIGNATIONS

MDIO DEVICE DESIGNATION	MACRO	RELEVANT PINS
0	XRS10L140 Device Generic Registers	N/A
1	Serial ATA Input Macro	SI0
2	Serial ATA Output Macro 0	SO0, SO1
3	Serial ATA Output Macro 1	SO2, SO3

The XRS10L140 registers are arranged as 8-bit fields with 8-bit addresses. These are mapped into the 16-bit MDIO address and data fields by setting the most significant byte of each to be 0. An example mapping from a macro address/data combination to an MDIO address & data combination is shown in Table 9+

TABLE 8: MDIO ADDRESSING

MACRO ADDRESS	MACRO DATA	MDIO ADDRESS	MDIO DATA
0x40	abcde	0x0040	00000000000abcde

NOTE: *The unused upper 3 bits in FBDIV are also set to 0 during MDIO writes and are undefined during MDIO reads.*

In the description of each register field, there is an entry describing its read/write status. This may fall into one of the following categories:

- R/W- register field is read/write
- RO - register field is read only
- LL - Latching Low - Used with bits that monitor some state internal to the XRS10L140. When the condition for the bit to go low is reached, the bit stays low until the next time it is read. Once it is read, its value reverts to the cur-rent state of the condition it monitors.
- LH - Latching High - When the condition for the bit to go high is reached, the bit stays high until the next time it is read. Once it is read, its value reverts to the current state of the condition it monitors.
- SC - When an SC bit is set, some action is initiated; once the action is complete, the bit is cleared.

5.2 Macro Registers

The registers outlined in this section are common to each of the three Serial ATA dual PHY macros as described in the previous section. As such, each listed register is present in each of the 1, 2, and 3 MDIO register spaces, and will perform the stated function on the specified Serial ATA lane.

The registers within each dual PHY macro are split into three sections:

Transmit/receive lane 0 registers:	Address range 000*****
PLL registers:	Address range 010*****
Bias generator registers:	Address range 011*****

TABLE 9: TRANSMIT/RECEIVE LANE REGISTERS (MDIO DEVICE 1, 2, 3)

ADDRESS HEX	BIT(S)	NAME	R/W	DEFAULT	DESCRPTION
N.0000	7:6	Reserved	RO	-	Reserved
	5:4	Receive_Test0[1:0]	R/W	00	PRBS checker control 00 = disable PRBS checkers 01 = enable 2^23-1 checkers 10 = enable 2^31-1 checkers 11 = enable 2^10-1 checkes
	3:2	Transmit_Test0[1:0]	R/W	00	Test Pattern Control 00 = Use input data from DATAIN 01 = Generate 2^23-1 PRBS 10 = Generate 2^31-1 PRBS 11 = Generate 2^10-1 PRBS
	1	selFourFive	R/W	1	0 = Output data is x8 1 = Output data is x10
	0	SATAPCIEXB	R/W	1	Tx output swing booster bit 0 = boost swing by 10% 1 = nominal swing
N.0001	7:3	RiseFall_Coef0[4:0]	R/W	00000	Output rise/fall time coefficient 00000 = +0ps 11111 = +25ps 01001 = SATA 3G 00010 = SATA 1.5G other = increases rise/fall times monotonically between 0 and 25ps
	2:0	Transmit_Eq0[2:0]	R/W	000	Transmit equalization contro 000 = 0% transmit preemphasis 001 = 6.5% transmit preemphasis 010 = 13% transmit preemphasis 011 = 19.5% transmit preemphasis 100 = 26% transmit preemphasis 101 = 32.5% transmit preemphasis 110 = 39% transmit preemphasis 111 = 45.5% transmit preemphasis

TABLE 9: TRANSMIT/RECEIVE LANE REGISTERS (MDIO DEVICE 1, 2, 3)

ADDRESS HEX	BIT(S)	NAME	R/W	DEFAULT	DESCRPTION
N.0002	7:6	mscProg0[1:0]	RW	01	Receive equalization control – boost at 1.5GHz
	5:3	Beacon_Swing0[2:0]	R/W	100	Transmit swing size for OOB Signals 000 = 800mV 001 = 700mV 010 = 600mV 011 = 500mV 100 = 400mV 101 = 300mV 110 = 200mV 111 = 0mV
	2:0	Output_Swing0[2:0]	R/W	100	Transmit swing size in normal opera-tion 000 = 800mV 001 = 700mV 010 = 600mV 011 = 500mV 100 = 400mV 101 = 300mV 110 =200mV 111 = 0mV
N.0003	7	enEqB	RO	1	Enable receive equalization 0 = enable equalization 1 = disable equalization
	6:4	noSigLevel0[2:0]	RW	001	Nominal threshold for no signal detect
	3:0	hpProgOvrd0[3:0]	RW	0000	High pole programming override value
N.0004	7:0	xCDROffs_F0[7:0]	RW	0x40	2's complement offset for Clock data recovery Offset = CDRoff*tbit/128 Value of xCDROffs0/1 when DIV2CLK=0
N.0005	7:0	Rx_Offset0	R/W		2's complement offset for Clock data recovery Offset = CDRoff*tbit/256 Value of xCDROffs0/1 when DIV2CLK=1
N.0006	7	xCDRmetamode	RO	0	Selection of clock to use on FSM
	6	xCDRrndT	RW	1	Randomizes tie breaker
	5	xCDRclkmode	RW	0	selects clock to use for FSM
	4	xCDRrotate	RW	0	Enables CDR rotation
	3:0	xCDRinc0[3:0]	RW	0x2	Increment for CDR
N.0007	7:5	xCDRupdnsw[2:0]	RW	000	Direction of count on FSM
	4:0	xCDRincF0[4:0]	RW	00100	Fast increment size for CDR

TABLE 9: TRANSMIT/RECEIVE LANE REGISTERS (MDIO DEVICE 1, 2, 3)

ADDRESS HEX	BIT(S)	NAME	R/W	DEFAULT	DESCRPTION
N.0008	7	Reserved	RO	-	Reserved
	6	xCDRenF		1	
	5	xCDRmisc	R/W	0	
	4:0	xCDRlimHF0[4:0]	RW	00111	
N.0009	7	Reserved	RO	-	Reserved
	6	xCDRmult2F_F	RW	0	Value of xCDRmult2F when DIV2CLK=0
	5	xCDRmult2F_H	RW	1	Value of xCDRmult2F when DIV2CLK=1
	4:0	xCDRlimLF0[4:0]	RW	0x18	
N.000A	7:6	Reserved	RO	-	Reserved
	5:0	MinBurstWidth0[5:0]	R/W	000100	Lower bound count of activity burst for COM FSM
N.000B	7:6	Reserved	RO	-	Reserved
	5:0	MaxBurstWidth0[5:0]	R/W	000111	Upper bound count of activity burst for COM FSM
N.000C	7:6	Reserved	RO	-	Reserved
	5:0	MinInitWidth0[5:0]	RW	001100	Lower bound count of idle for COMINIT/COM-RESET
N.000D	7:6	Reserved	RO	-	Reserved
	5:0	MaxWakeWidth0	RW	010110	Upper bound count of idle for COMINIT/COM-RESET
N.000E	7:6	Reserved	RO	-	Reserved
	5:0	MinWakeWidth0[5:0]	RW	000100	Lower bound count of idle for COMWAKE
N.000F	7:6	Reserved	RO	-	Reserved
	5:0	MaxWakeWidth0[5:0]		000111	Upper bound count of idle for COMWAKE
N.0010	7:6	Reserved	RO	-	Reserved
	5:3	rcvRef0[2:0]	RW	011	Percent of full swing that TX must reach during Receiver Detect to count as receiver present (not applicable to SATA PHY macros)
	2:0	squelchdivsel[2:0]		010	Value by which to divide squelch clock 000 = divide by 1 001 = divide by 2 010 = divide by 4 011 = divide by 6 100 = divide by 8 101 = divide by 10 110 = divide by 12 111 = divide by 14

TABLE 9: TRANSMIT/RECEIVE LANE REGISTERS (MDIO DEVICE 1, 2, 3)

ADDRESS HEX	BIT(S)	NAME	R/W	DEFAULT	DESCRPTION
N.0011	7:0	rcvdetdelay0[10:0] (lower 8 bits)			Number of SYSCLK cycles to wait between assertion of RECDET and clocking comparator
N.0012	7:3	Reserved	RO	-	Reserved
	2:0	rcvdetdelay0[10:0] (upper 3 bits)			Number of SYSCLK cycles to wait between assertion of RECDET and clocking comparator for receiver detect (not applicable to SATA PHY macros)
N.0013	7	orxpclkflip		0	Invert outgoing rxpclk for external use
	6	irxpclkflip		1	Invert incoming rxpclk for internal use
	5	rxpclkflip		0	line loopback fifo rxpclk flip
	4	otxpclkflip		0	Invert outgoing txpclk for external use
	3	itxpclkflip		0	Invert incoming txpclk for internal use
	2:0	clkTestSel0[2:0]		000	Selection for clock onto clockTest pin 000 = disable 001 = txpclk[0] 010 = rxclk[0] 011 = sysclk 100 = SSCtrig other = reserved Only clkTestSel0 is active; clkTestSel1 is a no-connect
N.0014	7:6	Reserved	RO	-	Reserved
	5:3	nidleCmin[2:0]		011	Number of idles required before declaring a COM* match
	2:0	nburstCmin[2:0]		0100	Number of bursts required before declaring a COM* match
N.0015	7	Reserved	RO	-	Reserved
	6:4	sysclk25divsel0[2:0]		011	Divider selection for sysclk-> sysclk25 000 = divide by 1 (sysclk is 25MHz) 001 = divide by 2 (sysclk is 50MHz) 010 = divide by 3 (sysclk is 75MHz) 011 = divide by 4 (sysclk is 100MHz) 100 = divide by 5 (sysclk is 125MHz) 101 = divide by 6 (sysclk is 150MHz) 110 = divide by 10 (sysclk is 250MHz) 111 = divide by 12 (sysclk is 300MHz)
	3:0	comburstnum[3:0]		0xf	number of bursts in com* sequence
N.0017 N.0016	7:0	wec0[15:0]	RO	-	PRBS error count Upper byte read clears both upper and lower bytes

TABLE 9: TRANSMIT/RECEIVE LANE REGISTERS (MDIO DEVICE 1, 2, 3)

ADDRESS HEX	BIT(S)	NAME	R/W	DEFAULT	DESCRPTION
N.0018	7:6	Reserved	RO	-	Reserved
	5:3	txbiasbuffselb0[2:0]		100	Tx Pre-driver swing size for aync beacon 000 = 800mV 001 = 700mV 010 = 600mV 011 = 500mV 100 = 400mV 101 = 300mV 110 = 200mV 111 = 0mV ***NOTE:*** *This feature is not used for SATA*
	2:0	txbiasbuffsela0[2:0]		100	Tx Pre-diver swing size in normal operation 000 = 800mV 001 = 700mV 010 = 600mV 011 = 500mV 100 = 400mV (sata default) 101 = 300mV
N.0019	7:5	Reserved	RO	-	Reserved
	4:0	rcSelH0[4:0]		00011	Output rise/fall time coefficient 00000 = +0ps 11111 = +25ps Other code increases rise/fall times monotonically between 0 and 25ps

The Rx_offset registers change the sampling point of the data relative to the bit boundary. The offset value is stored in two's complement format, with bit 0 being the LSB. The step size is a fraction of the bit time; it is constant across process and operating conditions but changes with the operating frequency. The eye diagram in **Figures 20** shows graphically the effect of changing the register value.

FIGURE 20. EFFECT OF SETTING RECEIVE OFFSET REGISTER

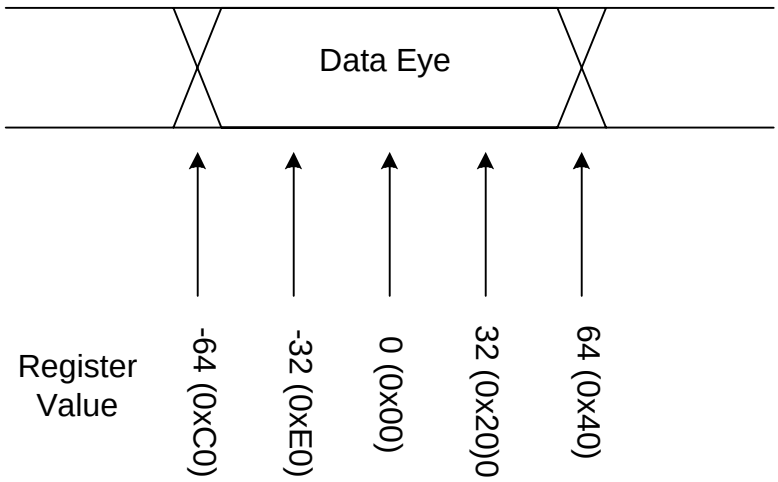


TABLE 10: PLL CONFIGURATION/DEBUG REGISTERS (MDIO DEVICE 1, 2, 3)

ADDRESS HEX	BIT(S)	NAME	R/W	DEFAULT	DESCRIPTION
N.0040	7:6	Reserved	RO	-	Reserved
	5:0	FBDIV[5:0]		100101	Divide value for feedback clock 110000 = divide by 5 100000 = divide by 10 100001 = divide by 15 100010 = divide by 20 100011 = divide by 25 100101 = divide by 30 (default) 100111 = divide by 50 101101 = divide by 60 Other - reserved
N.0041	7:6	Reserved	RO	-	Reserved
	5:0	REFDIV[5:0]		000000	Divide values for system clock 010000 = divide by 1 000000 = divide by 2 (default) 000001 = divide by 3 000010 = divide by 4 000011 = divide by 5 000101 = divide by 6 000110 = divide by 8 000111 = divide by 10 001101 = divide by 12 001110 = divide by 16 001111 = divide by 20 Others - reserved
N.0042	7:6	Reserved	RO	-	Reserved
	5:0	SSCInc	R/W	0x01	Step size for SSC increment
N.0043	7:6	Reserved	RO	-	Reserved
	5:0	SSCIncIntrv	R/W	01100	Interval between steps for SSC increment
N.0044	7:6	Reserved	RO	-	Reserved
	5:0	SSCMax	R/W	00000	Maximum value for spread

TABLE 10: PLL CONFIGURATION/DEBUG REGISTERS (MDIO DEVICE 1, 2, 3)

ADDRESS HEX	BIT(S)	NAME	R/W	DEFAULT	DESCRIPTION
N.0045	7:5	Reserved	RO	-	Reserved
	4	SSCmode	R/W	0	Selects position of spreading interpolator 0 = Interpolator in feedback path 1 = Interpolator in feedforward path
	3	SSCCenter	R/W	0	Center spread instead of down/upspread
	2	SSCInvert	R/W	0	Spread up instead of down
	1	SSCPDMBypass	R/W	0	Do not use the pulse density modulator
	0	SSCBypass	R/W	1	Bypass the saw generator and pulse density modulator and get increment from SSCMax (set SSCMax to 51 when SSCBypass is set to 0)
N.0046	7	PLLQpumpOvrd	RO	-	Override for charge pump programmability 0 = use value based on FB divider 1 = use value from PLLQpump Values based on FB divider: FBDIV[5:0] qpump[6:0] 11XXXX => 1111110 100000 => 0001110 100001 => 0000110 100010 => 0000011 100011 => 0000010 100101 => 0000010 100111 => 0000001 101101 => 0000001 Others => 0000000
	6:0	PLLQpump[6:0]			Charge Pump Programmability 000001 = Enable 1 charge pump unit 000010 = Enable 2 charge pump units 000011 = Enable 3 charge pump units 000110 = Enable 4 charge pump units 000111 = Enable 5 charge pump units 001110 = Enable 6 charge pump units 001111 = Enable 7 charge pump units 011110 = Enable 8 charge pump units 011111 = Enable 9 charge pump units 111110 = Enable 10 charge pump units 111111 = Enable 11 charge pump units

TABLE 10: PLL CONFIGURATION/DEBUG REGISTERS (MDIO DEVICE 1, 2, 3)

ADDRESS HEX	BIT(S)	NAME	R/W	DEFAULT	DESCRIPTION
N.0047	7:3	Reserved	RO	-	Reserved
	2	tdccovrd		0	1 = use tdccen bits to activate/disable transmit duty cycle correction ports 0 = use pwrdnTxB bits to activate/disable transmit duty cycle correction ports
	1:0	tdccen[1:0]		00	When tdccovrd is asserted, tdccen[N] enables/disables duty cycle correction from transmit lane N. 1 = enable duty cycle correction from lane N 0 = disable duty cycle correction from lane N
N.0048	7:1	Reserved	RO	-	Reserved
	0	pllClkDiv5en		1	1 = enable pllclkDiv5 0 = disable pllClkDiv5

TABLE 11: BIAS GENERATOR CONFIGURATION/DEBUG REGISTERS (MDIO DEVICE 1, 2, 3)

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
N.0060	7:3	Reserved			Reserved
	1	bgPwrdn		0	Powers down core of bandgap circuit 0 = Normal operation 1 = power down core of bandgap The bandgap voltage can be overdriven externally by setting both bgTesten and bgPwrdn
	0	bgTestEn		0	Bandgap test mode enable 0 = Normal operation 1 = Connect bandgap voltage to bgMuxOut

TABLE 11: BIAS GENERATOR CONFIGURATION/DEBUG REGISTERS (MDIO DEVICE 1, 2, 3)

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
N.0061	7:6	prcal50dccQrx[1:0]		00	Input DCC rcal bias for Q 00 = 50µA 01 = 75uA 10 = 25uA 11 = 100uA
	5:4	prcal50dccIrx[1:0]		00	Input DCC rcal bias for I 00 = 50uA 01 = 75uA 10 = 25uA 11 = 100uA
	3:2	prcal50DCCpll[1:0]		00	PLL DCC 50u rcal bias 00 = 50uA 01 = 75uA 10 = 25uA 11 = 100uA
	1:0	prcal50CLpll[1:0]		00	PLL 50u rcval bias 00 = 50uA 01 = 75uA 10 = 25uA 11 = 100uA
N.0062	7:4	pr100pampQrx[3:0]		0x0	Input amp r bias for Q 1010=50uA 0010=75uA 0000=100uA 0001=125uA 1100=150uA, 0111=175uA 1111=200uA
	3:0	pr100pampIrx[3:0]		0x0	Input amp r bias for I 1010=50uA 0010=75uA 0000=100uA 0001=125uA 1100=150uA 0111=175uA 1111=200uA

TABLE 11: BIAS GENERATOR CONFIGURATION/DEBUG REGISTERS (MDIO DEVICE 1, 2, 3)

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
N.0063	7:6	Reserved	RO	-	Reserved
	5:4	prcal50squelch[1:0]		00	Squelch 50u rcal bias 00 = 50uA 01 = 75uA 10 = 25uA 11 = 100uA
	3:2	pr50squelch1[1:0]		00	Squelch 50µ r bias 00 = 50uA 01 = 75uA, 10 = 25uA 11 = 100uA
	1:0	pr50squelch0[1:0]		00	Squelch 50µ r bias 00 = 50uA, 01 = 75µA 10 = 25µA 11 = 100µA
N.0064	7:4	pr100Tx[3:0]		0x0	Transmit r bias 1010=50uA 0010=75uA 0000=100uA 0001=125uA 1100=150uA 0111=175uA 1111=200uA
	3:0	pr100squelch[3:0]		0x0	Squelch 100u r bias 1010=50uA 0010=75uA 0000=100uA 0001=125uA 1100=150uA 0111=175uA 1111=200uA

TABLE 11: BIAS GENERATOR CONFIGURATION/DEBUG REGISTERS (MDIO DEVICE 1, 2, 3)

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
N.0065	7:6	prcal50spare0[1:0]		00	50u spare rcal bias 0 00 = 50uA 01 = 75uA 10 = 25uA 11 = 100uA
	5:4	prcal50DCCTx[1:0]		00	Transmit rcal bias 00 = 50uA 01 = 75uA 10 = 25uA 11 = 100uA
	3:0	prcal100Tx[3:0]		0x0	Transmit rcal bias 1010=50uA 0010=75uA 0000=100uA 0001=125uA 1100=150uA 0111=175uA 1111=200uA
N.0066	7:2	Reserved	RO	-	Reserved
	1:0	prcal50spare1[1:0]		00	50u spare rcal bias 0 00 = 50uA 01 = 75uA 10 = 25uA 11 = 100uA
N.0067	7:4	pr100ext1[3:0]		0x0	100u external bias 1010=50uA 0010=75uA 0000=100uA 0001=125uA 1100=150uA 0111=175uA 1111=200uA
	3:0	pr100ext0[3:0]		0x0	100u external bias 1010=50uA 0010=75uA 0000=100uA 0001=125uA 1100=150uA 0111=175uA 1111=200uA

TABLE 11: BIAS GENERATOR CONFIGURATION/DEBUG REGISTERS (MDIO DEVICE 1, 2, 3)

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
N.0068	7:4	Reserved	RO	-	Reserved
	3:0	prcal100pciPreamp [3:0]		0x0	100u external bias 1010=50uA 0010=75uA 0000=100uA 0001=125uA 1100=150uA 0111=175uA 1111=200uA

TABLE 12: POWERDOWN REGISTERS (MDIO DEVICES 1, 2 & 3)

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
1.0080 2.0080 3.0080	7:6	SIpwrdnDetB[1:0] SO01pwrdnDetB[1:0] SO23pwrdnDetB[1:0]	RW	11	Powers down the signal detector and COM* circuits 1 = normal operation 0 = power down
	5:4	SIpwrdnRxB[1:0] SO01pwrdnRxB[1:0] SO23pwrdnRxB[1:0]	RW	11	Powers down the receivers and CDR 1 = normal operation 0 = power down
	3:2	SIpwrdnTxDrvB[1:0] SO01pwrdnTxDrvB[1:0] SO23pwrdnTxDrvB[1:0]	RW	11	Powers down the transmitter 1 = normal operation 0 = power down
	1:0	SIpwrdnTxB[1:0] SO01pwrdnTxB[1:0] SO23pwrdnTxB[1:0]	RW	11	Powers down the transmit pipes and clock 1 = normal operation 0 = power down
1.0081 2.0081 3.0081	7:2	Reserved	RO	-	Reserved
	1	SIpwrdnBiasGen SO01pwrdnBiasGen SO23pwrdnBiasGen	RW	0	Powers down the bandgap. 1 = normal operation 0 = power down
	0	SIpwrdnPLLB SO01pwrdnPLLB SO23pwrdnPLLB	RW	1	Powers down the PLL 1 = normal operation 0 = power down

TABLE 13: BLOCK CONTROL SIGNALS (MDIO DEVICES 1, 2&3)

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
1.0082 2.0082 3.0082.	7:4	Reserved	RO	-	Reserved
	3:2	SIselLpbk[1:0] SO01selLpbk[1:0] SO23selLpbk[1:0]	RW	00	Serial Loopback Control 1 = Enable Serial Loopback 0 = Normal operation
	1:0	SIparLpbk[1:0] SO01parLpbk[1:0] SO23parLpbk[1:0]	RW	00	Parallel Loopback Control 1 = Enable Parallel Loopback 0 = Normal operation
1.0083 2.0083 3.0083	7:6	SISendBeacon[1:0] SO01SendBeacon[1:0] SO23SendBeacon[1:0] PSendBeacon[1:0]	RW	00	Causes beacon signal to be sent on link
	5:4	SItxsigsel1[1:0] SO01txsigsel1[1:0] SO23txsigsel1[1:0]	RW	00	Transmitter 1 source selection 00 = transmit data 01 = transmit internally generated beacon 10 = transmit externally generated beacon 11 = transmit idle/COM*
	3:2	SItxsigsel0[1:0] SO01txsigsel0[1:0] SO23txsigsel0[1:0]	RW	00	Transmitter 0 source selection 00 = transmit data 01 = transmit internally generated beacon 10 = transmit externally generated beacon 11 = transmit idle/COM*
	1:0	SIsysClkEn[1:0] SO01sysClkEn[1:0] SO23sysClkEn[1:0]	RW	00	Source of txPClk[1:0] SItxsigsel0[1:0] SO01txsigsel0[1:0]
1.0084 2.0084 3.0084	7:2	Reserved	RO	-	Reserved
	1:0	SIrcvDet[1:0] SO01rcvDet[1:0] SO23rcvDet[1:0]	RW/SC	00	Starts receiver detect cycle. Self clearing
1.0085 2.0085 3.0085	7:2	Reserved	RO	-	Reserved
	1:0	SIDIV2CLK[1:0] SO01DIV2CLK[1:0] SO23DIV2CLK[1:0]	RW	00	Divide reference clock by 2 for corresponding lane

TABLE 13: BLOCK CONTROL SIGNALS (MDIO DEVICES 1, 2&3)

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
1.0086 2.0086 3.0086	7:6	Reserved	RO	-	Reserved
	5:4	SIforceidle[1:0] SO01forceidle[1:0] SO23forceidle[1:0]	RW	00	Generate forceidle signal to lane
	3:2	SIcomtype[1:0] SO01comtype[1:0] SO23comtype[1:0]	RW	00	Type of COM sequence to generate when Comstart is asserted 1 = generate WAKE 0 = generate INIT
	1:0	SIcomstart[1:0] SO01comstart[1:0] SO23comstart[1:0]	RW/SC	00	Comstart signal. Self clearing
1.0087 2.0087 3.0087	7:6	SIcomfinish[1:0] SO01comfinish[1:0] SO23comfinish[1:0]	RO/LH	00	Signal generation initiated by comtype has finished
	5:4	SIsigValid[1:0] SO01sigValid[1:0] SO23sigValid[1:0]	RO/LH	00	Valid signal received on lane
	3:2	SICOMWAKE[1:0] SO01COMWAKE[1:0] SO23COMWAKE[1:0]	RO/LH	00	COMWAKE Sequence received on lane
	1:0	SICOMINIT[1:0] SO01COMINIT[1:0] SO23COMINIT[1:0]	RO/LH	00	COMINIT Sequence received on lane
1.0088 2.0088 3.0088	7:6	Reserved	RO	-	Reserved
	5:4	SIRXErr[1:0] SO01RXErr[1:0] SO23RXErr[1:0]	RO/LH	00	PRBS error on lane. Self clearing
	3:2	SIrcvAbsent[1:0] SO01rcvAbsent[1:0] SO23rcvAbsent[1:0]	RO/LH	00	No Receiver present on lane
	1:0	SIrcvPresent[1:0] SO01rcvPresent[1:0] SO23rcvPresent[1:0]	RO/LH	00	Receiver detected on lane

5.3 XRS10L140 Device Generic Registers

This section outlines generic registers relating to the XRS10L140 as a whole. These registers are accessed through MDIO device 0.

TABLE 14: RESET CONTROL SIGNALS

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
0.0000	7:2	Reserved	RO	-	Reserved
	1	simflag	RW	0	speed up flag for simulation only
	0	rseqstart	RW/SC	0	setting starts up reset controller. Self clear-ing
0.0003 0.0002	7:0	override_reg[15:0]	RW	0x00 0x00	Override register for resets [15] – ebables all overrides [14:9] spares [8] – rcal reset [7] – device macro1 [6] – device macro0 [5] – selector and multiplier [4] – device gasket 1 [3] – device gasket 0 [2] – host gasket [1] – host macro [0] – rcal enable
0.0004	3:0	resetPLLB_reg[3:0]	RW	0xf	Resets the PLL portion of the macros.
0.0005	7:0	resetDB_reg[7:0]	RW	0xff	Resets the digital portion of the macros 0 = reset the part 1 = normal operation
0.0006	7:0	resetCDRB_reg[7:0]	RW	0xff	Resets the CDR portion of the macros.
0.0011 0.0010	7:0	rcon_controlwords0[15:0]	RW	0x02 0x00	reset controller microwords
0.0013 0.0012	7:0	rcon_controlwords1[15:0]	RW	0x00 0x04	reset controller microwords
0.0015 0.0014	7:0	rcon_controlwords2[15:0]	RW	0x00 0x53	reset controller microwords
0.0017 0.0016	7:0	rcon_controlwords3[15:0]	RW	0x02 0x40	reset controller microwords
0.0019 0.0018	7:0	rcon_controlwords4[15:0]	RW	0x00 0x80	reset controller microwords
0.001B 0.001A	7:0	rcon_controlwords5[15:0]	RW	0x01 0x40	reset controller microwords
0.001D 0.001C	7:0	rcon_controlwords6[15:0]	RW	0x00 0xc0	reset controller microwords
0.001F 0.001E	7:0	rcon_controlwords7[15:0]	RW	0x01 0x20	reset controller microwords
0.0021 0.0020	7:0	rcon_controlwords8[15:0]	RW	0x00 0x00	reset controller microwords

TABLE 14: RESET CONTROL SIGNALS

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
0.0023 0.0022	7:0	rcon_controlwords9[15:0]	RW	0x00 0x00	reset controller microwords
0.0025 0.0024	7:0	rcon_controlwordsA[15:0]	RW	0x00 0x00	reset controller microwords
0.0027 0.0026	7:0	rcon_controlwordsB[15:0]	RW	0x00 0x00	reset controller microwords

TABLE 15: SATA PORT MULTIPLIER REGISTERS

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
0.0080	7	p_rx_areset_h	RW	0	Programmable auto reset for transmit elastic fifo (Host link layer) 1 = reset fifo when full or empty 0 = otherwise
	6	p_rx_ra_disable_h	RW	0	Programmable rate adjust disable for receive elastic fifo (Host link layer) 1 = disable 0 = enable
	5	p_tx_feclr_h	RW	0	programmable fifo error clear for transmit elastic fifo (Host link layer) 1 = clear sticky error 0 = otherwise
	4	p_tx_areset_h	RW	0	Programmable auto reset for transmit elastic fifo (Host link layer) 1 = reset fifo when full or empty 0 = otherwise
	3	p_tx_ra_disable_h	RW	0	Programmable rate adjust disable for transmit elastic fifo 1 = disable 0 = enable
	2:1	p_devport_sel[1:0]	RW	00	device port select for FIS routing in test mode
	0	p_test_mode	RW	0	1 = port multiplier in test mode 0 = otherwise

TABLE 15: SATA PORT MULTIPLIER REGISTERS

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
0.0081	7	p_rx_areset_d0	RW	0	Programmable auto reset for transmit elastic fifo (Device 0 link layer) 1 = reset fifo when full or empty 0 = otherwise
	6	p_rx_ra_disable_d0	RW	0	Programmable rate adjust disable for receive elastic fifo (Device 0 link layer) 1 = disable 0 = enable
	5	p_tx_feclr_d0	RW	0	Programmable fifo error clear for transmit elastic fifo (Device 0 link layer) 1 = clear sticky error 0 = otherwise
	4	p_tx_areset_d0	RW	0	Programmable auto reset for transmit elastic fifo (Device 0 link layer) 1 = reset fifo when full or empty 0 = otherwise
	3	p_tx_ra_disable_d0	RW	0	Programmable rate adjust disable for transmit elastic fifo 1 = disable 0 = enable
	2	p_as_mon_h	RW	0	Control bit that 1:monitors for unaligned Dword primitives (Host link layer) 0 = otherwise
	1	p_sd_disable_h	RW	0	Programmable scrambler/de-scrambler disable (Host link layer) 1 = disable 0 = enable
	0	p_rx_feclr_h	RW	0	Programmable fifo error clear for transmit elastic fifo (Host link layer) 1 = clear sticky error 0 = otherwise

TABLE 15: SATA PORT MULTIPLIER REGISTERS

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
0.0082	7	p_rx_areset_d1	RW	0	Programmable auto reset for transmit elastic fifo (Device 1 link layer) 1 = reset fifo when full or empty 0 = otherwise
	6	p_rx_ra_disable_d1	RW	0	Programmable rate adjust disable for receive elastic fifo (Device 1 link layer) 1 = disable 0 = enable
	5	p_tx_feclr_d1	RW	0	Programmable fifo error clear for transmit elastic fifo (Device 1 link layer) 1 = clear sticky error 0 = otherwise
	4	p_tx_areset_d1	RW	0	Programmable auto reset for transmit elastic fifo (Device 1 link layer) 1 = reset fifo when full or empty 0 = otherwise
	3	p_tx_ra_disable_d1	RW	0	Programmable rate adjust disable for transmit elastic fifo (Device 1 link layer) 1 = disable 0 = enable
	2	p_as_mon_d0	RW	1	Control bit that 1 = monitors for unaligned Dword primitives (Device 0 link layer) 0 = otherwise
	1	p_sd_disable_d0	RW	0	Programmable scrambler/de-scrambler disable (Device 0 link layer) 1 = disable 0 = enable
	0	p_rx_feclr_d0	RW	0	Programmable fifo error clear for transmit elastic fifo (Device 0 link layer) 1 = clear sticky error 0 = otherwise

TABLE 15: SATA PORT MULTIPLIER REGISTERS

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
0.0083	7	p_rx_areset_d2	RW	0	Programmable auto reset for transmit elastic fifo (Device 2 link layer) 1 = reset fifo when full or empty 0 = otherwise
	6	p_rx_ra_disable_d2	RW	0	Programmable rate adjust disable for receive elastic fifo (Device 2 link layer) 1 = disable 0 = enable
	5	p_tx_feclr_d2	RW	0	Programmable fifo error clear for transmit elastic fifo (Device 2 link layer) 1 = clear sticky error 0 = otherwise
	4	p_tx_areset_d2	RW	0	Programmable auto reset for transmit elastic fifo (Device 2 link layer) 1 = reset fifo when full or empty 0 = otherwise
	3	p_tx_ra_disable_d2	RW	0	Programmable rate adjust disable for transmit elastic fifo (Device 2 link layer) 1 = disable 0 = enable
	2	p_as_mon_d1	RW	1	Control bit that 1 = monitors for unaligned Dword primitives (Device 1 link layer) 0 = otherwise
	1	p_sd_disable_d1	RW	0	Programmable scrambler/de-scrambler disable (Device 1 link layer) 1 = disable 0 = enable
	0	p_rx_feclr_d1	RW	0	Programmable fifo error clear for transmit elastic fifo (Device 1 link layer) 1 = clear sticky error 0 = otherwise

TABLE 15: SATA PORT MULTIPLIER REGISTERS

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
0.0084	7	p_rx_areset_d3	RW	0	Programmable auto reset for transmit elastic fifo (Device 3 link layer) 1 = reset fifo when full or empty 0 = otherwise
	6	p_rx_ra_disable_d3	RW	0	Programmable auto reset for transmit elastic fifo (Device 3 link layer) 1 = reset fifo when full or empty 0 = otherwise
	5	p_tx_feclr_d3	RW	0	Programmable fifo error clear for transmit elastic fifo (Device 3 link layer) 1 = clear sticky error 0 = otherwise
	4	p_tx_areset_d3	RW	0	Programmable auto reset for transmit elastic fifo (Device 3 link layer) 1 = reset fifo when full or empty 0 = otherwise
	3	p_tx_ra_disable_d3	RW	0	Programmable rate adjust disable for transmit elastic fifo (Device 3 link layer) 1 = disable 0 = enable
	2	p_as_mon_d2	RW	1	Control bit that 1 = monitors for unaligned Dword primitives (Device 2 link layer) 0 = otherwise
	1	p_sd_disable_d2	RW	0	Programmable scrambler/de-scrambler disable (Device 2 link layer) 1 = disable 0 = enable
	0	p_rx_feclr_d2	RW	0	Programmable fifo error clear for transmit elastic fifo (Device 2 link layer) 1 = clear sticky error 0 = otherwise

TABLE 15: SATA PORT MULTIPLIER REGISTERS

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
0.0085	7:4	Reserved	RO	-	Reserved
	3	p_dvc_prt_en	RW	0	1 = enable all port multiplier ports on reset 0 = otherwise
	2	p_as_mon_d3	RW	1	Control bit that 1 = monitors for unaligned Dword primitives (Device 3 link layer) 0 = otherwise
	1	p_sd_disable_d3	RW	0	Programmable scrambler/de-scrambler disable (Device 3 link layer) 1 = disable 0 = enable
	0	p_rx_feclr_d3	RW	0	Programmable fifo error clear for transmit elastic fifo (Device 3 link layer) 1 = clear sticky error 0 = otherwise
0.0086	7:6	Reserved	RO	-	Reserved
	5:3	p_dvc1_wght[2:0]	RW	000	Device port 1 weight for weighted-round robin arbitration Valid values 1-7
	2:0	p_dvc0_wght[2:0]	RW	000	Device port 0 weight for weighted-round robin arbitration Valid values 1-7
0.0087	7:6	Reserved	RO	-	Reserved
	5:3	p_dvc3_wght[2:0]	RW	000	Device port 3 weight for weighted-round robin arbitration Valid values 1-7
	2:0	p_dvc2_wght[2:0]	RW	000	Device port 2 weight for weighted-round robin arbitration Valid values 1-7
0.0088	7:0	p_intvl_val[7:0]	RW	0xB7	programmable communication interval value for hot plug FSM Interval is 27.3us * count
0.0089	7	Reserved	RO	-	Reserved
	6:3	p_msb_rscnt[3:0]	RW	1000	The 4 MSB's of the 20 bit timeout value used to decide how long the PM should wait before issuing a restart
	2	p_dlock_err_clr	RW	0	1 = clear the stick deadlock error indicator 0 = otherwise
	1	p_restart_pm_en	RW	1	1 = port multiplier will restart if it enters deadlock 0 = otherwise
	0	p_pwrmng_on	RW	1	1 = power management turned on in port 0 = power management turned off in port
0.0090	7	Reserved	RO	-	Reserved
	6:4	p_col_ad[2:0]	RW	000	Col address of the SRAM in test mode
	3:0	p_row_ad[11:0]	RW	0x00	Row address of the SRAM in test mode

TABLE 15: SATA PORT MULTIPLIER REGISTERS

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
0.0091	7:0	p_row_ad[11:0]	RW	0x00	Row address of the SRAM in test mode
0.0092	7:0	p_wdata[7:0]	RW	0x00	Write data for the sram in test mode
0.0093	7:0	p_rdata[7:0]	RO	0x00	Read data from the sram in test mode
0.0094	7:2	Reserved	RO	-	Reserved
	1	p_wr_en	RW	0	1 = write op 0 = read op
	0	p_wr_toggle	RW	0	initiates an sram op
0.0095	7	o_rx_ferr_d2	RO	0	Observable receive elastic fifo sticky error (full or empty) (Device 2 link layer) 1 = error 0 = no error
	6	o_tx_ferr_d2	RO	0	Observable transmit elastic fifo sticky error (full or empty) (Device 2 link layer) 1 = error 0 = no error
	5	o_rx_ferr_d1	RO	0	Observable receive elastic fifo sticky error (full or empty) (Device 1 link layer) 1 = error 0 = no error
	4	o_tx_ferr_d1	RO	0	Observable transmit elastic fifo sticky error (full or empty) (Device 1 link layer) 1 = error 0 = no error
	3	o_rx_ferr_d0	RO	0	Observable receive elastic fifo sticky error (full or empty) (Device 0 link layer) 1 = error 0 = no error
	2	o_tx_ferr_d0	RO	0	Observable transmit elastic fifo sticky error (full or empty)(Device 0 link layer) 1 = error 0 = no error
	1	o_rx_ferr_h	RO	0	Observable receive elastic fifo sticky error (full or empty) (Host link layer) 1 = error 0 = no error
	0	o_tx_ferr_h	RO	0	Observable transmit elastic fifo sticky error (full or empty)(Host link layer) 1 = error 0 = no error

TABLE 15: SATA PORT MULTIPLIER REGISTERS

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
0.0096	7	o_dlock_err	RO	0	1 = a PM deadlock occurred 0 = otherwise
	6	spdmode_d3	RO	0	SPD mode signal from phy 3 1 = 3Gb/s mode 0 = 1.5Gb/s mode
	5	spdmode_d2	RO	0	SPD mode signal from phy 2 1 = 3Gb/s mode 0 = 1.5Gb/s mode
	4	spdmode_d1	RO	0	SPD mode signal from phy 1 1 = 3Gb/s mode 0 = 1.5Gb/s mode
	3	spdmode_d0	RO	0	SPD mode signal from phy 0 1 = 3Gb/s mode 0 = 1.5Gb/s mode
	2	pm_ssc_tx_en	RO	0	Dynamic SSC transmit enable signal
	1	o_rx_ferr_d3	RO	0	Observable receive elastic fifo sticky error (full or empty) (Device 3 link layer) 1 = error 0 = no error
	0	o_tx_ferr_d3	RO	0	Observable transmit elastic fifo sticky error (full or empty) (Device 3 link layer) 1 = error 0 = no error
0.0097	7:6	max_spd_to_dp3[1:0]	RO	00	SPD field from the dev 3 SCControl reg
	5:4	max_spd_to_dp2[1:0]	RO	00	SPD field from the dev 2 SCControl reg
	3:2	max_spd_to_dp1[1:0]	RO	00	SPD field from the dev 1 SCControl reg
	1:0	max_spd_to_dp0[1:0]	RO	00	SPD field from the dev 0 SCControl reg
0.0098	7:0	p_vct_fis_size[11:0]	RW	0x06	Programmable FIS size when VCT kicks in
0.0099	7	p_vct_en	RW	1	Enable for virtual cut-through
	6:4	p_vct_emp_wmark[2:0]	RW	0x3	Progammable watermark for VCT read from SRAM
	3:0	p_vct_fis_size[11:0]	RW	0x0	Programmable FIS size when VCT kicks in
0.009C	7:0	p_err_thres[14:0]	RW	0x00	Threshold for high error rate from port multiplier
0.009D	7	p_err_thres_en	RW	0	Enable for error counting
	6:0	p_err_thres[14:0]	RW	0x00	Threshold for high error rate from port multiplier

TABLE 16: SATA PORT SELECTOR REGISTERS

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
0.009A	7:6	Reserved	RO	-	Reserved
	5	p_nopass_cominit	RW	0	1 = do not pass 1st cominit 0 = pass 1st cominit from device(s) to host
	4	p_lcs_spd_sel	RW	0	1 = don't mix speeds; use the slowest 0 = mix speeds based on device abilities
	3	p_test_mode_sel	RW	0	1 = port selector in test mode 0 = port selector in normal mode
	2	p_host_sel	RW	0	Side band port selection 1 = Select Host port 2 0 = Select Host port 1
	1	p_side_mthd	RW	0	1 = p_host_sel based sideband selection 0 = external pin based sideband selection
	0	p_sel_mthd	RW	0	1 = Side-band port selection 0 = protocol based port selection

TABLE 17: CLOCK CONFIGURATION REGISTER

ADDRESS HEX	BIT(S)	NAME	RW	RESET VALUE	DESCRIPTION
0.0001	7:3	Reserved	RO	-	Reserved
	2	refClkSel	RW	0	1 = select CMU_REF 0 = select on chip crystal oscillator
	1	pwrdnRefClk	RW	0	Powers down reference clock
	0				
0.009B	7:4	Reserved	RO	-	Reserved
	3:1	clkMacroTestSel[2:0]	RW	000	000 = disabled 001 = Sata Output Macro 2 -->ClkTestIn<0> 010 = Sata Output Macro 0 -->ClkTestIn<1> 011 = Sata Input Macro -->ClkTestIn<2> 100 = Reserved 101 = SysClkBotLeft -->ClkTestIn<4> 110 = PLL Output -->ClkTestIn<5> 111 = PLL Test Clock -->ClkTestIn<6>
	0	clkTestEn	RW	0	0 = disable clock test output buffer 1 = enable clock test output buffer

6.0 FEATURES AND BENEFITS

TABLE 18: FEATURES AND BENEFITS

DISTINGUISHING FEATURE	COMPETITIVE ADVANTAGE	SYSTEM BENEFIT
Support for 3.0 Gbps and 1.5 Gbps	Backwards Compatibility to SATA Gen. 1	Can be used with both SATA Gen. 1 and Gen. 2 drives
Equalization and pre-emphasis on the receive front end	Superior analog front end. Very high signal integrity. Meets - • SATA Gen2i, Gen2x	Enables - • Longer distances on the copper/FR-4 • Improved signal integrity
Programmable Output Swing	Optimizes Power Consumption	Provides compliance to both SAS and SATA systems
Speed Negotiation	Locks to 3/1.5G SATA data without any external components.	Reduces system complexity and software effort to implement auto rate adaptation.
Fast Locking & Low Latency	Locks to incoming data with in 300 data edges. Latency is <25 clock cycles.	Enhances the overall system performance.
Built in Self Test.	Includes a PRBS generator and checker for self testing. PRBS patterns of 2^10-1, 2^23-1, and 2^31-1 are all available.	Makes testing of the storage sub-systems easier.
2 Wire MDIO Bus	Control and monitoring features are managed through a comprehensive register set instead of multiple pins.	Minimizes board space and system cost.
Power down modes	Supports the following modes of operation: • Active Mode - 90 mW • Partial Mode - <37.5 mW • Slumber Mode - <5 mW • Power down mode < 0.5mW	Provides full support of power management commands from the connected hosts and devices. Fully complies with the Serial ATA II port multiplier specification.
Spread Spectrum Clocking	Full support for receipt and generation of signals that have been configured for Spread Spectrum Clocking (SSC) support.	Reduces EMI to Enable FCC Compliance
Test and Loopback modes	Supports two forms of host loopback modes: and two forms of device-side loopback modes	Provide full testability in a system configuration.
Register Compatibility with ATA	Compliant with Legacy ATA Systems	Reduces software effort.
Low Power Consumption (1 Watt)	No need of heat sink or airflow.	Minimizes System Costs.

PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRS10L140	100 Pin QFP	-40°C to +85°C

REVISIONS

REV #	DATE	DESCRIPTION OF CHANGES
P1.0.0	March 2006	Initial Issue
P1.0.1	March 2006	New Logo, changed package designation from QFN to QFP
P1.0.2	June 2006	Added pin list and register information

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