2 - CHANNEL DS3/E3 ATM UNI/PPP COMBO IC

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HARDWARE MANUAL

The XRT79L72 is a two channel, ATM UNI/PPP Physical Layer Processor with integrated DS3/E3 framing controllers and Line Interface Units with Jitter Attenuators that are designed to support ATM direct mapping and cell delineation as well as PPP mapping and Frame processing. For ATM UNI applications, this device provides the ATM Physical Layer (Physical Medium Dependent and Transmission Convergence sub-layers) interface for the public and private networks at DS3/E3 rates. For Clear-Channel Framer applications, this device supports the transmission and reception of "user data" via the DS3/E3 payload.

The XRT79L72 includes DS3/E3 Framing, Line Interface Unit with Jitter Attenuator that supports mapping of ATM or HDLC framed data. A flexible parallel microprocessor interface is provided for configuration and control. Industry standard UTOPIA II and POS-PHY interface are also provided.

GENERAL FEATURES:

- Integrated T3/E3 Line Interface Unit
- Integrated Jitter Attenuator that can be selected either in Receive or Transmit path
- Flexible integrated Clock Multiplier that takes single frequency clock and generates either DS3 or E3 frequency.
- 8/16 bit UTOPIA Level I and II and PPP Multi-PHY Interface operating at 25, 33 or 50 MHz.
- HDLC Controller that provides the mapping/extraction of either bit or byte mapped encapsulated packet from DS3/E3 Frame.
- Contains on-chip 16 cell FIFO (configurable in depths of 4, 8, 12 or 16 cells), in both the Transmit (TxFIFO) and Receive Directions (RxFIFO)
- Contains on-chip 54 byte Transmit and Receive OAM Cell Buffer for transmission, reception and processing of OAM Cells
- Supports ATM cell or PPP Packet Mapping
- Supports M13 and C-Bit Parity Framing Formats
- Supports DS3/E3 Clear-Channel Framing.
- Includes PRBS Generator and Receiver
- Supports Line, Cell, and PLCP Loop-backs
- Interfaces to 8 Bit wide Intel, Motorola or PowerPC
- Low power 3.3V, 5V Input Tolerant, CMOS
- Available in 456 Lead PBGA Package
- JTAG Interface

LINE INTERFACE UNIT

- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Meets E3/DS3 Jitter Tolerance Requirements
- Detects and Clears LOS as per G.775.
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards
- Meets ETSI TBR 24 and GR-499 Jitter Transfer Requirements
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock
- On chip advanced crystal-less Jitter Attenuator
- Jitter Attenuator can be selected in Receive or Transmit paths
- 16 or 32 bits selectable FIFO size
- Meets the Jitter and Wander specifications described in T1.105.03b,ETSI TBR-24, Bellcore GR-253 and GR-499 standards
- Jitter Attenuator can be disabled
- Maximum power consumption 1.7W

DS3/E3 FRAMER

- DS3 framer supports both M13 and C-bit parity.
- DS3 framer meets ANSI T1.107 and T1.404 standards.
- Detects OOF,LOF,AIS,RDI/FERF alarms.
- Generation and Insertion of FEBE on received parity errors supported.
- Automatic insertion of RDI/FERF on alarm status.
- E3 framer meets G.832,G.751 standards.
- Framers can be bypassed.

ATM/PPP PROTOCOL PROCESSOR

TRANSMIT CELL PROCESSING

- Extracts ATM cells
- Supports ATM cell payload scrambling
- Maps ATM cells into E3 or DS3 frame
- PLCP frame and mapping of ATM cell streams

RECEIVE CELL PROCESSING

- Extraction of ATM cells from PLCP frame or directly from E3 or DS3 frame
- Termination of PLCP frame
- Supports payload cell de-scrambling

TRANSMIT PACKET PROCESSING

- Inserts PPP packets into data stream
- Maps HDLC data stream directly into DS3 or E3 frame
- Extracts in-band messaging packets
- Supports CRC-16/32, HDLC flag and Idle sequence generation

RECEIVE PACKET PROCESSING

- Extracts HDLC data stream from DS3 or E3 frame
- Inserts in-band messaging packets
- Detects and removes HDLC flags

UTOPIA/ SYSTEM INTERFACE

- 8/16 bit UTOPIA Level I and II and PPP Multi-PHY Interface operating at 25, 33 or 50 MHz.
- Compliant with ATM Forum UTOPIA II interface
- Programmable FIFO size for both Transmit and Receive direction
- Compliant to POS-PHY Level 2 interface

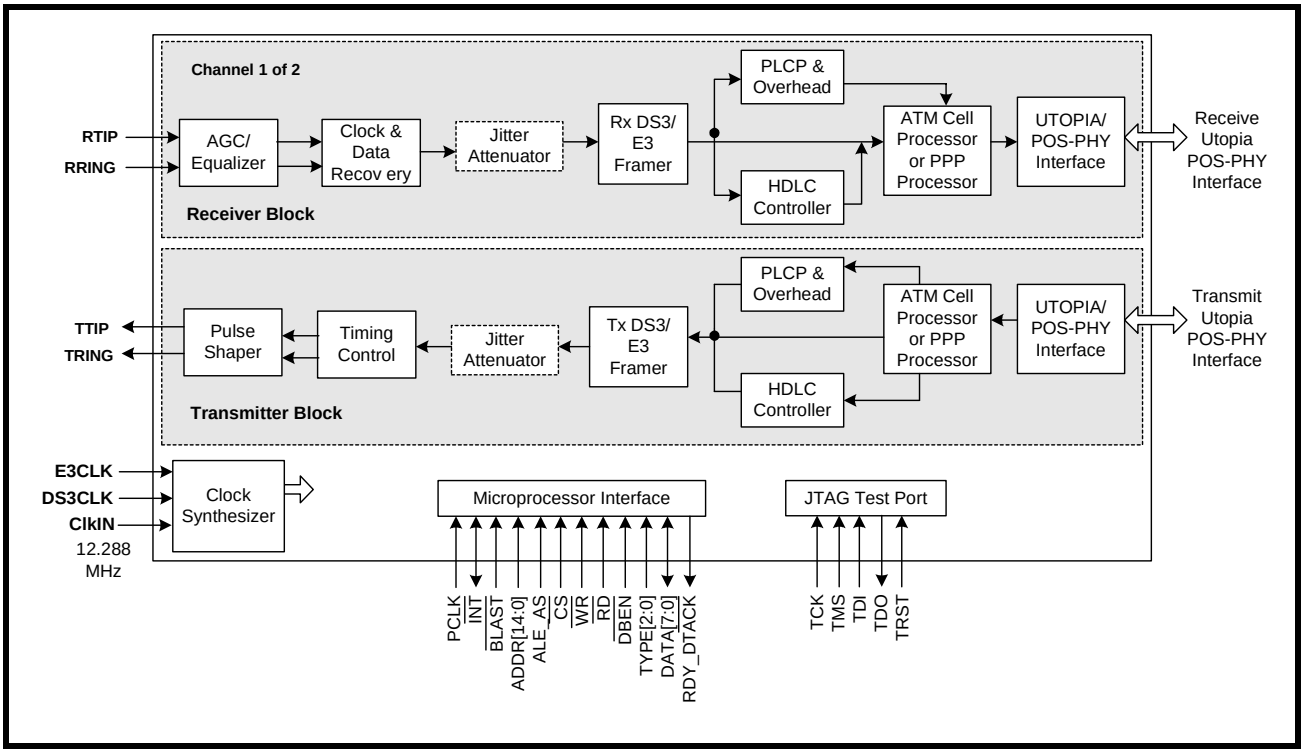
SERIAL INTERFACE

- Serial clock and data interface for accessing DS3/E3 framer
- Serial clock and data interface for accessing cell/packet processor

APPLICATIONS

- Digital Access and Cross Connect Systems
- 3G Base Stations
- DSLAMs
- Digital, ATM, WAN and LAN Switches

FIGURE 1. BLOCK DIAGRAM OF THE XRT79L72



PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT79L72IB	456 Lead PBGA	-40°C to +85°C

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PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
MICROPROCESSOR INTERFACE			
AB26 AC26 AD26 AB25 AA24 AD25 AC25 AB24 AF25 AE25 AF24 AE24 AD24 AC24 AF23	A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14	I	**Address Bus Input pins Microprocessor Interface:** These input pins permit the Microprocessor to identify on-chip registers and Buffer/ Memory locations (within the XRT79L72 device) whenever it performs READ and WRITE operations with the XRT79L71 device.
R22 T24 T25 T26 U22 U23 U24 U25	D0 D1 D2 D3 D4 D5 D6 D7	I/O	**Bi-Directional Data Bus pins Microprocessor Interface:** These pins are used to drive and receive data over the bi-directional data bus.
AB23	ALE/AS	I	**Address Latch Enable/Address Strobe:** This input pin is used to latch the address present at the Microprocessor Interface Address Bus pins A[14:0] into the Framer/UNI Microprocessor Interface block and to indicate the start of a READ or WRITE cycle. This input pin is active high, in the Intel Mode and active low in the Motorola Mode.
AE23	$\overline{CS}$	I	**Chip Select Input:** The user must assert this active low signal in order to select the Microprocessor Interface for READ and WRITE operations between the Microprocessor and the UNI/ Framer on-chip registers and RAM locations.
R23	$\overline{INT}$	O	**Interrupt Request Output:** This open-drain, active-low output signal will be asserted when the Framer/UNI device is requesting interrupt service from the Microprocessor. This output pin should typically be connected to the Interrupt Request input of the Microprocessor.
AD23	$\overline{RD}/\overline{DS}$	I	**READ Strobe Intel Mode:** If the Microprocessor Interface is operating in the Intel Mode, then this input pin will function as the $\overline{RD}$ (READ Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the Framer/UNI will place the contents of the addressed register within the Framer/UNI IC on the Microprocessor Bi-directional Data Bus D[7:0]. When this signal is negated, the Data Bus will be tri-stated. **Data Strobe Motorola Mode:** If the Microprocessor Interface is operating in the Motorola Mode, then this input will function as the $\overline{DS}$ (Data Strobe) signal.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
U26	RDY/$\overline{\text{DTACK}}$	O	**READY or DTACK:** This active-low output pin will function as the READY output when the Microprocessor Interface is configured to operate in the Intel Mode; and will function as the DTACK output when the Microprocessor Interface is running in the Motorola Mode. **Intel Mode - READY output:** When the Framer/UNI negates this output pin (e.g., toggles it "Low") it indicates to the Microprocessor that the current READ or WRITE operation is to be extended until this signal is asserted (e.g., toggled "High"). **Motorola Mode - DTACK Data Transfer Acknowledge Output:** The Framer/UNI will assert this pin in order to inform the Microprocessor that the present READ or WRITE cycle is nearly complete. If the Framer/UNI requires that the current READ or WRITE cycle be extended, then the Framer/UNI will delay its assertion of this signal. The 68000 family of Microprocessors requires this signal from its peripheral devices, in order to quickly and properly complete a READ or WRITE cycle.
AF4	$\overline{\text{RESET}}$	I	**Reset Input:** When this active-low signal is asserted, the Framer/UNI device will be asynchronously reset. When this occurs, all outputs will be tri-stated and all on-chip registers will be reset to their default values.
AA26	µPCLK	I	**Microprocessor Interface Clock Input:** This clock input signal is used for synchronous/burst/DMA data transfer operations. This clock can be running up to 33MHz.
AC23	$\overline{\text{WR}}$/R/$\overline{\text{W}}$	I	**Write Strobe Intel Mode:** If the Microprocessor Interface is configured to operate in the Intel Mode, then this active-low input pin functions as the WR (WRITE Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, the Framer/UNI will latch the contents of the bi-directional data D[7:0] into the addressed registers or Buffer location within the Framer/UNI IC. **R/W Input Pin Motorola Mode:** When the Microprocessor Interface Section is operating in the Motorola Mode, then this pin is functionally equivalent to the R/$\overline{\text{W}}$ pin. In the Motorola Mode, a READ operation occurs if this pin is at a logic "1". Similarly a WRITE operation occurs if this pin is at a logic "0".
AB22 AC22 AD22	PTYPE_0 PTYPE_1 PTYPE_2	I	**Microprocessor Type Select input:** These three input pins are used to configure the Microprocessor Interface block to readily support a wide variety of Microprocessor Interfaces. The relationship between the settings of these input pins and the corresponding Microprocessor Interface configuration is presented below. "000" = Intel Asynchronous Mode "001" = Motorola Asynchronous Mode "111" = Power PC Mode
AF22	$\overline{\text{DBEN}}$	I	**Bi-directional Data Bus Enable Input pin:** If the Microprocessor Interface is operating in the Intel-I960 Mode, then this input pin is used to enable the Bi-directional Data Bus. Setting this input pin "Low" enables the Bi-directional Data bus. Setting this input "High" tri-states the Bi-directional Data Bus.

PIN #	NAME	TYPE	DESCRIPTION
TEST AND DIAGNOSTIC			
AD5	TCK	I	**Test Clock input, Boundary Scan Clock input:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
AC5	TDI	I	**Test Data input, Boundary Scan Test Data Input:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
AB5	TDO	O	**Test Data output:** Boundary Scan Test Data Output:
AE5	TMS	I	**Test Mode Select, Boundary Scan Test Mode Select input pin:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
AF5	TRST	I	**Test Mode Reset, Boundary Scan Mode Reset Input pin:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
AD4	TESTMODE	***	**Factory Test Mode Pin:** Tie this pin to Ground.
AC17 AC13	Anaio1 Anaio0	I/O	**Analog Input/Output Test Pin:** These pins should be pulled "Low" for normal operation.

PIN #	NAME	TYPE	DESCRIPTION
GENERAL PURPOSE INPUT AND OUTPUT PINS			
U3 N26	DMO_0 DMO_1	O O	**Drive Monitor Output Pins:** For each channel, if the DMO output signal is "High", then it means that the drive monitor circuitry within the XRT79L72 has not detected any bipolar signals at the MTIP and MRING inputs (or via the Internal Drive Monitor circuit) within the last 128 ± 32 bit periods. If this output signal is "Low", then it means that bipolar signals are being detected at the MTIP and MRING input pins of the XRT79L72.
W1 W2 W3 W4	GPIO_0 GPIO_1 GPIO_2 GPIO_3	I/O	**General Purpose Input/Output Pins:** Each of these pins can be configured to function as either a general-purpose input or output pin. If a given pin (GPIO_X) is configured to function as an input pin, then the state of this input pin can be monitored by reading Bit X within the "Operation General Purpose Pin Data" Register (Address Location = 0x0147). If a given pin is configured to function as an output pin, then the state of this output pin (GPIO_X) can be controlled by writing the appropriate value into Bit X within the "Operation General Purpose Pin Data" Register. Finally, the user can configure a given GPIO_X pin to be an input pin by setting Bit X, within the "Operation General Purpose Pin Direction Control Register (Address = 0x014B) to "0". Conversely, the user can configure the GPIO_X pin to be an output pin by setting Bit X, within the "Operation General Purpose Pin Direction Control" Register (Address = 0x014B) to "1".

PIN #	NAME	TYPE	DESCRIPTION
TRANSMIT SYSTEM SIDE INTERFACE PINS			
AC4	NibbleIntf	I	**Nibble Interface Select Input pin:** This input pin permits the user to configure the Transmit Payload Data Input Interface and the Receive Payload Data Output Interface blocks to operate in either the "Serial" or the "Nibble-Parallel" Mode. Setting this input pin "high" configures each of these blocks to operate in the Nibble-Parallel Mode. In this mode, the "Transmit Payload Data Input Interface" block will accept the "outbound" payload data (from the System-Side terminal equipment) in a "nibble-parallel" manner via the "TxNib[3:0]" input pins. Further, the Receive Payload Data Output Interface block will output "inbound" payload data (to the System-Side terminal equipment) in a "nibble-parallel" via the "RxNib[3:0] output pins. Setting this input pin "low" configures each of these blocks to operate in the Serial Mode. In this mode, the Transmit Payload Data Input Interface block will accept the "outbound" payload data (from the System-Side terminal equipment) in a "serial" manner via the "TxSer" input pin. Further, the Receive Payload Data Output Interface block will output the "inbound" payload data (to the System-Side terminal equipment) in a serial manner, via the "RxSer" output pin.NOTE: ***NOTE:*** *This input pin is only active if the XRT79L72 device has been configured to operate in the Clear-Channel Framer Mode. The user is advised to tie this input pin to GND if the user intends to configure the XRT79L72 device to operate in the ATM UNI or PPP Modes.*

PIN #	NAME	TYPE	DESCRIPTION
U5 N24	TxFrame_0 TxFrame_1	O O	**Transmit End of DS3/E3 Frame Indicator:** These output pins will pulse "High" for one DS3 or E3 clock period, when the Transmit Section of the XRT79L72 is processing the last bit of a given DS3 or E3 frame. The implications of these output pins, for each mode of operation, are described below. **ATM UNI/PPP/High-Speed HDLC Controller Mode:** These output pins serve as an end-of-frame indication to the local terminal equipment. **Clear-Channel Framer Mode:** If the XRT79L72 is configured to operate in the Clear-Channel Framer mode, then these output pins serve to alert the Local Terminal Equipment that it needs to begin transmission of a new DS3 or E3 frame. Hence, the Local Terminal Equipment uses these output signals to maintain Framing Alignment with the XRT79L72.
AF1 W25	TxFrameRef_0 TxFrameRef_1	I I	**Transmit DS3/E3 Framer - Framing Alignment Input pin:** If the the Transmit Section of the XRT79L72 is configured to operate in the Local-Timing/Frame-Slave Mode, then the Transmit DS3/E3 Framer block will use these input signals as the Framing Reference. When the XRT79L72 is configured to operate in this mode any rising edge at these input pins will cause the Transmit DS3/E3 Framer block to begin its creation of a new DS3 or E3 frame. Consequently, the user must supply a clock signal that is equivalent to the DS3 or E3 frame rates to these input pins. Further, it is imperative that this clock signal be synchronized with the 44.736MHz or 34.368MHz clock signal applied to the TxInClk input pins. ***NOTE:*** *These input pins should be tied to GND if they are not to be used as the Transmit DS3/E3 Framer - Framing Reference input signals.*
U4 N25	TxInClk_0 TxInClk_1	I I	**Transmit DS3/E3 Framer Block - Timing Reference Signal:** If the Transmit Section of the XRT79L72 is configured to operate in the Local-Timing Mode, then it will use this signal as the Timing Reference. If the XRT79L72 is being operating in the DS3 Mode, then the user is expected to apply a high-quality 44.736MHz clock signal to these input pins. Likewise, if the XRT79L72 is being operated in the E3 Mode, then the user is expected to apply a high-quality 34.368MHz clock signal to these input pins. **A Note for Clear-Channel Framer Operation:** If the user is operating the XRT79L72 device in both the Clear-Channel Framer and Local-Timing modes, then the user should design or configure the System-Side terminal equipment circuitry, such that "outbound" DS3 or E3 data will be output, upon the falling edge of TxInClk. The Transmit Payload Data Input Interface (within the Transmit Section of the XRT79L72 device) will sample the data, applied to the "TxSer" input pin, upon the rising edge of TxInClk. ***NOTE:*** *This input pin should be tied to GND if the XRT79L72 device is configured to operate in the "Loop-Timing" Mode.*

PIN #	NAME	TYPE	DESCRIPTION
AD2 Y22	TxOH_0/ TxHDLCDat0_5 TxOH_1/ TxHDLCDat1_5	I I	**Transmit Overhead Data Input/Transmit HDLC Controller Data Bit 5 input pins:** The function of these input pins depend upon whether or not the XRT79L72 has been configured to operate in the High-Speed HDLC Controller Mode. **Non-High Speed HDLC Controller Mode - TxOH:** The Transmit Overhead Data Input Interface accepts overhead via these input pins, and insert this data into the overhead bit positions within the outbound DS3 or E3 frames. If the TxOHIns input pins are pulled "High", then the Transmit Overhead Data Input Interface will sample the overhead data, via these input pins, upon the falling edge of the TxOHClk output signals. Conversely, if the TxOHIns input pins are NOT pulled "High", then the Transmit Overhead Data Input Interface block will be inactive and will not accept any overhead data via the TxOH input pins. **High Speed HDLC Controller Mode - TxHDLCDat_5:** If the XRT79L72 is configured to operate in the High-Speed HDLC Controller mode, then the local terminal equipment will be provided with a byte-wide Transmit HDLC Controller byte-wide input interface. These input pins will function as Bit 5 within this byte wide interface. Data, residing on the Transmit HDLC Controller byte wide input interface, will be sampled upon the rising edge of the TxHDLCClk output signals.
AC2 W26	TxOHIns_0/ TxHDLCDat0_4 TxOHIns1/ TxHDLCDat1_4	I I	**Transmit Overhead Data Insert Input/Transmit HDLC Controller Data Bit 4 input pins:** The function of these input pins depend upon whether or not the XRT79L72 has been configured to operate in the High-Speed HDLC Controller Mode. **Non-High Speed HDLC Controller Mode - TxOHIns:** This input pins are used to either enable or disable the Transmit Overhead Data Input Interface block. If the Transmit Overhead Data Input Interface block is enabled, then it will accept overhead data from the local terminal equipment via the TxOH input pins; and insert this data into the overhead bit positions within the outbound DS3 or E3 data stream. Conversely, if the Transmit Overhead Data Input Interface block is disabled, then it will NOT accept overhead data from the local terminal equipment. Pulling these input pins "High" enables the Transmit Overhead Data Input Interface block. Pulling these input pins "Low" disables the Transmit Overhead Data Input Interface block. **High-Speed HDLC Controller Mode - TxHDLCDat_4:** If the XRT79L72 is configured to operate in the High-Speed HDLC Controller mode, then the local terminal equipment will be provided with a byte-wide Transmit HDLC Controller byte-wide input interface. These input pins will function as Bit 4 within this byte wide interface. Data, residing on the Transmit HDLC Controller byte wide input interface, will be sampled upon the rising edge of the TxHDLCClk output signals.
G3 A26	TxOHClk_0 TxOHClk_1	O O	**Transmit Overhead Clock Output:** These output pins functions as the Transmit Overhead Data Input Interface clock signals. If the user enables the Transmit Overhead Data Input Interface block by asserting the TxOHIns input pins, then the Transmit Overhead Data Input Interface block will sample and latch the data residing on the TxOH input pins upon the falling edge of these signals. ***NOTE:*** *The Transmit Overhead Data Input Interface block is disabled if the user has configured the XRT79L72 to operate in the High-Speed HDLC Controller Mode.*

PIN #	NAME	TYPE	DESCRIPTION
G2 D23	TxOHFrame_0/ TxHDLCClk_0 TxOHFrame_1/ TxHDLCClk_1	O O	**Transmit Overhead Framing Pulse/Transmit HDLC Controller Clock Output pin:** The function of these output pins depend upon whether or not the XRT79L72 has been configured to operate in the High-Speed HDLC Controller Mode. **Non-High-Speed HDLC Controller Mode - TxOHFrame:** These output pins pulse high for one TxOHClk period coincident with the instant the Transmit Overhead Data Input Interface would be accepting the first overhead bit within an outbound DS3 or E3 frame. **High Speed HDLC Controller Mode - TxHDLCClk:** This output pin functions as the "demand" clock output signal for the "Transmit HDLC Controller" byte-wide input interface. This clock signal is ultimately derived from either the TxInClk clock signal (for Local-Timing Applications) or the RxOutClk clock signal (for Loop-Timing Applications). Hence, the frequency of this clock signal is nominally one-eight of that of the TxInClk or the RxOutClk signals. The Transmit HDLC Controller block will sample the contents of the Transmit HDLC Controller byte-wide input interface, upon the rising edge of these clock output signals. Therefore, the local terminal equipment should be designed to output data onto the TxHDLCDatn_[7:0] bus upon the falling edge of these clock output signals.
R2 M24	TxOHEnable_0/ TxHDLCDat0_7 TxOHEnable_1/ TxHDLCDat0_2	I/O I/O	**Transmit Overhead Enable Output indicator/Transmit HDLC Controller Data Bit 7 Input:** The function of these input pins depend upon whether or not the XRT79L72 is configured to operate in the High Speed HDLC Controller Mode. **Non-High Speed HDLC Controller Mode - TxOHEnable:** The XRT79L72 will assert these output pins, for one TxInClk period, just prior to the instant that the Transmit Overhead Data Input Interface will be sampling and processing an overhead bit. If the local terminal equipment intends to insert its own value for an overhead bit, into the outbound DS3 or E3 data stream, then it is expected to sample the state of these signals, upon the falling edge of TxInClk. Upon sampling the TxOHEnable signal "High", the local terminal equipment should; (1) place the desired value of the overhead bit onto the TxOH input pin and (2) assert the TxOHIns input pin. The Transmit Overhead Data Input Interface block will sample and latch the data on the TxOH signal, upon the rising edge of the very next TxInClk input signal. **High-Speed HDLC Controller Mode - TxHDLCDat_7:** If the XRT79L72 is configured to operate in the High-Speed HDLC Controller mode, then the local terminal equipment will be provided with a byte-wide Transmit HDLC Controller byte-wide input interface. These input pins will function as Bit 7 (the MSB) within this byte wide interface. Data, residing on the Transmit HDLC Controller byte wide input interface, will be sampled upon the rising edge of the TxHDLCClk output signals.

PIN #	NAME	TYPE	DESCRIPTION
T3 M26	TxSer_0/ TxPOH_0/ SendMSG_0 TxSer_1/ TxPOH_1/ SendMSG_1	I I	**Transmit Payload Data Serial Input/Transmit PLCP Path Overhead Input/ Send HDLC Message Request Input:** The function of these input pins depend upon whether the XRT79L72 is configured to operate in the Clear-Channel Framer Mode, the High-Speed HDLC Controller Mode or in the ATM/PLCP Mode. **Clear-Channel Framer Mode - TxSer:** If the XRT79L72 is configured to operate in the Clear-Channel Framer mode, then these input pins function as the Transmit Payload Data Serial Input pins. In this case, the local terminal equipment is expected to apply all outbound data which is intended to be carried via the DS3 or E3 payload bits to these input pins. The Transmit Payload Data Input Interface will sample the data, residing at the TxSer input pin, upon the rising edge of TxInClk. **ATM/PLCP Mode - TxPOH:** If the XRT79L72 is configured to operate in the ATM Mode, and if within the ATM Mode, the chip is also configured to operate in the PLCP Mode, then these input pins function as the Transmit PLCP Path Overhead Input Pins. In this mode, the user can externally insert desired path overhead byte values into the outbound PLCP frames. The Transmit PLCP Path Overhead Input Pin (and Port) become active whenever the user asserts the TxPOHIns input pins by pulling them "High". In this case, the data, residing upon the TxPOH input pins will be sampled upon the rising edge of the TxPOHClk signals. ***NOTE:*** *These input pins are inactive if the XRT79L72 is configured to operate in the Direct-Mapped ATM Mode.* **High-Speed HDLC Controller Mode - SendMSG:** If the XRT79L72 is configured to operate in the High-Speed HDLC Controller Mode, then these input pins function as the Transmit HDLC Controller Input Interface enable input pin. If the user asserts these input pins by pulling them "High" then the Transmit HDLC Controller Input Interface will proceed to latch the data, residing on the TxHDLCDatn_[7:0] input pins, upon each rising edge of the TxHDLCClk signals. All data that is latched into the Transmit HDLC Controller Input Interface for the duration that the SendMSG input pin is "High" will be encapsulated into an HDLC frame and ultimately transported via the payload bits of the outbound DS3 or E3 data stream. If the user pulls these input pins "Low", then the Transmit HDLC Controller Input Interface will cease latching the data, residing on the TxHDLCDatn_[7:0] bus. ***NOTE:*** *These input pins are inactive if the XRT79L72 has been configured to operate in the PPP Mode.*
G1 C24	TxPOHFrame_0 TxPOHFrame_1	O O	**Transmit PLCP Frame Path Overhead Byte Serial Input Port - Beginning of Frame indicator:** These output pins, along with the TxPOH, TxPOHClk, and the TxPOHIns pins comprise the Transmit PLCP Frame POH Byte Insertion serial input port. These particular pins pulse "High" when the Transmit PLCP POH Byte Insertion serial input port is expecting the first bit of the Z6 byte at the TxPOH input pins. ***NOTE:*** *These pins are only active if the XRT79L72 has been configured to operate in the ATM/PLCP Mode.*

PIN #	NAME	TYPE	DESCRIPTION
F3 B25	TxPOHClk_0 TxPOHClk_1	O O	**Transmit PLCP Frame POH Byte Insertion Clock:** These pins, along with the TxPOH and the TxPOHMSB input pins, function as the Transmit PLCP Frame POH Byte serial input port. These output pins function as clock output signals that are used to sample the user's POH data at the TxPOH input pins. These output pins are always active, independent of the state of the TxPOHIns pins. ***NOTE:*** *These pins are only active if the XRT79L72 has been configured to operate in the ATM/PLCP Mode.*
R1 M25	TxOHInd_0/ TxPFrame_0/ TxHDLCDat0_6 TxOHInd_1/ TxPFrame_1/ TxHDLCDat1_6	I/O I/O	**Transmit Overhead Data Indicator Output/Transmit PLCP Frame Boundary Indicator Output/Transmit HDLC Controller Data Bit 6 input pin:** The function of these input/output pins depends upon whether the XRT79L72 has been configured to operate in the Clear-Channel Framer Mode, the ATM/PLCP Mode or the High-Speed HDLC Mode. **Clear-Channel Framer Mode - TxOHInd:** In the Clear-Channel Framer Mode, these output pins function as the transmit overhead data indicator for the local terminal equipment. These output pins are pulsed "High" for one DS3 or E3 bit period in order to indicate to the local terminal equipment that the Transmit Section of the Framer is going to be processing an overhead bit, upon the next rising edge of TxInClk., and will NOT latch the data that is applied to the TxSer input pins. Therefore, when the local terminal equipment samples the TxOHInd output pin "High", then it must not apply the next payload bit to TxSer input pin. These output pins serve as a warning that this particular payload bit is going to be ignored by the Transmit Section of the Framer, and will not be inserted into payload bits, within the outbound DS3 or E3 data stream. **ATM/PLCP Mode - TxPFrame:** If the XRT79L72 is configured to operate in the ATM UNI/PLCP Mode, then these output pins will denote the boundaries of outbound PLCP frames, as they are being processed by the Transmit PLCP Processor block. These outputs pulse "High" when the last nibble of a given PLCP frame is being routed to the Transmit DS3/E3 Framer block. These output pins are inactive if the XRT79L72 is operating in the Direct-Mapped ATM Mode. **High-Speed HDLC Controller Mode - TxHDLCDat_6:** If the XRT79L72 is configured to operate in the High-Speed HDLC Controller mode, then the local terminal equipment will be provided with a byte-wide Transmit HDLC Controller byte-wide input interface. These input pins will function as Bit 6 within this byte wide interface. Data, residing on the Transmit HDLC Controller byte wide input interface, will be sampled upon the rising edge of the TxHDLCClk output signals.

PIN #	NAME	TYPE	DESCRIPTION
T2 N22	TxNibClk_0/ TxGFCMSB_0/ SendFCS_0 TxNibClk_1/ TxGFCMSB_1/ SendFCS_1	I/O I/O	**Transmit Nibble Clock Output pin/Transmit GFC Byte - MSB Indicator Output/Send FCS Value Request Input:** The function of these input/output pins depend upon whether the XRT79L72 is configured to operate in the Clear-Channel Framer Mode, the High-Speed HDLC Controller Mode or in the ATM Mode. **Clear-Channel Framer Mode - TxNibClk:** When operating in the Nibble-Parallel Mode the XRT79L72 will derive this clock signal from either the TxInClk or the RxLineClk signals depending upon whether the chip is operating in the Local-Timing or Loop-Timing Mode. The user is advised to configure the Terminal Equipment to output the outbound payload data to the XRT79L72 onto the TxNibn_[3:0] input pins, upon the rising edge of these clock signals. The Transmit Payload Data Input Interface block will sample the data, residing on the TxNibn_[3:0] line, upon the falling edge these clock signals. ***NOTES:*** 1. *For DS3 applications, the XRT79L72 will output 1176 clock pulses to the local terminal equipment for each outbound DS3 frame.* 2. *For E3, ITU-T G.832 applications, the XRT79L72 will output 1074 clock pulses to the local terminal equipment for each outbound E3 frame.* 3. *For E3, ITU-T G.751 applications, the XRT79L72 will output 384 clock pulses to the local terminal equipment for each outbound E3 frame.* **ATM Mode - TxGFCMSB:** These signals, along with TxGFC and TxGFCClk combine to function as the Transmit GFC Nibble Field serial input port. These output signals will pulse "High" when the MSB (most significant bit) of the GFC nibble for a given outbound cell is expected at the TxGFC input pins. **High-Speed HDLC Controller Mode - SendFCS:** The local terminal equipment is expected to control both these input pins, along with the SendMSG input pins, during the construction and transmission of each outbound HDLC frame. These input pins are used to command the Transmit HDLC Controller block to compute and insert the computed FCS (Frame-Check Sequence) value into the back-end of the outbound HDLC frame, as a trailer. If the user has configured the Transmit HDLC Controller block to compute and insert a CRC-16 value into the outbound HDLC frame, then the local terminal equipment is expected to hold these input pins "High" for two periods of TxHDLCClk. Conversely, if the user has configured the Transmit HDLC Controller block to compute and insert a CRC-32 value into the outbound HDLC frame, then the local terminal equipment is expected to hold these input pins "High" for four (4) periods of TxHDLCClk. ***NOTES:*** 1. *These input/output pins are inactive if the XRT79L72 has been configured to operate in the PPP Mode.* 2. *These input/output pins are inactive if the XRT79L72 has been configured to operate in the Clear-Channel Framer/Serial mode.*

PIN #	NAME	TYPE	DESCRIPTION
E5 C21	TxGFCClk_0 TxGFCClk_1	O O	**Transmit GFC Nibble-Field Serial Input port - Clock Output signal:** These signals, along with TxGFC and TxGFCMSB combine to function as the Transmit GFC Nibble-field serial input port. These output signals function as the demand clock signal for this port. The user will specify the value of the GFC field, within a given ATM cell, by serially transmitting its four bit-value into the TxGFC input pins. The Transmit GFC Nibble-Field serial input port will latch the contents of TxGFC upon the rising edge of these clock signals. Hence, the local terminal equipment should be designed to place its outbound GFC bits on to the TxGFC line, upon the falling edge of these clock signals. ***NOTE:*** *These output pins are only active if the XRT79L72 has been configure to operate in the ATM Mode.*
AA1 V22	TxNib0_3/ TxPOHIns_0/ TxHDLCDat0_3 TxNib1_3/ TxPOHIns_1/ TxHDLCDat1_3	I I	**Transmit Nibble Interface - Bit 3/Transmit PLCP Path Overhead Insert enable/Transmit HDLC Controller Data Bus - Bit 3 input:** The function of these input pins depend upon whether the XRT79L72 is configured to operate in the Clear-Channel Framer Mode, the High-Speed HDLC Controller Mode or in the ATM/PLCP Mode. **Clear-Channel Framer Mode - TxNib_3:** If the XRT79L72 is configured to operate in the Nibble-Parallel Mode, then these input pins will function as the bit 3 (MSB) input to the Transmit Nibble-Parallel input interface. The Transmit Payload Data Input Interface block will sample these signals (along with TxNib_0 through TxNib_2) upon the falling edge of TxNibClk. ***NOTE:*** *These input pins are inactive if the XRT79L72 is configured to operate in the Serial Mode.* **ATM/PLCP Mode - TxPOHIns:** f the XRT79L72 is configured to operate in the ATM Mode, and if (within the ATM Mode, the chip is also configured to operate in the PLCP Mode), then these input pins function as the Transmit PLCP Path Overhead Port - Enable input pin. In this mode, the user can externally insert desired path overhead byte values into the outbound PLCP frames. The Transmit PLCP Path Overhead Input port becomes active whenever the user asserts these input pins by pulling them "High". Once this occurs, the data, residing upon the TxPOH input pins will be sampled upon the rising edge of the TxPOHClk signals. These input pins are inactive if the XRT79L72 is configured to operate in the Direct-Mapped ATM Mode. **High-Speed HDLC Controller Mode - TxHDLCDat_3:** If the XRT79L72 is configured to operate in the High-Speed HDLC Controller mode, then the local terminal equipment will be provided with a byte-wide Transmit HDLC Controller byte-wide input interface. These input pins will function as Bit 3 within this byte wide interface. Data, residing on the Transmit HDLC Controller byte wide input interface, will be sampled upon the rising edge of the TxHDLCClk output signals.

PIN #	NAME	TYPE	DESCRIPTION
AA2 V23	TxNib0_2/ TxStuff_Ctl_0/ TxHDLCDat0_2 TxNib1_2/ TxStuff_Ctl_1/ TxHDLCDat1_2	I I	**Transmit Nibble Input Interface - Bit 2/Transmit PLCP Stuff Control Input/ Transmit HDLC Controller Data Bus - Bit 2 Input:** The function of these input pins depend upon whether the XRT79L72 is configured to operate in the Clear-Channel Framer Mode, the High-Speed HDLC Controller Mode, or in the ATM/PLCP Mode. **Clear-Channel Framer Mode - TxNib_2:** If the XRT79L72 is configured to operate in the Nibble-Parallel Mode, then these input pins will function as the bit 1 input to the Transmit Nibble-Parallel input interface. The Transmit Payload Data Input Interface block will sample these signals (along with TxNibn_0, TxNibn_2 and TxNibn_3) upon the falling edge of TxNibClk ***NOTE:*** *These input pins are inactive if the XRT79L72 is configured to operate in the Serial Mode.* **ATM/PLCP Mode - TxStuff_Ctl:** These input pins are used to externally exercise or forego trailer nibble stuffing opportunities by the Transmit PLCP Processor. PLCP trailer nibble stuff opportunities occur in periods of three PLCP frames (375 us). The first PLCP frame (first, within a stuff opportunity period) will have 13 trailer nibbles appended to it. The second PLCP frame (second within a stuff opportunity period will have 14 trailer nibbles appended to it. The third PLCP frame (the location of the stuff opportunity) will contain 13 trailer nibbles if thess input pins are pulled "Low", and 14 trailer nibbles if these input pins are pulled "High". ***NOTE:*** *These input pins are inactive if the XRT79L72 is configured to operate in the Direct-Mapped ATM Mode.* **High-Speed HDLC Controller Mode - TxHDLCDat_2:** If the XRT79L72 is configured to operate in the High-Speed HDLC Controller mode, then the local terminal equipment will be provided with a byte-wide Transmit HDLC Controller byte-wide input interface. These input pins will function as Bit 1 within this byte wide interface. Data, residing on the Transmit HDLC Controller byte wide input interface, will be sampled upon the rising edge of the TxHDLCClk output signals.

PIN #	NAME	TYPE	DESCRIPTION
AA3 V24	TxNib0_1/ Tx8KREF_0/ TxHDLCDat0_1 TxNib1_1/ Tx8KREF_1/ TxHDLCDat1_1	I I	**Transmit Nibble Input Interface - Bit 1/Transmit PLCP Framing 8kHz Reference Input/Transmit HDLC Controller Data Bus - Bit 1 Input:** The function of these input pins depend upon whether the XRT79L72 is configured to operate in the Clear-Channel Framer Mode, the High-Speed HDLC Controller Mode, or in the ATM/PLCP Mode. **Clear-Channel Framer Mode - TxNib_1:** If the XRT79L72 is configured to operate in the Nibble-Parallel Mode, then these input pins will function as the bit 1 input to the Transmit Nibble-Parallel input interface. The Transmit Payload Data Input Interface block will sample this signals (along with TxNibn_0, TxNibn_2 and TxNibn_3) upon the falling edge of TxNibClk. ***NOTE:*** *These input pins are inactive if the XRT79L72 is configured to operate in the Serial Mode.* **ATM/PLCP Mode - Tx8KREF:** If the XRT79L72 is configured to operate in the ATM/PLCP Mode, then the Transmit PLCP Processor can be configured to synchronize its PLCP frame generation to these input clock signals. The Transmit PLCP Processor will also use these input signals to compute the nibble-trailer stuff opportunities. ***NOTE:*** *These input pins are inactive if the use has configured the XRT79L72 to operate in the Direct-Mapped ATM Mode.* **High-Speed HDLC Controller Mode - TxHDLCDat_1:** If the XRT79L72 is configured to operate in the High-Speed HDLC Controller mode, then the local terminal equipment will be provided with a byte-wide Transmit HDLC Controller byte-wide input interface. These input pins will function as Bit 1 within this byte wide interface. Data, residing on the Transmit HDLC Controller byte wide input interface, will be sampled upon the rising edge of the TxHDLCClk output signals.
AB1 V25	TxNib0_0/ TxGFC1_0 TxHDLCDat0_0 TxNib1_0/ TxGFC_1/ TxHDLCDat1_0	I I	**Transmit Nibble Interface - Bit 0/Transmit GFC Input pin/Transmit HDLC Controller Data Bus - Bit 0 Input:** The function of these input pins depend upon whether the XRT79L72 is configured to operate in the Clear-Channel Framer Mode, the High Speed HDLC Controller Mode or in the ATM Mode. **Clear-Channel Framer Mode - TxNib_0:** If the XRT79L72 is configured to operate in the Nibble-Parallel Mode, then these input pins will function as the bit 0 (LSB) input to the Transmit Nibble-Parallel input interface. The Transmit Payload Data Input Interface block will sample these signals (along with TxNibn_1 through TxNibn_3) upon the falling edge of TxNibClk. ***NOTE:*** *These input pins are inactive if the XRT79L72 is configured to operate in the Serial Mode.* **ATM Mode - TxGFC:** These signals, along with TxGFCMSB, and TxGFCClk combine to function as the Transmit GFC Nibble Field serial input port. The user will specify the value of the GFC field, within a given ATM cell, by serially transmitting its four bit-value into these input pins. Each of these four bits will be clocked into the port upon the rising edge of the TxGFCClk output signals. **High-Speed HDLC Controller Mode - TxHDLCDat_0:** If the XRT79L72 is configured to operate in the High-Speed HDLC Controller mode, then the local terminal equipment will be provided with a byte-wide Transmit HDLC Controller byte-wide input interface. These input pins will function as Bit 0 (the LSB) within this byte wide interface. Data, residing on the Transmit HDLC Controller byte wide input interface, will be sampled upon the rising edge of the TxHDLCClk output signals.

PIN #	NAME	TYPE	DESCRIPTION
T1 N23	TxCellTxed_0/ TxNibFrame_0/ ValidFCS_0 TxCellTxed_1/ TxNibFrame_1/ ValidFCS_1	O O	**Transmit Cell Generator indicator/Transmit Nibble Frame Indicator/Valid FCS Indicator output:** The function of these output pins depend upon whether the XRT79L72 has been configured to operate in the ATM Mode, the Clear-Channel Framer Mode or in the High-Speed HDLC Controller Mode. **ATM Mode - TxCellTxed:** This output pin pulses "High" each time the Transmit Cell Processor transmits a cell to either the Transmit PLCP Processor or the Transmit DS3/E3 Framer block. **Clear-Channel Framer Mode - TxNibFrame:** These output pins pulse "High" when the last nibble of a given DS3 or E3 frame is expected at the TxNibn[3:0] input pins. The purpose of these output pins are to alert the local terminal equipment that it needs to begin the transmission of a new DS3 or E3 frame to the XRT79L72. ***NOTE:*** *These output pins are not active if the XRT79L72 is configured to operate in the Serial-Mode.* **High-Speed HDLC Controller Mode - ValidFCS:** The combination of the RxIdle and ValidFCS output signals are used to convey information about data that is being output via the Receive HDLC Controller output Data bus (RxHDLCDatn_[7:0]). ***If RxIdle = "High":*** The Receive HDLC Controller block will drive these output pins "High" anytime the flag sequence octet (0x7E) is present on the RxHDLCDatn[7:0] output data bus. ***If RxIdle and ValidFCS are both "High":*** The Receive HDLC Controller block has received a complete HDLC frame, and has determined that the FCS value within this HDLC frame are valid. ***If RxIdle is "High" and ValidFCS is "Low":*** The Receive HDLC Controller block has received a complete HDLC frame, and has determined that the FCS value within this HDLC frame is invalid. ***If RxIdle is "High" and ValidFCS is "Low":*** The Receive HDLC Controller block has received an ABORT sequence.
D11	TxPERR	I	**Transmit Error Indicator from Link Layer:** This input signal is used to indicate that the current packet is ABORTED and must be discarded. This input pin should only be asserted when the last byte (or word) is be written onto the TxPData[15:0] input pins. If the Link Layer Processor block identifies a given "outbound" PPP Packet as being "erred", then the Transmit PPP Packet Processor block will transmit this particular packet (to the remote terminal equipment) as an Aborted Packet. ***NOTE:*** *This input pin is only active if the XRT79L72 has been configured to operate in the PPP Mode.*
C11	TxPEOP	I	**Transmit POS-PHY Interface - End of Packet:** The link layer processor toggles this output pin "High" whenever the Link Layer Processor is writing the last byte (or word) of a given Packet into the Transmit POS-PHY Data Bus (e.g., the TxPData[15:0] data input pins). ***NOTES:*** 1. *This input pin is only valid when the XRT79L72 is configured to operate in the PPP Mode.* 2. *This input pin is only valid when the Transmit POS-PHY Interface - Write Enable Input pin (TxPEn) is asserted.*

PIN #	NAME	TYPE	DESCRIPTION
C7	TxUPrty/ TxPPrty	I	**Transmit UTOPIA Data Bus - Parity Input/Transmit POS-PHY Interface - Parity Input:** The function of this input pin depends upon whether the XRT79L72 has been configured to operate in the ATM UNI or PPP Mode. **ATM UNI Mode - TxUPrty:** The ATM Layer processor will apply the parity value of the byte or word which is being applied to the Transmit UTOPIA Data Bus (e.g., TxUData[7:0] or TxUData[15:0]) inputs of the XRT79L72, respectively. ***NOTE:*** *This parity value should be computed based upon the odd-parity of the data applied at the Transmit UTOPIA Data Bus.* The Transmit UTOPIA Interface block within the XRT79L72 will independently compute an odd-parity value of each byte (or word) that it receives from the ATM Layer processor and will compare it with the logic level of this input pin. **PPP Mode - TxPPrty:** The Link Layer Processor will apply the parity value of the byte or word which is being applied to the Transmit POS-PHY Data Bus (e.g., TxPData[7:0] or TxPData[15:0]) inputs of the XRT79L72, respectively. ***NOTE:*** *This parity value should be computed based upon the odd-parity of the data applied to the Transmit POS-PHY Data Bus. The Transmit POS-PHY Interface block within the XRT79L72 will independently compute an odd-parity value of each byte (or word) that it receives from the Link Layer processor and will compare it will the logic level of this input pin. This input pin is only active if the user has configured the XRT79L72 device to operate in either the ATM UNI or the PPP Mode. The user should tie this input pin to GND if he/she intends to operate the XRT79L72 device in either the Clear-Channel Framer or High-Speed HDLC Controller Modes.*
D7	$\overline{\text{TxUEN}}$/ $\overline{\text{TxPEN}}$	I	**Transmit UTOPIA Interface Block - Write Enable/Transmit POS-PHY Interface - Write Enable:** The exact function of this input pin depends upon whether the XRT79L72 device has been configured to operate in the ATM UNI or PPP Mode. **ATM UNI Mode Operation - TxUENB* - Transmit UTOPIA Interface - Write Enable Input pin:** This active-low signal, from the ATM Layer processor enables the data on the Transmit UTOPIA Data Bus to be latched and written into the TxFIFO on the rising edge of TxUClk. When this signal is asserted (e.g., pulled to a logic "LOW" level), then the contents of the byte or word that is present, on the Transmit UTOPIA Data Bus (TxUData[15:0]), will be latched into the Transmit UTOPIA Interface block, on the rising edge of TxUClk. When this signal is negated, then the Transmit UTOPIA Data bus inputs will be tri-stated. **PPP Mode Operation - TxPENB*** This active-low signal, from the Link Layer processor enables the data on the Transmit POS-PHY Data Bus to latched and be written into the TxFIFO on the rising edge of TxPClk. When this signal is asserted (e.g., pulled to a logic "LOW" level), then the contents of the byte or word that is present, on the Transmit POS-PHY Data Bus (TxPData[15:0]), will be latched into the Transmit POS-PHY Interface block, on the rising edge of TxPClk.When this signal is negated, then the Transmit POS-PHY Data bus inputs will be tri-stated. ***NOTE:*** *This input pin is only active if the XRT79L72 device has been configured to operate in the ATM UNI or PPP Mode. The user should tie this input pin to GND if he/she intends to operate the XRT79L72 device in either the Clear-Channel Framer or High-Speed HDLC Controller Mode.*

PIN #	NAME	TYPE	DESCRIPTION
B9	TxUClav/ TxPPA	O	**Transmit UTOPIA Interface - Cell Available Output Pin/Transmit POS-PHY Interface - Packet Data Available Output pin:** The exact function of this output pin depends upon whether the XRT79L72 device has been configured to operate in the ATM UNI or PPP Mode.ATM UNI Mode - TxUClav - Transmit UTOPIA Interface - Cell Space Available Indicator Output pin:This output pin supports data flow control between the ATM Layer Processor and the Transmit UTOPIA Interface block. This signal is asserted (e.g., driven "high") whenever the TxFIFO is capable of receiving at least one more full ATM cell of data from the ATM Layer processor. This signal is negated (e.g., driven "low"), if the TxFIFO is not capable of receiving one more full ATM cell of data from the ATM Layer processor. The exact behavior of the "TxUClav" output pin, as a function of "UTOPIA Level" is presented below. **Multi-PHY Operation - UTOPIA Level 2:** When the XRT79L72 device is operating in a Multi-PHY Application and is configured to operate in the UTOPIA Level 2 Mode, then this signal will be tri-stated until the TxUClk cycle following the assertion of a valid address on the Transmit UTOPIA Address bus input pins (e.g., when the contents on the Transmit UTOPIA Address bus pins, TxUAddr[4:0], match that which have been assigned to this particular Transmit UTOPIA Interface block). Afterwards, this output pin will be driven either "high" or "low" depending upon the current fill status of the TxFIFO. **Multi-PHY Operation - UTOPIA Level 3:** When the XRT79L72 device is operating in a Multi-PHY Application, then this signal will be tri-stated until two TxUClk cycles following the assertion of a valid address on the Transmit UTOPIA Address bus input pins (e.g., if the contents of the Transmit UTOPIA Address bus input pins, TxUAddr[4:0], match that which have been assigned to this particular Transmit UTOPIA Interface block). Afterwards, this output pin will be driven either "high" or "low" depending upon the current fill status of the RxFIFO. **PPP Mode - TxPPA** Transmit POS-PHY Interface Packet Space Available Indicator OutputThe XRT79L72 device will drive this output pin "high" whenever a (programmable) number of bytes of empty space is available (for writing more PPP packet data) into the TxFIFO. The exact behavior of the TxPPA output pin, as a function of "POS-PHY Level" is presented below. **POS-PHY Level 2:** When the XRT79L72 device is configured to operate in the POS-PHY Level 2 Mode, then this signal will be tri-stated until the TxPClk cycle following the assertion of a valid address on the Transmit POS-PHY Address bus input pins (e.g., if the contents on the Transmit POS-PHY Address bus pins, TxPAddr[4:0], match that which have been assigned to this particular Transmit POS-PHY Interface block). Afterwards, this output pin will be driven either "high" or "low" depending upon the current fill status of the TxFIFO. **POS-PHY Level 3:** When the XRT79L72 device is configured to operate in the POS-PHY Level 3 Mode, then this signal will be tri-stated until two TxPClk cycles following the assertion of a valid address on the Transmit POS-PHY Address Bus input pins (e.g., if the contents on the Transmit POS-PHY Address bus pins, TxPAddr[4:0], match that which have been assigned to this particular Transmit POS-PHY Interface block). Afterwards, this output pin will be driven either "high" or "low" depending upon the current fill status of the TxFIFO.

PIN #	NAME	TYPE	DESCRIPTION
B7	TxUSoC/ TxPSoP	I	**Transmit UTOPIA - Start of Cell Input/Transmit POS-PHY - Start of Packet Input:** The function of this input signal depends upon whether the XRT79L72 has been configured to operate in the ATM UNI or in the PPP Mode. **ATM UNI Mode Operation - TxUSoC:** This input pin is driven by the ATM Layer Processor and is used to indicate the start of an ATM cell that is being transmitted from the ATM Layer Processor. This input pin must be pulsed "High" whenever the first byte (or word) of a new cell is present on the Transmit UTOPIA Data Bus (TxUData[15:0]). This input pin must remain "Low" at all other times. **PPP Mode Operation - TxPSoP/TxPSoC:** If the XRT79L72 has been configured to operate in the Packet-Mode, then this input pin is pulsed "High" to denote that the first byte (or word) of a given packet is placed on the TxPData[15:0] input pins.If the XRT79L72 has been configured to operate in the Cell-Chunk Mode, then this input pin is pulsed "High" to denote that the first byte of a packet chunk, if placed on the TxPData[15:0] input pins. ***NOTE:*** *This input pin is only valid if the XRT79L72 has been configured to operate in the PPP Mode.*
B11	TxTSX/ TxPSOF	I	**Transmit - Change of Port Indicator Input/Transmit - Start of PPP Packet (in Chunk Mode):** The exact function of this input pin depends upon whether the XRT79L72 device has been configured to operate in the Packet Mode or Cell-Chunk Mode, as is described below. **Packet Mode - TxTSX - Transmit POS-PHY Interface - Change of Port Indicator Output (POS-PHY Level 3, Packet Mode only):** The Link-Layer processor pulses this input pin "high" when an "in-band" port address is present on the "TxPData[15:11]" bus input pins. When this input pin and "TxPENB*" are both set "high" then the value of "TxPData[15:11]" is the address value of the TxFIFO (Transmit POS-PHY Port) to be selected. Subsequent write operations, into "TxPData[15:0]" will fill the TxFIFO (within the Transmit POS-PHY Port) corresponding to this particular "in-band" address. **Chunk Mode - TxPSOF - Receive Start of Packet Input Indicator:** The Link Layer processor pulses this input pin "high" in order to indicate that the first byte (or 16-bit word) of a given Packet is placed on the "TxPData[15:0]" pins. ***NOTE:*** *This input pin is only active if the XRT79L72 device has been configured to operate in the POS-PHY Level 3, Packet Mode or in the Chunk Mode. If the user intends to operate the XRT79L72 device in any other mode, then he/she should tie this input pin to GND.*
A7	TxUClkO/ TxPClkO	O	**Transmit UTOPIA Interface Clock/Transmit POS-PHY Interface Clock Output:** This output is derived from an internal PLL.

PIN #	NAME	TYPE	DESCRIPTION
B10	TxUClk/ TxPClk	I	**Transmit UTOPIA Interface Clock/Transmit POS-PHY Interface Clock Input:** The function of this input pin depends upon whether the XRT79L72 has been configured to operate in the ATM UNI or in the PPP Mode. **ATM UNI Mode - TxUClk:** The Transmit UTOPIA Interface clock is used to latch the data on the Transmit UTOPIA Data bus, into the Transmit UTOPIA Interface block. This clock signal is also used as the timing source for circuitry used to process the ATM cell data into and through the TxFIFO. During Multi-PHY operation, the data on the Transmit UTOPIA Address bus pins is sampled on the rising edge of TxUClk. **PPP Mode - TxPClk:** The Transmit POS-PHY Interface clock is used to latch the data on the Transmit POS-PHY Data bus, into the Transmit POS-PHY Interface block. This clock signal is also used as the timing source for circuitry used to process the Packet data into and through the TxFIFO. ***NOTE:*** *The XRT79L72 device can support TxUClk or TxPClk clock frequencies of up to 50MHz.*

PIN #	NAME	TYPE	DESCRIPTION
C8 B8 A8 E9 C9	TxUAddr_0 TxUAddr_1 TxUAddr_2 TxUAddr_3 TxUAddr_4	I	**Transmit UTOPIA Address Bus/Transmit POS-PHY Address Bus:** The exact function of these input pins depends upon whether the XRT79L72 device has been configured to operate in the ATM UNI or PPP Modes. **ATM UNI Mode -TxUAddr[4:0] - Transmit UTOPIA Address Bus:** These input pins comprise the Transmit UTOPIA Address Bus input pins. The Transmit UTOPIA Address Bus is only in use when the XRT79L72 is operating in the Multi-PHY mode. Whenever the ATM Layer processor wishes to poll or write data to a particular UNI (PHY-Layer) device, it will provide the address of the "target UNI" on the Transmit UTOPIA Address Bus. The contents of the Transmit UTOPIA Address Bus input pins are sampled on the rising edge of TxUClk clock signal. The Transmit UTOPIA Interface block will compare the data on the Transmit UTOPIA Address Bus with the pre-programmed UTOPIA Address value (which was loaded into the XRT79L72 device by writing the appropriate data into both the "Transmit UTOPIA Port Address" Register (Address = 0x0593) and the "Transmit UTOPIA Port Number" Register (Address = 0x0597). If these two values are identical and the TxUENB* input pin is asserted, then the TxUClav output pin will be driven to the appropriate state (based upon the TxFIFO fill level) for the Cell Level handshake mode of operation. If these two values do not match, then the Transmit UTOPIA Interface block will continue to tri-state the "TxUClav" output pin. ***NOTE:*** *These input pins are only active if the XRT79L72 device has been designed into a "Multi-PHY" Application. If the user intends to design the XRT79L72 into a "Single-PHY" Application, then he/she should tie these input pins to GND.* **PPP Mode - TxPAddr[4:0] - Transmit POS-PHY Interface Address Bus Input Pins:** These input pins comprise the Transmit POS-PHY Address Bus input pins. Whenever the Link Layer Processor wishes to poll or write data to a particular PHY-Layer device, it will provide the address of the "target PHY-Layer device" on the Transmit POS-PHY Address Bus. The contents of the Transmit POS-PHY Address Bus input pins are sampled on the rising edge of TxPClk. The XRT79L72 device will compare the data on the Transmit POS-PHY Address Bus with the pre-programmed POS-PHY Address value (which was loaded into the XRT79L72 device by writing the appropriate data into the "Transmit POS-PHY Interface - Transmit Control Register - Byte 0" (Address = 0x0582). If these two values are identical and the "TxPENB*" input pin is asserted, then the TxPPA output pin will be driven to the appropriate state (based upon the TxFIFO fill level). If these two values do not match, then the Transmit POS-PHY Interface block will continue to tri-state the "TxPPA" output pin. ***NOTE:*** *These input pins are only active if the XRT79L72 device has been configured to operate in either the ATM UNI or PPP Modes. The user should tie these input pins to GND if he/she wishes to operate the XRT79L72 device in either the "Clear-Channel Framer" or "High-Speed HDLC Controller" Modes.*

PIN #	NAME	TYPE	DESCRIPTION
A11	TxMod	I	**Transmit PPP Data Bus - Modulo Indicator:** This input pin is used to specify the number of valid packet octets are being placed on the TxPData[15:0] input pins. The Link Layer Processor is expected to set this input pin "Low" when both bytes on the TxPData[15:0] data bus is valid packet data. Conversely, the Link Layer Processor is expected to set this input pin "High" when only the upper octet has valid packet data. ***NOTES:*** 1. *This input pin is only active if the XRT79L72 has been configured to operate in the PPP Mode.* 2. *The Link Layer Processor is expected to set this input pin to the appropriate state, as each 16-bit word is being written into the TxPData[15:0] data bus.*
C3 B2 A1 A2 B3 A3 D5 C4 B4 A4 C5 B5 A5 C6 B6 A6	TxUData_0/ TxPData_0 TxUData_1/ TxPData_1 TxUData_2/ TxPData_2 TxUData_3/ TxPData_3 TxUData_4/ TxPData_4 TxUData_5/ TxPData_5 TxUData_6/ TxPData_6 TxUData_7/ TxPData_7 TxUData_8/ TxPData_8 TxUData_9/ TxPData_9 TxUData_10/ TxPData_10 TxUData_11/ TxPData_11 TxUData_12/ TxPData_12 TxUData_13/ TxPData_13 TxUData_14/ TxPData_14 TxUData_15/ TxPData_15	I	**Transmit UTOPIA Data Bus Inputs/Transmit POS-PHY Data Bus Inputs:** The function of these input pins depends upon whether the XRT79L72 is operating in the ATM UNI Mode or in the PPP Mode. **ATM UNI Operation - TxUData[15:0]:** These input pins comprise the Transmit UTOPIA Data Bus input pins. When the ATM Layer Processor wishes to transmit ATM cell data through the XRT72L72 ATM UNI, it must place this data on these pins. The data, on the Transmit UTOPIA Data Bus is latched into the Transmit UTOPIA Interface block upon the rising edge of TxUClk. **PPP Operation - TxPDATA[15:0]** These input pins comprise the Transmit POS-PHY Data Bus input pins. When a Network Processor wishes to transmit PPP data through the XRT79L72 Framer/UNI IC, it must place this data on these pins. The data, on the Transmit POS-PHY Data Bus is latched into the Transmit POS-PHY Interface block upon the rising edge of TxPClk.

PIN #	NAME	TYPE	DESCRIPTION
RECEIVE SYSTEM SIDE INTERFACE PINS			
M2 H23	RxAIS_0/ RxNib0_2/ RxHDLCDat0_2 RxAIS_1/ RxNib1_2/ RxHDLCDat1_2	O O	**Receive AIS Pattern Indicator/Receive Nibble Output Interface - Bit 2/ Receive HDLC Controller Data Bus - Bit 2 output pin:** The function of these output pins depend upon whether the XRT79L72 has been configured to operate in the Clear-Channel Framer/Nibble-Parallel Interface Mode, the High-Speed HDLC Controller Mode, or in the other modes. **Other Modes - RxAIS:** These output pins are driven "High" whenever the Receive Section of the XRT79L72 has detected and is currently declaring an AIS (Alarm Indicator Signal) condition. **Clear-Channel Framer/Nibble-Parallel Interface Mode - RxNib_2:** If the XRT79L72 is configured to operate in the Nibble-Parallel Mode, then these output pins will function as the bit 2 output from the Receive Nibble-Parallel output interface. The Receive Payload Data Output Interface block will output these signals (along with RxNibn_0, RxNibn_1, and RxNibn_3) upon the rising edge of the RxClk output signals. **High-Speed HDLC Controller Mode - RxHDLCDat_2:** These output pins along with RxHDLCDatn_[7:3] and RxHDLCDatn_[1:0] functions as the Receive HDLC Controller byte wide output data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signals. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signals.
M1 H24	RxRED_0/ RxNib0_3/ RxHDLCDat0_3 RxRED_1/ RxNib1_3/ RxHDLCDat1_3	O O	**Receive Section Red Alarm Indicator/Receive Nibble Interface Output pin - Bit 3/Receive HDLC Controller Data Bus output pin - Bit 3:** The function of this output pin depends upon whether the XRT79L72 has been configured to operate in the Clear-Channel Framer/Nibble-Parallel Mode, the High-Speed HDLC Controller Mode, or in some other mode. **Clear-Channel Framer/Nibble-Parallel Mode - RxNib_3:** The XRT79L72 will output Received data from the remote terminal equipment to the local terminal equipment via this pin, along with RxNib_0 through RxNib_2. This particular output pin functions as the LSB. The data at this pin is updated on the rising edge of the RxClk output signal. Hence, the user's local terminal equipment should sample this signal upon the falling edge of RxClk. **High-Speed HDLC Controller Mode - RxHDLCDat_3:** This output pin along with RxHDLCDat_[7:4] and RxHDLCDat_[2:0] functions as the Receive HDLC Controller byte wide output data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signal. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signal. **Other Modes - RxRED - RED Alarm/Defect Indicator Output pin:** The XRT79L72 device will assert this output pin (e.g., toggle it "high") in order to indicate that the Receive DS3/E3 Framer block is currently declaring at least one of the following defect conditions. • LOS - Loss of Signal Defect Condition • OOF - Out of Frame Defect Condition • AIS - Alarm Indication Signal Defect Condition. The XRT79L72 device will negate this output pin (e.g., toggle it "low") anytime that the Receive DS3/E3 Framer block is NOT currently declaring any of the above-mentioned defect conditions.

PIN #	NAME	TYPE	DESCRIPTION
M3 H22	RxOOF_0/ RxNib0_1/ RxHDLCDat0_1 RxOOF_1/ RxNib1_1/ RxHDLCDat1_1	O O	**Receive Out of Frame Indicator/Receive Nibble Interface Output pin - Bit 1/ Receive HDLC Controller Data Bus Output pin - Bit 1:** The function of these output pins depend upon whether the XRT79L72 has been configured to operate in the Clear-Channel Framer/Nibble-Parallel Mode or the High-Speed HDLC Controller Mode. **Clear-Channel Framer/Nibble-Parallel Mode - RxNib_1:** The XRT79L72 will output Received data from the remote terminal equipment to the local terminal equipment via these pins, along with RxNibn_0, RxNibn_2 and RxNibn_3: These particular output pins function as the LSB. The data at these pins are updated on the rising edge of the RxClk output signals. Hence, the user's local terminal equipment should sample these signals upon the falling edge of RxClk. **High-Speed HDLC Controller Mode - RxHDLCDat_1:** These output pins along with RxHDLCDatn_[7:2] and RxHDLCDatn_0 functions as the Receive HDLC Controller byte wide output data bus. The Receive HDLC Controller will output the contents of all HDLC frames via these output data bus, upon the rising edge of the RxHDLCClk output signals. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signals. **All other Modes - RxOOF:** The UNI Receive DS3 Framer will assert these output signals whenever it has declared an Out of Frame (OOF) condition with the incoming DS3 frames. These signals are negated when the framer correctly locates the F- and M-bits and regains synchronization with the DS3 frame.
M4 J22	RxNib0_0/ RxHDLCDat0_0 RxNib1_0/ RxHDLCDat1_0	O O	**Receive Nibble Interface Output pin - Bit 0/Receive HDLC Controller Data Bus output pin - Bit 0:** The function of these output pins depend upon whether the XRT79L72 has been configured to operate in the Clear-Channel/Nibble-Parallel Mode, the High-Speed HDLC Controller Mode, or in some other mode. **Clear-Channel/Nibble-Parallel Mode - RxNib_0:** The XRT79L72 will output Received data from the remote terminal equipment to the local terminal equipment via these pins, along with RxNibn_1 through RxNibn_3. These particular output pins function as the LSB. The data at these pins are updated on the rising edge of the RxClk output signals. Hence, the user's local terminal equipment should sample these signals upon the falling edge of RxClk. **High-Speed HDLC Controller Mode - RxHDLCDat_0:** These output pins along with RxHDLCDatn_[7:1] function as the Receive HDLC Controller byte wide output data bus. These particular output pins function as the LSB (Least Significant Bit) of the Receive HDLC Controller byte wide data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signals. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signals. ***NOTE:*** *These output pins are only active if the XRT79L72 is configured to operate in the Clear-Channel/Nibble-Parallel Mode or in the High-Speed HDLC Controller Mode. These outputs are inactive for all remaining modes.*

PIN #	NAME	TYPE	DESCRIPTION
M5 J23	RxLCD_0/ RxOutClk_0/ RxHDLCDat0_7 RxLCD_1/ RxOutClk_1/ RxHDLCDat1_7	O O	**Receive Loss of Cell Delineation indicator/Receive Output Clock signal/ Receive HDLC Controller Data Bus - Bit 7 Output:** The function of these output pins depend upon whether the XRT79L72 has been configured to operate in the ATM, Clear-Channel Framer or High Speed HDLC Controller Mode. **ATM Mode - RxLCD (Loss of Cell Delineation Defect Indicator)** The XRT79L72 device will assert this output pin (e.g., toggle it "high") anytime (and for the duration that) the Receive ATM Cell Processor block is declaring the LCD (Loss of Cell Delineation) defect condition. The XRT79L72 device will negate this output pin (e.g., toggle it "low") whenever the Receive ATM Cell Processor block is not currently declaring the LCD defect condition. **Clear-Channel Framer Mode - RxOutClk:** These clock signals function as the Transmit Payload Data Input Interface clock source, if the XRT79L72 has been configured to operate in the loop-timing mode. In this mode, the local terminal equipment is expected to input data to the TxSer input pins, upon the rising edge of these clock signals. The XRT79L72 will use the rising edge of these signals to sample the data on the TxSer inputs. **High-Speed HDLC Controller Mode - RxHDLCDat_7:** These output pins along with RxHDLCDatn_[6:0] functions as the Receive HDLC Controller byte wide output data bus. These particular output pins function as the MSB (Most Significant Bit) of the Receive HDLC Controller byte wide data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signals. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signals.
J2 E25	RxLOS_0 RxLOS_1	O O	**Framer/UNI - Loss of Signal Output Indicator:** These pins are asserted when the Receive Section of the XRT79L72 encounters 180 consecutive 0's (for DS3 applications) or 32 consecutive 0's (for E3 applications) via the RxPOS and RxNEG pins. These pins will be negated once the Receive DS3/E3 Framer has detected at least 60 "1s" out of 180 consecutive bits (for DS3 applications) or has detected at least four consecutive 32 bit strings of data that contain at least 8 "1s" in the receive path.
E2 D22	RxPRED_0 RxPRED_1	O O	**Receiver Red Alarm Indicator - Receive PLCP Processor:** • The XRT79L72 device will assert this output pin (e.g., toggle it "high") anytime (and for the duration that) the Receive PLCP Processor block is currently declaring any of the following defect conditions. PLCP OOF - Out of Frame Defect Condition • PLCP LOF - Loss of Frame Defect Condition Conversely, the XRT79L72 device will negate this output pin (e.g., toggle it "low") anytime (and for the duration that) the Receive PLCP Processor block is NOT declaring any of the above-mentioned defect conditions. ***NOTE:*** *These output pins are only valid if the XRT79L72 has been configured to operate in the ATM/PLCP Mode.*

PIN #	NAME	TYPE	DESCRIPTION
F1 E22	RxPOOF_0 RxPOOF_1	O O	**Receive PLCP Processor Block - PLCP Out of Frame Defect Indicator:** The XRT79L72 device will assert this output pin (e.g., toggle it "high") anytime (and for the duration that) the Receive PLCP Processor block is currently declaring the PLCP OOF (Out of Frame) defect condition. Conversely, the XRT79L72 device will negate this output pin (e.g., toggle it "low") anytime (and for the duration that) the Receive PLCP Processor block is NOT declaring the PLCP OOF defect condition. ***NOTE:*** *These output pins are only active if the XRT79L72 has been configured to operate in both the UNI and PLCP Mode.*
E3 E21	RxPLOF_0 RxPLOF_1	O O	**Receive PLCP Processor Block - PLCP Loss of Frame Defect Indicator Output** The XRT79L72 device will assert this output pin (e.g., toggle it "high") anytime (and for the duration that) the Receive PLCP Processor block is currently declaring the PLCP LOF (Loss of Frame) defect condition.Conversely, the XRT79L72 device will negate this output pin (e.g., toggle it "low") anytime (and for the duration that) the Receive PLCP Processor block is NOT declaring the PLCP LOF defect condition. ***NOTE:*** *These output pins are only active is the XRT79L72 has been configured to operate in the ATM/PLCP Mode.*
J4 F26	RxOHEnable_0/ RxHDLCDat0_5 RxOHEnable_1/ RxHDLCDat1_5	O O	**Receive Overhead Data Output Interface - Enable Output/Receive HDLC Controller Data Bus - Bit 5 output:** The function of these output pins depend upon whether the XRT79L72 has been configured to operate in the Clear-Channel Framer Mode or in the High-Speed HDLC Controller Mode. **Clear-Channel Framer Mode - RxOHEnable:** The XRT79L72 will assert these output signals for one RxOHClk period when it is safe for the local terminal equipment to sample the data on the RxOH output pins. **High-Speed HDLC Controller Mode - RxHDLCDat_5:** These output pins along with RxHDLCDatn_[4:0], RxHDLCDatn_6 and RxHDLCDatn_7 functions as the Receive HDLC Controller byte wide output data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signals. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signals.
J3 E26	RxOH_0/ RxHDLCDat0_6 RxOH_1/ RxHDLCDat1_6	O O	**Receive Overhead Data Output Interface - output/Receive HDLC Controller Data Bus - Bit 6 output:** The function of these output pins depend upon whether the XRT79L72 has been configured to operate in the Clear-Channel Framer mode or in the High-Speed HDLC Controller Mode. **Clear-Channel Framer Mode - RxOH:** All overhead bits, which are received via the Receive Section of the XRT79L72 will be output via these output pins, upon the rising edge of RxOHClk. **High-Speed HDLC Controller Mode - RxHDLCDat_6:** These output pins along with RxHDLCDatn_[5:0] and RxHDLCDatn_7 functions as the Receive HDLC Controller byte wide output data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signals. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signals.

PIN #	NAME	TYPE	DESCRIPTION
J5 F25	RxOHClk_0/ RxHDLCClk_0 RxOHClk_1/ RxHDLCClk_1	O O	**Receive Overhead Data Output Interface - clock/Receive HDLC Controller - Clock output:** The function of these output pins depend upon whether the XRT79L72 has been configured to operate in the Clear-Channel Framer mode or in the High-Speed HDLC Controller Mode. **Clear-Channel Framer Mode - RxOHClk:** The XRT79L72 will output the overhead bits within the incoming DS3 or E3 frames via the RxOH output pins, upon the falling edge of these clock signals. As a consequence, the user's local terminal equipment should use the rising edge of these clock signals to sample the data on both the RxOH and RxOHFrame output pins. ***NOTE:*** *These clock signals are always active.* **High-Speed HDLC Controller Mode - RxHDLCClk:** These output pins function as the Receive HDLC Controller Data bus clock output. The Receive HDLC Controller block outputs the contents of all received HDLC frames via the Receive HDLC Controller Data bus (RxHDLCDatn_[7:0]) upon the rising edge of these clock signals. Hence, the user's local terminal equipment should be designed/configured to sample these data upon the falling edge of these clock signals.
K1 F24	RxOHFrame_0/ RxHDLCDat0_4 RxOHFrame_1/ RxHDLCDat1_4	O O	**Receive Overhead Data Interface - Framing Pulse indicator/Receive HDLC Controller Data Bus - Bit 4 output:** The function of these output pins depend upon whether the XRT79L72 has been configured to operate in the Clear-Channel Framer Mode or in the High-Speed HDLC Controller Mode. **Clear-Channel Framer Mode - RxOHFrame:** These output pins pulse "High" whenever the Receive Overhead Data Output Interface block outputs the first overhead bit of a new DS3 or E3 frame. **High-Speed HDLC Controller Mode - RxHDLCDat_4:** These output pins along with RxHDLCDatn_[3:0] and RxHDLCDatn_[7:5] functions as the Receive HDLC Controller byte wide output data bus. The Receive HDLC Controller will output the contents of all HDLC frames via this output data bus, upon the rising edge of the RxHDLCClk output signals. Hence, the user's local terminal equipment should be designed/configured to sample this data upon the falling edge of the RxHDLCClk output clock signals.
N3 J26	RxFrame_0 RxFrame_1	0 O	**Receive Boundary of DS3 or E3 Frame Output indicator:** The function of these output pins depend upon whether or not the XRT79L72 is operating in the Clear-Channel Framer/Nibble-Parallel Mode. **Clear-Channel Framer/Nibble-Parallel Mode:** The Receive Section of the XRT79L72 will pulse these output pins "High" for one nibble period, when the Receive Payload Data Output interface block is driving the very first nibble of a given DS3 or E3 frame, on the RxNibn[3:0] output pins. **Clear-Channel Framer/Serial Mode:** The Receive Section of the XRT79L72 will pulse these output pins "High" for one bit period, when the Receive Payload Data Output interface block is driving the very first bit of a given DS3 or E3 frame, on the RxSer output pin. **All Other Modes:** The Receive Section of the XRT79L72 will pulse these output pins "High" when the Receive DS3/E3 Framer block is processing the first bit within a new DS3 or E3 frame.

PIN #	NAME	TYPE	DESCRIPTION
B1 D21	RxCellRxed_0 RxCellRxed_1	O O	**Receive Cell Processor - Cell Received Indicator:** These output pins pulse "High" each time the Receive Cell Processor receives a new cell from the Receive PLCP Processor or the Receive DS3/E3 Framer block. *These output pins are only active if the XRT79L72 has been configured to operate in the ATM UNI Mode.*
N1 J24	RxPOH_0/ RxSer_0 RxPOH_1/ RxSer_1	O O	**Receive PLCP Path Overhead Output pin/Receive Serial Output pin:** The function of these outputs depend upon whether the XRT79L72 has been configured to operate in the ATM/PLCP Mode or in the Clear-Channel Framer Mode. **ATM/PLCP Mode - RxPOH:** These output pins along with the RxPOHClk, RxPOHFrame and RxPOHIns pins comprise the Receive PLCP Frame POH Byte serial output port. For each PLCP frame, that is received by the Receive PLCP Processor, this serial output port will output the contents of all 12 POH (Path Overhead) bytes. The data that is output via these pins are updated on the rising edge of the RxPOHClk output clock signals. The RxPOHFrame pin will pulse "High" whenever the first bit of the Z6 byte is being output via these output pins. **Clear-Channel Framer Mode - RxSer:** If the XRT79L72 is configured to operate in the Clear-Channel Framer/Serial Mode, then the chip will output all received data, via these output pins. These output signals will be updated upon the rising edge of RxClk. ***NOTE:*** *The user should either configure the XRT79L72 to operate in the Gapped-Clock Mode, or validate the sampling of each bit from the RxSer output with the state of RxOHInd' output pin, in order to prevent the local terminal equipment from sampling overhead bits.* These output pins are only active if the XRT79L72 has been configured to operate in the ATM/PLCP or the Clear-Channel Framer/Serial Mode. These pins are inactive for all remaining modes of operation.

PIN #	NAME	TYPE	DESCRIPTION
N4 K22	RxPOHClk_0/ RxClk_0/ RxNibClk_0 RxPOHClk_1/ RxClk_1/ RxNibClk_1	O O	**Receive PLCP Path Overhead Serial Port Clock output/Receive Nibble-Parallel Output port clock/Receive Serial Clock output:** The function of these output pins depend upon whether the XRT79L72 has been configured to operate in the ATM/PLCP Mode or the Clear-Channel Framer Mode. **ATM/PLCP Mode - RxPOH_Clk:** These output clock pins along with RxPOH, RxPOHFrame and RxPOHIns pins comprise the Receive PLCP Frame POH Byte serial output port. All POH (Path Overhead) data that is output via the RxPOH output pin is updated on the rising edge of these clock signals. ***NOTE:*** *These output signals are inactive if the XRT79L72 has been configured to operate in the Direct-Mapped ATM Mode.* **Clear-Channel Framer Mode - RxClk:** These output pins are active whenever the XRT79L72 has been configured to operate in either the Serial or Nibble Parallel Mode, as is described below.Clear-Channel Framer/Serial Mode - RxClkIn this serial mode, these outputs are a 44.736MHz clock output signal (for DS3 applications) or 34.368MHz clock output signal (for E3 applications). The Receive Payload Data Output Interface will update the data via the RxSer output pin, upon the rising edge of these clock signals. The user is advised to design (or configure) the local terminal equipment to sample the RxSer data, upon the falling edge of these clock signals. **Clear-Channel Framer/Nibble-Parallel Mode - RxNibClk:** In the Nibble-Parallel Mode, the XRT79L72 will derive these clock signals from the RxLineClk signal. The XRT79L72 will pulse these clock signals 1176 times for each inbound DS3 frame or 1074 times for each inbound E3/ITU-T G.832 frame or 384 times for each inbound E3/ITU-T G.751 frame. The Receive Payload Data Output Interface block will update the data on the RxNibn[3:0] output upon the falling edge of these clock signals. The user is advised to design (or configure) the local terminal equipment to sample the data on the RxNibn[3:0] output pins, upon the rising edge of these clock signals.
F2 A25	RxPOHFrame_0 RxPOHFrame_1	O O	**Receive PLCP Frame POH Serial Output Port - Frame Indicator:** These output pins along with the RxPOH RxPOHClk and RxPOHIns pins comprise the Receive PLCP Frame POH Byte serial output port. These output pins provide framing information to external circuitry receiving and processing this POH (Path Overhead) data, by pulsing "High" whenever the first bit of the Z6 byte is being output via the RxPOH output pins. These pins are "Low" at all other times during this PLCP POH Framing cycle. ***NOTE:*** *These output pins are only active if the XRT79L72 has been configured to operate in the ATM/PLCP Modes.*

PIN #	NAME	TYPE	DESCRIPTION
N2 J25	RxPFrame_0/ RxOHInd_0 RxPFrame_1/ RxOHInd_1	O O	**Receive PLCP Frame Indicator/Receive Overhead Indicator Output:** The function of these output pins depend upon whether the XRT79L72 has been configured to operate in the ATM/PLCP, the Clear-Channel Framer/Serial or the Clear-Channel Framer/Nibble-Parallel Modes. **ATM/PLCP Mode - RxPFrame:** These output pins pulse "High" when the Receive PLCP Processor is receiving the last bit of a PLCP frame. ***NOTE:*** *These output pins are inactive if the XRT79L72 is configured to operate in the Direct-Mapped ATM Mode.* **Clear-Channel Framer/Serial Mode - RxOHInd:** These output pins pulse "High" for one bit-period whenever an overhead bit is being output via the RxSer output pin, by the Receive Payload Data Output Interface block. ***NOTE:*** *If the user configures the XRT79L72 to operate in the Gapped-Clock Mode, then these output pins will provide a demand clock to the local terminal equipment. In the Gapped-Clock Mode, these output pins will only provide a clock pulse, whenever a payload bit is being output via the RxSer output pin. These output pins will NOT generate a clock pulse, whenever an overhead is being output via the RxSer output pin.* **Clear-Channel Framer/Nibble-Parallel - RxOHInd:** These output pins pulse "High" for one nibble-period whenever an overhead nibble is being output via the RxNibn[3:0] output pins by the Receive Payload Data Output Interface block. ***NOTE:*** *1.If the XRT79L72 device has been configured to operate in both the DS3 and the Nibble-Parallel" Modes, then the RxOHInd output pin will be in-active and will pulled "LOW" at all times.* ***NOTE:*** *2.If the XRT79L72 device has been configured to operate in both the E3 and the Nibble-Parallel" Mode, then the RxOHInd output pin will be active and will pulse "high" to denote overhead nibbles.* ***NOTE:*** *3.The purpose of this output pin is to alert the System-Side terminal equipment that an*

PIN #	NAME	TYPE	DESCRIPTION
C1 A23	RxGFC_0/ RxIdle_0 RxGFC_1/ RxIdle_1	O O	**Receive GFC Nibble Field - Output Pin/Receive Idle Sequence Indicator:** The function of these output pins depend upon whether the XRT79L72 is operating in the ATM Mode or in the High-Speed HDLC Controller Mode. **ATM Mode - RxGFC:** These pins, along with the RxGFCClk and the RxGFCMSB pins form the Receive GFC Nibble-Field serial output port. These pins will serially output the contents of the GFC Nibble field of each cell that is processed via the Receive Cell Processor. This data is serially clocked out of this pin on the rising edge of the RxGFCClk signals. The MSB of each GFC value is designated by a pulse at the RxGFCMSB output pins. **High-Speed HDLC Controller Mode - RxIdle:** The combination of the RxIdle and ValidFCS output signals are used to convey information about data that is being output via the Receive HDLC Controller output Data bus (RxHDLCDatn_[7:0]). ***If RxIdle = "High":*** The Receive HDLC Controller block will drive this output pin "High" anytime the flag sequence octet (0x7E) is present on the RxHDLCDatn[7:0] output data bus. ***If RxIdle and ValidFCS are both "High":*** The Receive HDLC Controller block has received a complete HDLC frame, and has determined that the FCS value within this HDLC frame are valid. ***If RxIdle is "High" and ValidFCS is "Low":*** The Receive HDLC Controller block has received a complete HDLC frame, and has determined that the FCS value within this HDLC frame is invalid. ***If RxIdle is "High" and ValidFCS is "Low":*** The Receive HDLC Controller block has received an ABORT sequence.
C2 B22	RxGFCClk_0 RxGFCClk_1	O O	**Received GFC Nibble Serial Output Port Clock Signal:** These output pins function as a part of the Receive GFC Nibble-Field Serial Output Port, also consisting of the RxGFC and RxGFCMSB pins. These pins provide a clock pulse which allows external circuitry to latch in the GFC Nibble-Data via the RxGFC output pin. ***NOTE:*** *These output pins are only active if the XRT79L72 is operating in the ATM UNI Mode.*
D4 A22	RxGFCMSB_0 RxGFCMSB_1	O O	**Receive GFC Nibble Field - MSB Indicator:** These output pins function as a part of the Receive GFC Nibble Field Serial Output port which also consists of the RxGFC and RxGFCClk pins. These pins pulse "High" the instant that the MSB (Most Significant Bit) of a GFC Nibble is being output on the RxGFC pin. ***NOTE:*** *These output pins are only active if the XRT79L72 is operating in the ATM UNI Mode.*

PIN #	NAME	TYPE	DESCRIPTION
D15	RxUClav/RxPPA	O	**Receive UTOPIA - Cell Available/Receive POS-PHY Interface - Packet Available:** The function of this output pin depends upon whether the XRT79L72 has been configured to operate in the ATM UNI or PPP Mode. **ATM UNI Mode - RxUClav - Receive UTOPIA Interface - Cell Available Indicator Output:** The Receive UTOPIA Interface block will assert this output pin in order to indicate that the RxFIFO has some ATM cell data that needs to be read out by the ATM Layer Processor. This signal will be asserted (e.g., toggles to a logic "HIGH" level) if the RxFIFO contains at least one full ATM cell of data. This signal toggle "low" if the RxFIFO is depleted of data, or if it contains less than one full cell of data. The exact behavior of the RxUClav output pin, as a function of "UTOPIA Level" is presented below. **Multi-PHY Operation - UTOPIA Level 2:** When the XRT79L72 device is operating in a Multi-PHY Application and is configured to operate in the UTOPIA Level 2 Mode, then this signal will be tri-stated until the RxUClk cycle following the assertion of a valid address on the Receive UTOPIA Address bus input pins (e.g., if the contents on the Receive UTOPIA Address bus pins , RxUAddr[4:0], match that which have been assigned to this particular Receive UTOPIA Interface block). Afterwards, this output pin will be driven either "high" or "low" depending upon the current fill status of the RxFIFO. **Multi-PHY Operation - UTOPIA Level 3:** When the XRT79L72 device is operating in a Multi-PHY Application, then this signal will be tri-stated until two RxUClk cycles following the assertion of a valid address on the Receive UTOPIA Address bus input pins (e.g., if the contents of the Receive UTOPIA Address bus input pins, RxUAddr[4:0], match that which have been assigned to this particular Receive UTOPIA Interface block). Afterwards, this output pin will be driven either "high" or "low" depending upon the current fill status of the RxFIFO.PPP Mode - RxPPA - Receive POS-PHY Interface - Packet Available Indicator OutputThe XRT79L72 device will drive this output pin "high" whenever a (programmable) number of bytes of incoming PPP Packet data are available to be read from the RxFIFO by the Link Layer Processor. The exact behavior of the RxPPA output pin, as a function of "POS-PHY Level" is presented below. **POS-PHY Level 2:** When the XRT79L72 device is configured to operate in the POS-PHY Level 2 Mode, then this signal will be tri-stated until the RxPClk cycle following the assertion of a valid address on the Receive POS-PHY Address bus input pins (e.g., if the contents on the Receive POS-PHY Address bus pins, RxPAddr[4:0], match that which have been assigned to this particular Receive POS-PHY Interface block). Afterwards, this output pin will be driven either "high" or "low" depending upon the current fill status of the RxFIFO. **POS-PHY Level 3:** When the XRT79L72 device is configured to operate in the POS-PHY Level 3 Mode, then this signal will be tri-stated until two RxPClk cycles following the assertion of a valid address on the Receive POS-PHY Address bus input pins (e.g., if the contents on the Receive POS-PHY Address bus pins, RxPAddr[4:0], match that which have been assigned to this particular Receive POS-PHY Interface block). Afterwards, this output pin will be driven either "high" or "low" depending upon the current fill status of the RxFIFO.
A14	RxUClkO/ RxPClkO	O	**Receive UTOPIA Interface Clock/Receive POS-PHY Interface Clock Output:** This clock output signal is derived from an internal PLL.

PIN #	NAME	TYPE	DESCRIPTION
B12	RxUClk/ RxPClk	I	**Receive UTOPIA Interface Clock Input/Receive POS-PHY Interface Clock Input:** The function of this input pin depends upon whether the XRT79L72 is operating in the ATM UNI or PPP Mode. **ATM UNI Mode - RxUClk:** The byte (or word) data, on the Receive UTOPIA Data bus (RxUData[15:0]) is updated on the rising edge of this signal. The Receive UTOPIA Interface can be clocked at rates up to 50 MHz. **PPP Mode - RxPClk:** This byte (or word) data, on the Receive POS-PHY Data Bus (RxPData[15:0]) is updated on the rising edge of this signal. The Receive POS-PHY Interface can be clocked at rates up to 50MHz. ***NOTE:*** *The user should tie this pin to GND if he/she wishes to operate the XRT79L72 device in the Clear-Channel Framer or High-Speed HDLC Controller Modes.*
A13	RxPERR	O	**Receive POS-PHY Interface - Error Indicator:** This output pin indicates whether or not the Receive PPP Packet Processor block has detect any of the following types of erred packets within the incoming PPP Packet data-stream. • Packets with FCS Errors • Aborted Packets • RUNT Packets Anytime the Receive PPP Packet Processor block detects these types of PPP Packets, then the XRT79L72 device will pulse this output pin "high" coincident to whenever the Receive POS-PHY Interface block outputs the very last byte or 16-bit word of the erred packet via the "RxPData[15:0]" output pins.The XRT79L72 device will hold this output pin "low" at all other times. ***NOTE:*** *This output pin is only valid if the XRT79L72 has been configured to operate in the PPP Mode.*
C13	RxTSX/ RxPSOF	O	**Receive - Start of Transfer/Receive - Start of PPP Packet in Chunk Mode:** The function of this output pin depends upon whether the XRT79L72 has been configured to operate in the Packet Mode or Cell-Chunk Mode. **Packet Mode - RxTSX:** The XRT79L72 pulses this output pin "High" when an inband port address is present on the RxPData[7:0] bus. When this output pin is "High", the value of RxPData[7:0] is the address value of the RxFIFO to be selected. Subsequent read operations, from RxPData[15:0] will be from the RxFIFO corresponding to this inband address. **Chunk Mode - RxPSOF:** The XRT79L72 pulses this output pin "High" in order to indicate that the first byte (or word) of a given Packet is placed on the RxPData[15:0] pins. ***NOTE:*** *This output pin is only active if the XRT79L72 has been configured to operate in the PPP Mode.*

PIN #	NAME	TYPE	DESCRIPTION
C16	$\overline{\text{RxUEN}}$/ $\overline{\text{RxPEN}}$	I	**Receive UTOPIA Interface - Output Enable/Receive POS-PHY Interface - Output Enable:** The function of this output pin depends upon whether the XRT79L72 has been configured to operate in the ATM UNI or PPP mode. **ATM UNI Mode - $\overline{\text{RxUEN}}$:** This active-low input signal is used to control the drivers of the Receive UTOPIA Data Bus. When this signal is "High" (negated) then the Receive UTOPIA Data Bus is tri-stated. When this signal is asserted, then the contents of the byte or word that is at the front of the RxFIFO will be popped and placed on the Receive UTOPIA Data bus on the very next rising edge of RxUClk. **PPP Mode - $\overline{\text{RxPEN}}$:** This active-low input signal is used to control the drivers of the Receive POS-PHY Data Bus. When this signal is "High" (negated) then the Receive POS-PHY Data Bus is tri-stated. When this signal is asserted, then the contents of the byte or word that is at the front of the RxFIFO will be popped and placed on the Receive POS-PHY Data bus on the very next rising edge of RxPClk. ***NOTE:*** *The user should tie these input pins to GND, if he/she intends to operate the XRT79L72 device in either the Clear-Channel Framer or High-Speed HDLC Controller Modes.*
A16	RxUSoC/ RxPSOP/RxP-SOC	O	**Receive UTOPIA Interface - Start of Cell Indicator/Receive POS-PHY Interface - Start of Packet Indicator:** The function of this output pin depends upon whether the XRT79L72 has been configured to operate in the ATM UNI or in the PPP Mode. **ATM UNI Mode - RxUSoC:** This output pin allows the ATM Layer Processor to determine the boundaries of the ATM cells that are output via the Receive UTOPIA Data bus. The Receive UTOPIA Interface block will assert this signal when the first byte (or word) of a new cell is present on the Receive UTOPIA Data Bus; RxUData[15:0]. **PPP Mode - RxPSOP:** This output pin allows the Link Layer Processor to determine the boundaries of the PPP packets that are output via the Receive POS-PHY Data Bus. The Receive POS-PHY Interface block will assert this signal when the first byte (or word) of a new packet is present on the Receive POS-PHY Data Bus, RxP-Data[15:0]. **PPP Chunk Mode - RxPSOC - Receive Start of Chunk Indicator Output (Chunk Mode):** If the XRT79L72 device has been configured to operate in the "Chunk Mode, then the Receive POS-PHY Interface block will pulse this output pin "high" coincident to whenever it outputs the very first byte (or 16-bit word) of a given Chunk onto the Receive POS-PHY Data Bus (RxPData[15:0]) output pins. The Receive POS-PHY Interface block will keep this output pin "low" at all other times. ***NOTE:*** *In the "PPP Chunk" Mode, the RxPSOF output pin will function as the "Start of Packet" Output Indicator pin.*

PIN #	NAME	TYPE	DESCRIPTION
B16	RxUPrty/ RxPPrty	O	**Receive UTOPIA Interface - Parity Output pin/Receive POS-PHY Interface - Parity Output:** The function of this output pin depends upon whether the XRT79L72 has been configured to operate in the ATM UNI or the PPP Modes. **ATM UNI Mode - RxUPrty:** The Receive UTOPIA interface block will compute the odd-parity value of each byte (or word) that it will place in the Receive UTOPIA Data Bus. This odd-parity value will be output on this pin, while the corresponding byte (or word) is present on the Receive UTOPIA Data Bus **PPP Mode - RxPPrty:** The Receive POS-PHY Interface block will compute the odd-parity value of each byte (or word) that it will place in the Receive POS-PHY Data Bus. This odd parity value will be output on this pin, which the corresponding byte (or word) is present on the Receive POS-PHY Data Bus. ***NOTE:*** *This output pin will be in-active if the user has configured the XRT79L72 device to operate in either the Clear-Channel Framer or in the High-Speed HDLC Controller Modes.*
E13	RxPEOP	O	**Receive POS-PHY Interface - End of Packet:** The XRT79L72 drives this output pin "High" whenever the last byte of a given Packet is being output via the RxPData[15:0] data bus. ***NOTES:*** 1. *This output pin is only valid when the XRT79L72 is configured to operate in the PPP Mode.* 2. *This output pin is only valid when the Receive POS-PHY Interface - Read Enable Output pin.*
A9	RxPDVAL	O	**Receive POS-PHY Interface Signal Valid Indicator:** This output signal indicates whether or not the Receive POS-PHY Interface signals (e.g., PRData[15:0], RxPSOP, RxPEOP, RxPPrty, RxPERR) are valid. This output pin will be driven "High", when these signals are valid. Conversely, this output pin will be driven "Low" when these signals are NOT valid. ***NOTE:*** *This output pin is only active if the XRT79L72 has been configured to operate in the PPP Mode.*

PIN #	NAME	TYPE	DESCRIPTION
B14 C14 A15 B15 C15	RxAddr_0 RxAddr_1 RxAddr_2 RxAddr_3 RxAddr_4	I	**Receive UTOPIA Interface Address Bus input pins/Receive POS-PHY Interface Address Bus Input pins:** The exact function of these input pins depends upon whether the XRT79L72 device has been configured to operate in the ATM UNI or PPP Modes. **ATM UNI Modes - RxUAddr[4:0] - Receive UTOPIA Address Bus:** These input pins functions as the Receive UTOPIA Address bus inputs. These input pins are only active when the XRT79L72 device is operating in both the ATM UNI and Multi-PHY Modes. Whenever the ATM Layer Processor wishes to poll or read data from a particular UNI (PHY-Layer) device, it will provide the "UTOPIA Address" of the "target" PHY-Layer device on the Receive UTOPIA Address Bus. The Receive UTOPIA Address Bus input is sampled on the rising edge of the RxUClk signal. Each time the Receive UTOPIA Interface block samples the "Receive UTOPIA Address Bus", the contents of this address bus are compared with the pre-programmed UTOPIA Address value (which was loaded into the XRT79L72 device by writing the appropriate data into both the "Receive UTOPIA Port Address" Register (Address = 0x0513) and the "Receive UTOPIA Port Number" Register (Address = 0x0517). If these two values match, and the RxUENB* input pin is asserted, then the RxUClav output pin will be driven to the appropriate state (based upon the RxFIFO fill level). If these two address values do not match, then the Receive UTOPIA Interface block will continue to tri-state the "RxUClav" output pin. ***NOTE:*** *These input pins are only active if the XRT79L72 device has been designed into a "Multi-PHY" Application. If the user intends to design the XRT79L72 device into a "Single-PHY" Application, then he/she should tie these input pins to GND.* **PPP Mode - RxPAddr[4:0] - Receive POS-PHY Interface Address Bus Input Pins:** These input pins comprise the Receive POS-PHY Address Bus input pins. Whenever the Link Layer Processor wishes to poll or read PPP packet data from a particular PHY-Layer device, it will provide the address of the "target PHY-Layer device" on the Receive POS-PHY Address Bus. The contents of the Receive POS-PHY Address Bus input pins are sampled on the rising edge of RxPClk. The XRT79L72 device will compare the data on the Receive POS-PHY Address Bus with the pre-programmed POS-PHY Address value (which was loaded into the XRT79L72 device by writing the appropriate data into the "Receive POS-PHY Interface - Receive Control Register - Byte 0" (Address = 0x0502). If these two values are identical and the "RxPENB*" input pin is asserted, then the RxPPA output pin will be driven to the appropriate state (based upon the RxFIFO fill-level). If these two values do not match, then the Receive POS-PHY Interface block will continue to tri-state the "RxPPA" output pin. ***NOTE:*** *These input pins are only active if the XRT79L72 device has been configured to operate in either the ATM UNI or PPP Modes. The user should tie these input pins to GND if he/she wishes to operate the XRT79L72 device in either the "Clear-Channel Framer" or "High-Speed HDLC Controller" Modes.*

PIN #	NAME	TYPE	DESCRIPTION
A17 B17 C17 E17 A18 B18 C18 A19 B19 C19 D19 A20 B20 C20 A21 B21	RxUData_0/ RxPData_0 RxUData_1/ RxPData_1 RxUData_2/ RxPData_2 RxUData_3/ RxPData_3 RxUData_4/ RxPData_4 RxUData_5/ RxPData_5 RxUData_6/ RxPData_6 RxUData_7/ RxPData_7 RxUData_8/ RxPData_8 RxUData_9/ RxPData_9 RxUData_10/ RxPData_10 RxUData_11/ RxPData_11 RxUData_12/ RxPData_12 RxUData_13/ RxPData_13 RxUData_14/ RxPData_14 RxUData_15/ RxPData_15	O	**Receive UTOPIA Data Bus Input/Receive POS-PHY Data Bus Output pins:** The function of these output pins depends upon whether the XRT79L72 has been configured to operate in the ATM UNI or in the PPP Mode. **ATM UNI Mode - RxUData[15:0]:** These output pins function as the Receive UTOPIA Data Bus. ATM cell data that has been received from the Remote Terminal Equipment is output on the Receive UTOPIA Data Bus, where it can be read and processed by the ATM Layer Processor. **PPP Mode - RxPData[15:0]:** These output pins function as the Receive POS-PHY Data Bus output pins. PPP Packet data that has been received from the Remote Terminal Equipment is output on the Receive POS-PHY Data Bus, where it can be reads and processed by the Link Layer Processor.
B13	RxMod	O	**Receive PPP Data Bus - Modulus Indicator:** The XRT79L72 will indicate the number of valid packet octets that are being read out of the RxPData[15:0] output pins. The XRT79L72 will drive this output pin "Low" when both bytes of the RxPData[15:0] data bus consists of valid packet data. Conversely, the XRT79L72 will drive this output pin "High" when only the upper byte of the RxPData[15:0] data bus consists of valid packet data. The Link Layer Processor is expected to validate all packet data that it reads out of the RxPData[15:0] output pins by also reading the state of this output pin. ***NOTE:*** *This output pin is only active if the XRT79L72 has been configured to operate in the PPP Mode.*

PIN #	NAME	TYPE	DESCRIPTION
TRANSMIT LINE SIDE SIGNALS			
AE4	TxON	I	**Transmit Driver ON - Channel n:** This input pin is used to either enable or disable the Transmit Output Drivers of the XRT79L72. "Low" - Disables the XRT79L72 Transmit Output Drivers. In this setting, the TTIP and TRING output pins will be tri-stated. "High" - Enables the XRT79L72 Transmit Output Drivers if the individual register bits are set to "1". In this setting, the TTIP and TRING output pins will be enabled. ***NOTES:*** *1. Whenever the transmitters are turned off , the TTIP and TRING output pins will be tri-stated.* *2. These pins are internally pulled high.*
Y5	DS3CLK/ SFMCLK	I	**Clock Recovery PLL DS3 Reference Clock Input/12.288MHz SFM Reference Clock Input:** The exact function of this input pin depends upon whether or not the XRT79L72 device has been configured to operate in the SFM (Single Frequency Mode) Mode, as described below. If the XRT79L72 device is NOT operating in the Single-Frequency ModeIf the XRT79L72 has NOT been configured to operate in the SFM Mode, then this input pin will functions as the Reference Clock for the Clock Recovery PLL and the Jitter Attenuator PLL within the Receive DS3/E3 LIU Block, whenever the XRT79L72 device has been configured to operate in the DS3 Mode. ***NOTE:*** *For DS3/Non-SFM Modes of operation, the user is expected to supply a 44.736MHz ± 20ppm clock signal to this input pin.If the XRT79L72 device is operating in the Single-Frequency Mode* If the user has configured the XRT79L72 device to operate in the SFM Mode, then the user MUST apply a clock signal with a frequency of 12.288MHz ± 20ppm to this input pin. The SFM Synthesizer block (within the Receive DS3/E3 LIU Block) will then synthesize one of the appropriate line rate frequencies (e.g., 34.368MHz for E3 and 44.736MHz for DS3) based upon this 12.288MHz Reference Clock source. ***NOTE:*** *If the user does not intend to operate the XRT79L72 device in the SFM Mode, nor the DS3 Mode, then he/she should tie this input pin to GND.*

PIN #	NAME	TYPE	DESCRIPTION
Y1	E3CLK	I	**Clock Recovery PLL E3 Reference Clock Input:** The exact function of this input pin depends upon whether or not the XRT79L72 device has been configured to operate in the SFM (Single-Frequency Mode) Mode, as described below.If the XRT79L72 device is NOT operating in the Single-Frequency ModeIf the XRT79L72 device has NOT been configured to operate in the SFM Mode, then this input pin will function as a Reference Clock signal for the Clock Recovery PLL and the Jitter Attenuator PLL within the Receive DS3/E33 LIU Block, whenever the XRT79L72 device has been configured to operate in the E3 Mode. ***NOTE:*** *For E3/Non-SFM Modes of operation, the user is expected to supply a 34.368MHz ± 20ppm clock signal to this input pin.* If the XRT79L72 device is operating in the Single-Frequency ModeIf the user has configured the XRT79L72 device to operate in the SFM Mode, then the user MUST apply a clock signal with a frequency of 12.288 ± 20ppm to the "DS3CLK/SFMCLK" input pin (Ball Y5). Additionally, the user MUST tie this input pin to GND. ***NOTE:*** *If the user only intends to operate the XRT79L72 device in the DS3/Non-SFM Mode, then the user should tie this input pin to GND.*
AD10 AD14	TTIP_0 TTIP_1	O O	**Transmit Output - Positive Polarity Signal:** These output pins, along with the TRING output pins, function as the Transmit DS3/E3 output signal drivers for the XRT79L72. The user is expected to connect these signals and the TRING output signals to a 1:1 transformer. Whenever the Transmit Section of the XRT79L72 generates and transmits a positive-polarity pulse onto the line, these output pins will be pulsed to a "higher-voltage" than the TRING output pins. Conversely, whenever the Transmit Section of the XRT79L72 generates and transmit a negative-polarity pulse onto the line, these output pins will be pulsed to a "lower-voltage" than the TRING output pins. ***NOTE:*** *These output pins will be tri-stated whenever the user sets the TxONn input pin (or bit-field) to "0".*
AE10 AE14	TRING_0 TRING_1	O O	**Transmit Output - Negative Polarity Signal:** These output pins along with the TTIP output pins, function as the Transmit DS3/E3 output signal drivers for the XRT79L72. The user is expected to connect these signals and the TTIP output signals to a 1:1 transformer. Whenever the Transmit Section of the XRT79L72 generates and transmits a positive-polarity pulse onto the line, these output pins will be pulsed to a "lower-voltage" than the TTIP output pins. Conversely, whenever the Transmit Section of the XRT79L72 generates and transmit a negative-polarity pulse onto the line, these output pins will be pulsed to a "higher-voltage" than the TTIP output pins. ***NOTE:*** *These output pins will be tri-stated whenever the user sets the TxONn input pin (or bit-field) to "0".*

PIN #	NAME	TYPE	DESCRIPTION
AE2 Y23	TAISEN_0 TAISEN_1	I I	**Transmit Alarm Indication Signal Enable Input** This input pin permits the user to command the Transmit DS3/E3 Framer block to transmit an AIS pattern to the remote terminal equipment. Setting this input pin "high" configures the Transmit DS3/E3 Framer block to transmit AIS pattern to the remote terminal equipment. Setting this input pin "low" configures the Transmit DS3/E3 Framer block to NOT transmit an AIS pattern to the remote terminal equipment. ***NOTE:*** *For normal operation, or if the user wishes to control the "Transmit AIS" function via Software Control, the user should tie this input pin to GND.*
AE11 AE15	MTIP_0 MTIP_1	I I	**Transmit Drive Monitor Input pin - Positive Polarity Input:** These input pins along with MRING function as the Transmit Drive Monitor Output (DMO) input monitoring pins. If the user wishes to (1) monitor the Transmit Output line signal and (2) to perform this monitoring externally, then the user MUST connect these particular pins to the TTIPn output pin via a 274Ω series resistor. Similarly, the user MUST also connect the MRINGn input pin to the TRINGn output pin via a 274Ω series resistor. The MTIPn and MRINGn input pins will continuously monitor the Transmit Output line signal via the TTIPn and TRINGn output pins for bipolar activity. If these pins do not detect any bipolar activity for 128 bit periods, then the Transmit Drive Monitor circuit will drive the DMOn output pin "High" in order to denote a possible fault condition in the Transmit Output Line signal path. ***NOTE:*** *These input pins are inactive if the user choose to internally monitor the Transmit Output line signal.*
AD11 AD15	MRING_0 MRING_1	I I	**Transmit Drive Monitor Input pin - Positive Polarity Input:** These input pins along with MTIP function as the Transmit Drive Monitor Output (DMO) input monitoring pins. If the user wishes to (1) monitor the Transmit Output line signal and (2) to perform this monitoring externally, then the user MUST connect these particular pins to the TRINGn output pin via a 274Ω series resistor. Similarly, the user MUST also connect the MTIPn input pin to the TTIPn output pin via a 274Ω series resistor. The MTIPn and MRINGn input pins will continuously monitor the Transmit Output line signal via the TTIPn and TRINGn output pins for bipolar activity. If these pins do not detect any bipolar activity for 128 bit periods, then the Transmit Drive Monitor circuit will drive the DMOn output pin "High" in order to denote a possible fault condition in the Transmit Output Line signal path. *3. These input pins are inactive if the user choose to internally monitor the Transmit Output line signal.*

PIN #	NAME	TYPE	DESCRIPTION
RECEIVE LINE SIDE SIGNALS			
AD12 AD16	RTIP_0 RTIP_1	I I	**Receive Input - Positive Polarity Signal:** These input pins, along with the RRINGn input pins, function as the Receive DS3/E3 Line input signal receiver of the XRT79L72. The user is expected to connect these signals and the RRINGn input signals to a 1:1 transformer. Whenever the RTIP/RRING input pins are receiving a positive-polarity pulse within the incoming DS3 or E3 line signal, these input pins will be pulsed to a "higher-voltage" than the RRING input pins. Conversely, whenever the RTIP/RRING input pins are receiving a negative-polarity pulse within the incoming DS3 or E3 line signal, these input pins will be pulsed to a "lower-voltage" than the RRING input pins.

PIN #	NAME	TYPE	DESCRIPTION
AC12 AC16	RRING_0 RRING_1	I I	**Receive Input - Negative Polarity Signal:** These input pins, along the RTIPn input pins, function as the Receive DS3/E3 Line input signal receiver for the XRT79L72. The user is expected to connect these signals and the RTIPn input signals to a 1:1 transformer. Whenever the RTIP/RRING input pins are receiving a positive-polarity pulse within the incoming DS3 or E3 line signal, then these input pins will be pulsed to a "lower-voltage" than the RTIP input pins. Conversely, whenever the RTIP/RRING input pins are receiving a negative-polarity pulse within the incoming DS3 or E3 line signal, then these input pins will be pulsed to a "higher-voltage" than the RTIP input pins.
K2 G26	CLKOUT_0 CLKOUT_1	O O	**SFM Synthesizer/Clock Recovery PLL Reference Clock Output:** The exact source of this output signal depends upon whether the XRT79L72 device has been configured to operate in the SFM (Single-Frequency Mode) Mode, or not, as described below.If the XRT79L72 device is configured to operate in the SFM ModeIf the XRT79L72 device has been configured to operate in the SFM Mode, then the CLKOUT output pin (if enabled) will output a 44.736MHz clock signal (if the XRT79L72 device is configured to operate in the DS3 Mode) or a 34.368MHz clock signal (if the XRT79L72 device is configured to operate in the E3 Mode. ***NOTE:*** *1.In this case, the 44.736MHz or 33.368MHz clock (that is output via the CLKOUT signal) will ultimately be derived from the 12.288MHz clock signal that is being applied to the DS3CLK/SFMCLK input pin.* ***NOTE:*** *2.This output pin is only active if Bit 6 (SFM Clock Out Enable), within the LIU Channel Control Register (Address = 0x1306) has been set to "1".* If the XRT79L72 device is NOT configured to operate in the SFM ModeIf the XRT79L72 device has NOT been configured to operate in the SFM Mode, then frequencies of the CLKOUT output signal will be as follows. • If the XRT79L72 device has been configured to operate in the DS3 Mode, then the XRT79L72 device will simply output a buffered version of the signal that is being applied to the DS3CLK/SFMCLK input pin (which should be a 44.736MHz clock signal). • If the XRT79L72 device has been configured to operate in the E3 Mode, then the XRT79L72 device will simply output a buffered version of the signal that is being applied to the E3CLK input pin (which should be a 34.368MHz clock signal). ***NOTE:*** *This output pin is only if Bit 6 (SFM Clock Out Enable), within the "LIU Channel Control" Register (Address = 0x1306) has been set to "1".*

NAME	TYPE	DESCRIPTION
POWER PINS		
VDD	PWR	**3.3V Power Supply Pins** D6, D8, D9, D10, D12, D13, D14, D16, D17, D18, D20, L4, L23, M11, M12, M15, M16, N11, N12, N15, N16, P11, P12, P15, P16, R11, R12, R15, R16, T4, T23, AA4, AA23, AB8, AB18, AB20, AC7, AC19, AE9, AE21, AF6, AF9, AF13, AF17, AF18, AF21
JAAVDD	PWR	**3.3V Jitter Attenuator Analog Power Supply Pin** AE13, AE17
REFAVDD	PWR	**3.3V Reference Analog Power Supply Pin** AB13
RXAVDD	PWR	**3.3V Receive Analog Power Supply Pin** AB12, AB16, C10, C12
TXDVDD	PWR	**3.3V Transmit Digital Power Supply Pin** AF10, AF14
TXAVDD	PWR	**3.3V Transmit Analog Power Supply Pin** AC11, AC15

NAME	TYPE	DESCRIPTION
GROUND PINS		
GND	GND	**Ground Pins** A10, A12, E6, E7, E8, E10, E11, E12, E14, E15, E16, E18, E19, E20, F5, F22, L5, L11, L12, L13, L14, L15, L16, L22, M13, M14, N13, N14, P13, P14, R13, R14, T5, T11, T12, T13, T14, T15, T16, T22, AA5, AA22, AC6, AC18, AD9, AD21, AE8, AE20, AE22, AF7, AF19, AF8, AF12, AF16, AF20
JAAGND	GND	**3.3V Jitter Attenuator Analog Ground Pin** AD13, AD17
REFAGND	GND	**3.3V Reference Analog Ground Pin** AB14
RXAGND	GND	**3.3V Receive Analog Ground Pin** AE12, AE16
TXDGND	GND	**3.3V Transmit Digital Ground Pin** AC10, AC14
TXAGND	GND	**3.3V Transmit Analog Ground Pin** AF11, AF15

NAME	TYPE	DESCRIPTION
NO CONNECT PINS		
NC	NC	A24, B23, B24, B26, C22, C23, C25, C26, D1, D2, D3, D24, D25, D26, E1, E4, E23, E24, F4, F23, G4, G5, G22, G23, G24, G25, H1, H2, H3, H4, H5, H25, H26, J1, K3, K4, K5, K23, K24, K25, K26, L1, L2, L3, L24, L25, L26, N5, M22, M23, P1, P2, P3, P4, P5, P22, P23, P24, P25, P26, R3, R4, R5, R24, R25, R26, U1, U2, V1, V2, V3, V4, V5, V26, W5, W22, W23, W24, Y2, Y3, Y4, Y24, Y25, Y26, AA25, AB2, AB3, AB4, AB7, AB9, AB10, AB11, AB15, AB17, AB19, AB21, AC1, AC3, AC8, AC9, AC20, AC21, AD1, AD3, AD6, AD7, AD8, AD18, AD19, AD20, AE1, AE3, AE6, AE7, AE18, AE19, AE26, AF2, AF3, AF26

ELECTRICAL CHARACTERISTICS

TABLE 1: DC ELECTRICAL CHARACTERISTICSS

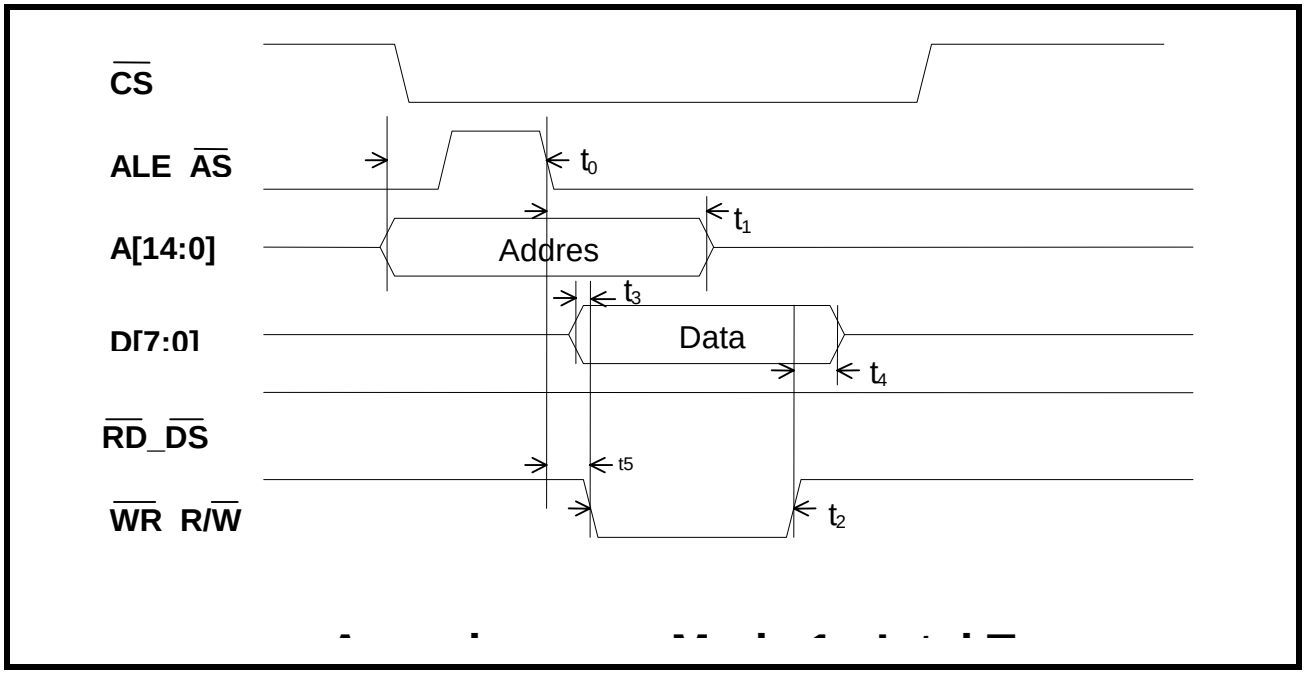
APPLIES TO ALL TTL-LEVEL INPUT AND CMOS LEVEL OUTPUT PINS - AMBIENT TEMPERATURE = 25°C						
SYMBOL	PARAMETER	TEST CONDITION		MIN	MAX	UNITS
VDDQ	I/O Supply Voltage			3.135	3.465	V
VIH	High-Level Input Voltage	VOUT ³ VOH(min)		2.0	VDD + 0.3	V
VIL	Low-Level Input Voltage	VOUT < VOL (max)		-0.3	0.3*VDD	V
VOH	High-Level Output Voltage	VDD = MIN VIN = VIH	IOH = -2mA	1.9		V
VOL	Low-Level Output Voltage	VDD = MIN VIN = VIL	IOL = 2mA		0.6	V
II	Input Current	VDD = MAX VIN = VDD or GND			±15	mA

AC ELECTRICAL CHARACTERISTIC INFORMATION

MICROPROCESSOR INTERFACE TIMING FOR REVISION A SILICON

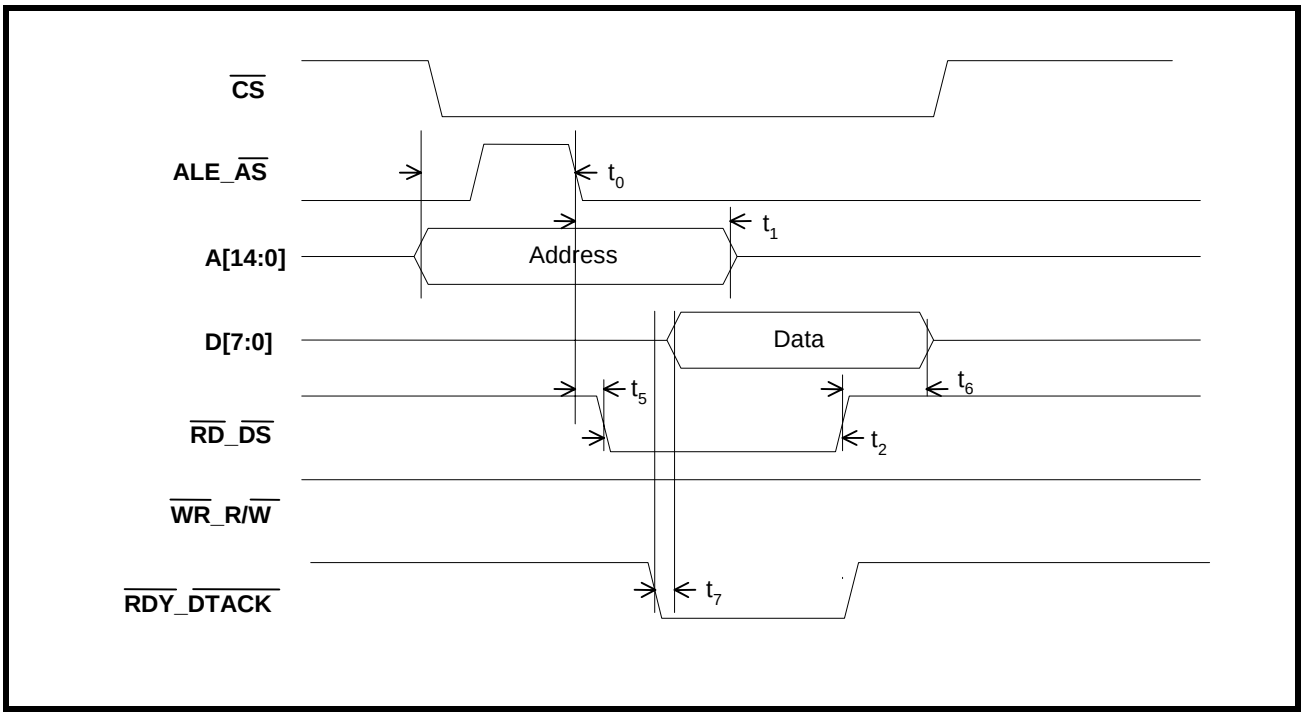
MICROPROCESSOR INTERFACE TIMING - ASYNCHRONOUS INTEL MODE

FIGURE 2. ASYNCHRONUS MODE 1 - INTEL TYPE PROGRAMMED I/O TIMING (WRITE CYCLE)



NOTE: *The values for "t0" through "t7", in this figure can be found in Table 2.*

FIGURE 3. ASYNCHRONUS MODE 1 - INTEL TYPE PROGRAMMED I/O TIMING (READ CYCLE)



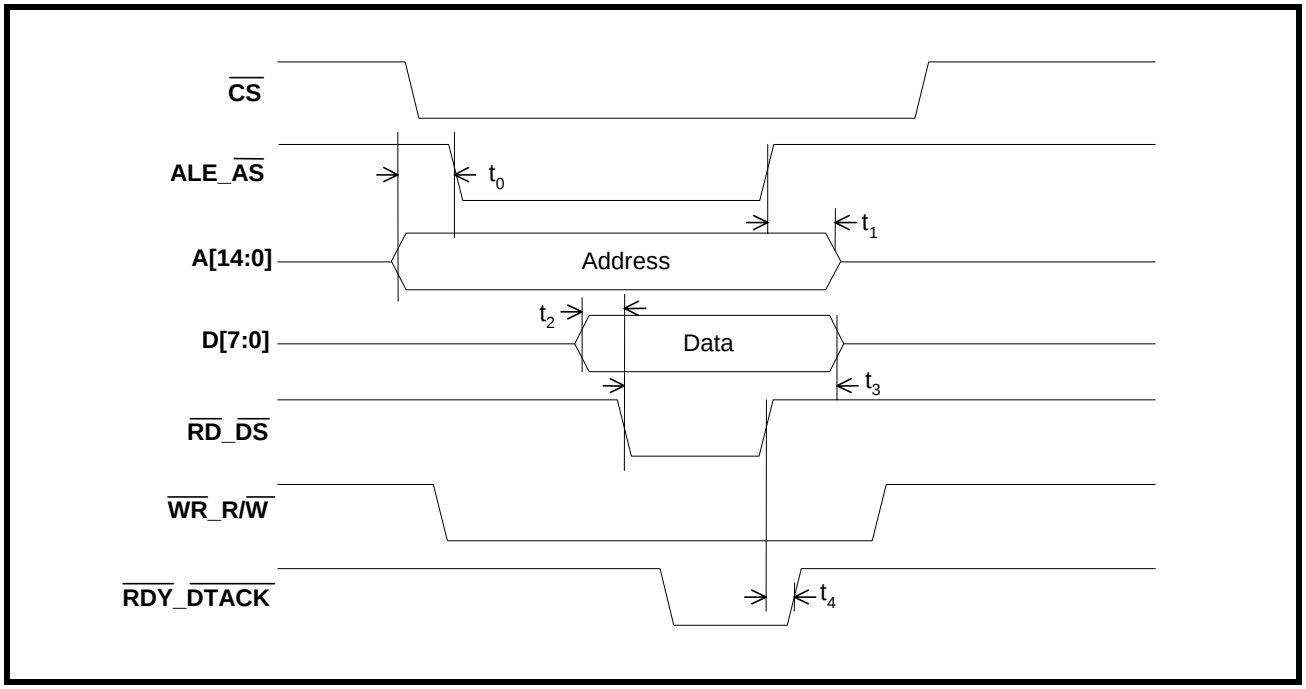
NOTE: The values for "t0" through "t7", in this figure can be found in Table 2.

TABLE 2: TIMING INFORMATION FOR THE MICROPROCESSOR INTERFACE, WHEN CONFIGURED TO OPERATE IN THE INTEL ASYNCHRONOUS MODE

Test Conditions: TA = 25°C, VCC = 3.3V±5% and 2.5V±5%, unless otherwise specified.				
TIMING	**DESCRIPTION**	**MIN.**	**TYP.**	**MAX.**
t0	Address setup time to pALE low	4	-	-
t1	Address hold time from pALE low	4	-	-
t2	pRD_L, pWR_L pulse width	320	-	-
t3	Data setup time to pWR_L low	0	-	-
t4	Data hold time from pWR_L high	0	-	-
t5	pALE low to pRD_L, pWR_L low	5	-	-
t6	Data invalid from pRD_L high	4	-	-
t7	Data valid from pRDY_L low	-	-	0
t8	pRDY inactive from pRD_L inactive	3		9

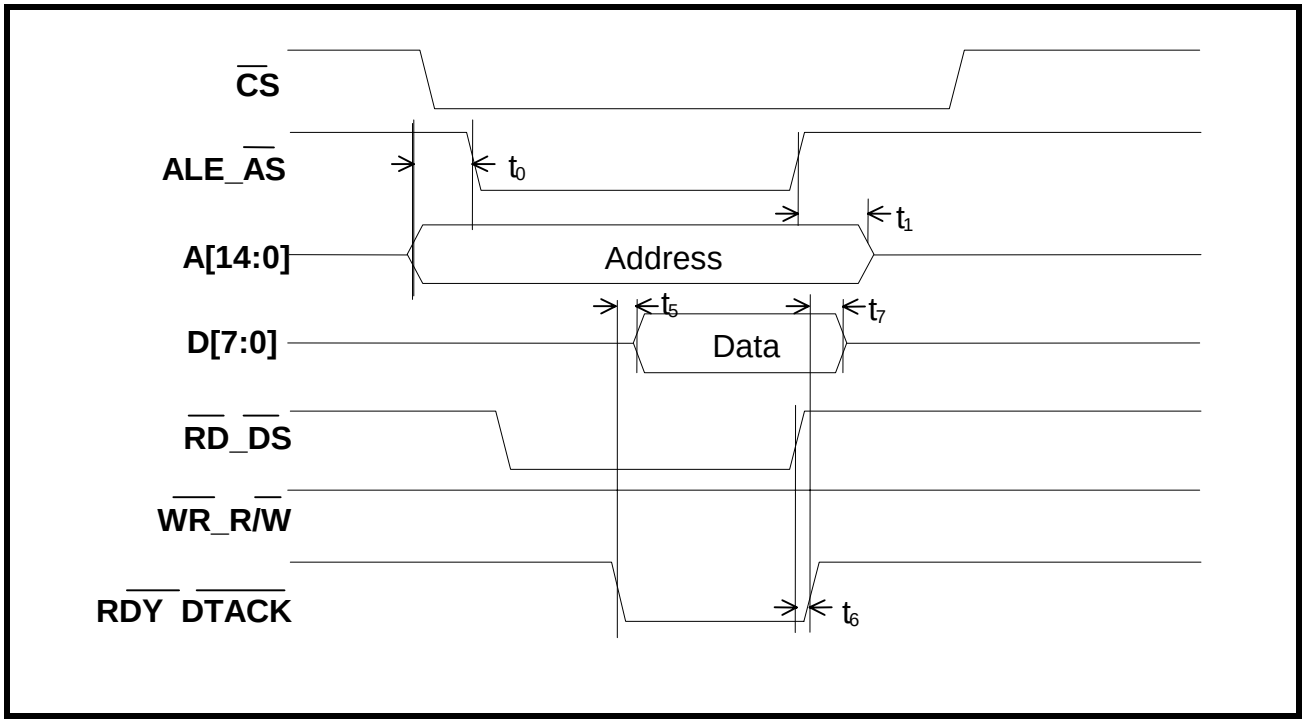
MICROPROCESSOR INTERFACE TIMING - ASYNCHRONOUS MOTOROLA (68K) MODE

FIGURE 4. ASYNCHRONUS MODE 2 - MOTOROLA 68K PROGRAMMED I/O TIMING (WRITE CYCLE)



NOTE: The values for "t0" through "t7" can be found in Table 3.

FIGURE 5. ASYNCHRONUS MODE 2 - MOTOROLA 68 PROGRAMMED I/O TIMING (READ CYCLE)



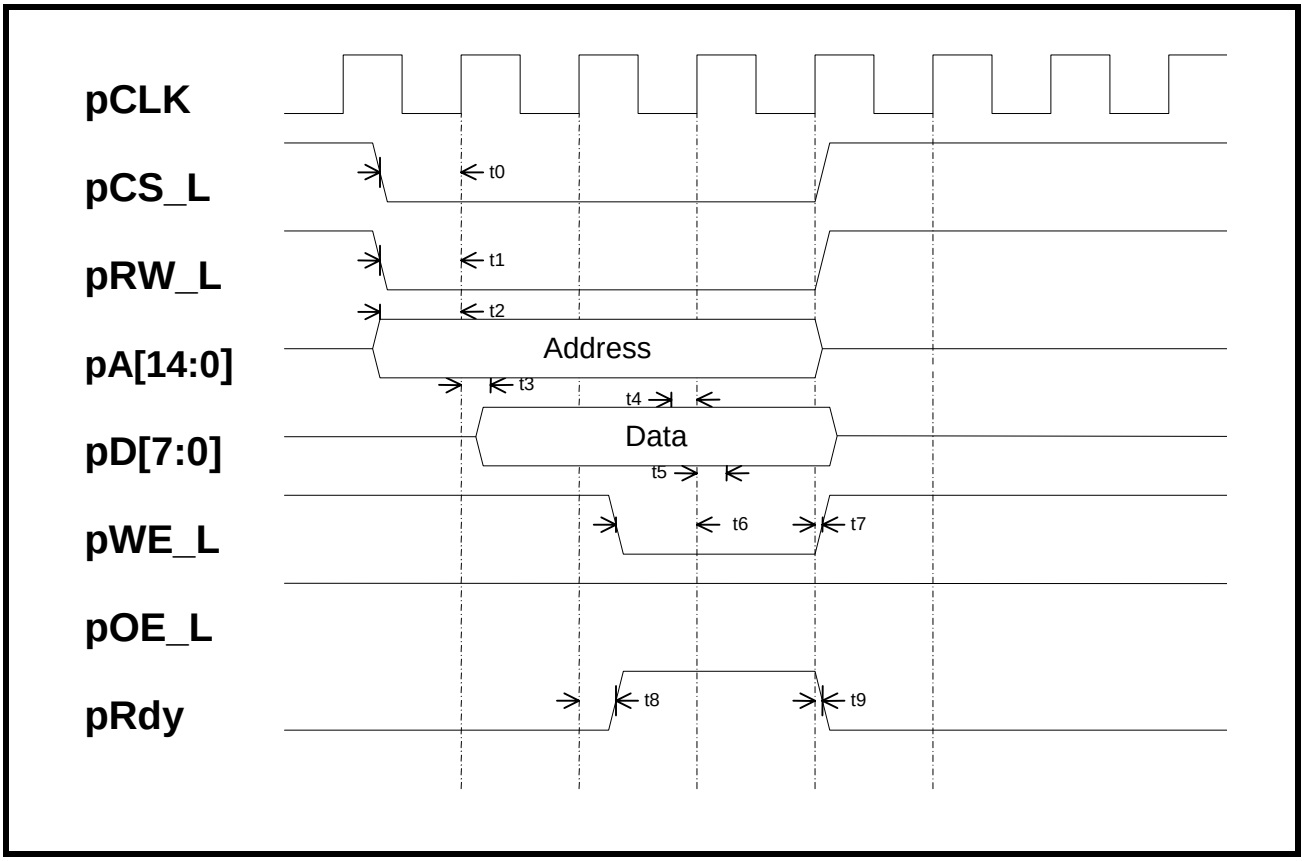
NOTE: The values for "t0" through "t7" can be found in Table 3.

TABLE 3: TIMING INFORMATION FOR THE MICROPROCESSOR INTERFACE WHEN CONFIGURED TO OPERATE IN THE MOTOROLA (68K) ASYNCHRONOUS MODE

Test Conditions: TA = 25°C, VCC = 3.3V±5% and 2.5V±5%, unless otherwise specified.				
TIMING	**DESCRIPTION**	**MIN.**	**TYP.**	**MAX**
t0	Address setup time to pALE low	6	-	-
t1	Address hold time to pALE high	6	-	-
t2	Data setup time to pDS_L low	0	-	-
t3	Data hold time to pDS_L low	160	-	-
t4	pDS_L high to pRDY_L high (Write Cycle)	-	-	16
t5	pRDY_L low to Data valid	-	-	15
t6	pDS_L high to pRDY_L high (Read Cycle)	-	-	16
t7	pRDY_L high to Data invalid	3	-	-

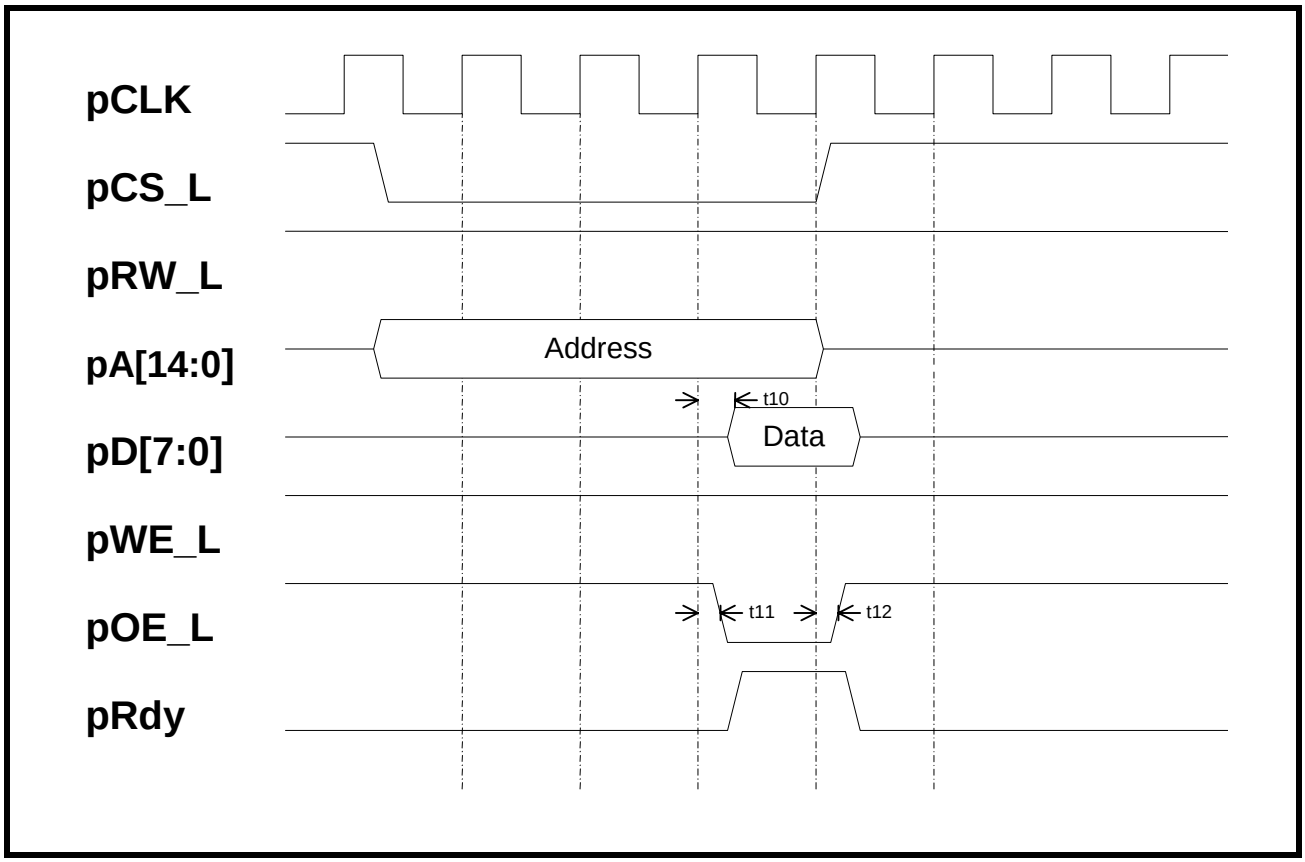
MICROPROCESSOR INTERFACE TIMING - POWER PC 403 SYNCHRONOUS MODE

FIGURE 6. SYNCHRONOUS MODE 3 - IBM POWERPC 403 INTERFACE TIMING (WRITE CYCLE)



NOTE: *The value for "t0" through "t12" can be found in Table 4.*

FIGURE 7. SYNCHRONOUS MODE 3 - IBM POWERPC 403 INTERFACE TIMING (READ CYCLE)



NOTE: The value for "t0" through "t12" can be found in Table 4.

TABLE 4: TIMING INFORMATION FOR THE MICROPROCESSOR INTERFACE, WHEN CONFIGURED TO OPERATE IN THE IBM POWER PC403 MODE

Test Conditions: TA = 25°C, VCC = 3.3V±5% and 2.5V±5%, unless otherwise specified.				
TIMING	**DESCRIPTION**	**MIN.**	**TYP.**	**MAX.**
t0	pCS_L low to PCLK high	4	-	-
t1	pRW_L low to PCLK high	9	-	-
t2	Address setup time to PCLK high	4	-	-
t3	Address hold time from PCLK high	2	-	-
t4	Data setup time (WRITE cycle)	4	-	-
t5	Data hold time (WRITE cycle) from PCLK High	0	-	-
t6	pWE_L low to Clock high	4	-	-
t7	Clock high to pWE_L high from PCLK high	0	-	-
t8	Clock high to pRDY high	4.4	-	10.5
t9	Clock high to pRDY low	4.2	-	10.4
t10	Clock high to Data valid (READ cycle)	-	-	11

TABLE 4: TIMING INFORMATION FOR THE MICROPROCESSOR INTERFACE, WHEN CONFIGURED TO OPERATE IN THE IBM POWER PC403 MODE

Test Conditions: TA = 25°C, VCC = 3.3V±5% and 2.5V±5%, unless otherwise specified.				
TIMING	**DESCRIPTION**	**MIN.**	**TYP.**	**MAX.**
t11	Clock high to pOE_L low	11	-	-
t12	Clock high to pOE_L high	1.5	-	4.1

DS3/E3 LIU INTERFACE - LINE SIDE ELECTRICAL CHARACTERISTIC INFORMATION

E3 LINE SIDE PARAMETERS

The XRT79L72 line output at the Transmit Output complies with the pulse template requirements as specified in ITU-T G.703 for 34.368Mbps operation. The pulse mask as specified in ITU-T G.703 for 34.368Mbps is shown below in Figure 8.

FIGURE 8. PULSE MASK FOR E3 (34.368MBPS) INTERFACE AS PER ITU-T G.703

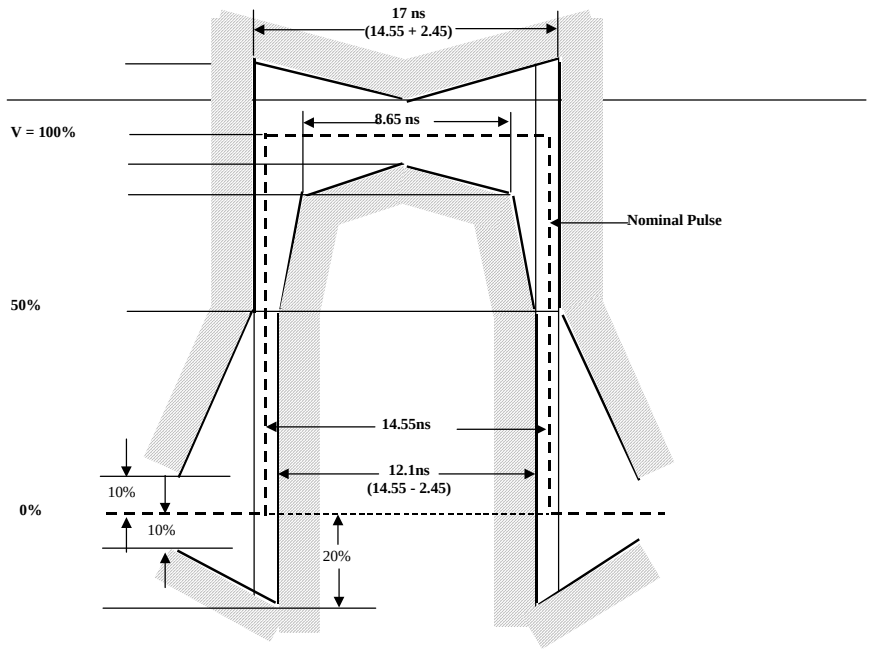


TABLE 5: E3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (Measured at secondary of the transformer)	0.9	1.0	1.1	V_{pk}
Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
Transmit Output Pulse Width	12.5	14.55	16.5	ns
Transmit Intrinsic Jitter (without Jitter Attenuator in theTransmit path)		0.01	0.015	UI_{PP}
Transmit Intrinsic Jitter (with Jitter Attenuator in the Transmit path)		0.02	0.03	UI_{PP}

TABLE 5: E3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1200		feet
Interference Margin	-20	-14		dB
Jitter Tolerance @ Jitter Frequency 800KHz	0.15	0.28		UI_{PP}
Signal level to Declare Loss of Signal			-35	dB
Signal Level to Clear Loss of Signal	-15			dB
Occurence of LOS to LOS Declaration Time	10		255	UI
Termination of LOS to LOS Clearance Time	10		255	UI

DS3 LINE SIDE PARAMETERS

The XRT79L72 will output pulses that comply with the Isolated DSX-3 Pulse Template requirements per Bellcore GR-499-CORE. The pulse mask as specified in Bellcore GR-499-CORE is shown below in Figure 9. Additionally, the Equations that define both the "Upper" and "Lower" curves of the Pulse Template requirement is presented below in Table 6.

FIGURE 9. BELLCORE GR-499-CORE PULSE TEMPLATE REQUIREMENTS FOR DS3 APPLICATIONS

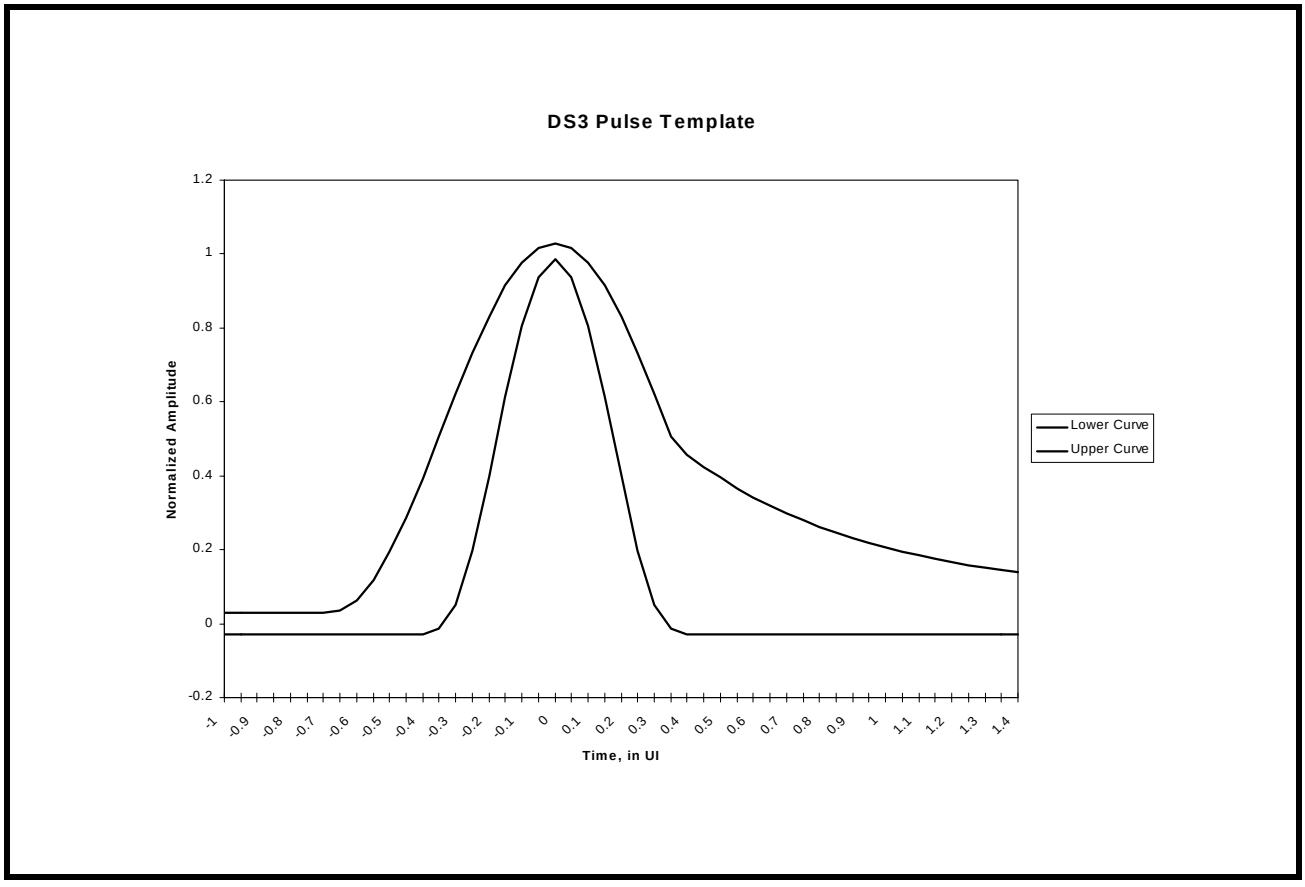


TABLE 6: DS3 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.36$	- 0.03
$-0.36 \leq T \leq 0.36$	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right\}\right] - 0.03$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.36$	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right\}\right] + 0.03$
$0.36 \leq T \leq 1.4$	$0.08 + 0.407 \times e^{-1.84[T-0.36]}$

TABLE 7: DS3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-499)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)	0.65	0.75	0.85	V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.9	1.0	1.1	V_{pk}
Transmit Output Pulse Width	10.10	11.18	12.28	ns
Transmit Output Pulse Amplitude Ratio	0.9	1.0	1.1	
Transmit Intrinsic Jitter (without Jitter Attenuator in Transmit path)		0.01	0.015	UI_{pp}
Transmit Intrinsic Jitter (withJitter Attenuator in Transmit path)		0.02	0.04	UI_{pp}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ 400 KHz (Cat II)	0.15			UI_{pp}
Signal Level to Declare Loss of Signal	Refer to Table 10			
Signal Level to Clear Loss of Signal	Refer to Table 10			

TRANSMIT UTOPIA INTERFACE

The purpose of the Transmit UTOPIA Interface block is to function as either a Standard UTOPIA Level 1, 2 or 3 Interface as it accepts ATM cell data from either an ATM Layer or ATM Adaptation Layer Processor, and routes this ATM cell data to the TxFIFO within the XRT79L72.

FIGURE 10. TIMING DIAGRAM FOR THE TRANSMIT UTOPIA INTERFACE BLOCK

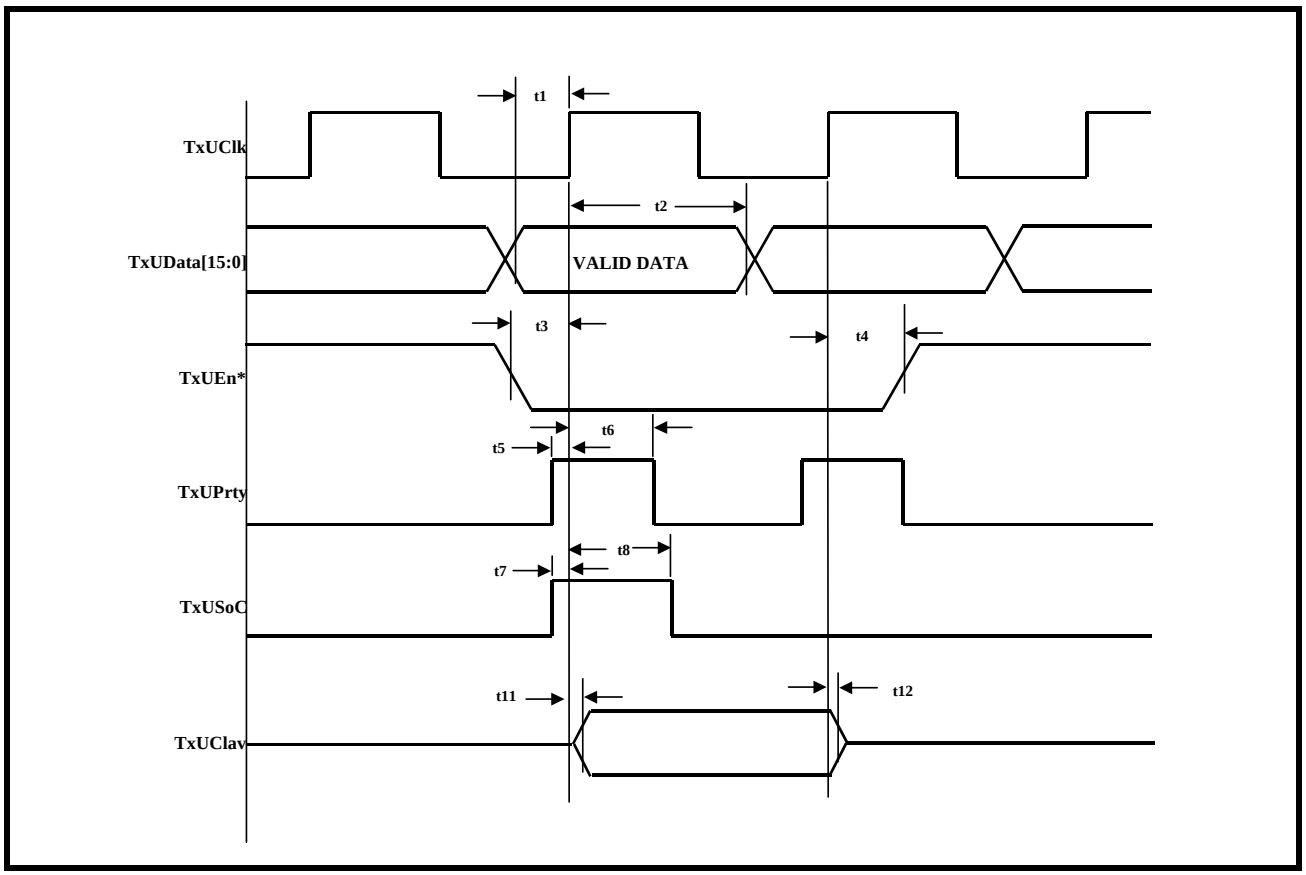


TABLE 8: TIMING INFORMATION FOR THE TRANSMIT UTOPIA INTERFACE BLOCK

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNITS
t1	TxUData[15:0] to rising edge of TxUClk Setup Time	4			ns
t2	TxUData[15:0] Hold Time from rising edge of TxUClk	1			ns
t3	TxUTOPIA Write Enable Setup Time to rising edge of TxUClk	4			ns
t4	TxUTOPIA Write Enable Hold Time from rising edge of TxUClk	1			ns
t5	TxUPrty Setup Time to rising edge of TxUClk	4			ns
t6	TxUPrty Hold Time from rising edge of TxUClk	1			ns
t7	TxUSoC Setup Time to rising edge of TxUClk	4			ns
t8	TxUSoC Hold Time from rising edge of TxUClk	1			ns
t9	TxUAddr[4:0] Setup Time to rising edge of TxUClk	4			ns
t10	TxUAddr[4:0] Hold Time from rising edge of TxUClk	1			ns

TABLE 8: TIMING INFORMATION FOR THE TRANSMIT UTOPIA INTERFACE BLOCK

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNITS
t11	TxUClav signal valid (not Hi-Z) from first TxUClk rising edge of valid and correct TxUAddr[4:0]	3.6		9.7	ns
t12	TxUClav signal Hi-Z from first TxUClk rising edge of different TxUAddr[4:0]	3.6		9.7	ns

TRANSMIT PAYLOAD DATA INPUT INTERFACE

TRANSMIT PAYLOAD DATA INPUT INTERFACE - TIMING REQUIREMENTS

TABLE 9: TIMING INFORMATION FO RTHE TRNASMIT PAYLOAD DATA INPUT INTERFACE BLOCK

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Transmit Payload Data Input Interface - Loop-Timed/Serial Mode (See Figure 11)						
t_1	Payload data (TxSer) set-up time to rising edge of RxOutClk	12			ns	
t_2	Payload data (TxSer) hold time, from rising edge of RxOutClk	0			ns	
t_3	RxOutClk to TxFrame output delay			5	ns	
t_4	RxOutClk to TxOHInd output delay			6	ns	
Transmit Payload Data Input Interface - Local Timed/Serial Mode (See Figure 12)						
t_5	Payload data (TxSer) set-up time to rising edge of TxInClk	4			ns	
t_6	Payload data (TxSer) hold time, from rising edge of TxInClk	0			ns	
t_7	TxFrameRef set-up time to rising edge of TxInClk	2			ns	Framer IC is Frame Slave
t_8	TxFrameRef hold-time, from rising edge of TxInClk	0			ns	Frame IC is Frame Slave
t_9	TxInClk to TxOHInd output delay			15	ns	
t_{10}	TxInClk to TxFrame output delay			13	ns	
Transmit Payload Data Input Interface - Looped-Timed/Nibble Mode (See Figure 13)						
t_{11}	TxNib set-up time to third rising edge of RxOutClk	30			ns	
t_{12}	Payload Nibble hold time, from latching edge of RxOutClk	30			ns	
t_{13}	TxNibClk to TxNibFrame output delay			25 31	ns ns	DS3 Applications E3 Applications
t_{13A}	Max Delay of Rising Edge of TxNibClk to Data Valid on TxNib[3:0]			20 27	ns ns	DS3 Applications E3 Applications
Transmit Payload Data Input Interface - Local-Timed/Nibble Mode (See Figure 14						

TABLE 9: TIMING INFORMATION FO RTHE TRNASMIT PAYLOAD DATA INPUT INTERFACE BLOCK

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{14}	TxNib set-up time to third rising edge of TxInClk			20 27	ns ns	DS3 Applications E3 Applications
t_{15}	Payload Nibble hold time, from latching edge of TxInClk	0			ns	
t_{16}	TxFrameRef set-up time, to latching edge of TxInClk			20 27	ns ns	DS3 Applications E3 Applications Framer IC is Frame Slave
t_{17}	TxFrameRef hold time, from latching edge of TxNib-Clk	0			ns	Framer IC is Frame Slave
t_{18}	TxNibClk to TxNibFrame output delay time	20		25 31	ns ns	DS3 Applications E3 Applications

FIGURE 11. TIMING DIAGRAM FOR THE TRANSMIT PAYLOAD DATA INPUT INTERFACE WHEN THE XRT79L72 IS OPERATING IN BOTH THE DS3 AND LOOP-TIMING MODES

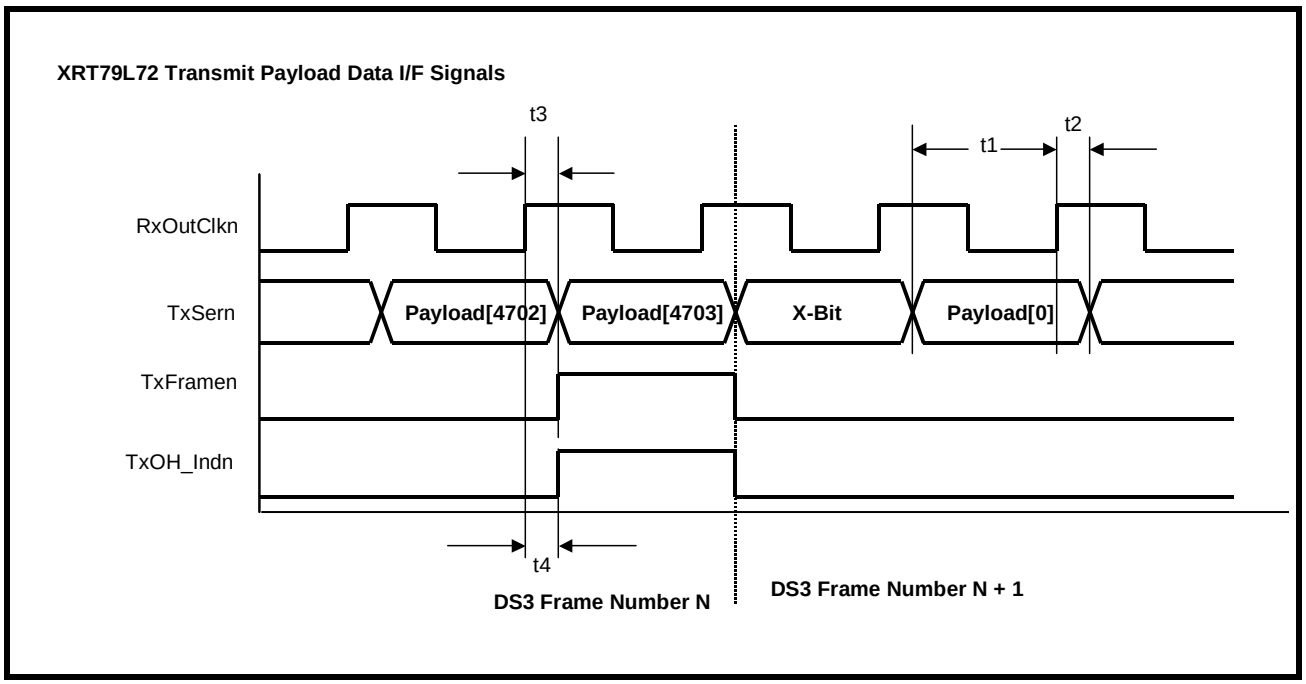


FIGURE 12. TIMING DIAGRAM FOR THE TRANSMIT PAYLOAD DATA INPUT INTERFACE WHEN THE XRT79L72 IS OPERATING IN BOTH THE DS3 AND LOCAL-TIMING MODES

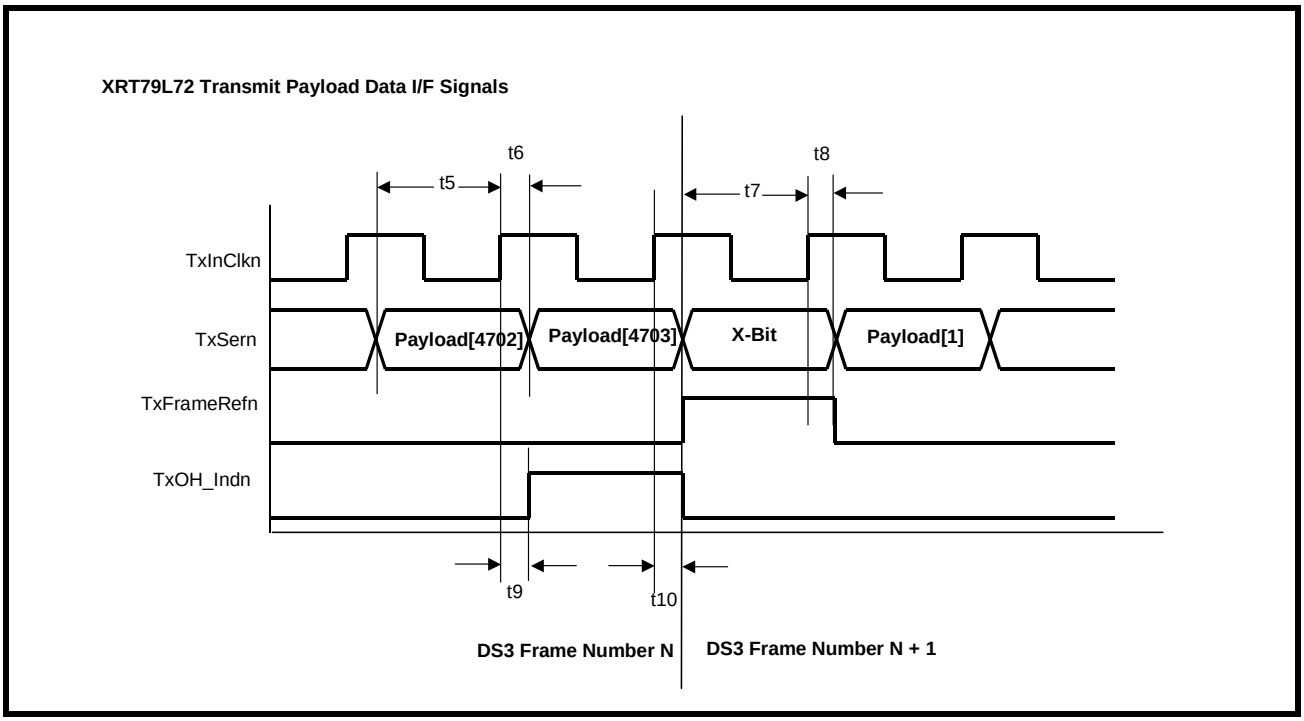


FIGURE 13. TIMING DIAGRAM FOR THE TRANSMIT PAYLOAD DATA INPUT INTERFACE WHEN THE XRT79L72 IS OPERATING IN BOTH THE DS3/NIBBLE-PARALLEL AND LOOP-TIMING MODES

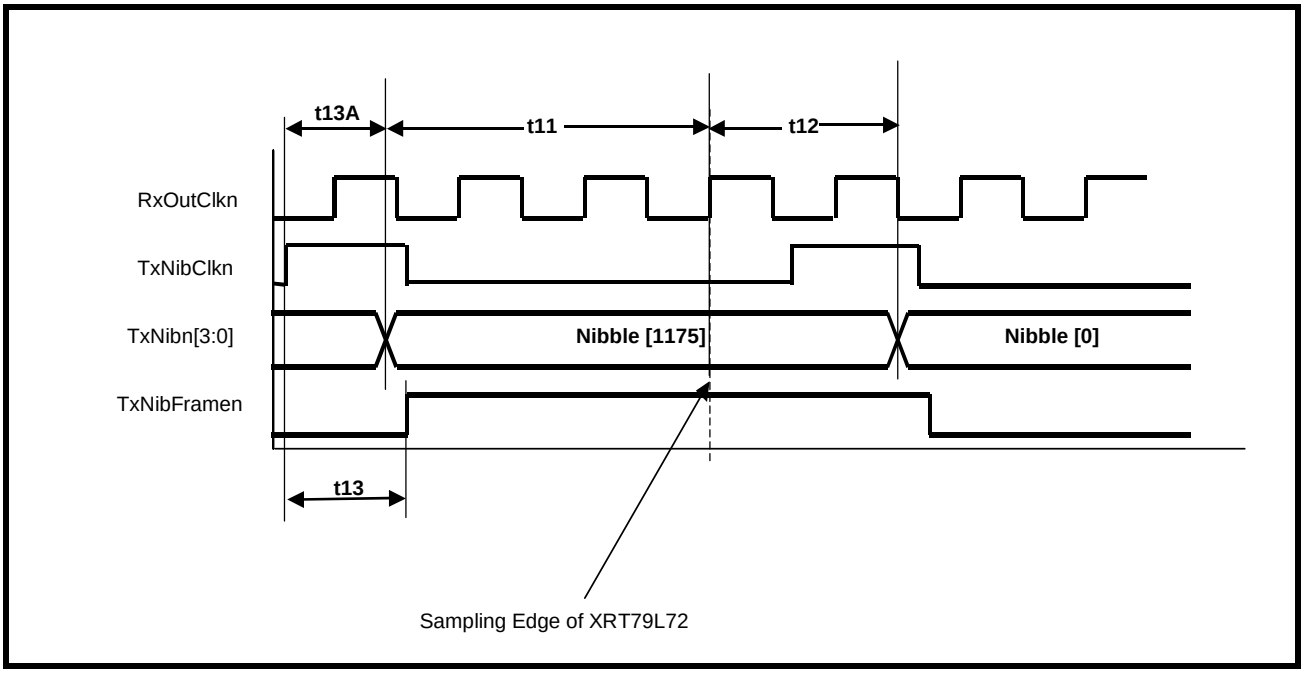
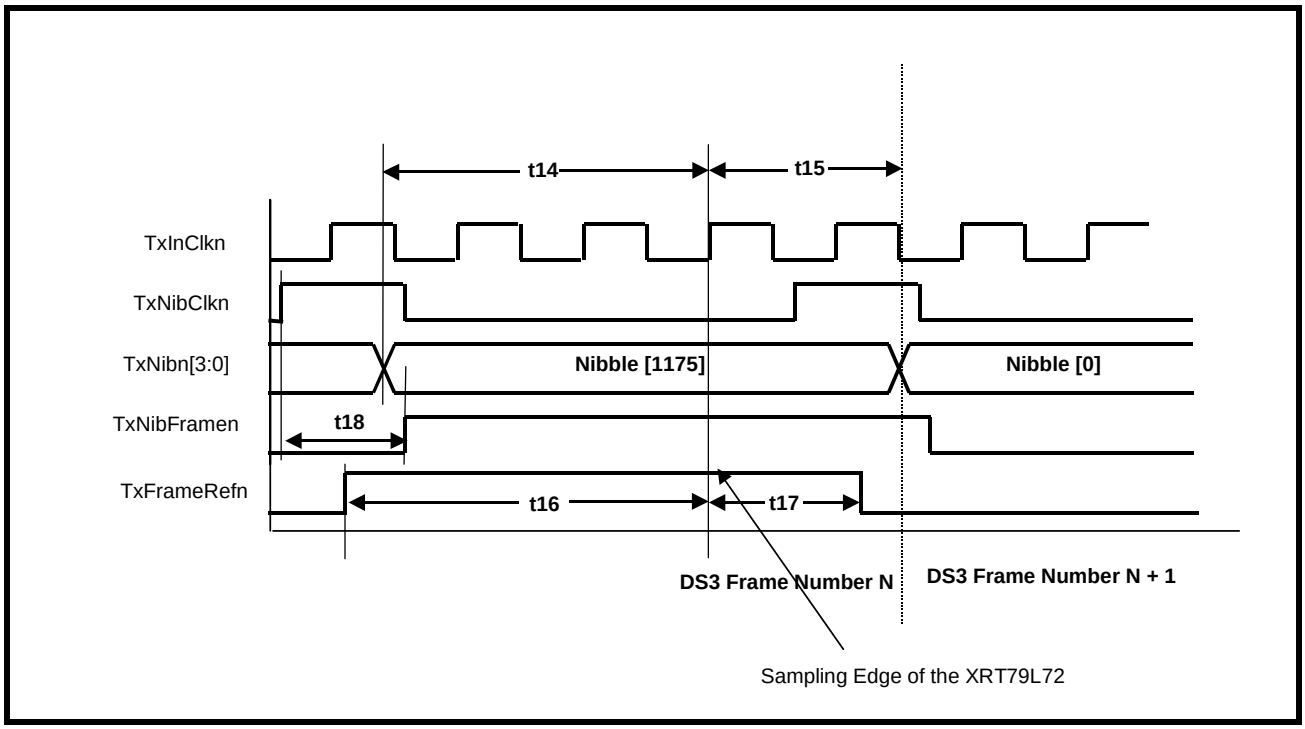


FIGURE 14. TIMING DIAGRAM FOR THE TRANSMIT PAYLOAD DATA INPUT INTERFACE WHEN THE XRT79L72 IS OPERATING IN BOTH THE DS3/NIBBLE-PARALLEL AND LOCAL-TIMING MODES



TRANSMIT OVERHEAD DATA INPUT INTERFACE

TRANSMIT OVERHEAD DATA INPUT INTERFACE - TIMING REQUIREMENTS

TABLE 10: TIMING INFORMATION FOR THE TRANSMIT OVERHEAD DATA INPUT INTERFACE BLOCK

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
Transmit Overhead Input Interface Timing - Method 1 (Figure 15)						
t_{21}	TxOHClk to TxOHFrame output delay			111	ns	DS3 Applications
				0	ns	E3, ITU-T G.832 Applications
				0	ns	E3, ITU-T G.751 Applications
t_{22}	TxOHIns set-up time, to falling edge of TxOHClk	194			ns	DS3 Applications
		305			ns	E3, ITU-T G.832 Applications
		17			ns	E3, ITU-T G.751 Applications
t_{23}	TxOHIns hold time, from falling edge of TxOHClk	48			ns	DS3 Applications
		110			ns	E3, ITU-T G.832 Applications
		7			ns	E3, ITU-T G.751 Applications
t_{24}	TxOH data set-up time, to falling edge of TxOHClk	194			ns	DS3 Applications
		305			ns	E3, ITU-T G.832 Applications
		17			ns	E3, ITU-T G.751 Applications
t_{25}	TxOH data hold time, from falling edge of TxOHClk	48			ns	DS3 Applications
		110			ns	E3, ITU-T G.832 Applications
		7			ns	E3, ITU-T G.751 Applications
Transmit Overhead Data Input Interface - Method 2 (Figure 16)						

TABLE 10: TIMING INFORMATION FOR THE TRANSMIT OVERHEAD DATA INPUT INTERFACE BLOCK

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
t_{26}	TXOHIns to TxInClk (rising edge) set-up Time	254			ns	DS3 Applications
		72			ns	E3, ITU-T G.832 Applications
		15			ns	E3, ITU-T G.751 Applications
t_{27}	TxInClk clock (rising edge) to TxOHIns hold-time	0			ns	DS3 Applications
		0			ns	E3, ITU-T G.832 Applications
		0			ns	E3, ITU-T G.751 Applications
t_{28}	TXOH to TxInClk (rising edge) set-up Time	254			ns	DS3 Applications
		72			ns	E3, ITU-T G.832 Applications
		15			ns	E3, ITU-T G.751 Applications
t_{29}	TxInClk clock (rising edge) to TxOH hold-time	0			ns	DS3 Applications
		0			ns	E3, ITU-T G.832 Applications
		0			ns	E3, ITU-T G.751 Applications
t_{29A}	TxOHEnable to TxOHIns/TxOH Delay	1			ns	

FIGURE 15. TIMING DIAGRAM FOR THE TRANSMIT OVERHEAD DATA INPUT INTERFACE (METHOD 1 ACCESS)

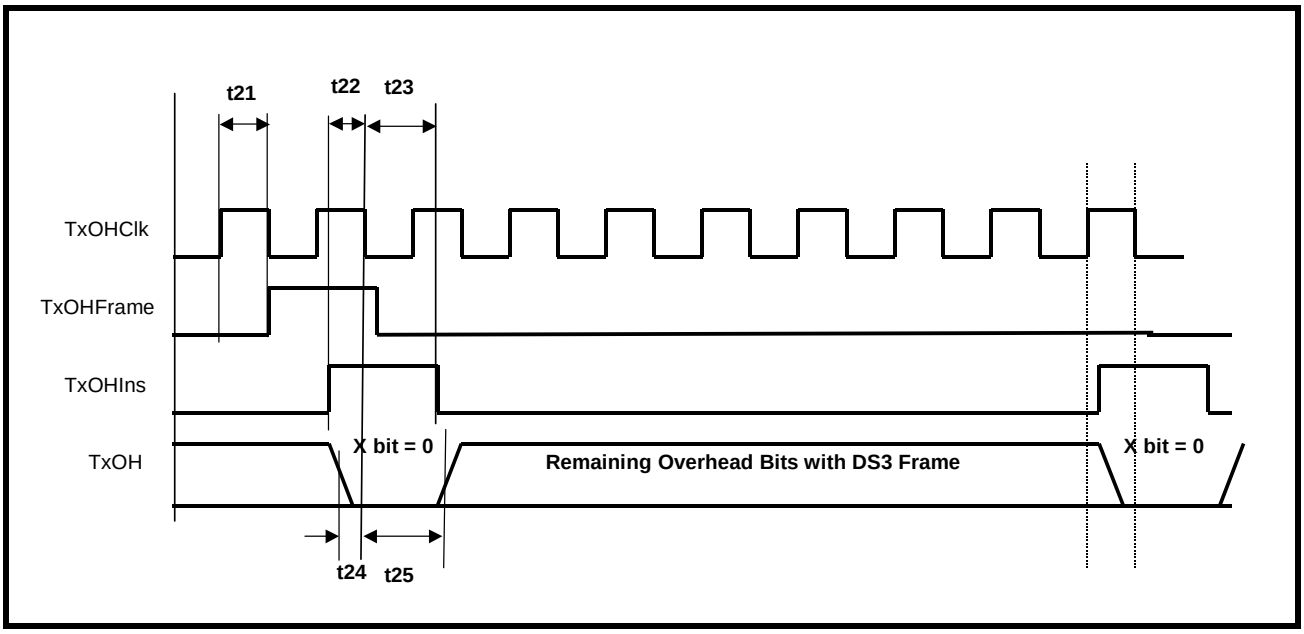
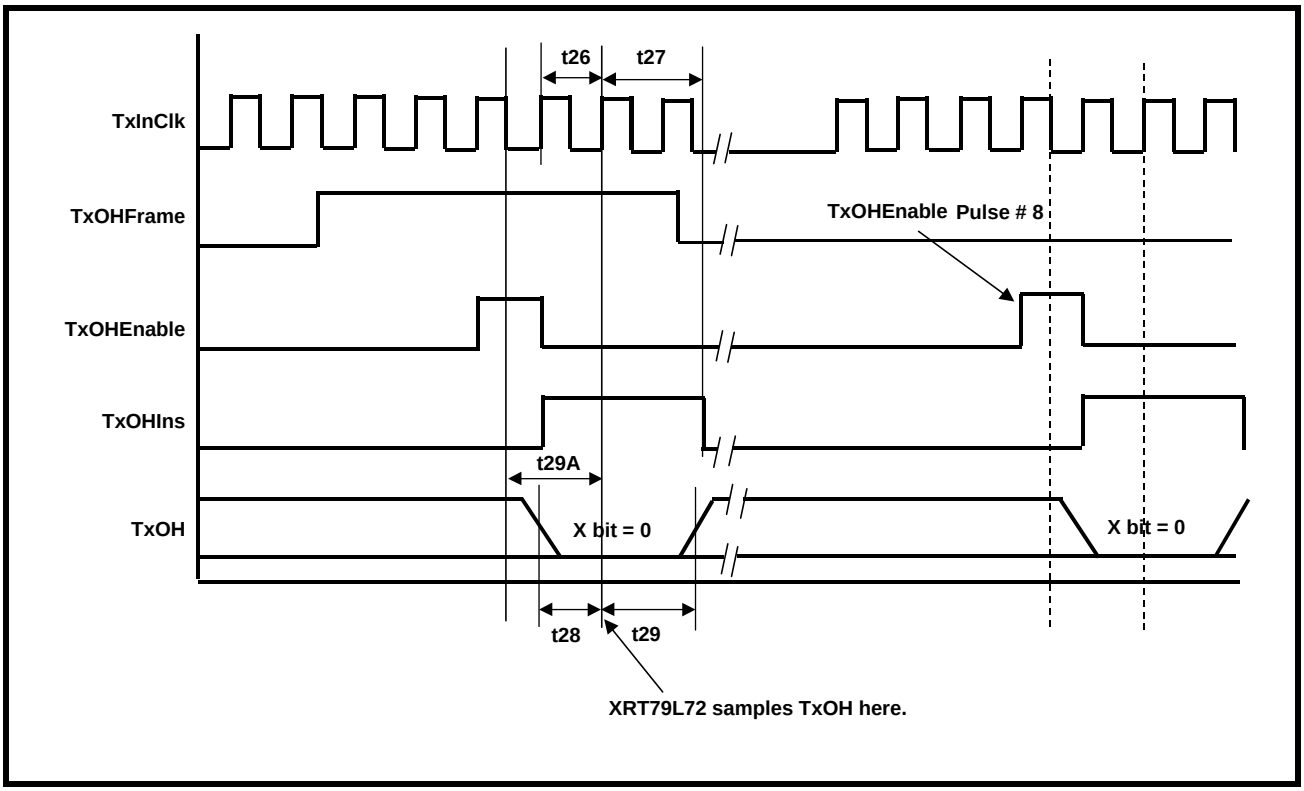


FIGURE 16. TIMING DIAGRAM FOR THE TRANSMIT OVERHEAD DATA INPUT INTERFACE (METHOD 2 ACCESS)



RECEIVE PAYLOAD DATA OUTPUT INTERFACE

RECEIVE PAYLOAD DATA OUTPUT INTERFACE - TIMING REQUIREMENTS

TABLE 11: TIMING INFORMATION FOR THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Receive Payload Data Output Interface Timing - Serial Mode Operation (See Figure 17)						
t_{50}	Rising edge of RxClk to Payload Data (RxSer) output delay			13	ns	DS3 Applications
				16	ns	E3 Applications
t_{51}	Rising edge of RxClk to RxFrame output delay			13	ns	DS3 Applications
				16	ns	E3 Applications
t_{52}	Rising edge of RxClk to RxOHInd output delay.			13	ns	DS3 Applications
				16	ns	E3 Applications
Receive Payload Data Output Interface Timing - Nibble Mode Operation (see Figure 18)						
t_{53}	Falling edge of RxClk to rising edge of RxFrame output delay			2.1	ns	
t_{54}	Falling edge of RxClk to rising edge of RxNib[3:0] output delay			2	ns	

FIGURE 17. TIMING DIAGRAM FOR THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE (SERIAL MODE)

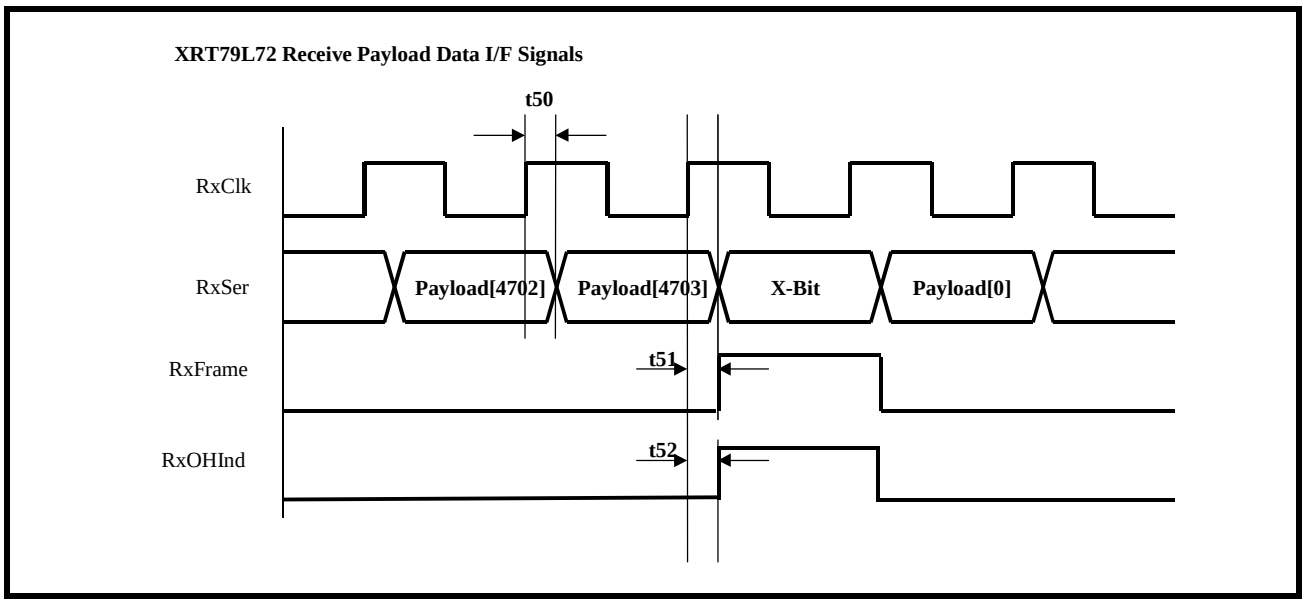
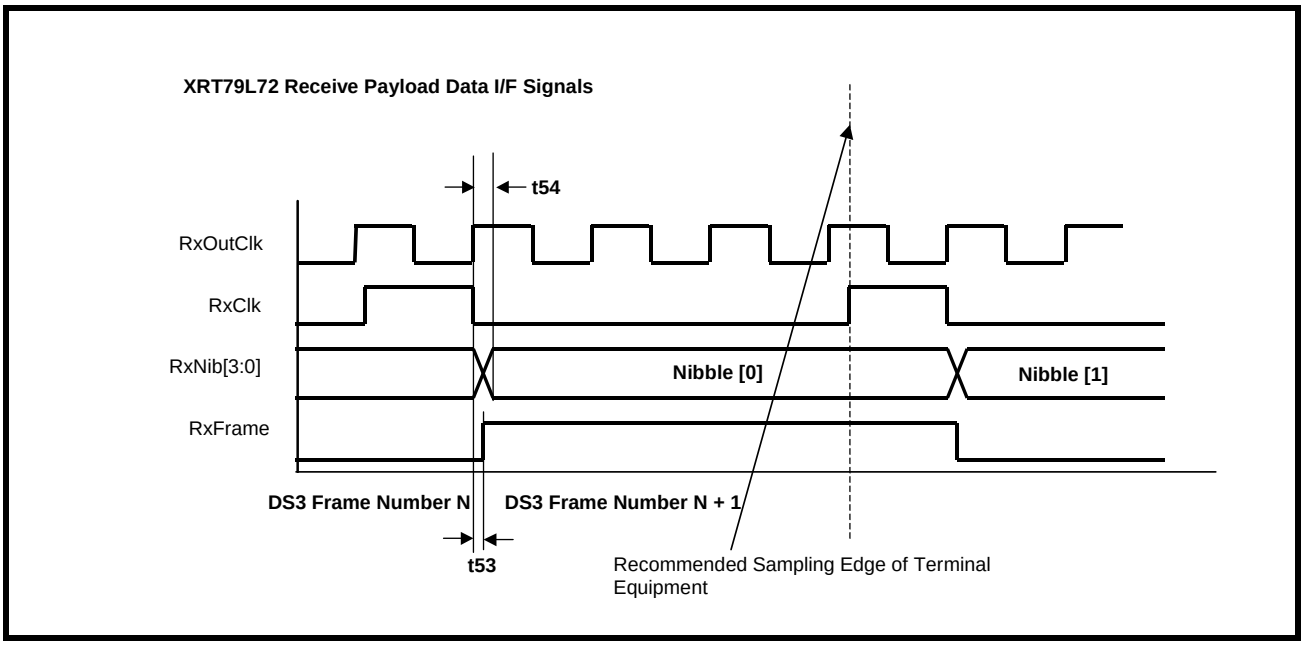


FIGURE 18. TIMING DIAGRAM FOR THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE (NIBBLE-PARALLEL MODE)



RECEIVE OVERHEAD DATA OUTPUT INTERFACE

RECEIVE OVERHEAD DATA OUTPUT INTERFACE - TIMING REQUIREMENTS

Table 13, Timing Information for the Receive Overhead Data Output Interface Block

AC ELECTRICAL CHARACTERISTICS (CONT.)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
Receive Overhead Data Output Interface Timing - Method 1 - Using RxOHClk (see Figure 15)						
t_{59A}	Falling edge of RxOHClk to RxOHFrame output	20		23	ns	DS3 Applications
		25		0	ns	E3 Applications
t_{59B}	Falling edge of RxOHClk to RxOH output delay	20		23	ns	DS3 Applications
		25		0	ns	E3 Applications
Receive Overhead Data Output Interface Timing - Method 2 - Using RxOHEnable (see Figure 16)						
t_{60}	Rising edge of RxOutClk to rising edge of RxOHEnable delay.	2		9.4	ns	
t_{60A}	Rising edge of RxOHFrame to rising edge of RxOHEnable delay			88	ns	DS3 Applications
				224	ns	E3, ITU-T G.832 Applications
				28	ns	E3, ITU-T G.751 Applications
t_{60B}	RxOH Data Valid to rising edge of RxOHEnable delay			88	ns	DS3 Applications
				85	ns	E3, ITU-T G.832 Applications
				28	ns	E3, ITU-T G.751 Applications

FIGURE 19. TIMING DIAGRAM FOR THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE (METHOD 1 - USING RXOHCLK)

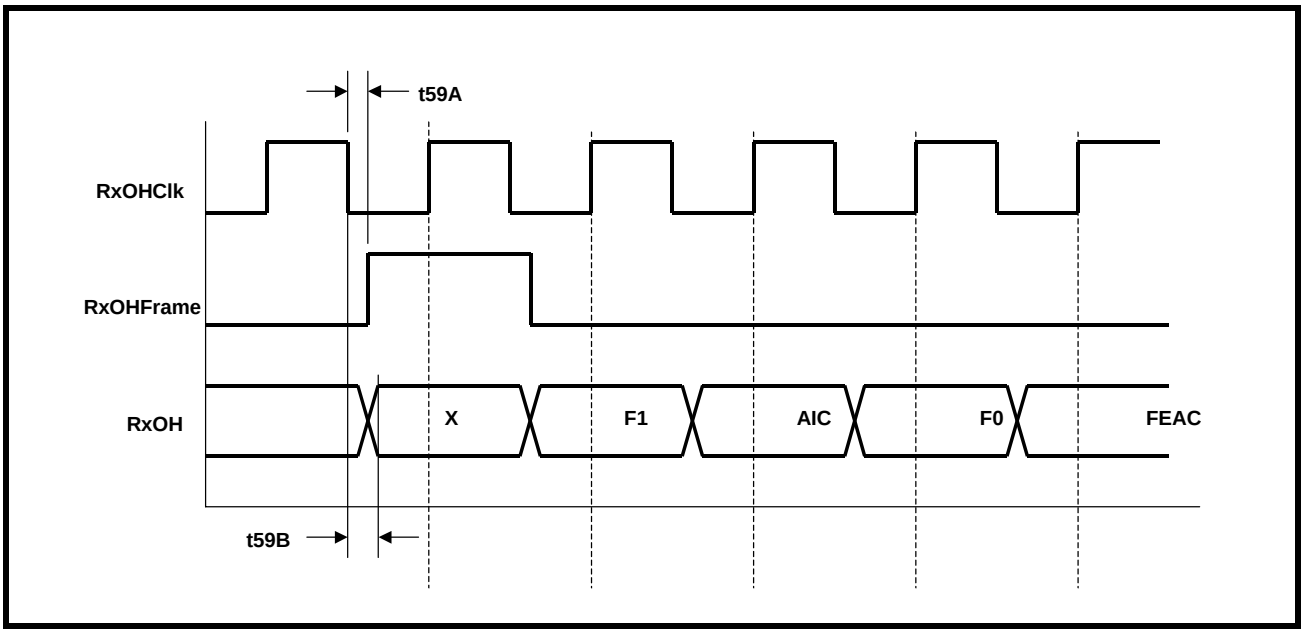
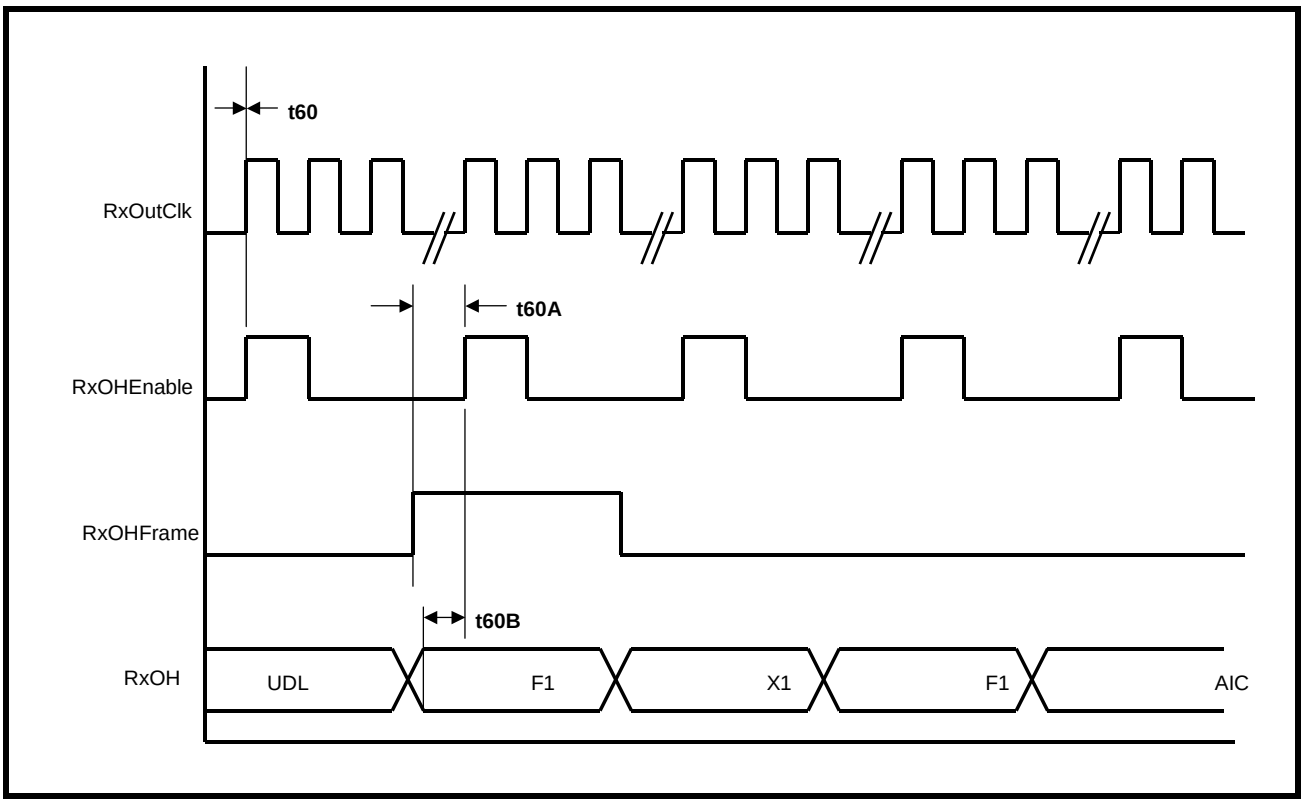


FIGURE 20. TIMING DIAGRAM FOR THE RECEIVE OVERHEAD DATA OUTPUT INTERFACE (METHOD 2 - USING RXOHENABLE)



RECEIVE UTOPIA INTERFACE

RECEIVE UTOPIA INTERFACE

The purpose of the Receive UTOPIA Interface block is to function as either a Standard UTOPIA Level 1, 2 or 3 Interface as it outputs ATM cell data to either an ATM Layer or ATM Adaptation Layer Processor.

FIGURE 21. TIMING DIAGRAM FOR THE RECEIVE UTOPIA INTERFACE BLOCK

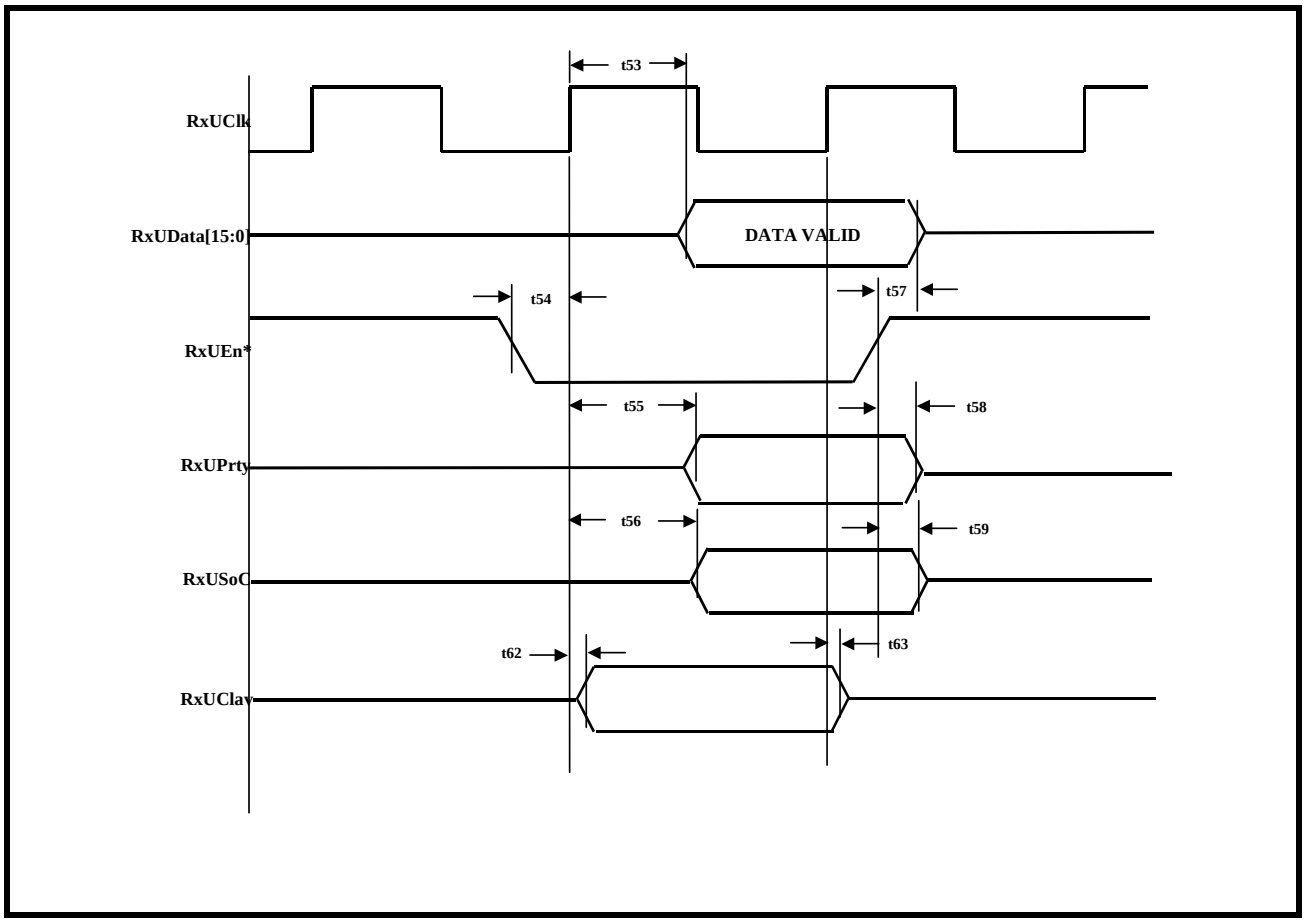


TABLE 12: TIMING INFORMATION FOR THE RECEIVE UTOPIA INTERFACE BLOCK

Symbol	PARAMETER	MIN.	TYP	MAX.	UNITS
Receive UTOPIA Interface Block (See Figure 22)					
t53	Delay time from rising edge of RxUClk to Data Valid at RxU-Data[15:0]	2.7		12	ns
t54	Rx UTOPIA Read Enable setup time to rising edge of RxUClk	4			ns
t55	Delay time from rising edge of RxUClk to valid RxUPrty bit	2.9		9.8	ns
t56	Delay time from rising edge of RxUClk to valid RxUSoC bit	3.5		9.7	ns
t57	Delay time from Read Enable false to Data Bus being tri-stated	1	11.5	16	ns
t58	Delay time from Read Enable false to RxUPrty bit being tri-stated	1	12	16	ns

TABLE 12: TIMING INFORMATION FOR THE RECEIVE UTOPIA INTERFACE BLOCK

Symbol	PARAMETER	MIN.	TYP	MAX.	UNITS
t59	Delay time from Read Enable false to RxUSoC bit being tri-stated	1	11.5	16	ns
t61	RxUAddr[4:0] Hold Time from rising edge of RxUClk	1			ns
t62	RxUClav signal valid (not Hi-Z) from first RxUClk rising edge of valid and correct RxUAddr[4:0]	2.5		8.6	ns
t63	RxUClav signal Hi-Z from first RxUClk rising edge of different RxUAddr[4:0].	2.5		8.6	ns
t58	Delay time from Read Enable false to RxUPrty bit being tri-stated	1	12	16	ns
t59	Delay time from Read Enable false to RxUSoC bit being tri-stated	1	11.5	16	ns
t60	RxUAddr[4:0] Setup Time to rising edge of RxUClk	4			ns
t61	RxUAddr[4:0] Hold Time from rising edge of RxUClk	1			ns
t62	RxUClav signal valid (not Hi-Z) from first RxUClk rising edge of valid and correct RxUAddr[4:0]	1	7.8	16	ns
t63	RxUClav signal Hi-Z from first RxUClk rising edge of different RxUAddr[4:0].	1	9.2	16	ns

ORDERING INFORMATION

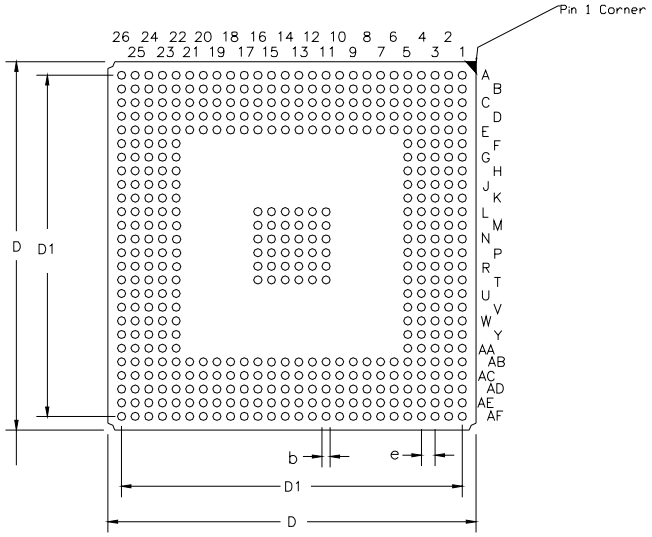
PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT79L72IB	456 Lead PBGA	-40^{0}C to +85^{0}C

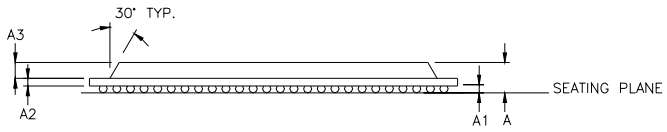
PACKAGE DIMENSIONS

EXAR

456 Ball Plastic Ball Grid Array
(27 mm x 27 mm 1.00mm pitch, PBGA)

Rev. 1.00





	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.083	0.138	2.10	3.50
A1	0.012	0.024	0.30	0.60
A2	0.010	0.028	0.25	0.70
A3	0.039	0.098	1.00	2.50
D	1.055	1.071	26.80	27.20
D1	0.984 BSC		25.00 BSC	
b	0.020	0.028	0.50	0.70
e	0.039 BSC		1.00 BSC	

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.0	03/05/04	First release of the XRT79L72 preliminary hardware manual.
P1.0.1	04/29/04	Changed Pin Numbers.
P1.0.2	02/22/05	Fix pin numbering and descriptions.

NOTICE