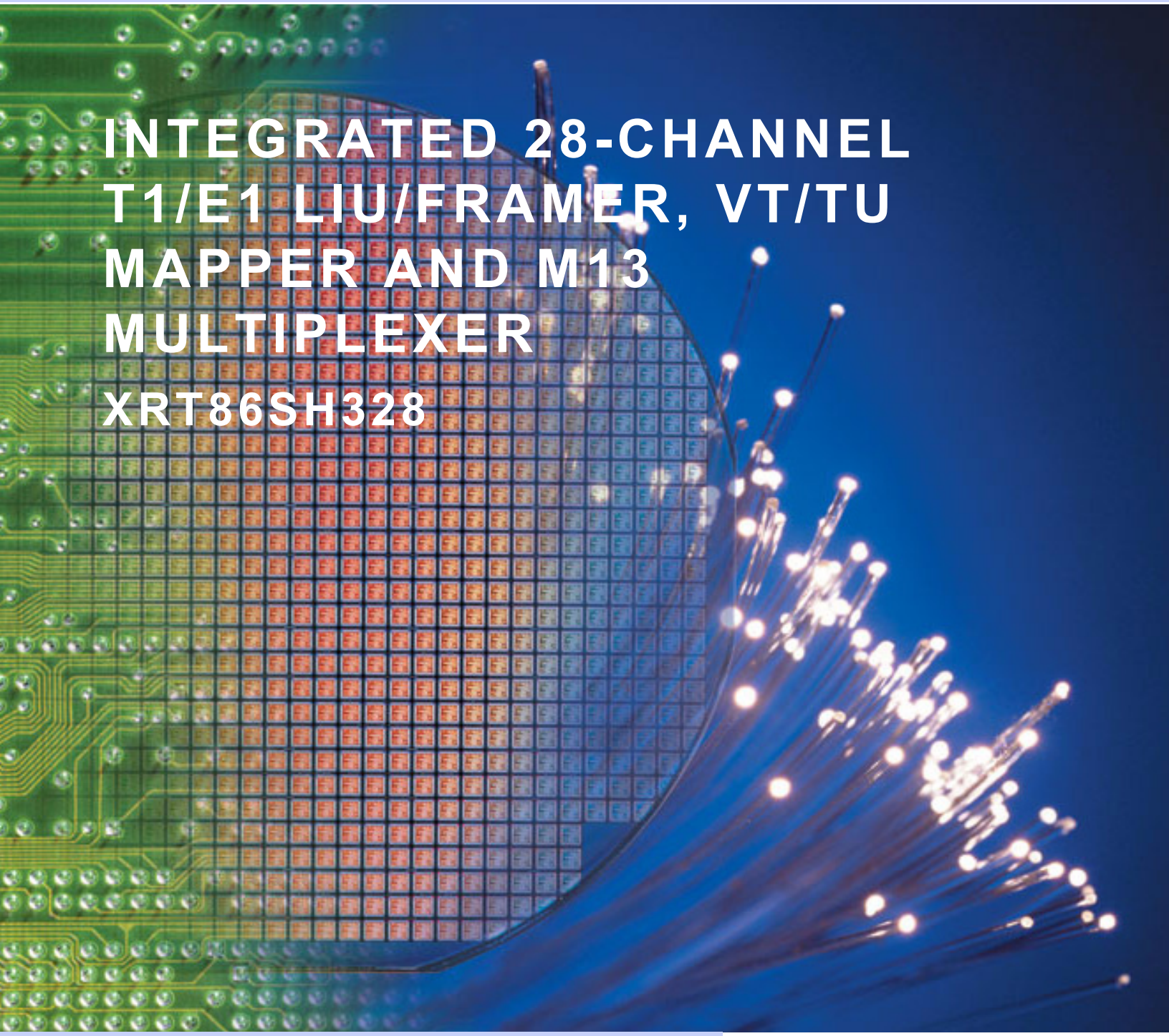
Datasheet, P1.0.1, September 2005



INTEGRATED 28-CHANNEL T1/E1 LIU/FRAMER, VT/TU MAPPER AND M13 MULTIPLEXER

XRT86SH328

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1 GENERAL DESCRIPTION

The XRT86SH328 is an integrated VT/TU Mapper with 28 port T1/E1 Line Interface Units. The XRT86SH328 contains integrated DS1/E1/J1 Framers for performance monitoring.

The XRT86SH328 processes the Section, Line and Path overhead in the SONET/SDH data-stream. The processing of path overhead bytes within the STS-1s or TUG-3s include 64 bytes (of buffer) for storing the (Section Trace and Path Trace) messages. Path Overhead bytes can be accessed either by on-chip registers or a Serial Output Port.

Each of the 28 T1 or E1 Channels use an internal De-Synchronizer circuit with an internal pointer leak algorithm. This removes the jitter due to mapping and pointer adjustments from the T1 or E1 signals that are de-mapped from the incoming SONET/SDH data-stream. These De-Synchronizer circuits do not need any external clock references for its operation.

The Transmit Blocks permit flexible insertion of TOH and POH bytes via both Hardware and Software control.

The Receive Blocks receive a SONET STS-1 signals or an SDH STM-1 signal and performs the necessary Transport and Path Overhead Processing.

A PRBS Pattern Generator and Receiver is implemented within each of the 28 T1/E1 channels in order to implement and measure Bit-Error performance.

A general purpose Microprocessor Interface is included for control, configuration and monitoring.

1.1 FEATURES

- Provides mapping of up to 28 T1 streams as Asynchronous VT1.5 into an STS-1 SPE or TU-11 tributary unit into an STM-1/VC-3 or TUG-3 from STM-1/VC-4
- Supports 28 T1 streams M13 multiplexed into a serial DS3
- Supports 21 E1 streams M13 multiplexed into a serial DS3 (compliant with ITU-T G.747)
- 28 T1 Streams M13 Multiplexed into a DS3 and DS3 is asynchronously mapped into STS-1.
- 21 E1 Streams M13 Multiplexed into a DS3 (ITU-T G.747) and DS3 is asynchronously mapped into STS-1.
- Supports 21 E1 mapped as Asynchronous VT2 into an STS-1 SPE or TU-12 tributary units into STM-1/VC-3 or TUG-3 from a STM-1/VC-4.
- Supports TU cross-mapping function TU-12/VC-11/T1.
- Supports mixed mapping of VT-G/VT1.5 and VT-G/VT2.
- Supports mixed mapping of TUG-2/TU-11 and TUG-2/TU-12
- 28 VT1.5/TU-11 or 21 VT-2/TU-12 tributaries can be passed as transparent between SONET/SDH Telecom Bus on the line side and Clock and Data on the system side.
- Supports Unframed T1/E1 signals
- Supports DS1/E1 Performance Monitoring in both Egress and Ingress direction
- VC-11/VC-12 Tandem Connection Monitoring support
- Complies with the Category I Intrinsic Jitter Requirements for DS1 signals being de-mapped from SONET, per Telcordia GR-253-CORE
- Complies with the "Mapping Jitter Generation Specification" for DS1 and E1 signals being de-mapped from SDH, per ITU-T G.783
- Complies with the "Combined Jitter Generation Specification" for DS1 and E1 signals being de-mapped from SDH, per ITU-T G.783
- Line and Facility Loop-backs
- Each of the 28 T1/E1 Channels includes a PRBS Generator and Receiver.
- Each of the 28 VT-Mapper blocks are capable of generating BIP-2 and REI errors upon software command (for diagnostic purposes).
- ·The Transmit and Receive DS3 Framer blocks support both the M13(M23) and the C-bit Parity Framing formats.
- Integrated 28 T1/E1/J1 Short-Haul Line Interface Units
- IEEE 1149.1 Standard Boundary Scan
- Low Power: 1.8V Power Supply for Core Logic; 3.3V Power Supply for I/O
- General Purpose Microprocessor Interface

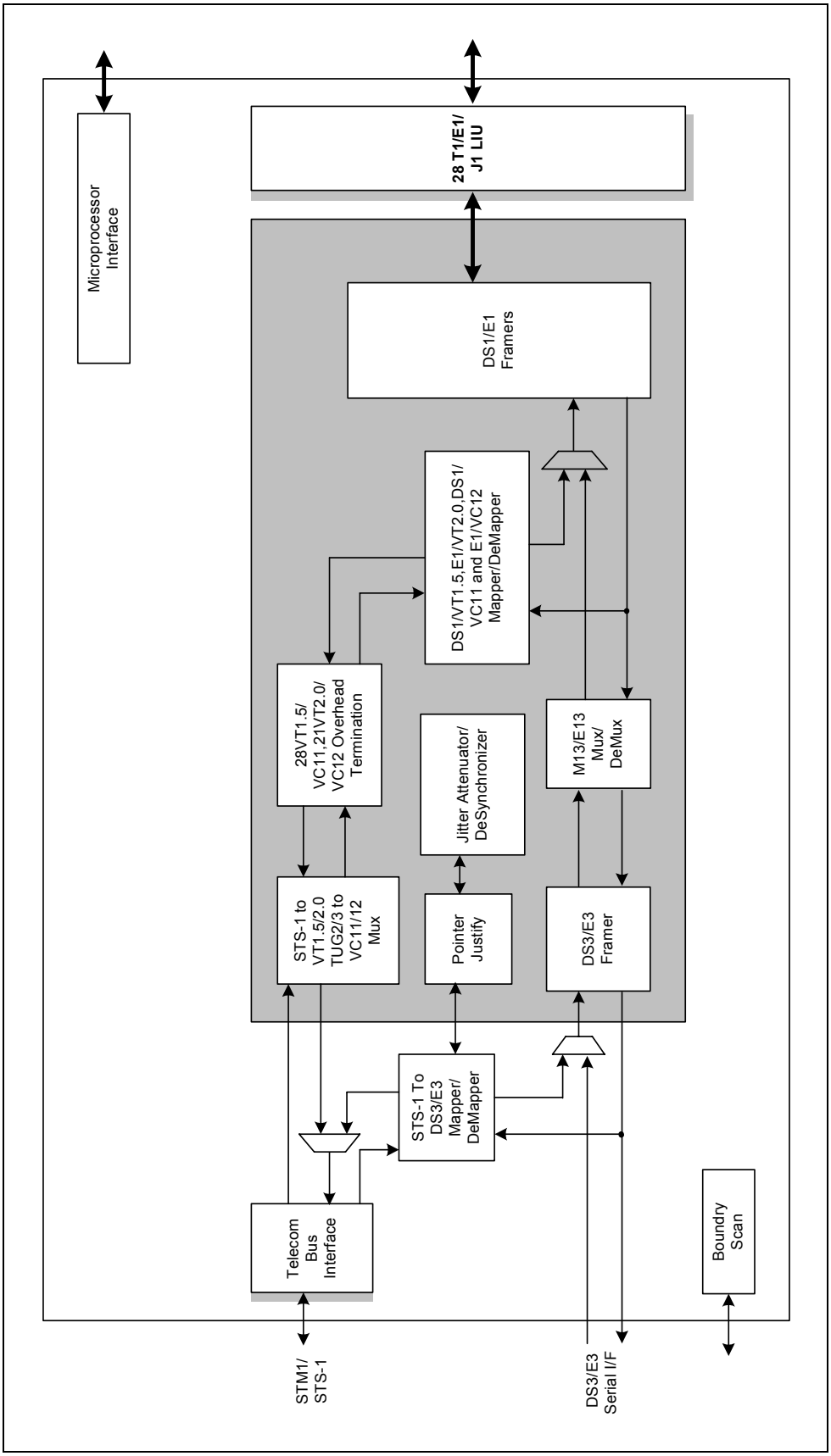
1.2 APPLICATIONS

- Channelized and Unchannelized DS3 applications
- T1/E1 Terminals
- SONET/SDH ADM

Table 1 Ordering Information

Product Number	Package Type	Operating Temperature Range
XRT86SH328IB	568 Ball BGA	-25°C to +85°C

Figure 1 Block Diagram of the XRT86SH328



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2 XRT86SH328 PIN DESCRIPTIONS

Table 2 Microprocessor Interface - Pin Descriptions

Pin/Ball Number	Pin Name	Type	Description
AA30 V27 W29 W30 V29 U28 U29 T27 T29 R28 R27 R30 P29 N29 N28 M30 M29 L30	A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17	**I**	**Address Bus Input pins (Microprocessor Interface):** These pins permit the Microprocessor to identify on-chip registers and Buffer/Memory locations (within the XRT86SH328) whenever it performs READ and WRITE operations with the XRT86SH328.
U26 U27 T26 T30 R29 P27 P26 N27	D0 D1 D2 D3 D4 D5 D6 D7	**I/O**	**Bi-Directional Data Bus pins (Microprocessor Interface):** These pins are used to drive and receive data over the bi-directional data bus, whenever the Microprocessor performs READ or WRITE operations with the Microprocessor Interface of the XRT86SH328.

Table 2 Microprocessor Interface - Pin Descriptions

Pin/Ball Number	Pin Name	Type	Description
V30	ALE/AS	I	**Address Latch Enable/Address Strobe:** The function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in. **Intel-Asynchronous Mode - ALE** If the Microprocessor Interface of the XRT86SH328 has been configured to operate in the Intel-Asynchronous Mode, then this active-high input pin is used to latch the address (present at the Microprocessor Interface Address Bus pins (A[17:0]) into the XRT86SH328 Microprocessor Interface block and to indicate the start of a READ or WRITE cycle. Pulling this input pin "High" enables the input bus driver s for the Address Bus input pins (A[17:0]). The contents of the Address Bus will be latched into the XRT86SH328 Microprocessor Interface circuitry, upon the falling edge of this input signal. **Motorola-Asynchronous (68K) Mode - AS*** If the Microprocessor Interface has been configured to operate in the Motorola-Asynchronous Mode, then this active-low input pin is used to latch the data (residing on the Address Bus, A[17:0]) into the Microprocessor Interface circuitry of the XRT86SH328. Pulling this input pin "Low" enables the input bus drivers for the Address Bus input pins. The contents of the Address Bus will be latched into the Microprocessor Interface circuitry, upon the rising edge of this signal. **Power PC 403 Mode - No Function - Tie to GND:** If the Microprocessor Interface has been configured to operate in the Power PC 403 Mode, then this input pin has no role nor function and should be tied to GND.
U30	$\overline{CS}$	I	**Chip Select Input:** This active low signal must be asserted in order to select the Microprocessor Interface for READ and WRITE operations between the Microprocessor and the XRT86SH328 on-chip registers and buffer/memory locations.
N30	$\overline{INT}$	O	**Interrupt Request Output:** This active-low output signal will be asserted when the XRT86SH328 is requesting interrupt service from the Microprocessor. This output pin should typically be connected to the Interrupt Request input of the Microprocessor.

Table 2 Microprocessor Interface - Pin Descriptions

Pin/Ball Number	Pin Name	Type	Description
V28	$\overline{RD}$/ $\overline{DS}$/ $\overline{WE}$	I	**READ Strobe/Data Strobe:** The function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in. **Intel-Asynchronous Mode - RD* - READ Strobe Input:** If the Microprocessor Interface is operating in the Intel-Asynchronous Mode, then this input pin will function as the RD* (Active Low Read Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the XRT86SH328 will place the contents of the addressed register (or buffer location) on the Microprocessor Interface Bi-directional data bus (D[7:0]). When this signal is negated, then the Data Bus will be tri-stated **.Motorola-Asynchronous (68K) Mode - DS* - Data Strobe** :If the Microprocessor Interface is operating in the Motorola-Asynchronous Mode, then this input pin will function as the DS* (Data Strobe) input signal. **Power PC 403 Mode - WE* - Write Enable Input:** If the Microprocessor Interface is operating in the Power PC 403 Mode, then this input pin will function as the WE* (Write Enable) input pin. Anytime the Microprocessor Interface samples this active-low input signal (along with CS* and WR/R/W*) also being asserted (at a logic low level) upon the rising edge of µPCLK, then the Microprocessor Interface will (upon the very same rising edge of µPCLK) latch the contents on the Bi-Directional Data Bus (D[7:0]) into the target on-chip register or buffer location within the XRT86SH328.

Table 2 Microprocessor Interface - Pin Descriptions

Pin/Ball Number	Pin Name	Type	Description
R26	$\overline{\text{RDY}}$/ $\overline{\text{DTACK}}$/ RDY	O	**READY or DTACK Output:** The function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in. **Intel-Asynchronous Mode - RDY* - Ready Output:** If the Microprocessor Interface has been configured to operate in the Intel-Asynchronous Mode, then this output pin will function as the active-low READY output.During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic low level, ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic "Low" level, then it is now safe for it to move on and execute the next READ or WRITE cycle. If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "High" level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic low level. **Motorola-Asynchronous Mode - DTACK* - Data Transfer Acknowledge Output** If the Microprocessor Interface has been configured to operate in the Motorola-Asynchronous Mode, then this output pin will function as the active-low DTACK output.During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic low level, ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic "Low" level, then it is now safe for it to move on and execute the next READ or WRITE cycle. If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "High" level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic low level. **Power PC 403 Mode - RDY - Ready Output:** If the Microprocessor Interface has been configured to operate in the Power PC 403 Mode, then this output pin will function as the active-high READY output.During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic high level, ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has sampled this signal being at the logic "High" level (upon the rising edge of PCLK), then it is now safe for it to move on and execute the next READ or WRITE cycle. If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "Low" level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it samples this output pin being at the logic low level. *Note: The Microprocessor Interface will update the state of this output pin upon the rising edge of µPCLK.*
P1	$\overline{\text{RESET}}$	I	**Hardware Reset Input:** When this active-low signal is asserted, the XRT79L71 device will be asynchronously reset. When this occurs, all outputs will be tri-stated and all on-chip registers will be reset to their default values.

Table 2 Microprocessor Interface - Pin Descriptions

Pin/Ball Number	Pin Name	Type	Description
T28	µPCLK	I	**Microprocessor Interface Clock Input:** This clock input signal is only used if the Microprocessor Interface has been configured to operate in one of the Synchronous Modes (e.g., Power PC 403 Mode). If the Microprocessor Interface is configured to operate in one of these modes, then it will use this clock signal to do the following. • To sample the CS*, WR*/R/W*, A[17:0], D[7:0], RD*/DS* and DBEN input pins, and • To update the state of the D[7:0] and the RDY/DTACK output signals. *Notes:* *1. The Microprocessor Interface can work with µPCLK frequencies ranging up to 33MHz.* *2. This pin is inactive if the Microprocessor Interface is configuredto operate in either the Intel-Asynchronous or the Motorola-Asynchronous Modes. In this case, this pin should be tied to ground.*

Table 2 Microprocessor Interface - Pin Descriptions

Pin/Ball Number	Pin Name	Type	Description
Y30	$\overline{WR}$/ R/$\overline{W}$	I	**Write Strobe/Read-Write Operation Identifier:** The function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in. **Intel-Asynchronous Mode - WR* - Write Strobe Input:** If the Microprocessor Interface is configured to operate in the Intel-Asynchronous Mode, then this input pin functions as the WR* (Active Low WRITE Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the input buffers (associated with the Bi-Directional Data Bus pin, D[7:0]) will be enabled. The Microprocessor Interface will latch the contents on the Bi-Directional Data Bus (into the target register or address location, within the XRT86SH328) upon the rising edge of this input pin. **Motorola-Asynchronous Mode - R/W* - Read/Write Operation Identification Input Pin:** If the Microprocessor Interface is operating in the Motorola-Asynchronous Mode, then this pin is functionally equivalent to the R/W* input pin. In the Motorola Mode, a READ operation occurs if this pin is held at a logic "1", coincident to a falling edge of the RD/DS* (Data Strobe) input pin. Similarly a WRITE operation occurs if this pin is at a logic "0", coincident to a falling edge of the RD/DS* (Data Strobe) input pin. **Power PC 403 Mode - R/W* - Read/Write Operation Identification Input:** If the Microprocessor Interface is configured to operate in the Power PC 403 Mode, then this input pin will function as the Read/Write Operation Identification Input pin. Anytime the Microprocessor Interface samples this input signal at a logic low (while also sampling the CS* input pin "Low") upon the rising edge of µPCLK, then the Microprocessor Interface will (upon the very same rising edge of µPCLK) latch the contents of the Address Bus (A[17:0]) into the Microprocessor Interface circuitry, in preparation for this forthcoming READ operation. At some point (later in this READ operation) the Microprocessor will also assert the DBEN*/OE* input pin, and the Microprocessor Interface will then place the contents of the target register (or address location within the XRT86SH328) upon the Bi-Directional Data Bus pins (D[7:0]), where it can be read by the Microprocessor . Anytime the Microprocessor Interface samples this input signal at a logic high (while also sampling the CS* input pin a logic "Low") upon the rising edge of µPCLK, then the Microprocessor Interface will (upon the very same rising edge of µPCLK) latch the contents of the Address Bus (A[17:0]) into the Microprocessor Interface circuitry, in preparation for the forthcoming WRITE operation. At some point (later in this WRITE operation) the Microprocessor will also assert the RD*/DS*/WE* input pin, and the Microprocessor Interface will then latch the contents of the Bi-Directional Data Bus (D[7:0]) into the contents of the target register or buffer location (within the XRT86SH328).

Table 2 Microprocessor Interface - Pin Descriptions

Pin/Ball Number	Pin Name	Type	Description
AH1 AG2 AF3	PTYPE_0 PTYPE_1 PTYPE_2	I	**Microprocessor Type Select input:** These three input pins are used to configure the Microprocessor Interface block to readily support a wide variety of Microprocessor Interfaces. The relationship between the settings of these input pins and the corresponding Microprocessor Interface configuration is presented below. **PTYPE[2:0] / Microprocessor Interface Mode** 000 – Intel-Asynchronous Mode 001 – Motorola-Asynchronous Mode (Motorola 68K) 010 – Intel X86 011 – Intel i960 100 – IDT3051/52 (MIPS) 101 – Power PC 403 Mode
P30	$\overline{\text{DBEN}}$	I	**Bi-directional Data Bus Enable Input pin:** This input pin is used to either enable or tri-state the Bi-Directional Data Bus pins (D[7:0]). Setting this input pin "Low" enables the Bi-directional Data bus. Setting this input "High" tri-states the Bi-directional Data Bus.
P28	$\overline{\text{BLAST}}$	I	**Last Burst Transfer Indicator input pin:** If the Microprocessor Interface is operating in the Intel-I960 Mode, then this input pin is used to indicate (to the Microprocessor Interface block) that the current data transfer is the last data transfer within the current burst operation.The Microprocessor should assert this input pin (by toggling it "Low") in order to denote that the current READ or WRITE operation (within a BURST operation) is the last operation of this BURST operation. If the Microprocessor Interface has been configured to operate in the Intel-Asynchronous, the Motorola-Asynchronous or the Power PC 403 Mode, tie this input pin to GND.

Table 2 Microprocessor Interface - Pin Descriptions

Pin/Ball Number	Pin Name	Type	Description
Y29	$\overline{\text{REQ\_0}}$	O	**DMA Cycle Request Output - DMA Controller 0 (Write):** This output pin is used to indicate that the DMA transfers (Write) are requested by a given Transmit DS1/E1 Framer block. A given Transmit DS1/E1 Framer block will request a DMA transfer (e.g., from the external DMA controller to the target Transmit HDLC Buffer in the XRT86SH328) only when the Transmit HDLC Buffer status bit indicates that there is space for a complete HDLC Message. The DMA Write cycle starts by the Transmit DS1/E1 Framer block asserting the DMA Request ($\overline{\text{REQ0*}}$) "Low". In response to this action, the DMA Controller should then assert the $\overline{\text{ACK\_0}}$ (DMA Acknowledge) output pin (by toggling it "Low") to indicate that it is ready to start the transfer. The external DMA Controller should then place new data on the Microprocessor Data bus each time the Write Signal or Data Strobe signal is strobed "Low". The XRT86SH328 will assert this output pin (toggle it "Low") when at least one of the Transmit HDLC Buffers are empty and can receive one more HDLC Message. The XRT86SH328 will de-assert this output pin (toggle it "High") when the HDLC buffer can no longer receive another HDLC Message. *Note: This pin is only active if the on-chip T1/E1 Framer blocks are used. If the XRT86SH328 is operated with the T1/E1 Framer blocks by-passed or the on-chip DMA Controller is not used, then leave this output pin floating.*
W27	$\overline{\text{REQ\_1}}$	O	**DMA Cycle Request Output - DMA Controller 1 (READ):** This output pin is used to indicate that DMA transfers (Read) are requested by a given Receive DS1/E1 Framer block. A given Receive DS1/E1 Framer block will request a DMA Transfer (e.g., from the target Receive HDLC Buffer within the XRT86SH328 to the external DMA Controller) only when a given Receive HDLC Buffer contains a complete HDLC Message. The DMA Read cycle starts by the Receive DS1/E1 Framer block asserting the DMA Request ($\overline{\text{REQ\_1}}$) output pin "Low". The DMA Controller should then respond to this action by asserting the $\overline{\text{ACK\_1}}$ (e.g., toggling it "Low") to indicate that it is ready to accept the data from the XRT86SH328 device. The Receive DS1/E1 Framer block should then place new data on the Microprocessor Data Bus, each time the READ signal is strobed. The XRT86SH328 will assert this output pin (toggle it "Low") when at least one of the Receive HDLC Controller Buffers contains a complete HDLC message that needs to be read by the Microprocessor.The XRT86SH328 will de-assert this output pin by toggling it "High",when the Receive HDLC Buffer is depleted. *Note: This pin is only active if the on-chip T1/E1 Framer blocks are used. If the XRT86SH328 is operated with the T1/E1 Framer blocks by-passed or the on-chip DMA Controller is not used, then leave this output pin floating.*

Table 2 Microprocessor Interface - Pin Descriptions

Pin/Ball Number	Pin Name	Type	Description
W28	$\overline{ACK\_0}$	I	**DMA Cycle Acknowledge Input - DMA Controller 0 (Write):** The external DMA Controller should assert this input pin "Low" when the following two conditions are met. 1.After the Internal DMA Controller, within the XRT86SH328 has asserted (e.g., toggled "Low"), the $\overline{REQ\_0}$ output signal. 2.Whenever the external DMA Controller is ready to transfer data from external memory to the selected Transmit HDLC Buffer. At this point, the DMA transfer between the external memory and the selected Transmit HDLC Buffer may begin. After completion of the DMA cycle, the external DMA Controller should de-assert this input pin (by toggling it "High") after the DMA Controller within the XRT86SH328 has de-asserted the $\overline{REQ\_0}$ output pin. The external DMA Controller must de-assert this input pin in order to acknowledge the end of the DMA cycle. *Note: This input pin is internally pulled "High". Therefore, if t the DMA Controller within the XRT86SH328 is not used, then either leave this input pin floating or pull it "High".*
AA29	$\overline{ACK\_1}$	I	DMA Cycle Acknowledge Input - DMA Controller 1 (Read): The external DMA Controller should assert this input pin (by toggling it "Low") when the following two conditions are met: 1.After the DMA Controller, within the XRT86SH328 has asserted the $\overline{REQ\_1}$ output signal (by toggling it "Low"). 2.Whenever the External DMA Controller is ready to transfer data from the selected Receive HDLC Buffer to external memory. At this point, the DMA transfer between the selected Receive HDLC Buffer and the external memory may begin. After completion of the DMA cycle, the external DMA Controller should de-assert this input pin after the DMA Controller within the XRT86SH328 has de-asserted the $\overline{REQ\_1}$ output pin. The external DMA Controller must do this in order to acknowledge the end of the DMA cycle. *Note: This input pin is internally pulled "High". Therefore, if t the DMA Controller within the XRT86SH328 is not used, then either leave this input pin floating or pull it "High".*

Table 3 Boundary Scan and other Test Pins - Descriptions

Pin/Ball Number	Pin Name	Type	Description
F4	TCK	I	**Test Clock input:** Boundary Scan Clock input *Note: This input pin should be pulled "Low" for normal operation.*
H6	TDI	I	**Test Data input:** Boundary Scan Test Data Input: *Note: This input pin should be pulled "Low" for normal operation.*
E4	TDO	O	**Test Data output :** Boundary Scan Test Data Output.

Table 3 Boundary Scan and other Test Pins - Descriptions

Pin/Ball Number	Pin Name	Type	Description
C2	TMS	I	**Test Mode Select:** **Boundary Scan Test Mode Select input pin.** *Note: This input pin should be pulled "Low" for normal operation.*
G5	TRST	I	**Test Mode Reset:** Boundary Scan Mode Reset Input pin. *Note: This input pin should be pulled "Low" for normal operation.*
R4	TESTMODE	I	**For Factory Use Only:** Tie this pin to GND
L1	SCAN_MODE	I	**For Factory Use Only:** Tie this pin to GND
AD5	SCAN_ENB	I	**For Factory Use Only:** Tie this pin to GND
C15	ATP_RING1	I	**Analog Test Point - Ring 1:** This pin, along with ATP_TIP1, TMS and TCK are used to perform continuity checks between the TTIP/TRING and RTIP/RRING pins associated with T1/E1 Channels 0 through 13.
AF15	ATP_RING2	I	**Analog Test Point - Ring 2:** This pin, along with ATP_TIP2, TMS and TCK are used to perform continuity checks between the TTIP/TRING and RTIP/RRING pins associated with T1/E1 Channels 14 through 27.
E15	ATP_TIP1	I/O	**Analog Test Point - Tip 1:** This pin, along with ATP_RING1, TMS and TCK are used to perform continuity checks between the TTIP/TRING and RTIP/RRING pins associated with T1/E1 Channels 0 through 13.
AJ14	ATP_TIP2	I/O	Analog Test Point - Tip 2: This pin, along with ATP_RING2, TMS and TCK are used to perform continuity checks between the TTIP/TRING and RTIP/RRING pins associated with T1/E1 Channels 14 through 27
D15	ANALOG1	O	**For Factory Use Only:** Tie this pin to GND
AH14	ANALOG2	I	**For Factory Use Only:** Tie this pin to GND
AG14	SENSE	O	**For Factory Use Only:** Leave this pin floating
A14	SENSE1	O	**For Factory Use Only:** Leave this pin floating
General Purpose Input and Output Pins			

Table 3 Boundary Scan and other Test Pins - Descriptions

Pin/Ball Number	Pin Name	Type	Description
AF2 AE3 AD4 AC5 C1 G4 D2 H5	GPIO_0 GPIO_1 GPIO_2 GPIO_3 GPIO_4 GPIO_5 GPIO_6 GPIO_7	I/O	**General Purpose Input/Output Pins:** Each of these pins can be configured to function as either a general-purpose input or output pin. If a given pin (GPIO_X) is configured to function as an input pin, then the state of this input pin can be monitored by reading Bit X within the Operation General Purpose Pin Data Register (Address Location = 0x0147). If a given pin is configured to function as an **output pin**, then the state of this output pin (GPIO_X) can be controlled by writing the appropriate value into Bit X within the Operation General Purpose Pin Data Register. To configure a given GPIO_X pin to be an **input pin**, set Bit X, within the Operation General Purpose Pin Direction Control Register (Address = 0x014B) to "0". To configure the GPIO_X pin to be an **output pin**, set X, within the Operation General Purpose Pin Direction Control Register (Address = 0x014B) to "1".
T3	EXT_INT_0/ REF A	I/O	**External Interrupt Input Pin/REF A Output pin:** The function of this input/output pin depends upon whether the REF A output has been configured as a Clock Driver Output or into the Tri-state mode,. **If REF A is Tri-stated - External Interrupt Input pin - EXT_INT_0:** If the XRT86SH328 is configured accordingly, it will generate an interrupt (to the Microprocessor) anytime this input pin is pulled to a logic "HIGH". **If REF A configured to function as a Clock Driver Output - REF A:** then it can be configured to do either of the following. • To output a replica of a selected Recovered DS1/E1 Clock signal (from any one of the 28 Receive DS1/E1 LIU Channels). • To output a 19.44MHz clock signal that was synthesized from a selected Recovered DS1/E1 Clock signal (from any one of the 28 Receive DS1/E1 LIU Channels).
T5	EXT_INT_1/ REF B	I/O	**External Interrupt Input Pin/REF B Output pin:** The function of this input/output pin depends upon whether the REF A output has been configured as a Clock Driver Output or into the Tri-state mode,. **If REF A is Tri-stated - External Interrupt Input pin - EXT_INT_1:** If the XRT86SH328 is configured accordingly, it will generate an interrupt (to the Microprocessor) anytime this input pin is pulled to a logic "HIGH". **If REF B is configured to function as a Clock Driver Output - REF B:** If REF B is configured to function as a Clock Driver output, then it can be configured to do either of the following. • To output a replica of a selected Recovered DS1/E1 Clock signal (from any one of the 28 Receive DS1/E1 LIU Channels). • To output a 19.44MHz clock signal that was synthesized from a selected Recovered DS1/E1 Clock signal (from any one of the 28 Receive DS1/E1 LIU Channels).

Table 4 Low-Speed Side Interface - T1/E1 Line Signals - Pin Descriptions

Pin/Ball Number	Pin Name	Type	Description
E27	RTIP_0	I	**Receive T1/E1 Line Input - Positive Polarity Signal - Channel n:** This input pin, along with the corresponding RRING_n input pin, functions as the Receive DS1/E1 Line Signal input for the XRT86SH328. Connect this signal and the corresponding RRING_n input signal to a 2:1 transformer. Whenever the RTIP_n/RRING_n input pins are receiving a positive-polarity pulse within the incoming DS1 or E1 line signal, then this input pin will be pulsed to a higher-voltage than that of the corresponding RRING_n input pin. Conversely, whenever the RTIP_n/RRING_n input pins are receiving a negative-polarity pulse within the incoming DS1 or E1 line signal, then this input pin will be pulsed to a lower-voltage than that of the corresponding RRING_n input pin. *Note: RTIP_3, RTIP_7, RTIP_11, RTIP_15, RTIP_19, RTIP_23 and RTIP_27 should not be used for VT-Mapping or M13 MUX Applications that involve E1 signals.*
F23	RTIP_1		
E23	RTIP_2		
C24	RTIP_3		
C22	RTIP_4		
E18	RTIP_5		
E17	RTIP_6		
C13	RTIP_7		
D12	RTIP_8		
D10	RTIP_9		
A5	RTIP_10		
F9	RTIP_11		
A2	RTIP_12		
A1	RTIP_13		
AE5	RTIP_14		
AF6	RTIP_15		
AK2	RTIP_16		
AJ5	RTIP_17		
AK6	RTIP_18		
AK8	RTIP_19		
AH12	RTIP_20		
AK18	RTIP_21		
AH19	RTIP_22		
AH21	RTIP_23		
AG22	RTIP_24		
AJ26	RTIP_25		
AG25	RTIP_26		
AG27	RTIP_27		

Table 4 Low-Speed Side Interface - T1/E1 Line Signals - Pin Descriptions

Pin/Ball Number	Pin Name	Type	Description
D28	RRING_0	I	**Receive T1/E1 Line Input - Negative Polarity Signal - Channel n:** This input pin, along with the corresponding RTIP_n input pin, functions as the Receive DS1/E1 Line Signal input for the XRT86SH328. Connect this signal and the corresponding RTIP input signal to a 2:1 transformer. Whenever the RTIP_n/RRING_n input pins are receiving a positive-polarity pulse within the incoming DS1 or E1 line signal, then this input pin will be pulsed to a lower-voltage than that of the corresponding RTIP_n input pin. Conversely, whenever the RTIP_n/RRING_n input pins are receiving a negative-polarity pulse within the incoming DS1 or E1 line signal, then this input pin will be pulsed to a higher-voltage than that of the corresponding RTIP_n input pin. *Note: RRING_3, RRING_7, RRING_11, RRING_15, RRING_19, RRING_23 and RRING_27 should not be used for VT-Mapping or M13 MUX Applications that involve E1 signals.*
D26	RRING_1		
C26	RRING_2		
A27	RRING_3		
D21	RRING_4		
C20	RRING_5		
A20	RRING_6		
A12	RRING_7		
A10	RRING_8		
E11	RRING_9		
B6	RRING_10		
E8	RRING_11		
B3	RRING_12		
B1	RRING_13		
AE4	RRING_14		
AJ2	RRING_15		
AG6	RRING_16		
AF9	RRING_17		
AJ7	RRING_18		
AJ9	RRING_19		
AJ11	RRING_20		
AF17	RRING_21		
AF18	RRING_22		
AJ22	RRING_23		
AF21	RRING_24		
AH25	RRING_25		
AE23	RRING_26		
AH28	RRING_27		

Table 4 Low-Speed Side Interface - T1/E1 Line Signals - Pin Descriptions

Pin/Ball Number	Pin Name	Type	Description
C28	TTIP_0	O	**Transmit T1/E1 Line Output - Positive Polarity Signal - Channel n:** This output pin, along with the corresponding TRING_n output pin, function as the Transmit DS1/E1 output signal drivers for Channel n within the XRT86SH328. Connect this signal and the corresponding TRING_n output signal to a 1:2 transformer. Whenever the Transmit Section of a given channel within the XRT86SH328 generates and transmits a positive-polarity pulse (onto the line), this output pin will be pulsed to a higher-voltage than its corresponding TRING_n output pins. Conversely, whenever the Transmit Section of a given channel within the XRT86SH328 generates and transmit a negative-polarity pulse (onto the line), this output pin will be pulsed to a lower-voltage than that of the corresponding TRING_n output pins. *Notes:* 1. *This output pin will be tri-stated whenever the TxON input pin (or bit-field) is set to "0".* 2. *TTIP_3, TTIP_7, TTIIP_11, TTIP_15, TTIP_19, TTIP_23 and TTIP_27 should not be used for VT-Mapping or M13 MUX Applications that involve E1 signals.*
D25	TTIP_1		
C25	TTIP_2		
A26	TTIP_3		
D20	TTIP_4		
B20	TTIP_5		
D17	TTIP_6		
D14	TTIP_7		
A11	TTIP_8		
D11	TTIP_9		
C8	TTIP_10		
A4	TTIP_11		
C5	TTIP_12		
E5	TTIP_13		
AF4	TTIP_14		
AE8	TTIP_15		
AJ4	TTIP_16		
AJ6	TTIP_17		
AJ8	TTIP_18		
AF13	TTIP_19		
AF14	TTIP_20		
AK17	TTIP_21		
AK19	TTIP_22		
AJ21	TTIP_23		
AJ23	TTIP_24		
AG23	TTIP_25		
AF23	TTIP_26		
AG26	TTIP_27		

Table 4 Low-Speed Side Interface - T1/E1 Line Signals - Pin Descriptions

Pin/Ball Number	Pin Name	Type	Description
E26	TRING_0	O	**Transmit T1/E1 Line Output - Negative Polarity Signal - Channel n:**
E24	TRING_1		This output pin, along with the corresponding TTIP_n output pin, function as the Transmit DS1/E1 output signal drivers for Channel n within the XRT86SH328.
D24	TRING_2		Connect this signal and the corresponding TTIP_n output signal to a 1:2 transformer.
B25	TRING_3		Whenever the Transmit Section of a given channel within the XRT86SH328 generates and transmits a positive-polarity pulse (onto the line), this output pin will be pulsed to a lower-voltage than its corresponding TTIP_n output pins.
A24	TRING_4		Conversely, whenever the Transmit Section of a given channel within the XRT86SH328 generates and transmit a negative-polarity pulse (onto the line), this output pin will be pulsed to a higher-voltage than that of the corresponding TTIP_n output pin.
B21	TRING_5		*Notes:*
C18	TRING_6		*1. This output pin will be tri-stated whenever the TxON input pin (or bit-field) is set to "0".*
E14	TRING_7		*2. TRING_3, TRING_7, TRING_11, TRING_15, TRING_19, TRING_23 and TRING_27 should not be used for VT-Mapping or M13 MUX Applications that involve E1 signals.*
C12	TRING_8		
B9	TRING_9		
E10	TRING_10		
C6	TRING_11		
F8	TRING_12		
C3	TRING_13		
AH2	TRING_14		
AG5	TRING_15		
AH5	TRING_16		
AK4	TRING_17		
AG10	TRING_18		
AJ10	TRING_19		
AK11	TRING_20		
AH17	TRING_21		
AJ19	TRING_22		
AF19	TRING_23		
AK25	TRING_24		
AF22	TRING_25		
AJ27	TRING_26		
AF25	TRING_27		

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
G26	RxDS1CLK_0/ EG_TE1RxDATA_2	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 0/Egress Direction T1/E1 Data Drop Port - Output Data Bus - pin # 2:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_[0:27] - Receive DS1/E1 Serial Clock Output Pin - Channel_[0:27]:** This output pin, along with RxDS1DATA_[0:27]: and RxDS1Frame_[0:27] will function as the Receive Serial Data Output port for Channel_[0:27]. The Receive Serial Data Output Port (within the XRT86SH328) will update the Receive-Direction output data (via the RxDS1DATA_[0:27] output pin) to the System-Side Terminal Equipment upon either the rising or falling edge of this output clock signal (depending upon user configuration). **If the XRT86Sh382 has been configured to operate in the various Aggregation Modes - EG_TE1RxDATA_2 - Egress Direction T1/E1 Data Drop Port - Output Data Bus - Bit 2:** This output pin, along with EG_TE1RxDATA_[7:0], EG_TE1RxValid, EG_TE1RxOHInd[4:0], EG_TE1RxSLOT0 and EG_TE1RxCLK function as the byte-wide Egress Direction - Drop Port. This Drop Port can be used for cross-connecting of T1/E1 Time-slots with other XRT86SH328 devices. The Egress Direction - Drop Port actually drops out the contents of all Egress Direction T1 or E1 data that is being handled by the XRT86SH328. All Egress Direction T1 or E1 data will be output via a byte-wide port (e.g., the EG_TE1RxDATA[7:0] output pins). This particular pin will function as bit 2 within this byte wide output port. As the Egress Direction Drop port outputs the contents of the Egress Direction T1/E1 traffic, it will update the contents of the EG_TE1RxDATA[7:0] output data bus upon the rising edge of EG_TE1RxCLK. *Note: The above Aggregation Modes include all of the following.* • *The VT-Mapper Mode (w/ T1/E1 Framing)* • *The M13 MUX Mode (w/ T1/E1 Framing)* • *The M13 MUX to STS-1 Mode* • *The Transmux Mode*
H26	RxDS1CLK_1/ EG_TE1RxDATA_5	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 1/Egress Direction T1/E1 Data Add Port - Output Data Bus - pin # 5:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_1 - Receive DS1/E1 Serial Clock Output pin - Channel 1:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH382 has been configured to operate in the various Aggregation Modes - EG_TE1RxDATA_5 - Egress Direction T1/E1 Data Drop Port - Output Data Bus - Bit 5:** See Pin **G26 on page # 19** for Pin Description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
J26	RxDS1CLK_2/ RxDS3OHInd	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 2/DS3 Receive Overhead Indicator Output pin:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_2:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 has been configured to operate in the M13 MUX Mode - RxDS3OHInd:** This output pin pulses “High” for one bit period coincident to whenever the Receive DS3Framer block is currently processing an overhead bit. **If the XRT86SH328 has been configured to operate in the VT-Mapper mode - NO FUNCTION:** Leave this pin floating.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
K26	RxDS1CLK_3/ EG_TE1RxOHInd_0	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 3/Egress Direction T1/ E1 Data Drop Port - Data Type Indicator Output - Pin # 0:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_3:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - EG_TE1RxOHInd_0:** This output pin, along with EG_TE1RxDATA[7:0], EG_TE1RxValid, EG_TE1RxOHInd[4:0], EG_TE1RxSLOT0 and EG_TE1RxCLK function as the byte-wide Egress Direction - Drop Port. This Drop Port cann be used for cross-connecting of T1/E1 Time-slots with other XRT86SH328 devices. his particular pin will function as the Overhead Indicator - Bit 0 output within this byte wide output port. As the Egress Direction Drop port outputs the contents of the Egress Direction T1/E1 traffic, this output pin (along with EG_TE1RxOHInd[4:1]) will indicate (1) whether the data, residing on EG_TE1RxDATA[7:0] contains any overhead bits, and (2) which of the 8 bits (within EG_TE1RxDATA[7:0]) is an overhead bit. The relationship between the states of the EG_TE1RxOHInd[4:0] output, and how the user should interpret the data, residing on the EG_TE1RxDATA[7:0] output pins is tabulated below.

EG_TE1RxOHInd[4:0]	What's on EG_TE1RxDATA[7:0] Bus?
00 xxx	All bits on bus are T1/E1 payload bits
01 000	EG_TE1RxDATA_0 contains an overhead bit
01 001	EG_TE1RxDATA_1 contains an overhead bit
01 010	EG_TE1RxDATA_2 contains an overhead bit
01 011	EG_TE1RxDATA_3 contains an overhead bit
01 100	EG_TE1RxDATA_4 contains an overhead bit
01 101	EG_TE1RxDATA_5 contains an overhead bit
01 110	EG_TE1RxDATA_6 contains an overhead bit
01 111	EG_TE1RxDATA_7 contains an overhead bit
11 000	EG_TE1RxDATA_0 contains a multi-frame alignment bit
11 001	EG_TE1RxDATA_1 contains a multi-frame alignment bit
11 010	EG_TE1RxDATA_2 contains a multi-frame alignment bit
11 011	EG_TE1RxDATA_3 contains a multi-frame alignment bit
11 100	EG_TE1RxDATA_4 contains a multi-frame alignment bit
11 101	EG_TE1RxDATA_5 contains a multi-frame alignment bit
11 110	EG_TE1RxDATA_6 contains a multi-frame alignment bi
11 111	EG_TE1RxDATA_7 contains a multi-frame alignment bit

This signal will be updated upon the rising edge of EG_TE1RxCLK.

Note: The above Aggregation Modes include all of the following.

- *The VT-Mapper Mode (w/ T1/E1 Framing)*
- *The M13 MUX Mode (w/ T1/E1 Framing)*
- *The M13 MUX to STS-1 Mode*
- *The Transmux Mode*

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
J28	RxDS1CLK_4/ RxDS3OHEnable	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 4/Receive DS3 Overhead Data Port - Enable Output pin:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_4:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 has been configured to operate in the M13 MUX Mode - RxDS3OHEnable:** The XRT86SH328 will assert this output signal for one RxDS3OHClk period when it is safe for the system-side terminal equipment to sample the DS3 overhead data on the RxDS3OH output pin. This particular output pin is only used when employing Receive DS3 Overhead Data Extraction Method 2. The Receive Overhead Data Output Interface will assert this signal (e.g., pulse it "High") for one RxDS3Clk period, coincident to whenever it is safe for the System-Side Terminal Equipment to sample the overhead bit that is being output via the RxDS3OH output pin. This output pin will remain "Low" at all other times. If Method 2 is used, then the System-Side Terminal Equipment must be designed (or configure) such that it will sample and latch the RxDS3OH output (from the XRT86SH328), upon the falling edge of RxDS3Clk coincident to whenever the RxDS3OHEnable output pin is sampled "High". **If the XRT86SH328 has been configured to operate in the VT-Mapper Mode - NO FUNCTION:** Leave this pin floating.
L27	RxDS1CLK_5/ RxDS3OHCLK	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 5/Receive DS3 Overhead Data Output Port - Clock Output signal:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_5:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 has been configured to operate in the M13 MUX Mode - RxDS3OHClk:** The XRT86SH328 will output the overhead bits (within the incoming DS3 frames) via the RxDS3OH output pin, upon the falling edge of this clock signal. As a consequence, the user's system-side terminal equipment should use the rising edge of this clock signal to sample the data on both the RxDS3OH and RxDS3OHFrame output pins. *Note: This clock signal is always active.* **If the XRT86SH328 has been configured to operate in the VT-Mapper mode - NO FUNCTION:** Leave this output pin floating.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
M27	RxDS1CLK_6/ EG_TE1RxCLK	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 6/Egress Direction T1/ E1 Data Drop Port - Byte Wide Clock Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_6:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Mode - EG_TE1RxCLK:** This output pin, along with EG_TE1RxDATA[7:0], EG_TE1RxValid and EG_TE1RxOHInd[4:0] function as the byte-wide Egress Direction - Drop Port. This Drop Port cann be used for cross-connecting of T1/E1 Time-slots with other XRT86SH328 devices, This particular pin will function as the Clock Output within this byte-wide output port. As the Egress Direction Drop port outputs the contents of the Egress Direction T1/E1 traffic, it will update the contents of the EG_TE1RxDATA[7:0] output data bus, the EG_TE1RxOHInd[4:0] and EG_TE1RxValid output pins, upon the rising edge of this clock output signal. *Note: The above Aggregation Modes include all of the following.* • *The VT-Mapper Mode (w/ T1/E1 Framing)* • *The M13 MUX Mode (w/ T1/E1 Framing)* • *The M13 MUX to STS-1 Mode* • *The Transmux Mode*

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
P3	RxDS1CLK_7/ TxSTS-1CLK/ TxDS3CLK	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 7/Transmit DS3/STS-1 Clock Output (Shared Port):** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **A. If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_7:** See Pin **G26 on page # 19** for pin description. **B. If the XRT86SH328 has been configured to operate in the various Aggregation Modes - TxSTS-1CLK/TxDS3CLK:** The XRT86SH328 will transmit the outbound DS3/STS-1 data-stream (via the TxSTS-1DATA/TxDS3POS and TxDS3NEG output) to an off-chip DS3/STS-1 LIU IC, upon either the rising or falling edge of this clock output signal. This output pin should be connected to the TxCLK (Transmit Clock Input) of the off-chip DS3/STS-1 LIU IC or an Aggregation device (such as the XRT94L33/31 or XRT94L43 devices). *Notes:* *1. The above Aggregation Modes include all of the following.* • *The VT-Mapper Mode (w/ T1/E1 Framing)* • *The M13 MUX Mode (w/ T1/E1 Framing)* • *The M13 MUX to STS-1 Mode* • *The Transmux Mode* *2. Only use this particular output pin (for DS3 applications) if the STS-1 and the DS3 Ports are configured to be shared. If the STS-1 and DS3 Ports are configured to be separate (which would be necessary for Transmux applications), then use the TxDS3CLK signal at Ball AB30.* **C. If the XRT86SH328 device has been configured to exchange STS-1/STS-3/STM Data via the Telecom Bus Interface - NO FUNCTION:** Leave this pin floating.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
M2	RxDS1CLK_8/ TxA_C1J1V1_FP	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 8/Egress Direction - T1/ E1 Data - Overhead Indicator Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_8:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 has been configured to output STS-1/STM-1 data via the Transmit STS-1/STM-1 Telecom Bus Interface - TxA_C1J1V1_FP:** This output pin pulses “High” under the following three conditions: • Coincident to whenever the C1/J0 byte of the outbound STS-1/STS-3/STM-1 signal is being output via the TxA_D[7:0] output, and • Coincident to whenever the J1 byte(s) of the outbound STS-1/STS-3/STM-1 signal is being output via the TxA_D[7:0] output • Coincident to whenever the V1 byte(s) of the outbound STS-1/STS-3/STM-1 signal is being output via the TxA_D[7:0] output *Notes:* *1. The transmit STS-1/STS-3/STM-1 Telecom Bus Interface will indicate that it is currently transmitting the C1/J0 byte (via the TxA_D[7:0] output pins) by pulsing this output pin “High” for one period of the TxA_CLK and keeping the TxA_PL output pin “Low”.* *2. The transmit STS-1/STS-3/STM-1 Telecom Bus Interface will indicate that it is currently transmitting the J1 or V1 byte (via the TxA_D[7:0] output pins) by pulsing this output pin “High” for one period of the TxA_CLK and keeping the TxA_PL output pin “High”.*
K2	RxDS1CLK_9/ TxA_D_0	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 9/Transmit STS-1/STS-3/STM-1 Telecom Bus Interface - Data Bus Output pin - Bit 0 Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_9:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 has been configured to output STS-1/STM-1 data via the Transmit STS-1/STM-1 Telecom Bus Interface - TxA_D_0** This output pin, along with TxA_D[0:7] function as the Transmit STS-1/STM-1 Telecom Bus Interface - Data Bus output pins. If the Transmit STS-1/STM-1 Telecom Bus Interface is enabled, then all outbound STS-1/STM-1 data is output via these pins (in a byte-wide manner), upon the rising edge of the TXA_CLK output pin. *Notes:* *1. The pin TXA_D7 will output the MSB (Most Significant Bit) of each byte that is output via the Transmit STS-12/STM-4 Telecom Bus Interface.* *2. The pin TXA_D0 will output the LSB (Least Significant Bit) of each byte that is output via the Transmit STS-12/STM-4 Telecom Bus Interface.* **All other modes - No Function:** If the XRT86SH328 is NOT configured to operate in either of the above modes, then this output pin has no function and can be left floating.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
J2	RxDS1CLK_10/ TxA_D_3	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 10/Transmit STS-1/ STS-3/STM-1 Telecom Bus Interface - Data Bus Output pin - Bit 3 Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_10:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 has been configured to output STS-1/STM-1 data via the Transmit STS-1/STM-1 Telecom Bus Interface - TxA_D_3** See Pin **K2 on page # 25** for pin description
J3	RxDS1CLK_11/ TxA_D_6	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 11/Transmit STS-1/ STS-3/STM-1 Telecom Bus Interface - Data Bus Output pin - Bit 6 Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_11:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 has been configured to output STS-1/STM-1 data via the Transmit STS-1/STM-1 Telecom Bus Interface - TxA_D_6** See Pin **K2 on page # 25** for pin description.
E1	RxDS1CLK_12/ TxOHEnable	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 12/Transmit STS-1/ STM-1 TOH/POH Data Input Port- Enable Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_12:** See Pin **G26 on page # 19** for pin description. **If the XRT86Sh328 has been configured to operate in one of the Sonet/ SDH modes: TxOHEnable:** This output pin along with TxOH, TxOHCLK, TxOHFrame and TxOHIns function as the transmit STS-1 or STS-3/STM-1 Data Input Port. If the System-Side Terminal Equipment intends to insert its own value for an overhead TOH or POH byte, into the outbound STS-1 or STS-3/STM-1 data-stream, then it is expected to sample the state of this output signal. Upon sampling the TxOHEnable signal high, the System-Side Terminal Equipment should (1) place the desired value of the overhead bits onto the TxOH input pin and (2) assert the TxOHIns input pin. The Transmit STS-1 TOH or POH Processor block will sample and latch the data on the TxOH input signal, upon the rising edge of the very next TxOHClk input signal. **If the XRT86Sh328 has been configured to operate in any other mode -NO FUNCTION:** Leave this pin floating.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
H4	RxDS1CLK_13/ TxTUPOHClk	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 13/Transmit VC-4 POH Data Input Port - Clock Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_13:** See Pin **G26 on page # 19** for pin description. **If the XRT86Sh328 (along with two other devices) has been configured to operate in the STM-1/TUG-3 Mode - TxTUPOHCLK:** This output pin, along with the TxTUPOH, TxTUPOHEnable, TxTUPOHFrame, TxTUPOHIns function as the Transmit VC-4 POH Data Input Port. The transmit VC-4POH Data Input Port will latch the data residing on the TxTUPOH and TxTUPOHIns input pins upon the rising edge of this clock output signal. **If the XRT86SH328 has been configured to operate in M13 MUX Mode -NO FUNCTION:** Leave this pin floating.
AB5	RxDS1CLK_14/ RxTUPOHValid	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 14/Receive VC-4 POH Data Output Port - Overhead Indicator Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_14:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 (along with two other devices) has been configured to operate in the STM-1/TUG-3 Mode - RxTUPOHValid:** This output pin, along with the RxTUPOH, RxTUPOHClk and RxTUPOHFrame pins function as the Receive VC-4 POH Data Output Port. This output pin will toggle and be held “High” coincident to whenever the Receive VC-4 POH Data Output Port outputs VC-4 POH data, via the RxTUPOH output pin. **If the XRT86SH328 has been configured to operate in M13 MUX Mode -NO FUNCTION:** Leave this pin floating.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AB4	RxDS1CLK_15/ RxTUPOHClk	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 15/Receive VC-4 POH Data Output Port- Clock Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_15:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 (along with two other devices) has been configured to operate in the STM-1/TUG-3 Mode - RxTUPOHCLK:** This output pin, along with the RxTUPOH, RxTUPOHValid and RxTUPOHFrame pins function as the Receive VC-4 POH Data Output Port. The Receive VC-4POH Data Ourput Port will update the data via the RxTUPOH, RxTUPOHValid and RxTUPOHFrame upon the rising edge of this clock output signal. **If the XRT86SH328 has been configured to operate in M13 MUX Mode -NO FUNCTION:** Leave this pin floating.
Y5	RxDS1CLK_16/ RxOHFrame	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 16/Receive STS-1/STM-1 TOH/POH Overhead Data Output Port- Frame Boundry Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_16:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 has been configured to operate in any SONET/SDH Mode - RxOHFrame** This output pin along with the RxOH, RxOHCLK and RxPOHInd pins will function as the Receive STS-1/STM-1 TOH/POH data Output Port. The Receive STS-1/STM-1 TOH/POH Data Output Port will pulse this output pin “High” for one RxOHCLK period coincident to whenever it outputs the very first OH bit within an given STS-1/STS-3 or STM-1 frame. *Note: This output pin will function in this role if the XRT86SH328 has been configured to operate in either of the following modes* • VT-*Mapper to STS-1 Mode* • *M1*3 MUX which is Asynchronously Mapped to STS-1 Mode **If the XRT86SH328 device has been configured to operate in the M13 MUX Mode – NO FUNCTION:** Leave this output pin floating.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
W5	RxDS1CLK_17/ RxOHClk	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 17/Receive STS-1/STM-1 TOH/POH Overhead Data Output Port – Clock Output signal:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_17:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 device has been configured to operate in any "SONET/ SDH" Mode – RxOHCLK:** This output pin, along with the RxOH, RxOHFrame and RxPOHInd will function as the Receive TOH/POH Data Output Port. The Receive TOH/POH Data Output Port will update the data (via the RxOH, RxOHFrame and RxPOHInd output pins upon the rising edge of this clock output signal. *Note: This output pin will function in this role if the XRT86SH328 device has been configured to operate in either of the following modes* • *VT-Mapper to STS-1 Mode* • *M13 MUX which is Asynchronously Mapped to STS-1 Mode* **If the XRT86SH328 device has been configured to operate in the M13 MUX Mode – NO FUNCTION:** Leave this output pin floating.
Y2	RxDS1CLK_18	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 18/Egress Direction - T1/E1 Data - Overhead Indicator Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_18:** See Pin **G26 on page # 19** for pin description. **All other modes - No Function:** If the XRT86SH328 is NOT configured to operate in the 28-Channel DS1/E1 Framer mode, then this output pin has no function and can be left floating.
W1	RxDS1CLK_19	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 19/Egress Direction - T1/E1 Data - Overhead Indicator Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_19:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 has been configured in any other mode - NO FUNCTION:** Leave this output pin floating.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
U3	RxDS1CLK_20	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 20/Egress Direction - T1/E1 Data - Overhead Indicator Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_20:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 is configured to operate in any other mode - No Function:** If the XRT86SH328 is configured to operate in any other mode, then this output pin has no function and can be left floating.
AB30	RxDS1CLK_21/ TxDS3CLK	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 21//Tranmit DS3 Line Interface – Clock Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_21:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 has been configured to transmit/receive DS3 data via the high-speed side of the chip - TxDS3CLK:** **If the XRT86SH328 has been configured to operate in the Aggregation Mode, then its exact behavior will depend upon the following.** Whether the chip has been configured to Share STS-1 and DS3 Interfaces. **a. If the XRT86SH328 has been configured NOT to share STS-1 and DS3 interface - TxDS3CLK:** The Transmit DS3 Framer block will transmit the outbound DS3 data-stream (via the TXDS3POS and TXDS3NEG output pins) upon either the rising or falling edge of this clock output signal. Connect this output pin to the Transmit Clock Input of an off-chip DS3/E3/STS-1 LIU IC. **b. If the XRT86SH328 has been configured to share STS-1 and DS3 Ports or exchange STS-1/STS-3/STM-1 via the Telecom Bus Interface - NO FUNCTION:** This output pin can be left floating.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AD30	RxDS1CLK_22/ TxDS3OHClk	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 22/Transmit DS3 Overhead Data Input Port – Clock Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_22:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 has been configured to operate in the M13 MUX Mode - TxDS3OHClk:** This output pin functions as the Transmit Overhead Data Input Interface clock signal. If the Transmit Overhead Data Input Interface block is enabled by asserting the TxDS3OHIns input pin, then the Transmit Overhead Data Input Interface block will sample and latch the data (residing on the TxDS3OH input pin) upon the falling edge of this signal. **If the XRT86SH328 has been configured to operate in the VT-Mapper Mode – NO FUNCTION:** This output pin can be left floating.
AD29	RxDS1CLK_23/ IG_TE1RxDATA_4	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 23/Ingress Direction T1/ E1 Data Drop Port - Data Bus Output pin # 4:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_23:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1RxDATA_4:** This output pin, along with IG_TE1RxDATA[7:0] , IG_TE1RxValid, IG__TE1RxOHInd[4:0], IG_TE1RxSLOT0 and IG_TE1RxCLK function as the byte-wide Ingress Direction - Drop Port. This Drop Port can be used for cross-connecting of T1/E1 time-slots with other XRT86SH328 devices. The Ingress Direction - Drop Port actually drops out the contents of all Ingress Direction T1 or E1 data that is being handled by the XRT86SH328. All Ingress Direction T1 or E1 data will be output via a byte-wide port (e.g., the IG_TE1RxDATA[7:0] output pins). This particular pin will function as bit 4 within this byte wide output port. As the Ingress Direction Drop port outputs the contents of the Ingress Direction T1/E1 traffic, it will update the contents of the IG_TE1RxDATA[7:0] output data bus upon the rising edge of IG_TE1RxCLK. *Note: The above Aggregation Modes include all of the following* • *The VT-Mapper Mode (w/ T1/E1 Framing)* • *The M13 MUX Mode (w/ T1/E1 Framing)* • *The M13 MUX to STS-1 Mode* • *The Transmux Mode*

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AD28	RxDS1CLK_24/ IG_TE1RxDATA_7	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 24/Ingress Direction T1/ E1 Data Drop Port - Data Bus Output pin # 7:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_24:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Mode - IG_TE1RxDATA_7:** See Pin **AD29 on page # 31** for pin description.
AE28	RxDS1CLK_25/ IG_TE1RxSLOT0	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 25/Ingress Direction T1/ E1 Data Drop Port - Channel # 0 Indicator Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_25:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1RxSLOT0:** This output pin, along with IG_TE1RxDATA[7:0], IG_TE1RxOHInd[4:0], IG_TE1RxValid and IG_TE1RxCLK function as the byte-wide Ingress Direction - Drop Port. This Drop Port can be used for cross-connecting of T1/E1 time-slots with other XRT86SH328 devices. The Ingress Direction - Drop Port actually drops out the contents of all Ingress Direction T1 or E1 data that is being handled by the XRT86SH328. All Ingress Direction T1 or E1 data will be output via a byte-wide port (e.g., the IG_TE1RxDATA[7:0] output pins). This particular output pin will is used to indicate whenever T1/E1 data (associated with Ingress Direction T1/E1 Channel 0) is being output via the IG_TE1RxDATA[7:0] output data bus. This output pin will pulse "High" for one IG_TE1RxCLK clock period coincident to whenever data, pertaining to Ingress Direction T1/E1 Channel 0 is being output via the IG_TE1RxDATA[7:0] output data bus. This output pin will be at a logic "LOW" at all other times. This output pin is updated upon the rising edge of IG_TE1RxCLK. *Note: The above Aggregation Modes include all of the following.* *The VT-Mapper Mode (w/ T1/E1 Framing)* *The M13 MUX Mode (w/ T1/E1 Framing)* *The M13 MUX to STS-1 Mode* *The Transmux Mode*

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

<table>
<tr><th>Pin/Ball #</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td>AJ30</td><td>RxDS1CLK_26/
IG_TE1RxOHInd_2</td><td>O</td><td>
Receive DS1/E1 Serial Clock Output Pin - Channel 26/Ingress Direction T1/E1 Data Drop Port - Data Type Indicator output pin # 2:
The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in.
If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_26:
See Pin G26 on page # 19 for pin description.
If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1RxOHInd_2:
This output pin, along with IG_TE1RxDATA[7:0], IG_TE1RxValid, IG_TE1RxOHInd[4:0], IG_TE1RxSLOT0 and IG_TE1RxCLK function as the byte-wide Ingress Direction - Drop Port. This Drop Port can be used for cross-connecting of T1/E1 time-slots with other XRT86SH328 devices. This particular pin will function as the Overhead Indicator - Bit [4:0] output within this byte wide output port.As the Ingress Direction Drop port outputs the contents of the Ingress Direction T1/E1 traffic, this output pin (along with IG_TE1RxOHInd[4:3] and IG_TE1RxOHInd[1:0]) will indicate (1) whether the data, residing on IG_TE1RxDATA[7:0] contains any overhead bits, and (2) which of the 8 bits (within IG_TE1RxDATA[7:0]) is an overhead bit. The relationship between the states of the IG_TE1RxOHInd[4:0] output, and how the user should interpret the data, residing on the IG_TE1RxDATA[7:0] output pins is tabulated below.
<table>
<tr><th>IG_TE1RxOHInd[4:0]</th><th>What's on IG_TE1RxDATA[7:0] Bus?</th></tr>
<tr><td>00 xxx</td><td>All bits on bus are T1/E1 payload bits</td></tr>
<tr><td>01 000</td><td>IG_TE1RxDATA_0 contains an overhead bit</td></tr>
<tr><td>01 001</td><td>IG_TE1RxDATA_1 contains an overhead bit</td></tr>
<tr><td>01 010</td><td>IG_TE1RxDATA_2 contains an overhead bit</td></tr>
<tr><td>01 011</td><td>IG_TE1RxDATA_3 contains an overhead bit</td></tr>
<tr><td>01 100</td><td>IG_TE1RxDATA_4 contains an overhead bit</td></tr>
<tr><td>01 101</td><td>IG_TE1RxDATA_5 contains an overhead bit</td></tr>
<tr><td>01 110</td><td>IG_TE1RxDATA_6 contains an overhead bit</td></tr>
<tr><td>01 111</td><td>IG_TE1RxDATA_7 contains an overhead bit</td></tr>
<tr><td>11 000</td><td>IG_TE1RxDATA_0 contains a multi-frame alignment bit</td></tr>
<tr><td>11 001</td><td>IG_TE1RxDATA_1 contains a multi-frame alignment bit</td></tr>
<tr><td>11 010</td><td>IG_TE1RxDATA_2 contains a multi-frame alignment bit</td></tr>
<tr><td>11 011</td><td>IG_TE1RxDATA_3 contains a multi-frame alignment bit</td></tr>
<tr><td>11 100</td><td>IG_TE1RxDATA_4 contains a multi-frame alignment bit</td></tr>
<tr><td>11 101</td><td>IG_TE1RxDATA_5 contains a multi-frame alignment bit</td></tr>
<tr><td>11 110</td><td>IG_TE1RxDATA_6 contains a multi-frame alignment bi</td></tr>
<tr><td>11 111</td><td>IG_TE1RxDATA_7 contains a multi-frame alignment bit</td></tr>
</table>
This signal will updated upon the rising edge of IG_TE1RxCLK.
Note: The above Aggregation Modes include all of the following.
• The VT-Mapper Mode (w/ T1/E1 Framing)
• The M13 MUX Mode (w/ T1/E1 Framing)
• The M13 MUX to STS-1 Mode
• The Transmux Mode
</td></tr>
</table>

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AF27	RxDS1CLK_27/ IG_TE1RxCLK	O	**Receive DS1/E1 Serial Clock Output Pin - Channel 27/Ingress Direction T1/ E1 Data Drop Port - Byte Wide Clock Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1CLK_27:** See Pin **G26 on page # 19** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1RxCLK:** This output pin, along with IG_TE1RxDATA[7:0], IG_TE1RxValid, IG_TE1RxOHInd[4:0], and IG_TE1RxSLOT0 function as the byte-wide Ingress Direction - Drop Port. This Drop Port can be used for cross-connecting of T1/E1 time-slots with other XRT86SH328 devices. This particular pin will function as the Byte-Wide Clock output signal within this byte wide output port. As the Ingress Direction Drop port outputs the contents of the Ingress Direction T1/E1 traffic, all data (that is updated on via the IG_TE1RxOHInd[4:0], the IG_TE1RxDATA[7:0] and the IG_TE1RxSLOT0 outputs) will be updated upon the rising edge of this output clock signal. *Note: The above Aggregation Modes include all of the following* • *The VT-Mapper Mode (w/ T1/E1 Framing)* • *The M13 MUX Mode (w/ T1/E1 Framing)* • *The M13 MUX to STS-1 Mode* • *The Transmux Mode*
B30	RxDS1DATA_0/ EG_TE1RxDATA_1	O	**Receive DS1/E1 Serial Data Output Pin - Channel 0/Egress Direction T1/E1 Data Drop Port - Data Bus Output pin # 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_0:** This output pin, along with RxDS1CLK_0 and RxDS1Frame_0 will function as the Receive Serial Data Output port for Channel 0.The Receive Serial Data Output Port (within the XRT86SH328) will update the Receive-Direction output data (via this output pin) upon either the rising or falling edge of the RxDS1CLK_0 output clock signal (depending upon user configuration). **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1RxDATA_1:** **See Pin G26 on page # 19 for pin description.**
C30	RxDS1DATA_1/ EG_TEIRxDATA_4	O	**Receive DS1/E1 Serial Data Output Pin - Channel 1/Egress Direction T1/E1 Data Drop Port - Data Bus Output pin # 4:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_1:** See Pin **B30 on page # 34** for pin description. **If the XRT86SL832 device has been configured to operate in the various Aggregation Modes - EG_TE1RxDATA_4:** See Pin **G26 on page # 19** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
H27	RxDS1DATA_2/ EG_TE1RxDATA_7	O	**Receive DS1/E1 Serial Data Output Pin - Channel 2/Egress Direction T1/E1 Data Drop Port - Data Bus Output pin # 7:** The function of this output depends on which mode the XRT86SH328 has been configured in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_2:** See Pin **B30 on page # 34** for pin description. **If the XRT86SL832 device has been configured to operate in the various Aggregation Modes - EG_TE1RxDATA_7:** See Pin **G26 on page # 19** for pin description.
G29	RxDS1DATA_3/ EG_TE1RxSLOT0	O	**Receive DS1/E1 Serial Data Output Pin - Channel 3/Egress Direction T1/E1 Data Drop Port - Channel 0 Indicator Output:** The function of this output depends on which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_3:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - EG_TE1RxSLOT0:** This output pin, along with EG_TE1RxDATA[7:0], EG_TE1RxOHInd[4:0], EG_TE1RxValid and EG_TE1RxCLK function as the byte-wide Ingress Direction - Drop Port. This Drop Port can be used for cross-connecting of T1/E1 time-slots with other XRT86SH328 devices. The Egress Direction - Drop Port actually drops out the contents of all Egress Direction T1 or E1 data that is being handled by the XRT86SH328. All Egress Direction T1 or E1 data will be output via a byte-wide port (e.g., the EG_TE1RxDATA[7:0] output pins). This particular output pin will is used to indicate whenever T1/E1 data (associated with Egress Direction T1/E1 Channel 0) is being output via the EG_TE1RxDATA[7:0] output data bus. This output pin will pulse "High" for one EG_TE1RxCLK clock period coincident to whenever data, pertaining to Egress Direction T1/E1 Channel 0 is being output via the EG_TE1RxDATA[7:0] output data bus. This output pin will be at a logic "LOW" at all other times. This output pin is updated upon the rising edge of EG_TE1RxCLK. *Note: The above Aggregation Modes include all of the following.* • *The VT-Mapper Mode (w/ T1/E1 Framing)* • *The M13 MUX Mode (w/ T1/E1 Framing)* • *The M13 MUX to STS-1 Mode* • *The Transmux Mode*
H29	RxDS1DATA_4/ EG_TE1RxOHInd_2	O	**Receive DS1/E1 Serial Data Output Pin - Channel 4/Egress Direction T1/E1 Data Drop Port - Data Type Indicator output pin # 2:** The function of this output pin depends on which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_4:** See Pin **B30 on page # 34** for pin description. **If the XRT86SL832 device has been configured to operate in the various Aggregation Modes - EG_TE1RxOHInd_2:** **See Pin K26 on page # 21 for pin description**

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
K28	RxDS1DATA_5/ RxDS3OH	O	**Receive DS1/E1 Serial Data Output Pin - Channel 5/Receive DS3 Overhead Data Output Port – Data Output:** The function of this output pin depends on which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_5:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 has been configured to operate in the M13 MUX Mode - RxDS3OH:** All DS3 overhead bits, which are received via the Receive Section of the XRT86SH328 will be output via this output pin, upon the rising edge of RxDS3OHClk. **If the XRT86SH328 has been configured to operate in the VT-Mapper Mode – NO FUNCTION:** This output pin can be left floating.
K30	RxDS1DATA_6/ EG_TE1RxOHInd_4	O	**Receive DS1/E1 Serial Data Output Pin - Channel 6/Egress Direction T1/E1 Data Drop Port - Data Type Indicator output pin # 4:** The function of this output pin depends on which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_6:** See Pin **B30 on page # 34** for pin description. **If the XRT86SL832 device has been configured to operate in the various Aggregation Modes - EG_TE1RxOHInd_4:** **See Pin K26 on page # 21 for pin description**

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
R5	RxDS1DATA_7/ TxSTS-1DATA/ TxDS3POS	O	**Receive DS1/E1 Serial Data Output Pin - Channel 7/Egress Direction - T1/ E1 Data - Output - pin 1/Transmit DS3/STS-1 Data Output pin (shared Port):** The function of this output pin depends on which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_7:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - TxSTS-1DATA/TxDS3POS:** If the XRT86SH328 has been configured to operate in an Aggregation Mode, then its exact behavior will depend upon the following • Whether the chip has been configured to output DS3 or STS-1 data • Whether the chip has been configured to Share STS-1 and DS3 Interfaces. **1. If the XRT83SH328 has been configured to output DS3 data via the High-Speed side of the chip - TxDS3POS** The Transmit DS3 Framer block will output the positive-polarity portion of the outbound DS3 data (towards the off-chip DS3/E3 LIU IC) via this output pin. The XRT86SH328 will update this outbound DS3 data upon the user-selected edge of the TXDS3LINECLK output signal.The Negative-Portion of the outbound DS3 data (towards the off-chip DS3 LIU IC) will be output via the TxDS3NEG output pin. **2. If the XRT83SH328 has been configured to output STS-1 data via the High-Speed Side of the chip - TxSTS-1DATA** The Transmit STS-1 TOH Processor block will output the outbound STS-1 data via this output pin. The outbound STS-1 data-stream will be updated upon the user-selected edge of the TXSTS1CLK output pin. *Notes:* 1. *If the XRT86SH328 is configured to operate in either the STS-1 Mode, or in the Single-Rail Mode (if also configured to operate in the DS3 Mode), then all outbound DS3 or STS-1 data will be output via this output pin (towards the off-chip DS3/E3/STS-1 LIU IC).* 2. *Only use this particular output pin (for DS3 applications) if the STS-1 and the DS3 Ports are configured to be shared. If the STS-1 and DS3 Ports are configured to be separate (which would be necessary for Transmux applications), then use the TxDS3POS signal at Ball Y28.*

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
N3	RxDS1DATA_8/ TxA_PL	O	**Receive DS1/E1 Serial Data Output Pin - Channel 8/Transmit STS-1/STM-1 Telecom Bus Interface - Payload Indicator:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_8:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 has been configured to output STS-1/STM-1 data via the Transmit STS-1/STM-1 Telecom Bus Interface - TxA_PL:** This output pin indicates whether or not TOH (Transport Overhead) bytes are being output via the TXA_D[7:0] output pins. This output pin is pulled "Low" for the duration that the Transmit STS-1/STM-1 Telecom Bus Interface is transmitting a Transport Overhead byte via the TXA_D[7:0] output pins. Conversely, this output pin is pulled "High" for the duration that the Transmit STS-1/STM-1 Telecom Bus Interface is transmitting something other than a Transport Overhead byte (e.g., the POH or STS-1/STS-3c SPE bytes) via the TXA_D[7:0] output pins. **All other modes - No Function:** If the XRT86SH328 is NOT configured to operate in either of the above modes, then this output pin has no function and can be left floating.
K1	RxDS1DATA_9/ TxA_ALARM	O	**Receive DS1/E1 Serial Data Output Pin - Channel 9/Transmit STS-1/STM-1 Telecom Bus Interface - ALARM Indicator Output:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_9:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 has been configured to output STS-1/STM-1 data via the Transmit STS-1/STM-1 Telecom Bus Interface - TxA_ALARM:** This output pin pulses "High", coincident to the instant that the Transmit STS-1/ STM-1 Telecom Bus Interface is transmitting a byte (via the TxA_D[7:0] output pin) of an STS-1/STM-1 signal that is carrying the AIS-P indicator. This output pin is "Low" for all other conditions. **All other modes - No Function:** If the XRT86SH328 is NOT configured to operate in either of the above modes, then this output pin has no function and can be left floating.
H1	RxDS1DATA_10/ TxA_D_2	O	**Receive DS1/E1 Serial Data Output Pin - Channel 10/Transmit STS-1/STM-1 Telecom Bus Interface - Data Bus output pin # 2:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_10:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 has been configured to output STS-1/STM-1 data via the Transmit STS-1/STM-1 Telecom Bus Interface - TxA_D_2** See Pin **K2 on page # 25** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
H2	RxDS1DATA_11/ TxA_D_5	O	**Receive DS1/E1 Serial Data Output Pin - Channel 11/Transmit STS-1/STM-1 Telecom Bus Interface - Data Bus output pin # 6:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 device has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_11:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 has been configured to output STS-1/STM-1 data via the Transmit STS-1/STM-1 Telecom Bus Interface - TxA_D_5** See Pin **K2 on page # 25** for pin description.
H3	RxDS1DATA_12/ TxOHClk	O	**Receive DS1/E1 Serial Data Output Pin - Channel 12/Transmit STS-1/STM-1 TOH/POH Overhead Data Output Port – Clock Output:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_12:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 device has been configured to operate in any SONET/ SDH Mode – TxOHClk:** This output pin, along with the TxOH, TxOHFrame, and TxPOHInd will function as the “Transmit STS-1/STM-1 TOH/POH Data Input Port. The Transmit STS-1/STM-1 TOH/POH Data Input Port will sample the data being provided to the TxOH and TxOHIns input pins upon the rising edge of this clock output signal. This output pin will function in this role if the XRT86SH328 device has been configured to operate in either of the following modes. • *VT-Mapper to STS-1 Mode* • *M13 MUX which is Asynchronously Mapped to STS-1 Mode*
D1	RxDS1DATA_13/ TxTUPOHEnable	O	**Receive DS1/E1 Serial Data Output Pin - Channel 13/Transmit VC-4 POH Data Input Port – Enable Output:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_13:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 (along with two other devices) has been configured to operate in the STM-1/TUG-3 Mode – TxTUPOHEnable:** This output pin, along with the TxTUPOH, TxTUPOHCLK, TxTUPOHIns and TxTUPOHFrame function as the “Transmit VC-4 POH Data Input Port. This output pin will be driven “High” for the duration that the Transmit VC-4 POH Data Input Port is ready to externally accept (and insert) VC-4 POH Data into the output VC-4 data-stream. This output pin will be updated upon the rising edge of TxTUPOHCLK.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AC4	RxDS1DATA_14	O	**Receive DS1/E1 Serial Data Output Pin - Channel 14:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_14:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 is NOT configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - No Function:** If the XRT86SH328 is NOT configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode, then this pin has no function and can be left floating.
AA5	RxDS1DATA_15/ RxTUPOH	O	**Receive DS1/E1 Serial Data Output Pin - Channel 15//Receive VC-4 POH Data Output Port – Data Output:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_15:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 (along with two other devices) has been configured to operate in the STM-1/TUG-3 Mode – RxTUPOH:** This output pin, along with the RxTUPOHClk and RxTUPOHFrame function as the “Receive VC-4 POH Data Output Port. This output pin will output the contents of the VC-4 POH bytes within the incoming VC-4 data-streams. This output is updated upon the rising edge of RxTUPOHCLK. **If the XRT86SH328 has been configured to operate in the M13 MUX Mode – NO FUNCTION:** Leave this output pin “floating”.
AB3	RxDS1DATA_16/ RxPOH_Ind	O	**Receive DS1/E1 Serial Data Output Pin - Channel 16/Receive STS-1/STM-1 TOH/POH Overhead Data Output Port – POH Indicator Output:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_16:** See Pin **B30 on page # 34** for pin description. If the XRT86SH328 has been configured to operate in any SONET/SDH Mode – RxPOH_Ind: This output pin, along with the RxOH, RxOHFrame, and RxOHClk will function as the Receive STS-1/STM-1 TOH/POH Data Output Port. The Receive STS-1/STM-1 TOH/POH Data Output Port will toggle this output pin “High” coincident to whenever it outputs POH byte data via the RxOH output pin. This output pin is updated upon the rising edge of RxOHClk. This output pin will function in this role if the XRT86SH328 device has been configured to operate in either of the following modes. • *VT-Mapper to STS-1 Mode* • *M13 MUX which is Asynchronously Mapped to STS-1 Mode* **If the XRT86SH328 device has been configured to operate in the M13 MUX Mode – NO FUNCTION:** Leave this output pin “floating”.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
Y4	RxDS1DATA_17/ RxOHValid	O	**Receive DS1/E1 Serial Data Output Pin - Channel 17/Receive STS-1/STM-1 TOH/POH Overhead Data Output Port – OH Valid Indicator Output:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_17:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 device has been configured to operate in any SONET/ SDH Mode – RxOHValid:** This output pin, along with the RxOH, RxOHFrame and RxOHClk will function as the Receive STS-1/STM-1 TOH/POH Data Output Port. This output pin will toggle and be held at the logic “High” level for the duration that the Receive STS-1/STM-1 TOH/POH Output Port outputs valid TOH or POH data via the RxOH output pin. This output pin will be at the logic “LOW” level at all other times. **If the XRT86SH328 device has been configured to operate in the M13 MUX Mode – NO FUNCTION:** This output pin can be left floating.
W4	RxDS1DATA_18	O	**Receive DS1/E1 Serial Data Output Pin - Channel 18/Egress Direction - T1/ E1 Data - Output - pin 1:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_18:** See Pin **B30 on page # 34** for pin description. **All other modes – NO FUNCTION:** If the XRT86SH328 is NOT configured to operate in the 28-Channel DS1/E1 Framer mode, then this output pin has no function and can be left floating.
V4	RxDS1DATA_19	O	**Receive DS1/E1 Serial Data Output Pin - Channel 19/Egress Direction - T1/ E1 Data - Output - pin 1:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_19:** See Pin **B30 on page # 34** for pin description. **All other modes – NO FUNCTION:** If the XRT86SH328 is NOT configured to operate in the 28-Channel DS1/E1 Framer mode, then this output pin has no function and can be left floating.
U4	RxDS1DATA_20	O	**Receive DS1/E1 Serial Data Output Pin - Channel 20/Egress Direction - T1/ E1 Data - Output - pin 1:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_20:** See Pin **B30 on page # 34** for pin description. **All other modes – NO FUNCTION:** If the XRT86SH328 is NOT configured to operate in the 28-Channel DS1/E1 Framer mode, then this output pin has no function and can be left floating.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
Y28	RxDS1DATA_21/ TxDS3POS	O	**Receive DS1/E1 Serial Data Output Pin - Channel 21/Transmit DS3 Line Interface – Positive Polarity Data Output:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_21:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - TxDS3POS:** The Transmit DS3 Framer block will output the positive-polarity portion of the outbound DS3 data (towards the off-chip DS3/E3 LIU IC) via this output pin. The XRT86SH328 will update this outbound DS3 data upon the user-selected edge of the TXDS3CLK output signal. The Negative-Portion of the outbound DS3 data (towards the off-chip DS3/E3 LIU IC) will be output via the TxDS3NEG output pin. *Notes:* *1. The above Aggregation Modes include all of the following.* • *The VT-Mapper Mode (w/ T1/E1 Framing)* • *The M13 MUX Mode (w/ T1/E1 Framing)* • *The M13 MUX to STS-1 Mode* • *The Transmux Mode* *2. Only use this particular output pin (for DS3 applications) if the STS-1 and the DS3 Ports are configured to be separate. If the STS-1 and DS3 Ports to are configured to be shared, then use the TxDS3POS signal at Ball R5.*
W26	RxDS1DATA_22/ TxDS3OHEnable	O	**Receive DS1/E1 Serial Data Output Pin - Channel 22//Transmit DS3 Overhead Data Input Interface – Enable Output:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_22:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 has been configured to operate in the M13 MUX or Transmux Mode - TxDS3OHEnable:** The Transmit DS3 Framer block will assert this output pin, for one Tx44MHzClk_In period, just prior to the instant that the Transmit Overhead Data Input Interface will be sampling and processing an overhead bit. If the System-Side terminal equipment intends to insert its own value for an overhead bit, into the outbound DS3 data stream, then it is expected to sample the state of this signal, upon the falling edge of Tx44MHzClk_In. Upon sampling the TxDS3OHEnable signal high, the System-Side terminal equipment should (1) place the desired value of the overhead bit, onto the TxDS3OH input pin and (2) assert the TxDS3OHIns input pin. The Transmit Overhead Data Input Interface block will sample and latch the data on the TxDS3OH signal, upon the rising edge of the very next Tx44MHzClk_In input signal. **If the XRT86SH328 has been configured to operate in the VT-Mapper Mode – NO FUNCTION:** This output pin can be left floating.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
Y26	RxDS1DATA_23/ IG_TE1RxDATA_3	O	**Receive DS1/E1 Serial Data Output Pin - Channel 23/Ingress Direction T1/ E1 Data Drop Port - Data Bus Output pin # 3:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_23:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1RxDATA_3:** See Pin **AD29 on page # 31** for pin description.
AA26	RxDS1DATA_24/ IG_TE1RxDATA_6	O	**Receive DS1/E1 Serial Data Output Pin - Channel 24/Ingress Direction T1/ E1 Data Drop Port - Data Bus Output pin # 6:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_24:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1RxDATA_6:** See Pin **AD29 on page # 31** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AA25	RxDS1DATA_25/ IG_TE1RxVALID	O	**Receive DS1/E1 Serial Data Output Pin - Channel 25/Ingress Direction T1/ E1 Data Drop Port - Data Valid Output pin:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_25:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1RxVALID:** This output pin, along with IG_TE1RxDATA[7:0], IG_TE1RxOHInd[4:0], IG_TE1RxSLOT0 and IG_TE1RxCLK function as the byte-wide Ingress Direction - Drop Port. This Drop Port can be used to for "cross-connecting of T1/ E1 Time-slots with other XRT86SH328 devices. The Ingress Direction - Drop Port actually drops out the contents of all Ingress Direction T1 or E1 traffic that is being handled by the XRT86SH328. All Ingress Direction T1 or E1 data will be output via a byte-wide port (e.g., the IG_TE1RxDATA[7:0] output pins). This particular pin will function as the Valid Data output pin for the Port. This output pin will be pulsed "HIGH" coincident to whenever valid T1 or E1 data is being output via the IG_TE1RxDATA[7:0] output data bus. Conversely, this output pin will be pulsed "LOW" coincident to whenever in-valid T1 or E1 data is being output via the IG_TE1RxDATA[7:0] output data bus. *Notes:* *1. In this case, valid T1 or E1 data is defined as that which has been assigned user traffic. In contrast, in valid T1 or E1 data is defined as that which is inactive and has NOT assigned any user traffic.* *2. The above Aggregation Modes include all of the following* • *The VT-Mapper Mode (w/ T1/E1 Framing)* • *The M13 MUX Mode (w/ T1/E1 Framing)* • *The M13 MUX to STS-1 Mode* • *The Transmux Mode*
AF28	RxDS1DATA_26/ IG_TE1RxOHInd_1	O	**Receive DS1/E1 Serial Data Output Pin - Channel 26/Ingress Direction T1/ E1 Data Drop Port - Data Type Indicator output pin # 1:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_26:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1RxOHInd_1:** See Pin **AJ30 on page # 33** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AC25	RxDS1DATA_27/ IG_TE1RxOHInd_4	O	**Receive DS1/E1 Serial Data Output Pin - Channel 27/Ingress Direction T1/ E1 Data Drop Port - Data Type Indicator Output pin # 4:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1DATA_27:** See Pin **B30 on page # 34** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1RxOHInd_4:** See Pin **AJ30 on page # 33** for pin description.
C29	RxDS1FRAME_0/ EG_TE1RxDATA_0	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 0/Egress Direction T1/E1 Data Drop Port- Data Bus Output pin # 0:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_0:** This output pin, along with RxDS1CLK_0 and RxDS1DATA_0 will function as the Receive Serial Data Output port for Channel 0. The Receive Serial Data Output Port (within the Channel 0 of the XRT86SH328) will pulse this output pin "High" (for one RxDS1CLK_0 period) coincident to whenever the Receive Serial Data Output Interface outputs the very first bit of a given DS1 or E1 frame. The Receive Serial Data Output Interface block will hold this output pin "Low" for the remainder of the DS1 or E1 frame period. **If the XRT86SL832 device has been configured to operate in the various Aggregation Modes - EG_TE1RxDATA_0:** See Pin **G26 on page # 19** for pin description.
D29	RxDS1FRAME_1/ EG_TE1RxDATA_3	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 1/Egress Direction T1/E1 Data Drop Port - Data Bus Output pin # 3:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_1:** See Pin **C29 on page # 45** for pin description. **If the XRT86SL832 device has been configured to operate in the various Aggregation Modes - EG_TE1RxDATA_3:** See Pin **G26 on page # 19** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
D30	RxDS1FRAME_2/ EG_TE1RxDATA_6	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 2/Egress Direction T1/E1 Data Drop Port - Data Bus Output pin # 6:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_2:** See Pin **C29 on page # 45** for pin description. **If the XRT86SL832 device has been configured to operate in the various Aggregation Modes - EG_TE1RxDATA_6:** See Pin **G26 on page # 19** for pin description.
E30	RxDS1FRAME_3/ EG_TE1RxValid	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 3/Egress DirectionT1/E1 Data Drop Port - Valid Data Output Indicator:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_3:** See Pin **C29 on page # 45** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - EG_TE1RxVALID:** This output pin, along with EG_TE1RxDATA[7:0], EG_TE1RxOHInd[4:0], EG_TE1RxSLOT0 and EG_TE1RxCLK function as the byte-wide Egress Direction - Drop Port.. This Drop Port can be used to for “cross-connecting of T1/E1 Time-slots with other XRT86SH328 devices. The Egress Direction - Drop Port actually drops out the contents of all Egress Direction T1 or E1 traffic that is being handled by the XRT86SH328. All Egress Direction T1 or E1 data will be output via a byte-wide port (e.g., the EG_TE1RxDATA[7:0] output pins). This particular pin will function as the Valid Data output pin for the Port. This output pin will be pulsed "HIGH" coincident to whenever valid T1 or E1 data is being output via the EG_TE1RxDATA[7:0] output data bus. Conversely, this output pin will be pulsed "LOW" coincident to whenever in-valid T1 or E1 data is being output via the EG_TE1RxDATA[7:0] output data bus. *Notes:* *1. In this case, valid T1 or E1 data is defined as that which has been assigned user traffic. In contrast, in valid T1 or E1 data is defined as that which is inactive and has NOT assigned any user traffic.* *2. 2. The above Aggregation Modes include all of the following.* • *The VT-Mapper Mode (w/ T1/E1 Framing)·* • *The M13 MUX Mode (w/ T1/E1 Framing)* • *The M13 MUX to STS-1 Mode* • *The Transmux Mode*

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
G30	RxDS1FRAME_4/ EG_TE1RxOHInd_1	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 4/Egress Direction T1/E1 Data Drop Port - Data Type Indicator output pin # 1:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_4:** See Pin **C29 on page # 45** for pin description. **If the XRT86SL832 device has been configured to operate in the various Aggregation Modes - EG_TE1RxOHInd_1:** See Pin **K26 on page # 21** for pin description
J29	RxDS1FRAME_5/ RxDS3OHFrame	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 5/Receive DS3 Overhead Data Output Port – Frame Boundary Output:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_5:** See Pin **C29 on page # 45** for pin description. **If the XRT86SH328 has been configured to operate in the M13 MUX Mode - RxDS3OHFrame:** The XRT86SH328 will assert this output signal for one RxDS3OHClk period when it is safe for the system-side terminal equipment to sample the data on the RxDS3OH output pin. **If the XRT86SH328 has been configured to operate in the VT-Mapper Mode – NO FUNCTION:** This output pin can be left floating.
L28	RxDS1FRAME_6/ EG_TE1RxOHInd_3	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 6/Egress Direction T1/E1 Data Drop Port - Data Type Indicator output pin # 3:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_6:** See Pin **C29 on page # 45** for pin description. **If the XRT86SL832 device has been configured to operate in the various Aggregation Modes - EG_TE1RxOHInd_3:** See Pin **K26 on page # 21** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
P2	RxDS1FRAME_7/ TxSTS-1FRAME/ TxDS3NEG	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 7/ransmit STS-1 LIU Interface – Frame Boundary Output/Transmit DS3 LIU Interface – Negative-Polarity Data Output:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **A. If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_7:** See Pin **C29 on page # 45** for pin description. **B. If the XRT86SH328 has been configured to output DS3 data via the High-Speed side of the chip:** The function of this output pin depends upon whether the Transmit DS3 LIU Interface block has been configured to operate in the Single-Rail or Dual-Rail Mode. **B1. If the Transmit DS3 LIU Interface Block has been configured to operate in the Single-Rail Mode - NO FUNCTION:** Leave this output pin floating. **B2. If the Transmit DS3 LIU Interface block has been configured to operate in the Dual-Rail Mode - TxDS3NEG:** The Transmit DS3 Framer block will output the negative-polarity portion of the outbound DS3 data (towards the off-chip DS3/E3 LIU IC) via this output pin. The XRT86SH328 will update this output DS3 data upon the user-selected edge of the TXDS3CLK output signal (Ball P3).The Positive-Polarity Portion of the outbound DS3 data (towards the off-chip DS3/E3 LIU IC) will be output via the TxDS3POS output pin (Ball R5). *Note: Only use this particular output pin (for DS3 applications) if the STS-1 and the DS3 Ports are configured to be shared. If the STS-1 and DS3 Ports are configured to be separate (which would be necessary for Transmux applications), then use the TxDS3NEG signal at Ball V26.* **C. If the XRT86SH328 has been configured to output STS-1 data via the High-Speed Side of the chip - TxSTS-1Frame:** The Transmit STS-1 TOH Processor block will pulse this output pin "HIGH" coincident to whenever it outputs the very first bit of an outbound STS-1 frame, via the TxSTS-1DATA output pin. *Note: For STS-1 Applications, to interface the XRT86SH328 to an off-chip DS3/ E3/STS-1 LIU IC, then DO NOT connect this pin to the TNEG input pin of the LIU IC.*

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
M1	RxDS1FRAME_8/ TxA_CLK	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 8/Transmit STS-1/STS-3/STM-1 Telecom Bus Interface – Clock Output pin:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_8:** See Pin **C29 on page # 45** for pin description. **If the XRT86SH328 has been configured to output STS-1/STM-1 data via the Transmit STS-1/STM-1 Telecom Bus Interface - TxA_CLK:** This output clock signal functions as the clock source for the Transmit STS-1/ STM-1 Telecom Bus. All signals, that are output via the Transmit STS-1/STM-1 Telecom Bus, are updated upon the rising edge of this clock signal. This clock signal operates at 6.48MHz (for STS-1 applications) and 19.44MHz (for STM-1 applications). **All other modes – NO FUNCTION:** This output pin can be left floating.
L2	RxDS1FRAME_9/ TxA_DP	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 9/Transmit STS-1/STS-3/STM-1 Telecom Bus Interface – Data Parity Output pin:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_9:** See Pin **C29 on page # 45** for pin description. **If the XRT86SH328 has been configured to output STS-1/STM-1 data via the Transmit STS-1/STM-1 Telecom Bus Interface - TxA_DP:** This output pin can be configured to function as one of the following. 1.The EVEN or ODD parity value of the bits which are output via the TXA_D[7:0] output pins. 2.The EVEN or ODD parity value of the bits which are being output via the TXA_D[7:0] output pins and the states of the TXA_PL and TXA_C1J1 output pins. Any one of these configuration selections can be made by writing the appropriate value into the Telecom Bus Control Register (Direct Address = ?). **All other modes – NO FUNCTION:** This output pin can be left floating.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
J1	RxDS1FRAME_10/ TxA_D_1	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 10/Transmit STS-1/STS-3/STM-1 Telecom Bus Interface – Data Bus Output pin – Bit 1 Output:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_10:** See Pin **C29 on page # 45** for pin description. **If the XRT86SH328 has been configured to output STS-1/STM-1 data via the Transmit STS-1/STM-1 Telecom Bus Interface - TxA_D_1** See Pin **K2 on page # 25** for pin description. **All other modes – NO FUNCTION:** This output pin can be left floating.
G1	RxDS1FRAME_11/ TxA_D_4	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 11/Transmit STS-1/STS-3/STM-1 Telecom Bus Interface – Data Bus Output pin – Bit 4 Output:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_11:T** See Pin **C29 on page # 45** for pin description. **If the XRT86SH328 has been configured to output STS-1/STM-1 data via the Transmit STS-1/STM-1 Telecom Bus Interface - TxA_D_4** See Pin **K2 on page # 25** for pin description. **All other modes – NO FUNCTION:** This output pin can be left floating.
G2	RxDS1FRAME_12/ TxA_D_7	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 12/Transmit STS-1/STS-3/STM-1 Telecom Bus Interface – Data Bus Output pin – Bit 7 Output1:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_12:** See Pin **C29 on page # 45** for pin description. **If the XRT86SH328 has been configured to output STS-1/STM-1 data via the Transmit STS-1/STM-1 Telecom Bus Interface - TxA_D_7** See Pin **K2 on page # 25** for pin description. **All other modes – NO FUNCTION:** This output pin can be left floating

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
G3	RxDS1FRAME_13/ TxTUPOHFrame	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 13/Transmit VC-4 POH Data Input Port – Frame Boundary Output:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_13:** See Pin **C29 on page # 45** for pin description. **If the XRT86SH328 has been configured (along with two other devices) has been configured to operate in the STM-1/TUG-3 Mode – TxTUPOHFrame:** This output pin, along with the TxTUPOH, TxTUPOHEnable, TxTUPOHClk and TxTUPOHIns function as the Transmit VC-4 POH Data Input Port. The Transmit VC-4 POH Data Input Port will pulse this output pin “high” (for one TxTUPOHClk period) coincident to whenever the Transmit VC-4 POH Data Input port is ready to externally accept the very first VC-4 POH bit via the TxTUPOH input pin. This output pin will be updated upon the rising edge of TxTUPOHClk. **If the XRT86SH328 device has been configured to operate in the “M13 MUX” Mode – NO FUNCTION:** Leave this output pin floating.
AG1	RxDS1FRAME_14	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 14/Egress Direction - T1/E1 Data - Output - pin 1:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_14:** See Pin **C29 on page # 45** for pin description. **All other modes – NO FUNCTION:** This output pin can be left floating

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AD2	RxDS1FRAME_15/ RxTUPOHFrame	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 15/Receive VC-4 POH Data Output Port – Frame Boundary Output:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_15:** See Pin **C29 on page # 45** for pin description. **If the XRT86SH328 has been configured (along with two other devices) has been configured to operate in the STM-1/TUG-3 Mode – RxTUPOHFrame:** This output pin, along with the RxTUPOH and RxTUPOHClk will function as the Receive VC-4 POH Data Output Port. The Receive VC-4 POH Data Output Port will pulse this output pin “high” coincident to whenever it outputs the very first bit of the VC-4 POH, within the incoming VC-4 data-stream. The Receive VC-4 POH Data Output Port will update this output pin upon the rising edge of RxTUPOHClk. **If the XRT86SH328 device has been configured to operate in the “M13 MUX” Mode – NO FUNCTION:** Leave this output pin floating.
AC2	RxDS1FRAME_16	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 16/Egress Direction - T1/E1 Data - Output - pin 1:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_16:** See Pin **C29 on page # 45** for pin description. **All other modes – NO FUNCTION:** This output pin can be left floating
AA3	RxDS1FRAME_17/ RxOH	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 17//Receive STS-1/STM-1 TOH/POH Overhead Data Output Port – Data Output:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_17:** See Pin **C29 on page # 45** for pin description. **If the XRT86SH328 has been configured to operate in any “SONET/SDH” Mode – RxOH:** This output pin, along with the RxOHClk, RxOHFrame and RxPOHInd will function as the “Receive STS-1/STM-1TOH/POH Data Output Port. The Receive STS-1/STM-1 TOH/POH Data Output Port will output the contents of all TOH and POH bytes (within the incoming STS-1/STM-1 data-stream) via this output pin. The Receive STS-1/STM-1 TOH/POH Data Output Port will update the contents of this output pin, upon the rising edge of RxOHClk. **All other modes – NO FUNCTION:** This output pin can be left floating

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AA1	RxDS1FRAME_18	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 18/Egress Direction - T1/E1 Data - Output - pin 1:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_18:** See Pin **C29 on page # 45** for pin description. **All other modes – NO FUNCTION:** This output pin can be left floating
W2	RxDS1FRAME_19	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 19/Egress Direction - T1/E1 Data - Output - pin 1:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_19:** See Pin **C29 on page # 45** for pin description. **All other modes – NO FUNCTION:** This output pin can be left floating
V1	RxDS1FRAME_20	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 20/Egress Direction - T1/E1 Data - Output - pin 1:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_20:** See Pin **C29 on page # 45** for pin description. **All other modes – NO FUNCTION:** This output pin can be left floating

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
V26	RxDS1FRAME_21/ TxDS3NEG	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 21/Transmit DS3 LIU Interface – Negative Polarity Data Output pin:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **A. If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_21:** See Pin **C29 on page # 45** for pin description. **B. If the XRT86SH328 has been configured to output DS3 data via the High-Speed side of the chip:** The function of this output pin depends upon whether the Transmit DS3 LIU Interface block has been configured to operate in the Single-Rail or Dual-Rail Mode. **B.1 If the Transmit DS3 LIU Interface Block has been configured to operate in the Single-Rail Mode - NO FUNCTION:** Leave this output pin floating. **B.2 If the Transmit DS3 LIU Interface block has been configured to operate in the Dual-Rail Mode - TxDS3NEG:** The Transmit DS3 Framer block will output the negative-polarity portion of the outbound DS3 data (towards the off-chip DS3/E3 LIU IC) via this output pin. The XRT86SH328 will update this output DS3 data upon the user-selected edge of the TXDS3CLK output signal (Ball AB30). The Positive-Polarity Portion of the outbound DS3 data (towards the off-chip DS3/E3 LIU IC) will be output via the TxDS3POS output pin (Ball Y28). *Note: Only use this particular output pin (for DS3 applications) if the STS-1 and the DS3 Ports are configured to be separate. If the STS-1 and DS3 Ports are configured to be separate, then use the TxDS3NEG signal at Ball P2.*
Y27	RxDS1FRAME_22/ TxDS3OHFrame	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 22/Transmit DS3 Overhead Data Input Port – Frame Boundary Output:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_22:** See Pin **C29 on page # 45** for pin description. **If the XRT86SH328 has been configured to operate in any of the M13 MUX Modes – TxDS3OHFrame:** This output pin pulses “High” for one TxDS3OHClk period coincident with the instant the Transmit DS3 Overhead Data Input Interface would be accepting the first overhead bit within an outbound DS3 frame. **If the XRT86SH328 device has been configured to operate in the VT-Mapper Mode – NO FUNCTION:** Leave this output pin floating.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AE30	RxDS1FRAME_23/ IG_TE1RxDATA_2	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 23/Egress Direction - T1/E1 Data - Output - pin 1:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_23:** See Pin **C29 on page # 45** for pin description. **If the XRT86SH328 device has been configured to operate in the various Aggregation Modes - IG_TE1RxDATA_2:** See Pin **AD29 on page # 31** for pin description.
AE29	RxDS1FRAME_24/ IG_TE1RxDATA_5	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 24/Ingress Direction T1/E1 Data Drop Port - Data Bus Output pin # 5:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_24:** See Pin **C29 on page # 45** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1RxDATA_5:** See Pin **AD29 on page # 31** for pin description.
AB26	RxDS1FRAME_25/ TxDS3OHInd	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 25//Transmit DS3 Overhead Data Input Interface – Overhead Indicator Output:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_25:** See Pin **C29 on page # 45** for pin description. ----------
AC26	RxDS1FRAME_26/ IG_TE1RxOHInd_0	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 26/Ingress Direction T1/E1 Data Drop Port - Data Type Indicator output pin # 0:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_26** See Pin **C29 on page # 45** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1RxOHInd_0:** See Pin **AJ30 on page # 33** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AG28	RxDS1FRAME_27/ IG_TE1RXOHInd_3	O	**Receive DS1/E1 Serial Data Output Interface - Frame Boundary Output Indicator - Channel 27/Ingress Direction T1/E1 Data Drop Port - Data Type Indicator output pin # 3:** The function of this output pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - RxDS1FRAME_27:** See Pin **C29 on page # 45** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1RxOHInd_3:** See Pin **AJ30 on page # 33** for pin description.
E28	TxDS1CLK_0/ EG_TE1TxDATA_1	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 0/ Egress Direction T1/E1 Data Add Port - Data Bus Input # 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_0:** This input pin, along with TxDS1DATA_n and TxDS1Frame_n will function as the Transmit Serial Data Input port for Channel_n. n = [27:0] If the XRT86SH328 is configured to operate in the 28-Channel DS1/E1 Clear-Channel Framer mode, then this input pin functions as the Transmit Payload Data Serial Input pin. In this case, the System-Side terminal equipment is expected to apply all outbound data (which is intended to be carried via the DS1 or E1 payload bits) to this input pin. The Transmit Payload Data Input Interface will sample the data, residing at the TxDS1DATA_n input pin, upon either the rising or falling edge of TxDS1CLK_n (depending upon user configuration). **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - EG_TE1TxDATA_1:** This input pin, along with EG_TE1TxDATA[7:0], EG_TE1TxValid, EG_TE1TxOHInd[4:0], EG_TE1TxSLOT0 and EG_TE1TxCLK function as the byte-wide Egress Direction - Add Port. This Add Port can be used for cross-connecting of T1/E1 Time-slots with other XRT86SH328 devices. The Egress Direction - Add Port can be configured to accept T1 and E1 data and to insert this data into the Egress Direction T1 or E1 traffic, within the XRT86SH328. The Egress Direction - Add Port will accept all of this data via the EG_TE1TxDATA[7:0] input pins. This particular pin will function as bit 1 within this byte wide input port. The Egress Direction Add Port will sample the data on the EG_TE1TxDATA[7:0] input data bus, upon the rising edge of EG_TE1TxCLK. *Notes:* *1. The Egress Direction – Add Port will only accept data via the EG_TE1TxDATA[7:0] input pins, if "EG_TE1TxValid" is at a logic "High".* *2. The above Aggregation Modes include all of the following.* • *The VT-Mapper Mode (w/ T1/E1 Framing)* • *The M13 MUX Mode (w/ T1/E1 Framing)* • *The M13 MUX to STS-1 Mode* • *The Transmux Mode*

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
E29	TxDS1CLK_1/ EG_TE1TxDATA_4	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 1/ Egress Direction T1/E1 Data Add Port - Data Bus Input pin # 4:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_1:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - EG_TE1TxDATA_4:** See Pin **E28 on page # 56**
F29	TxDS1CLK_2/ EG_TE1TxDATA_7	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 2/ Egress Direction T1/E1 Data Add Port - Data Bus Input # 7:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_2:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - EG_TE1TxDATA_7:** See Pin **E28 on page # 56**

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
F30	TxDS1CLK_3/ EG_TE1TxOHInd_0	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 3/ Egress Direction T1/E1 Data Add Port - Data Type Indicator Input - pin 0:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_3:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - EG_TE1TxOHInd_0:** This input pin, along with EG_TE1TxDATA[7:0], EG_TE1TxValid, EG_TE1TxSLOT0 and EG_TE1TxCLK function as the byte-wide Egress Direction – Add Port. This Add Port can be used for cross-connecting T1/E1 Time-slots with other XRT86SH328 devices. This particular pin will function as the Overhead Indicator – Bit 0 input within this byte wide input port. As the Egress Direction Add Port accepts its incoming data, this input pin (along with EG_TE1TxOHInd[4:1]) will indicate (1) whether the data, residing on EG_TE1TxDATA[7:0] is an overhead bit. The relationship between the states of the EG_TE1TxOHInd[4:0] input pins, and how the Add Port will interpret this is tabulated below.

EG_TE1TxOHInd[4:0]	What the Add Port will inerpret is on EG_TE1TxDATA[7:0] Bus
00 xxx	All bits on bus are T1/E1 payload bits
01 000	EG_TE1TxDATA_0 contains an overhead bit
01 001	EG_TE1TxDATA_1 contains an overhead bit
01 010	EG_TE1TxDATA_2 contains an overhead bit
01 011	EG_TE1TxDATA_3 contains an overhead bit
01 100	EG_TE1TxDATA_4 contains an overhead bit
01 101	EG_TE1TxDATA_5 contains an overhead bit
01 110	EG_TE1RxDATA_6 contains an overhead bit
01 111	EG_TE1TxDATA_7 contains an overhead bit
11 000	EG_TE1TxDATA_0 contains a multi-frame alignment bit
11 001	EG_TE1TxDATA_1 contains a multi-frame alignment bit
11 010	EG_TE1TxDATA_2 contains a multi-frame alignment bit
11 011	EG_TE1TxDATA_3 contains a multi-frame alignment bit
11 100	EG_TE1TxDATA_4 contains a multi-frame alignment bit
11 101	EG_TE1TxDATA_5 contains a multi-frame alignment bit
11 110	EG_TE1TxDATA_6 contains a multi-frame alignment bi
11 111	EG_TE1TxDATA_7 contains a multi-frame alignment bit

This signal will be sampled upon the rising edge of EG_TE1TxCLK.

Note: The "above-mentioned" Aggregation Modes include all of the following

- *The VT-Mapper Mode (w/ T1/E1 Framing)*
- *The M13 MUX Mode (w/ T1/E1 Framing)*
- *The M13 MUX to STS-1 Mode*
- *The Transmux Mode*

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
H30	TxDS1CLK_4/ EG_TE1TxCLK	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 4/ Egress Direction T1/E1 Data Add Port - Byte Wide Clock Input pin:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_4:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes – EG_TE1TxCLK:** This input pin, along with EG_TE1TxDATA[7:0], EG_TE1TxValid, EG_TE1TxOHInd[4:0] and EG_TE1TxSLOT0 function as the byte-wide Egress Direction – Add Port. This Add Port can be used to permit cross-connecting of T1/E1 Time-slots with other XRT86SH328 devices. The Egress Direction – Add Port can be configured to accept T1 and E1 data and to insert this data into the Egress Direction T1 or E1 traffic, within the XRT86SH328. The Egress Direction Add Port will sample the data on the EG_TE1TxDATA[7:0] and EG_TE1TxValid inputs upon the rising edge of this input clock signal.
K29	TxDS1CLK_5/ RxDS3LOS	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 5/ Receive DS3 LIU Interface - LOS Input pin:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_5:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to operate in the DS3 M13 MUX Mode -RxDS3LOS Input Pin (Dedicated DS3 Port):** The user is expected to connect this input pin to the RLOS output from the DS3/ E3/STS-1 LIU IC. Anytime the LIU IC declares the LOS defect condition (within the incoming DS3 data-stream) and asserts its RLOS output pin, then it will assert this input pin. The Receive DS3 Framer block will automatically declare the LOS defect condition for the duration that this input pin is pulled to a logic “High”. **If the XRT86SH328 device has been configured to operate in one of the VT-Mapper Modes – NO FUNCTION:** Tie this pin to GND.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
N26	TxDS1CLK_6/ RxDS3CLK	I/O	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 6/ Receive DS3 LIU Interface – Clock Input (Dedicated DS3 Port:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_6:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to operate in the DS3 M13 MUX Mode - RxDS3CLK:** The Receive DS3 Framer block uses this input pin to sample and latch the data that is present on the RxDS3POS and RxDS3NEG (for Dual-Rail Operation only) inputs. This input clock signal also functions as the timing source for the Receive Direction signal and circuitry within the Receive DS3 Framer block. Connect this input to the Recovered Clock Output of an off-chip DS3/E3/STS-1 LIU IC. *Note: Only use this particular input pin (for DS3 applications) if the STS-1 and the DS3 Ports are configured to be separated. If the STS-1 and DS3 Ports are configured to be shared, then use the RxDS3CLK signal at Ball T1.* **If the XRT86SH328 device has been configured to operate in one of the VT-Mapper Modes – NO FUNCTION:** Tie this pin to GND.
P4	TxDS1CLK_7	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 7/ Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_7:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to operate in any other mode – NO FUNCTION:** Tie this input pin to GND.
M3	TxDS1CLK_8	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 8/ Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_8:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to operate in any other mode – NO FUNCTION:** Tie this input pin to GND.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
L3	TxDS1CLK_9	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 9/ Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_9:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to operate in any other mode – NO FUNCTION:** Tie this input pin to GND.
M5	TxDS1CLK_10	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 10/ Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_10:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to operate in any other mode – NO FUNCTION:** Tie this input pin to GND.
L5	TxDS1CLK_11	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 11/ Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_11:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to operate in any other mode – NO FUNCTION:** Tie this input pin to GND.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
K5	TxDS1CLK_12/ TxPOH_Ind	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 12/ Transmit STS-1/STM-1 TOH/POH Data Input Interface – POH Indicator Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_12:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to operate in any SONET/SDH Mode – TxPOHInd:** This output pin, along with the TxOH, TxOHClk, TxOHFrame and TxOHIns pins will function as the Transmit STS-1/STM-1 TOH/POH Data Input Port. The Transmit STS-1/STM-1 TOH/POH Data Input Port will toggle and hold this output pin “high”, coincident to whenever it is ready to accept POH data via the TxOH input pin. The Transmit STS-1/STM-1 TOH/POH Data Input Port will update this output pin upon the rising edge of TxOHClk. *Note: This output pin will function in this role if the XRT86SH328 has been configured to operate in either of the following modes.* • *VT-Mapper to STS-1 Mode* • *M13 MUX which is Asynchronously Mapped to STS-1 Mode*
F3	TxDS1CLK_13/ TxTUPOH	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 13/ Transmit VC-4 POH Data Input Port – Data Input** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_13:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 device (along with two other devices) has been configured to operate in the STM-1/TUG-3 Mode – TxTUPOH:** This output pin, along with the TxTUPOHEnable, TxTUPOHClk, TxTUPOHFrame and TxTUPOHIns function as the Transmit VC-4 POH Data Input Port. The Transmit VC-4 POH Data Input Port will latch the data, residing on this and the TxTUPOHIns input pins upon the rising edge of the TxTUPOHClk output signal. *Note: This output pin will function as the TxTUPOH output pin, whenever the XRT86SH328 has been configured to operate in any of the following modes* • *VT-Mapper to STS-1 Mode* • *Transmux Mode* **If the XRT86SH328 has been configured to operate in the M13 MUX Mode – NO FUNCTION:** Leave this output pin “floating”.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AF1	TxDS1CLK_14	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 14/ Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_14:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to operate in any other mode – NO FUNCTION:** Tie this input pin to GND.
AD1	TxDS1CLK_15/ RxD_D_6	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 15// Receive STS-1/STM-1 Telecom Bus Interface – Data Bus Input pin # 6:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_15:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to accept STS-1/STM-1 data via the Receive STS-1/STM-1 Telecom Bus Interface - RxD_D_6:** This input pin, along with RxD_D[7:0] function as the Receive STS-1/STM-1 Telecom Bus Interface Receive Input data bus. All incoming STS-1/STM-1 data is sampled and latched into the XRT86SH328, via these input pins upon the rising edge of the RXD_CLK input pin. *Notes:* 1. *Insure that the MSB (Most Significant bit) of each incoming byte is input to the RXD_D7 input pin.* 2. *Also insure that the LSB (Least Significant bit) of each incoming byte is input to the RXD_D0 input pin.*
AB2	TxDS1CLK_16/ RxD_D_3	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 16/ Receive STS-1/STM-1 Telecom Bus Interface - Data Bus Input pin # 3:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_16:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to accept STS-1/STM-1 data via the Receive STS-1/STM-1 Telecom Bus Interface - RxD_D_3:** See Pin **AD1 on page # 63** for pin description.
Y3	TxDS1CLK_17/ RxD_D_0	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 17// Receive STS-1/STM-1 Telecom Bus Interface – Data Bus Input pin # 0:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_17:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to accept STS-1/STM-1 data via the Receive STS-1/STM-1 Telecom Bus Interface - RxD_D_0:** See Pin **AD1 on page # 63** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
Y1	TxDS1CLK_18/ RxD_C1J1V1_FP	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 18/ Receive STS-1/STM-1 Telecom Bus Interface – C1J1V1 Indicator Input pin:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_18:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to accept STS-1/STM-1 data via the Receive STS-1/STM-1 Telecom Bus Interface – RxD_C1J1V1_FP:** Composite Timing - This signal contains two pieces of timing information, SONET/SDH frame phase and payload frame phase. One pulse will occur on RxD_C1J1 when RxD_PL is inactive to indicate a SONET/SDH frame pulse. In STS-3c/STM-1, one pulse will occur with RxD_PL active to indicate the J1 byte poaition. In STS-3, three pulses will occur When RxD_PL is active.
U5	TxDS1CLK_19/ RxSTS-1LOS/ RxDS3LOS	I/O	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 19/ Receive DS3/STS-1 LIU Interface – LOS Input Pin:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_19:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 device has been configured to operate in the DS3 M13 MUX Mode – RxDS3LOS Input Pin (Shared Port):** If the XRT86SH328 is configured to operate in the Shared-LIU Interface Mode, then connect this input pin to the RLOS output from the DS3/E3/STS-1 LIU IC. Anytime the LIU IC declares the LOS defect condition (within the incoming DS3 data-stream) and asserts its RLOS output pin, then it will assert this input pin. The Receive DS3 Framer block will automatically declare the LOS defect condition for the duration that this input pin is pulled to a logic “High”. **If the XRT86SH328 has been configured to operate in the VT-Mapper to STS-1 Mode – NO FUNCTION:** Tie this pin to GND.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
T1	TxDS1CLK_20/ RxSTS-1CLK/ RxDS3CLK	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 20// Receive DS3/STS-1 LIU Interface – Clock Input (Shared Port):** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **A. If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_20:** See Pin **E28 on page # 56** for pin description. **B. If the XRT86SH328 has been configured to transmit/receive data (on the high-speed side of the chip) on the STS-1 (e.g., EC-1) Mode - RxSTS-1CLK:** The Receive STS-1 TOH Processor block uses this input pin to sample and latch the data that is present on the RxSTS-1DATA input pin. This input clock signal also functions as the timing source for the Receive Direction signal and circuitry within the Receive STS-1 TOH and POH Processor blocks. **C. If the XRT86SH328 has been configured to operate in the DS3 M13 MUX Mode - RxDS3CLK:** The Receive DS3 Framer block uses this input pin to sample and latch the data that is present on the RxDS3POS and RxDS3NEG (for Dual-Rail Operation only) inputs. This input clock signal also functions as the timing source for the Receive Direction signal and circuitry within the Receive DS3 Framer block. Connect this input to the Recovered Clock Output of an off-chip DS3/E3/STS-1 LIU IC. *Note: Only use this particular input pin (for DS3 applications) if the STS-1 and the DS3 Ports are configured to be separated. If the STS-1 and DS3 Ports are configured to be shared, then use the RxDS3CLK signal at Ball T1.*
AA28	TxDS1CLK_21/ IG_TE1RxDATA_1(0)	I/O	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 21/ Ingress Direction - T1/E1 Data Drop Port - Data Bus Output - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_21:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1RxDATA_1:** See Pin **AD29 on page # 31** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AA27	TxDS1CLK_22/ IG_TE1TxDATA_1	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 0/ Ingress Direction T1/E1 Data Add Port - Data Bus Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_22:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1TxDATA_1:** This input pin, along with the other IG_TE1TxDATA[7:0], EG_TE1TxValid, EG_TE1TxOHInd[4:0], EG_TE1TxSLOT0 and EG_TE1TxCLK function as the byte-wide Ingress Direction - Add Port. This Add Port can be used for cross-connecting of T1/E1 Time-slots with other XRT86SH328 devices. The Ingress Direction – Add Port accepts the contents of user-selected T1/E1 data (via this port) and inserts this data into the Ingress Direction T1 or E1 data that is being handled by the XRT86SH328. This particular pin will function as bit 1 within this byte wide input port. The Ingress Direction Add port will sample all incoming data (via this port) and all input signals upon the rising edge of IG_TE1TxCLK. *Notes:* *1. The IG_TE1TxDATA[7:0] data bus is only active if IG_TE1TxValid is sampled at the logic "High" level.* *2. The above Aggregation Modes include all of the following.* • *The VT-Mapper Mode (w/ T1/E1 Framing)* • *The M13 MUX Mode (w/ T1/E1 Framing)* • *The M13 MUX to STS-1 Mode* • *The Transmux Mode*
AB27	TxDS1CLK_23/ IG_TE1TxDATA_3	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 23/ Ingress Direction T1/E1 Data Add Port - Data Bus Input - pin 3:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_23:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1TxDATA_3:** See Pin **AA27 on page # 66** for pin description.
AF29	TxDS1CLK_24/ IG_TE1TxDATA_6	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 24/ Ingress Direction T1/E1 Data Add Port - Data Bus Input - pin 6:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_24:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1TxDATA_6:** See Pin **AA27 on page # 66** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AG29	TxDS1CLK_25/ IG_TE1TxSLOT0	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 25/ Ingress Direction T1/E1 Data Add Port - Channel # 0 Indicator Input:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_25:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 device has been configured to operate in the various Aggregation Modes – IG_TE1TxSLOT0:** This input pin, along with IG_TE1TxDATA[7:0], IG_TE1TxOHInd[4:0], IG_TE1TxValid and IG_TE1TxCLK function as the byte-wide Ingress Direction – Add Port. This Add Port can be used for cross-connecting of T1/E1 Time-slots with other XRT86SH328 devices. The Ingress Direction – Add Port can accept a user-selected set of T1/E1 data, and insert this data into the Ingress Direction T1 or E1 traffic. The user is expected to assert this input pin coincident to whenever T1/E1 data (associated with Ingress Direction T1/E1 Channel 0) is being applied to the IG_TE1TxDATA[7:0] input data bus. The user should pulse this input pin “High” for one IG_TE1TxCLK clock period. This input signal will be sampled upon the rising edge of IG_TE1TxCLK.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AD26	TxDS1CLK_26/ IG_TE1TxOHInd_2	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 26/ Ingress Direction T1/E1 Data Add Port - Data Type Indicator Input pin # 2:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_26:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 device has been configured to operate in the various Aggregation Modes – IG_TE1TxOHInd_2:** This input pin, along with IG_TE1TxDATA[7:0], IG_TE1TxValid, IG_TE1TxSLOT0 and IG_TE1TxCLK function as the byte-wide Ingress Direction – Add Port. This Add Port can be used for cross-connecting T1/E1 Time-slots with other XRT86SH328 devices. This particular pin will function as the Overhead Indicator – Bit 2 input within this byte wide input port. As the Ingress Direction Add Port accepts its incoming data, this input pin (along with IG_TE1TxOHInd[4:2] and IG_TE1TxOHInd[1:0]) will indicate (1) whether the data, residing on IG_TE1TxDATA[7:0] is an overhead bit. The relationship between the states of the "IG_TE1TxOHInd[4:0] input pins, and how the Add Port will interpret this is tabulated below.

IG_TE1TxOHInd[4:0]	What the ADD Port will Interpret is on IG_TE1TxDATA[7:0] Bus?
00 xxx	All bits on bus are T1/E1 payload bits
01 000	IG_TE1TxDATA_0 contains an overhead bit
01 001	IG_TE1TxDATA_1 contains an overhead bit
01 010	IG_TE1TxDATA_2 contains an overhead bit
01 011	IG_TE1TxDATA_3 contains an overhead bit
01 100	IG_TE1TxDATA_4 contains an overhead bit
01 101	IG_TE1TxDATA_5 contains an overhead bit
01 110	IG_TE1TxDATA_6 contains an overhead bit
01 111	IG_TE1TxDATA_7 contains an overhead bit
11 000	IG_TE1TxDATA_0 contains a multi-frame alignment bit
11 001	IG_TE1TxDATA_1 contains a multi-frame alignment bit
11 010	IG_TE1TxDATA_2 contains a multi-frame alignment bit
11 011	IG_TE1TxDATA_3 contains a multi-frame alignment bit
11 100	IG_TE1TxDATA_4 contains a multi-frame alignment bit
11 101	IG_TE1TxDATA_5 contains a multi-frame alignment bit
11 110	IG_TE1TxDATA_6 contains a multi-frame alignment bi
11 111	IG_TE1TxDATA_7 contains a multi-frame alignment bit

Note: This signal will be sampled upon the rising edge of IG_TE1TxCLK.

- *The above-mentioned Aggregation Modes include all of the following.*
- *The VT-Mapper Mode (w/ T1/E1 Framing)*
- *The M13 MUX Mode (w/ T1/E1 Framing)*
- *The M13 MUX to STS-1 Mode*
- *The Transmux Mode*

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AJ29	TxDS1CLK_27/ IG_TE1TxCLK	I	**Transmit DS1/E1 Serial Data Input Interface - Clock Input - Channel 27/ Ingress Direction T1/E1 Data Add Port - Byte Wide Clock Input pin:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1CLK_27:** See Pin **E28 on page # 56** for pin description. **If the XRT86SH328 device has been configured to operate in the various Aggregation Modes – IG_TE1TxCLK:** This input pin, along with IG_TE1TxDATA[7:0], IG_TE1TxValid, IG_TE1TxOHInd[4:0] and IG_TE1TxSLOT0 function as the byte-wide Ingress Direction – Add Port. This Add Port can be used to permit cross-connecting of T1/E1 Time-slots with other XRT86SH328 devices. The Ingress Direction – Add Port can be configured to accept T1 and E1 data and to insert this data into the Ingress Direction T1 or E1 traffic, within the XRT86SH328. The Ingress Direction Add Port will sample the data on the IG_TE1TxDATA[7:0] and IG_TE1TxValid inputs upon the rising edge of this input clock signal.
F27	TxDS1DATA_0/ EG_TE1TxDATA_0	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 0/ Egress Direction T1/E1 Data Add Port - Data Bus Input pin # 0:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_0:** This input pin, along with TxDS1CLK_n and TxDS1Frame_n will function as the Transmit Serial Data Input port for Channel_n. *Note: n = [27:0]* If the XRT86SH328 is configured to operate in the 28-Channel DS1/E1 Clear-Channel Framer mode, then this input pin functions as the Transmit Payload Data Serial Input pin. In this case, the System-Side terminal equipment is expected to apply all outbound data (which is intended to be carried via the DS1 or E1 payload bits, within Channel 0) to this input pin. The Transmit Payload Data Input Interface will sample the data, residing at the TxDS1DATA_n input pin, upon either the rising or falling edge of TxDS1CLK_n (depending upon user configuration). **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - EG_TE1TxDATA_0:** See Pin **E28 on page # 56**
F28	TxDS1DATA_1/ EG_TE1TxDATA_3	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 1/ Egress Direction T1/E1 Data Add Port - Data Bus Input pin 3:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_1:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - EG_TE1TxDATA_3:** See Pin **E28 on page # 56** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
G28	TxDS1DATA_2/ EG_TE1TxDATA_6	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 2/ Egress Direction T1/E1 Data Add Port - Data Bus Input pin # 6:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_2:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - EG_TE1TxDATA_6:** See Pin **E28 on page # 56** for pin description.
H28	TxDS1DATA_3/ EG_TE1TxSLOT0	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 3/ Egress Direction T1/E1 Data Add Port - Channel # 0 Indicator Input:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_3:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes – EG_TE1TxSLOT0:** This input pin, along with EG_TE1TxDATA[7:0], EG_TE1TxOHInd[4:0], EG_TE1TxValid and EG_TE1TxCLK function as the byte-wide Ingress Direction – Add Port. This Add Port can be used to permit cross-connecting of T1/E1 Time-slots with other XRT86SH328 devices. The Egress Direction – Add Port can accept a user-selected set of T1/E1 data, and insert this data into the Ingress Direction T1 or E1 traffic. The user is expected to assert this input pin coincident to whenever T1/E1 data (associated with Ingress Direction T1/E1 Channel 0) is being applied to the EG_TE1TxDATA[7:0] input data bus. The user should pulse this input pin “High” for one EG_TE1TxCLK clock period. This input signal will be sampled upon the rising edge of EG_TE1TxCLK.
K27	TxDS1DATA_4/ EG_TE1TxOHInd_2	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 4/ Egress Direction T1/E1 Data Add Port - Data Type Indicator Input pin # 2:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_4:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes – EG_TE1TxOHInd_2** See Pin **F30 on page # 58** for pin description.
J30	TxDS1DATA_5/ EG_TE1TxOHInd_4	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 5/ Egress Direction T1/E1 Data Add Port - Data Type Indicator Input pin 4:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_5:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes – EG_ EG_TE1TxOHInd_4** See Pin **F30 on page # 58** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
M28	TxDS1DATA_6/ RxDS3POS	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 6/ Receive DS3 LIU Interface - Positive Polarity Input:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **A. If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_6:** See Pin **F27 on page # 69** for pin description. **B. If the XRT86SH328 has been configured to transmit/receive data (on the high-speed side of the chip) in the DS3 Mode - RxDS3POS:** If the XRT86SH328 has been configured to operate in the M13 MUX Mode, then the function of this input pin depends upon whether the Receive DS3 LIU Interface block has been configured to operate in the Single-Rail or Dual-Rail Mode. **B.1 If the Receive DS3 LIU Interface Block has been configured to operate in the Single-Rail Mode.** If the Receive DS3 LIU Interface block (within the XRT86SH328) has been configured to operate in the Single-Rail Mode, then the XRT86SH328 will receive the incoming DS3 data-stream via this input pin. The XRT86SH328 will sample this incoming DS3 data upon the user-selected edge of the RxDS3CLK input signal (Ball N26). **B.2 If the Receive DS3 LIU Interface Block has been configured to operate in the Dual-Rail Mode:** If the Receive DS3 LIU Interface block (within the XRT86SH328) has been configured to operate in the Dual-Rail Mode, then the XRT86SH328 will accept the positive-polarity portion of the incoming DS3 data-stream via this input pin. The Receive DS3 LIU Interface block will sample this incoming data upon the user-selected edge of the RxDS3CLK input clock signal (Ball N26). In this configuration setting, the XRT86SH328 will accept the negative-polarity portion of the incoming DS3 data-stream via the RxDS3NEG input pin (Ball L29). *Note: Only use this particular input pin (for DS3 applications). If the STS-1 and the DS3 Ports are configured to be separated. If the STS-1 and DS3 Ports are configured to be shared, then use the RxDS3POS signal at Ball U1.*
N2	TxDS1DATA_7	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 7/ Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_7:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to operate in any other mode – NO FUNCTION:** Tie this input pin to GND.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
N4	TxDS1DATA_8/ TxCLK/TxSBCLK	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 8/ Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_8:** See Pin **F27 on page # 69** for pin description. TxCLK - Input transmit OC-3 clock (77MHz) TxSBCLKClock signal for high-rate transmit device.
N5	TxDS1DATA_9	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 9/ Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_9:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to operate in any other mode – NO FUNCTION:** Tie this input pin to GND.
L4	TxDS1DATA_10	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 10/ Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_10:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to operate in any other mode – NO FUNCTION:** Tie this input pin to GND.
F1	TxDS1DATA_11/ TxOHIns	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 11/ Transmit STS-1/STM-1 TOH/POH Data Input Port - Insert Data Command Input:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_11:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 device has been configured to operate in one of the SONET/SDH Mode - TxOHIns:** If the System-Side Terminal Equipment intends to insert it own value for a given overhead TOH or POH byte, into the outbound STS-1 or STS-3/STM-1 data-stream, then the System-Side Terminal Equipment is expected to assert this input pin (by pulling it "High") coincident to whenever the Transmit STS-1/STM-1 TOH/POH Overhead Data Input Port is processing that (or those) particular TOH or POH bytes. This input pin is sampled upon the rising edge of TxOHClk.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
F2	TxDS1DATA_12/ TxOH	I/O	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 12/ Transmit STS-1/STM-1 TOH/POH Data Input Port - Data Input:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_12:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 device has been configured to operate in one of the SONET/SDH Modes - TxOH:** If the System-Side Terminal Equipment intends to insert it own value for a given overhead TOH or POH byte, into the outbound STS-1 or STS-3/STM-1 data-stream, then the System-Side Terminal Equipment is expected to (1) apply the "desired" value of this particular TOH or POH byte to this input pin (in a serial manner) while (2) asserting the TxOHIns input pin (by pulling it "High") coincident to whenever the Transmit STS-1/STM-1 TOH/POH Overhead Data Input Port is processing that (or those) particular TOH or POH bytes. This input pin is sampled upon the rising edge of TxOHClk.
J5	TxDS1DATA_13/ TxTUPOHIns	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 13/ Transmit VC-4 POH Dat Input Port - Insert Data Command Input:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_13:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 device (along with two other devices) has been configured to operate in the STM-1/TUG-3 Mode - TxTUPOHIns:** This input pin, along with the TxTUPOH, TxPOHEnable, TxTUPOHFrame and TxTUPOHClk pins function as the "Transmit VC-4 POH Data Input"port. The user is expected to pull this input pin "High" anytime the user wishes to externally insert their VC-4 POH data into the outbound VC-4 data-stream. The Transmit VC-4 POH Data Input Port will sample the state of this input pin upon the rising edge of TxTUPOHClk. Anytime the Transmit VC-4 POH Data Input Port samples this input pin "High" then it will externally insert the VC-4 POH data (within the outbound VC-4 data-stream) with the data that it also samples via the TxTUPOH input pin. If the user does not wish to externally insert their own VC-4 POH data into the outbound VC-4 data-stream, this input pin should be tied to GND.
AE2	TxDS1DATA_14	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 14/ Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_14:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to operate in any other mode - NO FUNCTION:** Tie this input pin to GND.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AE1	TxDS1DATA_15/ RxD_D_7	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 15/ Receive STS-1/STM-1 Telecom Bus Interface - Data Bus Input pin # 7:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_15:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to accept STS-1/STM-1 data via the Receive STS-1/STM-1 Telecom Bus Interface - RxD_D_7:** See Pin **AD1 on page # 63** for pin description.
AC1	TxDS1DATA_16/ RxD_D_4	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 16/ Receive STS-1/STM-1 Telecom Bus Interface - Data Bus Input pin # 4:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_16:T** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to accept STS-1/STM-1 data via the Receive STS-1/STM-1 Telecom Bus Interface - RxD_D_4:** See Pin **AD1 on page # 63** for pin description.
AA2	TxDS1DATA_17/ RxD_D_1	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 17/ Receive STS-1/STM-1 Telecom Bus Interface - Data Bus Input pin # 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_17:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to accept STS-1/STM-1 data via the Receive STS-1/STM-1 Telecom Bus Interface - RxD_D_1:** See Pin **AD1 on page # 63** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
V5	TxDS1DATA_18/ RxD_DP	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 18/ Receive STS-1/STS-3/STM-1 Telecom Bus Interface - Data Parity Input Pin:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_18:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to accept STS-1/STM-1 data via the Receive STS-1/STM-1 Telecom Bus Interface - RxD_DP:** This input pin can be configured to function as one of the following. 1.The EVEN or ODD parity value of the bits which are input via the RXD_D[7:0] input pins. 2.The EVEN or ODD parity value of the bits which are being input via the RXD_D[7:0] input and the states of the RXD_PL and RXD_C1J1V1 input pins. The Receive STS-1/STS-3/STM-1 Telecom Bus Interface will use this pin to compute and verify the parity within the incoming STS-1/STS-3/STM-1 data-stream. *Note: The user should tie this pin to GND if the STS-1/STS-3/STM-1 Telecom Bus Interface is configured to operate in the "e-Phase ON Mode.*
V2	TxDS1DATA_19/ RxD_CLK	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 19/ Receive STS-1/STS-3/STM-1 Telecom Bus Interface - Clock Input Pin:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_19:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to accept STS-1/STS-3/STM-1 data via the Receive STS-1/STM-1 Telecom Bus Interface - RxD_CLK:** This input clock signal functions as the clock source for the Receive STS-1/ STS-3/STM-1 Telecom Bus Interface. All Receive STS-1/STS-3/STM-1 Telecom Bus Interface input signals are sampled upon the rising edge of this input clock signal. This clock signal should operate at 6.48MHz (for STS-1 Applications) or 19.44MHz (for STS-3/STM-1 Applications).

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
U1	TxDS1DATA_20/ RxSTS-1DATA/ RxDS3POS	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 20/ Receive STS-1 LIU Interface - Receive Data Input/Receive DS3 LIU Interface - Positive Polarity Data Input:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **A. If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_20:** See Pin **F27 on page # 69** for pin description. **B. If the XRT86SH328 has been configured to transmit/receive data (on the high-speed side of the chip) in the STS-1 (e.g., EC-1) Mode - RxSTS-1DATA:** If the XRT86SH328 has been configured to transmit and receive data (on the high-speed side of the chip) via the STS-1/EC-1 format, then the XRT86SH328 will receive the incoming STS-1 data-stream via this input pin. The XRT86SH328 will sample this incoming STS-1 data upon the user selected edge of the RxSTS-1CLK input signal. **C. If the XRT86SH328 has been configured to transmit/receive data (on the high-speed side of the chip) in the DS3 Mode - RxDS3POS:** If the XRT86SH328 has been configured to operate in the M13 MUX Mode, then the function of this input pin depends upon whether the Receive DS3 LIU Interface block has been configured to operate in the Single-Rail or Dual-Rail Mode. **C.1 If the Receive DS3 LIU Interface Block has been configured to operate in the Single-Rail Mode.** If the Receive DS3 LIU Interface block (within the XRT86SH328) has been configured to operate in the Single-Rail Mode, then the XRT86SH328 will receive the incoming DS3 data-stream via this input pin.The XRT86SH328 will sample this incoming DS3 data upon the user-selected edge of the RxDS3CLK input signal (Ball T1). **C.2 If the Receive DS3 LIU Interface Block has been configured to operate in the Dual-Rail Mode:** If the Receive DS3 LIU Interface block (within the XRT86SH328) has been configured to operate in the Dual-Rail Mode, then the XRT86SH328 will accept the positive-polarity portion of the incoming DS3 data-stream via this input pin. The Receive DS3 LIU Interface block will sample this incoming data upon the user-selected edge of the RxDS3CLK input clock signal (Ball T1).In this configuration setting, the XRT86SH328 will accept the negative-polarity portion of the incoming DS3 data-stream via the RxDS3NEG input pin (Ball U2). *Note: Only use this particular input pin (for DS3 applications) if the STS-1 and the DS3 Portsare configured to be shared. If the STS-1 and DS3 Ports are configured to be separate (which would be necessary for Transmux applications), then use the RxDS3POS signal at Ball M28.*

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AB29	TxDS1DATA_21/ TxDS3OH	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 21/ Transmit DS3 Overhead Data Input Interface - Data Input pin:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_21:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to operate in the M13 MUX Modes - TxDS3OH:** The Transmit DS3 Overhead Data Input Interface block accepts overhead via this input pin, and insert this data into the appropriate overhead bit positions within the very next outbound DS3 frames. If the TxDS3OHIns input pin is pulled "High", then the Transmit DS3 Overhead Data Input Interface will sample the overhead data residing on this input pin, upon either the rising edge of Tx44MHzClk_In, or the falling edge of the TxDS3OHClk output clock signal (depending upon the Insertion Method used). Conversely, if the TxDS3OHIns input pin is NOT pulled "High", then the Transmit DS3 Overhead Data Input Interface block will be inactive and will NOT accept any overhead data via the TxDS3OH input pin.
AB28	TxDS1DATA_22/ TxDS3OHIns	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 22/ Transmit DS3 Overhead Data Input Interface - Overhead Insert Input:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_22:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to operate in one of M13 MUX Modes - TxDS3OHIns:** This input pin permits the user to either enable or disable the Transmit DS3 Overhead Data Input Interface block. If the Transmit DS3 Overhead Data Input Interface block is enabled, then it will accept overhead data (from the System-Side terminal equipment) via the TxDS3OH input pin; and insert this data into the overhead bit positions within the outbound DS3 data stream. Conversely, if the Transmit DS3 Overhead Data Input Interface block is disabled, then it will NOT accept overhead data from the System-Side terminal equipment.ulling this input pin "High" enables the Transmit DS3 Overhead Data Input Interface block. Pulling this input pin "Low" disables the Transmit DS3 Overhead Data Input Interface block.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AF30	TxDS1DATA_23/ TxDS3AISEn	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 23/ Transmit DS3 AIS Command Inpu:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_23:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to operate in one of the M13 MUX Modes - TxDS3AISEn:** This input pin permits the user to command the Transmit DS3 Framer block to transmit an AIS pattern to the remote terminal equipment. Setting this input pin "High" configures the Transmit DS3 Framer block to transmit an AIS pattern to the remote terminal equipment. Setting this input pin "Low" configures the Transmit DS3 Framer block to NOT transmit an AIS pattern to the remote terminal equipment. *Note: For normal operation, or if the user wishes to control the Transmit AIS function, via Software Control; the user should tie this input pin to GND.*
AC27	TxDS1DATA_24/ IG_TE1TxDATA_5	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 24/ Ingress Direction Add Port - Data Bus Input - Pin 5:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_24:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1TxDATA_5:** See Pin **AA27 on page # 66** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AD27	TxDS1DATA_25/ IG_TE1TxValid	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 25/ Ingress Direction - Add Port - Valid Data Input:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_25:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 device has been configured to operate in the various Aggregation Modes - IG_TE1TxValid:** This input pin, along with IG_TE1TxDATA[7:0], IG_TE1TxOHInd[4:0], IG_TE1TxSLOT0 and IG_TE1TxCLK function as the byte-wide Ingress Direction - Add Port. This Add Port can be used to permit cross-connecting of T1/E1 time-slots with other XRT86SH328 devices. The Ingress Direction - Add Port can be configured to accept T1 and E1 data and to insert this data into the "Ingress Direction" T1 or E1 traffic, within the XRT86SH328. The Ingress Direction - Add Port will accept all of this data via the IG_TE1TxDATA[7:0] input pins, provided that this particular input (IG_TE1TxValid) is sampled at the logic "High" level. The Ingress Direction Add Port will ignore all data that is sampled at the IG_TE1TxDATA[7:0] inputs, this input pin is also sampled at the logic "Low" level. The Ingress Direction Add Port will sample this input pin upon the rising edge of IG_TE1TxCLK. *Notes:The above-mentioned Aggregation Modes include all of the following.* • *The VT-Mapper Mode (w/ T1/E1 Framing)* • *The M13 MUX Mode (w/ T1/E1 Framing)* • *The M13 MUX to STS-1 Mode* • *The Transmux Mode*
AH29	TxDS1DATA_26/ IG_TE1TxOHInd_1	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 26/ Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_26:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 device has been configured to operate in the various Aggregation Modes – IG_TE1TxOHInd_1:** See Pin **AD26 on page # 68** for pin description.
AE26	TxDS1DATA_27/ IG_TE1TxOHInd_4	I	**Transmit DS1/E1 Serial Data Input Interface - Data Input - Channel 27/ Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1DATA_27:** See Pin **F27 on page # 69** for pin description. **If the XRT86SH328 device has been configured to operate in the various Aggregation Modes – IG_TE1TxOHInd_4:** See Pin**AD26 on page # 68** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
H25	TxDS1FRAME_0	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 0/Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_0:** This input pin, along with TxDS1CLK_n and TxDS1DATA_n will function as the Transmit Serial Data Input port for Channel_n. *Note: n= [27:0}* If the XRT86SH328 is configured to operate in the 28-Channel DS1/E1 Clear-Channel Framer mode, then this input pin functions as the Transmit Payload Data Serial Input Interface - Framing Alignment pin for Channel-n. In this case, any rising edge at this input pin will cause the Transmit DS1/E1 Framer block (associated with Channel-n) to begin its creation of a new DS1 or E1 frame. Consequently, the user must supply an 8kHz clock signal to this input pin. Further, it is imperative that this 8kHz clock signal be synchronized with the 1.544MHz or 2.048MHz clock signal applied to the TxDS1CLK_n input pin. *Notes:* 1. *This input pin should be tied to GND if it is not to be used as the Transmit DS1/E1 Framer block - Framing Reference input signal.* 2. *The Transmit Payload Data Input Interface will sample the data, residing at the TxDS1FRAME_n input pin, upon either the rising or falling edge of TxDS1CLK_n (depending upon user configuration).* **If the XRT86SH328 has been configured to operate in any other mode - NO FUNCTION:** Tie this input pin to GND.
G27	TxDS1FRAME_1/ EG_TE1TxDATA_2	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 1/Egress Direction - Add Port - Input Data Bus - Pin 2:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_1:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - EG_TE1TxDATA_2:** See Pin **E28 on page # 56** for pin description.
K25	TxDS1FRAME_2/ EG_TE1TxDATA_5	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 2/Egress Direction - Add Port - Input Data Bus- pin 5:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_2:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - EG_TE1TxDATA_5:** See Pin **E28 on page # 56** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
J27	TxDS1FRAME_3/ EG_TE1TxVALID	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 3/Egress Direction - Add Port - Valid Data Input:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_3:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes – EG_TE1TxValid:** This input pin, along with EG_TE1TxDATA[7:0], EG_TE1TxOHInd[4:0], EG_TE1TxSLOT0 and EG_TE1TxCLK function as the byte-wide Egress Direction – Add Port. This Add Port can be used for cross-connecting of T1/E1 time-slots with other XRT86SH328 devices. The Egress Direction – Add Port" can be configured to accept T1 and E1 data and to insert this data into the Egress Direction T1 or E1 traffic, within the XRT86SH328. The Ingress Direction – Add Port will accept all of this data via the EG_TE1TxDATA[7:0] input pins, provided that this particular input (EG_TE1TxValid) is sampled at the logic "High" level. The Egress Direction Add Port will ignore all data that is sampled at the EG_TE1TxDATA[7:0] inputs, this input pin is also sampled at the logic "Low" level. The Egress Direction Add Port will sample this input pin upon the rising edge of EG_TE1TxCLK. *Notes:The above-mentioned Aggregation Modes include all of the following.* • *The VT-Mapper Mode (w/ T1/E1 Framing)* • *The M13 MUX Mode (w/ T1/E1 Framing)* • *The M13 MUX to STS-1 Mode* • *The Transmux Mode*
L26	TxDS1FRAME_4/ EG_TE1TxOHInd_1	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 4/Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_4:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - EG_TE1TxOHInd_1:** See Pin **F30 on page # 58** for pin description.
M26	TxDS1FRAME_5/ EG_TE1TxOHInd_3	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 5/Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_5:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - EG_TE1TxOHInd_3:** See Pin **F30 on page # 58** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
L29	TxDS1FRAME_6/ RxDS3NEG	I/O	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 6/Receive DS3 LIU Interface - Negative Polarity Input pin:** The function of this input pin depends upon which mode the XRT86SH328 has been configured to operate in,. **A. If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_6:** See Pin **H25 on page # 80** for pin description. **B. If the XRT86SH328 has been configured to transmit/receive data (on the high-speed side of the chip) in the DS3 Mode - RxDS3NEG:** If the XRT86SH328 has been configured to operate in the M13 MUX Mode, then the function of this input pin depends upon whether the Receive DS3 LIU Interface block has been configured to operate in the Single-Rail or Dual-Rail Mode. **B.1: If the Receive DS3 LIU Interface block has been configured to operate in the Single-Rail Mode - NO FUNCTION:** Connect this pin to GND. **B.2 If the Receive DS3 LIU Interface block has been configured to operate in the Dual-Rail Mode - RxDS3NEG:** If the Receive DS3 LIU Interface block (within the XRT86SH328) has been configured to operate in the Dual-Rail Mode, then the XRT86SH328 will accept the negative-polarity portion of the incoming DS3 data-stream via this input pin. The Receive DS3 LIU Interface block will sample this incoming data upon the user-selected edge of the RxDS3CLK Input clock signal (Ball N26).In this configuration setting, the XRT86SH328 will accept the positive-polarity portion of the incoming DS3 data-stream via the RxDS3POS input pin (Ball M28). *Note: Only use this particular input pin (for DS3 applications) if the STS-1 and the DS3 Ports are configured to be separated. If the STS-1 and DS3 Ports are configured to be shared, then use the RxDS3NEG signal at Ball U2.*
N1	TxDS1FRAME_7	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 7/Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_7:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in any other mode - NO FUNCTION:** Tie this input pin to GND.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
P5	TxDS1FRAME_8/ TxSBFP_IN_OUT	I/O	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 8/Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_8:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in the STS-3 TB Mode: TxSBFP_IN_OUT** Use this pin as an input of a reset pulse for synchronization. The first byte of data (VC Payload) should be provided N cycles later (controlled by latency count). As an output pin , an output pulse indicates the fame boundry as slot 0.
M4	TxDS1FRAME_9	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 9/Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_9:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in any other mode - NO FUNCTION:** Tie this input pin to GND.
K3	TxDS1FRAME_10	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 10:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_10:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in any other mode - NO FUNCTION:** Tie this input pin to GND.
K4	TxDS1FRAME_11	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 11:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_11:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in any other mode - NO FUNCTION:** Tie this input pin to GND.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
J4	TxDS1FRAME_12/ TxOHFrame	I/O	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 12/Transmit STS-1/STM-1 TOH/POH Data Input Port - Frame Boundary Indicator Output:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_12:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in one of the SONET/ SDH Modes - TxOHFrame:** This output pin, along with TxOH, TxOHClk, TxOHEnable and TxOHIns function as the Transmit STS-1/STM-1 TOH/POH Data Input Port. The Transmit STS-1/STM-1 TOH/POH Data Input Port will pulse this output pin "High" for one period of TxOHClk, coincident to whenever it is processing the very first TOH byte of a given outbound STS-1/STS-3/STM-1 frame. The Transmit STS-1/STM-1 TOH/POH Data Input Port will keep this output pin at a logic "Low" at all other times.
E2	TxDS1FRAME_13	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 13:** :The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_13:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in any other mode - NO FUNCTION:** Tie this input pin to GND.
AA6	TxDS1FRAME_14	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 14/Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_14:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in any other mode - NO FUNCTION:** Tie this input pin to GND.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AC3	TxDS1FRAME_15	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 15/Egress Direction - T1/E1 Data Input - pin 1:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_15:** **This input pin, along with TxDS1CLK_15 and TxDS1DATA_15 will function as the Transmit Serial Data Input port for Channel 15.** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in any other mode - NO FUNCTION:** Tie this input pin to GND.
AA4	TxDS1FRAME_16/ RxD_D_5	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 16/Receive STS-1/STM-1 Telecom Bus Interface - Data Bus input pin # 5:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_16:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to accept STS-1/STM-1 data via the Receive STS-1/STM-1 Telecom Bus Interface - RxD_D_5:** See Pin **AD1 on page # 63** for pin description.
AB1	TxDS1FRAME_17/ RxD_D_2	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 17/Receive STS-1/STM-1 Telecom Bus Interface - Data Bus Input pin # 2:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_17:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to accept STS-1/STM-1 data via the Receive STS-1/STM-1 Telecom Bus Interface - RxD_D_2:** See Pin **AD1 on page # 63** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
W3	TxDS1FRAME_18/ RxD_ALARM	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 18/Receive STS-1/STM-1 Telecom Bus Interface - ALARM Input:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_18:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to accept STS-1/STM-1 data via the Receive STS-1/STM-1 Telecom Bus Interface - RxD_ALARM:** This input pin pulses "High" corresponding to any STS-1 signal that is carrying the AIS-P indicator. More specifically, this input pin will be pulsed "High" coincident to whenever a byte, corresponding to given STS-1 signal (that is carrying the AIS-P indicator) is being placed on the Receive STS-1/STS-3/STM-1 Telecom Bus - Data Bus Input pins (RxD_D[7:0]). This input pin should be pulled "low" at all other times. *Note: If the RxD_ALARM input signal pulses "High" for any given STS-1 signal (within the incoming STS-12), then the XRT86SH328 will automatically declare the AIS-P defect for that particular STS-1 channel.*
V3	TxDS1FRAME_19/ RxD_PL	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 19/Receive STS-3/STM-1 Telecom Bus Interface - Payload Data Indicator Output Signal:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_19:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to transmit/receive STS-1/STS-3 or STM-1 data via the Telecom Bus - RxD_PL:** This input pin indicates whether or not the Receive STS-1/STM-1 Telecom Bus Interface is currently receiving Transport Overhead bytes or non-Transport Overhead bytes (e.g., STS-1 SPE, STS-3c SPE,VC-3 or VC-4 data) via the RXD_D[7:0] input pins.This input pin should be pulled "Low" for the duration that "STS-1/STM-1 Receive STS-3/STM-1 Telecom Bus Interface is receiving a Transport Overhead byte via the "RXD_D[7:0]" input pins. Conversely, this input pin should be pulled "High" for the duration that the Receive STS-1/STM-1 Telecom Interface Bus is receiving something other than a Transport Overhead byte via the RXD_D[7:0] input pins.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
U2	TxDS1FRAME_20/ RxSTS-1FRAME/ RxDS3NEG	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 20/Receive STS-1 LIU Interface - Frame Boundary input/Receive DS3 LIU Interface - Negative Polarity Data Inpu:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **A. If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_20:** See Pin **H25 on page # 80** for pin description. **B. If the XRT86SH328 has been configured to transmit/receive data (on the high-speed side of the chip) in the STS-1 (e.g., EC-1) Mode - RxSTS-1FRAME:** ---------- **C. If the XRT86SH328 has been configured to transmit/receive data (on the high-speed side of the chip) in the DS3 Mode - RxDS3NEG:** If the XRT86SH328 has been configured to operate in the M13 MUX Mode, then the function of this input pin depends upon whether the Receive DS3 LIU Interface block has been configured to operate in the Single-Rail or Dual-Rail Mode. **C.1: If the Receive DS3 LIU Interface block has been configured to operate in the Single-Rail Mode - NO FUNCTION:** Connect this pin to GND. **C.2 If the Receive DS3 LIU Interface block has been configured to operate in the Dual-Rail Mode - RxDS3NEG:** If the Receive DS3 LIU Interface block (within the XRT86SH328) has been configured to operate in the Dual-Rail Mode, then the XRT86SH328 will accept the negative-polarity portion of the incoming DS3 data-stream via this input pin. The Receive DS3 LIU Interface block will sample this incoming data upon the user-selected edge of the RxDS3CLK Input clock signal (Ball T1). In this configuration setting, the XRT86SH328 will accept the positive-polarity portion of the incoming DS3 data-stream via the RxDS3POS input pin (Ball U1). *Note: Only use this particular input pin (for DS3 applications) if the STS-1 and the DS3 Ports are configured to be shared. If the STS-1 and DS3 Ports are configured to be separate (which would be necessary for Transmux applications), then use the RxDS3NEG signal at Ball L29.*
AC30	TxDS1FRAME_21/ IG_TE1RxDATA_0(O)	I/O	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 21/Ingress Direction - Drop Port - Data Bus Output - pin 0:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_21:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1RxDATA_0:** See Pin **AD29 on page # 31** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AC29	TxDS1FRAME_22/ IG_TE1TxDATA_0	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 22/Ingress Direction - Add Port - Data Bus Input - Pin 0:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_22:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1TxDATA_0:** See Pin **AA27 on page # 66** for pin description.
AC28	TxDS1FRAME_23/ IG_TE1TxDATA_2	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 23/Ingress Direction - Add Port - Data Bus Input - Pin 2:** The function of this input pin depends upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_23:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1TxDATA_2:** See Pin **AA27 on page # 66** for pin description.
AG30	TxDS1FRAME_24/ IG_TE1TxDATA_4	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 24/Ingress Direction - Add Port - Data Bus Input - Pin 4:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_24:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1TxDATA_4:** See Pin **AA27 on page # 66** for pin description.
AH30	TxDS1FRAME_25/ IG_TE1TxDATA_7	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 25/Ingress Direction - Add Port - Data Bus Input - Pin 7:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_25:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 has been configured to operate in the various Aggregation Modes - IG_TE1TxDATA_7:** See Pin **AA27 on page # 66** for pin description.

Table 5 Low-Speed Side Interface - System-Side Signals- Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
AE27	TxDS1FRAME_26/ IG_TE1TxOHInd_0	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 26/Ingress Direction -T1/E1 Data Add Port - Data Type Indicator - Bit 0:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_26:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 device has been configured to operate in the various Aggregation Modes – IG_TE1TxOHInd_0** See Pin**AD26 on page # 68** for pin description.
AK30	TxDS1FRAME_27/ IG_TE1TxOHInd_3	I	**Transmit DS1/E1 Serial Data Input Interface - Frame Alignment Input - Channel 27/Ingress Direction T1/E1 Data Add Port - Data Type Indicator Input Pin # 3:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel DS1/E1 Framer/LIU Mode - TxDS1FRAME_27:** See Pin **H25 on page # 80** for pin description. **If the XRT86SH328 device has been configured to operate in the various Aggregation Modes – IG_TE1TxOHInd_3:** See Pin**AD26 on page # 68** for pin description.

Table 6 Miscellaneous Timing/Clock Signals - Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
F5	EXT_OSC_ENB	I	**External Oscillator Enable:** For all applications, the user should tie this input pin to GND.

Table 6 Miscellaneous Timing/Clock Signals - Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
E3	MCLK	I	**Master Clock PLL Reference Clock Signal Input:** **This input pin functions as the reference input pin to the MCLK (or Master Clock) PLL. The MCLK PLL can accept any of the following clock frequencies via this input pin:** • 8kHz • 1.544MHz • 2.048MHz • 12.352MHz • 16.384MHz **From these input clock signals, the MCLK PLL can be configured to any of the following signals for each of the 28 DS1/E1 LIU Channels within the XRT86SH328.** • 1.544MHz and 64 x 1.544MHz • 2.048MHz and 64 x 2.048MHz Each of these clock signals will be MUX and routed to the appropriate channels (depending upon which mode the channel has been configured to operate in). Ultimately, the 1.544MHz/2.048MHz clock signals (that are synthesized by the MCLK PLL) can be configured to function as the timing source for the Transmit DS1/E1 Framer block circuitry (for 28-Channel Framer & LIU Applications. • The 64 X signals are used internally by the XRT86SH328 for the following purposes. • The Microprocessor Interface will use this signal to update the contents on all on-chip registers via this 64 X clock signal • The Transmit (or Egress Direction) DS1/E1 LIU Block circuitry will use this 64 X clock signal to oversample and process the data that it accepts from up-stream circuitry. • The CDR (Clock and Data Recovery) Block within the Receive (or Ingress Direction) DS1/E1 LIU Block circuitry will use this 64 X clock signal to oversample and process the data that it accepts from the line. • The Jitter Attenuator block (within either the Transmit or Receive DS1/E1 LIU Block circuitry) will use this 64X clock signal to oversample and process the data that it accepts from the upstream circuitry.
R3	Tx51_19MHz	I	**Transmit STS-1 Timing Reference Input - 51.84MHz or 19.44MHz Clock Input:** The function of this output pin is dependent upon which mode the XRT86SH328 has been configured to operate in. **If the XRT86SH328 has been configured to transport data over an EC-1 (Electrical STS-1 Interface)** In this case, the XRT86SH328 will be configured to transmit data (on the high-speed side of the chip) at a rate of 51.84MHz. In this case, the user should supply a 51.84MHz clock signal to this input pin. The Transmit STS-1 POH and TOH Processor blocks will use this clock signal as its timing reference. **If the XRT86SH328 has been configured to transport data over an STS-1/STM-1 Telecom Bus Interface** In this case, the XRT86SH328 will be configured to output either an STS-1 or STS-3/STM-1 signal via the Transmit STS-1/STM-1 Telecom Bus Interface. In this case, the user should supply a 19.44MHz clock signal to this input pin. The Transmit STS-1 POH and TOH Processor blocks will use this clock signal as its timing reference.I **f the XRT86SH328 has been configured to operate in the M13 MUX Mode** In the M13 MUX Mode, the XRT86SH328 will M13-MUX 28 DS1 or 21 E1 signals into a DS3 signal. In this configure tie this input pin to GND.

Table 6 Miscellaneous Timing/Clock Signals - Pin Descriptions

Pin/Ball #	Pin Name	Type	Description
R2	Tx44MHzCLK_In	I	**Transmit DS3 Timing Reference Input:** **If the user intends to operate the chip in either of the following modes** • The M13 MUX Mode • The M13 MUX to STS-1 Mode • Then the user must apply a 44.736MHz ± 20ppm clock signal to this input pin. The Transmit DS3 Framer block will use this clock signal as its timing source. If the user does not intend to operate the XRT86SH328 in either of these modes, then either tie this pin to GND or leave it floating.
R1	EXT_OSC	I	**External Oscillator Input:** For all applications, the user should tie this input pin to GND.
T4	DS2INCLK	I	**Receive DS2 Clock Input:** **The user is expected to supply a 6.312MHz clock signal to this input pin, if the XRT86SH328 has been configured to operate in either of the following modes.** • The M13 MUX Mode • The M13 MUX to STS-1 Mode The user can either supply the 6.312MHz clock signal (that is generated by the XRT86SH328, and is output via the DS2OUTCLK output pin) or the user can supply their own locally generated 6.312MHz clock signal to this input pin. *Note: If tthe XRT86SH328 is configured to operate in any of the other modes (e.g., modes other than the M13 MUX or the M13 MUX to STS-1 Modes), then this input pin must be tied to GND.*
T2	DS2OUTCLK	O	**Transmit DS2 Clock Output:** This output signal will generate a 6.312MHz clock signal (which has been synthesized by the XRT86SH328). For M13 Mode, and M13 MUX to STS-1 Mode applications, this particular output signal can be connected to the DS2INCLK input signal (Ball T4) in order permit the chip to properly support either of these modes.

Table 7 Power and Ground - Pin Descxriptions

Pin/Ball #	Pin Name	Type	Description
G6, D3, D16, C16, AC6, AD6, AJ1, AF5, AE7, AK1, AF7, AE9, AG7, AE10, AG8, AF10, AH8, AF11, AF16, AJ15, AH15, AK7, AH10, AK9, AH11, AG13, AH13, AJ13, AG16, AK16, AG17, AH18, AK20, AJ20, AH20, AG20, AK23, AG21, AJ24, AH23, AH24, AK27, AE22, AH26, AF24, AH27, AF26, AD25, G25, F26, F24, A30, C27, A29, B27, F21, D23, E21, C23, A25, B23, C21, A22, D19, C19, B19, B18, C17, E16, A15, C14, B13, B12, B11, C11, E12, A8, C9, A6, B7, C7, D8, D7, B4, E7, C4, D5, B2, P18, N18, N17, V18, V17, U18, P13, N14, N13, V14, V13, U13	GND		
J6, AD3, AF12, AB25, P17, R17, U17, P16, P15, T16, T15, R16, R15, U16, U15, P14, T14, R14, U14, T17	1.8V VDD		

Table 7 Power and Ground - Pin Descxriptions

Pin/Ball #	Pin Name	Type	Description
K6, AK3, AB6, AG3, AG4, AH4, AJ3, AF8, AH6, AH9, AG11, AH7, AK5, AG9, AG12, AK10, AJ12, AK12, AK13, AJ16, AH16, AJ17, AJ18, AG18, AG19, AK21, AK22, AH22, AF20, AK26, AK24, AJ25, AE21, AG24, AK28, AK29, AJ28, AE24, J25, D27, B29, E25, B28, F22, A28, E22, B26, D22, B24, E20, E19, B22, A21, D18, A19, A18, B14, A13, D13, E13, A9, C10, B8, A7, D9, E9, B5, A3, D6, F7, D4, T18, R18, N16, N15, V16, V15, T13, R13	3.3V DIGITAL VDD		
AH3, A23, A16, B17, A17, B15, B10, B16, F10, E6, AK15, AG15, AK14	ANALOG 3.3V VDD		

The information in this document is subject to change without notice.

Datasheet **Revision History:**		**September 1, 2005**	P1.0.1
Previous Version:			
Date	**Rev.**	**Subjects (major changes since last version)**	**Approved on**
07/05/05	**P1.0.0**	**Preliminary rease**	
09/01/2005	**P1.0.1**	**Added definitions to pin description tables**	

Edition September 1, 2005

**Published by Exar Corporation,
48720 Kato Road,
Fremont, CA 94538**

NOTICE: