XRT86VX38A GENERAL DESCRIPTION

The XRT86VX38A is an eight-channel 1.544 Mbit/s or 2.048 Mbit/s DS1/E1/J1 framer and Long-haul/Short-hual LIU integrated solution featuring R^3 technology (Relayless, Reconfigurable, Redundancy) and BITS Timing element. The physical interface is optimized with internal impedance, and with the patented pad structure, the XRT86VX38A provides protection from power failures and hot swapping.

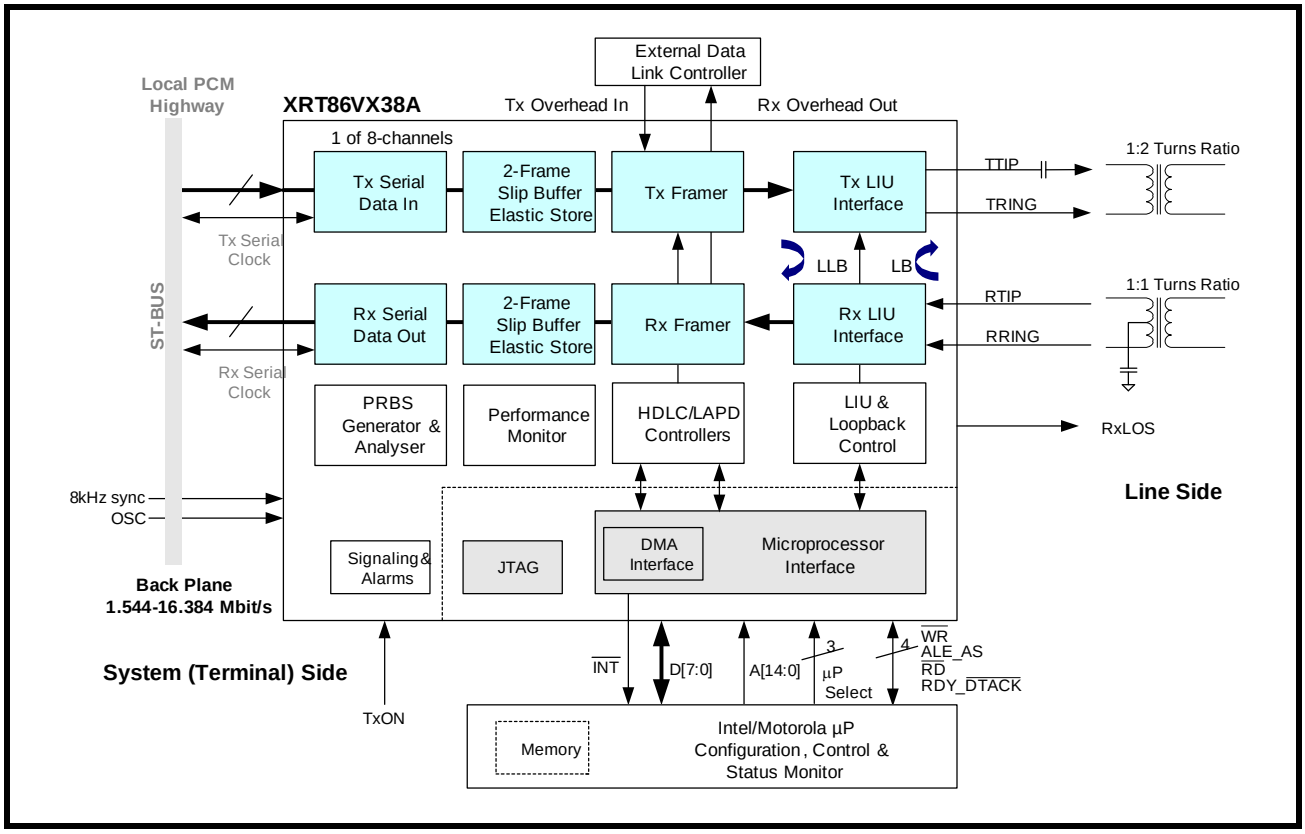
The XRT86VX38A contains an integrated DS1/E1/J1 framer and LIU which provide DS1/E1/J1 framing and error accumulation in accordance with ANSI/ITU_T specifications. Each framer has its own framing synchronizer and transmit-receive slip buffers. The slip buffers can be independently enabled or disabled as required and can be configured to frame to the common DS1/E1/J1 signal formats.

Each Framer block contains its own Transmit and Receive T1/E1/J1 Framing function. There are 3 Transmit HDLC controllers per channel which encapsulate contents of the Transmit HDLC buffers into LAPD Message frames. There are 3 Receive HDLC controllers per channel which extract the payload content of Receive LAPD Message frames from the incoming T1/E1/J1 data stream and write the contents into the Receive HDLC buffers. Each framer also contains a Transmit and Overhead Data Input port, which permits Data Link Terminal Equipment direct access to the outbound T1/E1/J1 frames. Likewise, a Receive Overhead output data port permits Data Link Terminal Equipment direct access to the Data Link bits of the inbound T1/E1/J1 frames.

The XRT86VX38A fully meets all of the latest T1/E1/J1 specifications: ANSI T1/E1.107-1988, ANSI T1/E1.403-1995, ANSI T1/E1.231-1993, ANSI T1/E1.408-1990, AT&T TR 62411 (12-90) TR54016, and ITU G-703, G.704, G706 and G.733, AT&T Pub. 43801, and ETS 300 011, 300 233, JT G.703, JT G.704, JT G706, I.431. Extensive test and diagnostic functions include Loop-backs, Boundary scan, Pseudo Random bit sequence (PRBS) test pattern generation, Performance Monitor, Bit Error Rate (BER) meter, forced error insertion, and LAPD unchannelized data payload processing according to ITU-T standard Q.921.

Applications and Features (next page)

FIGURE 1. XRT86VX38A 8-CHANNEL DS1 (T1/E1/J1) FRAMER/LIU COMBO



APPLICATIONS

- High-Density T1/E1/J1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- T1/E1/J1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs): T1/E1/J1 and Fractional T1/E1/J1
- BITS Timing
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)
- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated DS1 interfaces
- Multichannel DS1 Test Equipment
- T1/E1/J1 Performance Monitoring
- Voice over packet gateways
- Routers

FEATURES

- Backwards compatible to the XRT86VX38
- Supports Section 13 - Synchronization Interface (BITS timing) in ITU G.703 for both Tx and Rx Paths
- Supports SSM Synchronous Messaging Generation (BOC for T1, National Bits for E1) on the Transmit Path
- Supports SSM Synchronous Messaging Extraction (BOC for T1, National Bits for E1) on the Receive Path
- Supports a Customized Section 13 - Synchronization Interface in G.703 at 1.544MHz
- BITS functionality (generation and extraction) can be enabled by channel or globally **-** *New Feature*
- DS-0 Monitoring on both Transmit and Receive Time Slots
- Supports SSM Synchronization Messaging per ANSI T1.101-1999 and ITU G.704
- Independent, full duplex DS1 Tx and Rx Framer/LIUs
- Each channel has full featured Long-haul/Short-haul LIU
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx provide up to 8.192 MHz asynchronous back plane connections with jitter and wander attenuation
- Supports input PCM and signaling data at 1.544, 2.048, 4.096 and 8.192 Mbits. Also supports 2-channel multiplexed 12.352/16.384 (HMVIP/H.100) Mbit/s on the back plane bus
- Programmable output clocks for Fractional T1/E1/J1
- Supports Channel Associated Signaling (CAS) and Common Channel Signaling (CCS)
- Supports ISDN Primary Rate Interface (ISDN PRI) signaling
- Extracts and inserts robbed bit signaling (RBS)

- 3 Integrated HDLC controllers for Tx and Rx, each controller having two 96-byte buffers (buffer 0 / buffer 1)
- 3 Full SS7 Controllers per channel that support continuous LSSU and FISU transmission and interrupt filtering of continuous SS7 received messages. **-** *New Feature*
- Timeslot assignable HDLC
- V5.1 or V5.2 Interface
- Automatic Performance Report Generation (PMON Status) can be inserted into the transmit LAPD interface every 1 second or for a single transmission
- Supports SPRM and NPRM
- Alarm Indication Signal with Customer Installation signature (AIS-CI) - *Hardware enhancement*
- Remote Alarm Indication with Customer Installation (RAI-CI) - *Hardware enhancement*
- Simultaneous RAI-CI and AIS-CI monitoring - *New Feature*
- Gapped Clock interface mode for Transmit and Receive.
- Supports RxCLK clock squelch upon LOS - *New Feature*
- Intel/Motorola and Power PC interfaces for configuration, control and status monitoring
- Parallel search algorithm for fast frame synchronization
- Wide choice of T1 framing structures: SF/D4, ESF, SLC®96, T1DM and N-Frame (non-signaling)
- Direct access to D and E channels for fast transmission of data link information
- Full BERT (supports TR-25) Controller for generation and detection on system and line side of the chip
- PRBS, QRSS, and Network Loop Code generation and detection
- Seven Independent, simultaneous Loop Code Detectors per Channel
- Programmable Interrupt output pin
- Supports programmed I/O and DMA modes of Read-Write access
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms
- Detects OOF, LOF, LOS errors and COFA conditions
- Loopbacks: Local (LLB) and Line remote (LB)
- Facilitates Inverse Multiplexing for ATM
- Performance monitor with one second polling
- Boundary scan (IEEE 1149.1) JTAG test port
- Accepts external 8kHz Sync reference
- 3.3V CMOS operation with 5V tolerant inputs, 1.8V Inner Core
- Offered in 256-pin fpBGA and 329-pin fpBGA packages with -40°C to +85°C operation

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86VX38AIB329	329 Fine Pitch Ball Grid Array	-40°C to +85°C
XRT86VX38AIB256	256 Fine Pitch Ball Grid Array	-40°C to +85°C

329 BALL - FINE PITCH BALL GRID ARRAY (BOTTOM VIEW - SEE PIN LIST FOR DESCRIPTION)

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	A
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	B
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	C
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	D
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	E
O	O	O	O	O										O	O	O	O	O	F
O	O	O	O	O		O	O	O	O	O	O	O		O	O	O	O	O	G
O	O	O	O	O		O	O	O	O	O	O	O		O	O	O	O	O	H
O	O	O	O	O		O	O	O	O	O	O	O		O	O	O	O	O	J
O	O	O	O	O		O	O	O	O	O	O	O		O	O	O	O	O	K
O	O	O	O	O		O	O	O	O	O	O	O		O	O	O	O	O	L
O	O	O	O	O		O	O	O	O	O	O	O		O	O	O	O	O	M
O	O	O	O	O		O	O	O	O	O	O	O		O	O	O	O	O	N
O	O	O	O	O										O	O	O	O	O	P
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	R
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	T
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	U
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	V
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	W

256 BALL - FINE PITCH BALL GRID ARRAY (BOTTOM VIEW - SEE PIN LIST FOR DESCRIPTION)

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	A
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	B
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	C
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	D
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	E
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	F
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	G
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	H
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	J
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	K
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	L
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	M
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	N
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	P
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	R
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	T

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1.0 PIN LISTS

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
A1	VDD
A2	VDDPLL18
A3	VSS
A4	DGND
A5	TDI
A6	VSS
A7	RXSIG0
A8	RXSYNC0
A9	TXSYNC0
A10	TXSIG0
A11	RXSERCLK1
A12	VDD
A13	TXSYNC1
A14	TXSER1
A15	VSS
A16	RXCASYNC2
A17	RXCRCSYNC2
A18	RxSCLK2
A19	VDD
B1	GNDPLL
B2	VDDPLL18
B3	VDDPLL18
B4	DVDD18
B5	RXTSEL
B6	VDD
B7	TMS
B8	RXLOS0
B9	VDD
B10	TXMSYNC0
B11	TXSERCLK0
B12	RXSIG1

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
B13	RXLOS1
B14	TXMSYNC1
B15	TXSIG1
B16	RXSERCLK2
B17	RXSER2
B18	TXSIG2
B19	RXSER3
C1	RTIP0
C2	RVDD0
C3	GNDPLL
C4	VDDPLL18
C5	VSS
C6	AGND
C7	aTEST
C8	MCLKIN
C9	TRST
C10	TCK
C11	RxSCLK0
C12	RXSER1
C13	RXSYNC1
C14	RXCASYNC1
C15	RXSYNC2
C16	RXSIG2
C17	TXSERCLK2
C18	TXMSYNC2
C19	RXCRCSYNC3
D1	RRING0
D2	RGND0
D3	TTIP0
D4	TVDD0
D5	GNDPLL
D6	AVDD18

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
D7	TDO
D8	RXSER0
D9	RXSERCLK0
D10	RXCRCSYNC0
D11	TXSER0
D12	RXCRCSYNC1
D13	VDD18
D14	TXSERCLK1
D15	RXLOS2
D16	TXSYNC2
D17	TXSER2
D18	RXSIG3
D19	RXCASYNC3
E1	RTIP1
E2	RVDD1
E3	TRING0
E4	TGND0
E5	ANALOG
E6	VDD18
E7	VSS
E8	VDD18
E9	VDD18
E10	RXCASYNC0
E11	VDD18
E12	VDD18
E13	VDD18
E14	RxSCLK1
E15	VDD18
E16	VDD
E17	RXSYNC3
E18	RXLOS3
E19	TXSYNC3

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
F1	RRING1
F2	VSS
F3	TTIP1
F4	TRING1
F5	VDD
F15	VDD18
F16	RXSERCLK3
F17	RxSCLK3
F18	TXSERCLK3
F19	TXSER3
G1	RVDD2
G2	RGND1
G3	TGND1
G4	TVDD1
G5	VDD18
G7	VDD18
G8	VSS
G9	VDD18
G10	VSS
G11	VDD18
G12	VSS
G13	VDD18
G15	DATA7
G16	TXMSYNC3
G17	$\overline{WR}$ / R/$\overline{W}$
G18	TXSIG3
G19	$\overline{CS}$
H1	RTIP2
H2	RGND2
H3	TRING2
H4	TTIP2
H5	VSS

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
H7	VSS
H8	VSS
H9	VSS
H10	VSS
H11	VSS
H12	VSS
H13	VSS
H15	ADDR12
H16	DATA6
H17	ADDR14
H18	DATA5
H19	ADDR13
J1	RRING2
J2	RVDD3
J3	TGND2
J4	TVDD2
J5	VDD18
J7	VDD18
J8	VSS
J9	VSS
J10	VSS
J11	VSS
J12	VSS
J13	VDD18
J15	ADDR11
J16	ADDR9
J17	VDD
J18	$\overline{\text{INT}}$
J19	DATA4
K1	RTIP3
K2	RGND3
K3	TRING3

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
K4	TTIP3
K5	TVDD3
K7	VSS
K8	VSS
K9	VSS
K10	VSS
K11	VSS
K12	VSS
K13	VSS
K15	ADDR8
K16	DATA2
K17	ALE / $\overline{\text{AS}}$
K18	ADDR10
K19	PTYPE2
L1	RRING3
L2	RVDD4
L3	TTIP4
L4	TRING4
L5	TGND3
L7	VDD18
L8	VSS
L9	VSS
L10	VSS
L11	VSS
L12	VSS
L13	VDD18
L15	VDD18
L16	ADDR4
L17	ADDR6
L18	DATA3
L19	ADDR7
M1	RTIP4

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
M2	RGND4
M3	TGND4
M4	TVDD4
M5	VDD18
M7	VSS
M8	VSS
M9	VSS
M10	VSS
M11	VSS
M12	VSS
M13	VSS
M15	ADDR3
M16	$\overline{\text{RDY}}$ / $\overline{\text{DTACK}}$
M17	ADDR1
M18	ADDR2
M19	ADDR5
N1	RRING4
N2	RVDD5
N3	TTIP5
N4	TRING5
N5	TVDD5
N7	VDD18
N8	VSS
N9	VDD18
N10	VSS
N11	VDD18
N12	VSS
N13	VDD18
N15	VSS
N16	DATA0
N17	$\overline{\text{RD}}$ / $\overline{\text{DS}}$ / $\overline{\text{WE}}$
N18	PTYPE1

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
N19	ADDR0
P1	RTIP5
P2	VSS
P3	TGND5
P4	RVDD6
P5	TGND6
P15	VDD18
P16	VDD
P17	PTYPE0
P18	PCLK
P19	DATA1
R1	RRING5
R2	RGND5
R3	TVDD6
R4	TRING6
R5	TTIP6
R6	VSS
R7	RXCRCSYNC7
R8	TXMSYNC6
R9	VDD18
R10	VDD18
R11	VDD
R12	VDD18
R13	VDD
R14	VDD18
R15	VDD
R16	$\overline{\text{REQ1}}$
R17	RXSERCLK4
R18	VDD
R19	$\overline{\text{ACK1}}$
T1	RTIP6
T2	RGND6

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
T3	TTIP7
T4	TVDD7
T5	8KEXTOSC
T6	VDD18
T7	VDD
T8	RXSYNC7
T9	RXCASYNC7
T10	RXSYNC6
T11	TXSERCLK5
T12	RXSERCLK6
T13	TXMSYNC5
T14	RxSCLK5
T15	RXSERCLK5
T16	TXSYNC4
T17	RXSYNC4
T18	$\overline{\text{ACK0}}$
T19	$\overline{\text{REQ0}}$
U1	RRING6
U2	RVDD7
U3	TRING7
U4	VDD
U5	TXSERCLK7
U6	TXSIG7
U7	RXSERCLK7
U8	RxSCLK7
U9	RXSIG7
U10	TXSIG6
U11	RxSCLK6
U12	VSS
U13	TXSYNC5
U14	RXSYNC5
U15	RXLOS5

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
U16	TXMSYNC4
U17	RXCASYNC4
U18	RXSIG4
U19	RXLOS4
V1	VDD
V2	TGND7
V3	RGND7
V4	$\overline{\text{RESET}}$
V5	E1OSCCLK
V6	TXMSYNC7
V7	RXLOS7
V8	RXSER7
V9	TXSYNC6
V10	RXCRCSYNC6
V11	RXLOS6
V12	RXSIG6
V13	TXSER5
V14	RXSER5
V15	RXCASYNC5
V16	TXSIG4
V17	TXSERCLK4
V18	RXSER4
V19	RXCRCSYNC4
W1	VSS
W2	RTIP7
W3	RRING7
W4	TXON
W5	T1OSCCLK
W6	TXSER7
W7	TXSYNC7
W8	TXSERCLK6
W9	TXSER6

TABLE 1: 329 BALL LIST BY BALL NUMBER

PIN	PIN NAME
W10	RXCASYNC6
W11	VDD
W12	RXSER6
W13	TXSIG5
W14	RXSIG5
W15	VDD
W16	RXCRCSYNC5
W17	TXSER4
W18	RxSCLK4
W19	VSS

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
A1	GNDPLL
A2	GNDPLL
A3	VDDPLL18
A4	VDDPLL18
A5	RxTSEL
A6	TMS
A7	RXLOS0
A8	RXCRCSYNC0
A9	RXCASYNC0
A10	RXSERCLK1
A11	RXSYNC1
A12	TXMSYNC1
A13	RXSYNC2
A14	TXSYNC2
A15	RxSCLK2
A16	VDD
B1	RTIP0
B2	RVDD0
B3	VDDPLL18
B4	ANALOG
B5	AGND
B6	TDO
B7	RXSER0
B8	RXSERCLK0
B9	RXSYNC0
B10	RxSCLK0
B11	RXSER1
B12	TXSYNC1
B13	TXSERCLK1
B14	RXSER2
B15	TXSERCLK2

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
B16	RXSER3
C1	RRING0
C2	RGND0
C3	TTIP0
C4	GNDPLL
C5	AVDD18
C6	DVDD18
C7	aTEST
C8	TDI
C9	TXSYNC0
C10	RXCRCSYNC1
C11	RXLOS1
C12	TXSER1
C13	RXSERCLK2
C14	RXCRCSYNC2
C15	TXMSYNC2
C16	RXSYNC3
D1	RTIP1
D2	RVDD1
D3	TRING0
D4	TVDD0
D5	VDDPLL18
D6	DGND
D7	TRST
D8	TCK
D9	TXMSYNC0
D10	TXSERCLK0
D11	RXCASYNC1
D12	RxSCLK1
D13	RXCASYNC2
D14	TXSER2
D15	RXSERCLK3

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
D16	RXLOS3
E1	RRING1
E2	RGND1
E3	TTIP1
E4	TRING1
E5	TGND0
E6	MCLKIN
E7	VSS
E8	VDD
E9	VSS
E10	TXSER0
E11	VDD
E12	RXCRCSYNC3
E13	RXCASYNC3
E14	TXMSYNC3
E15	TXSYNC3
E16	TXSERCLK3
F1	RTIP2
F2	RVDD2
F3	TGND1
F4	TVDD1
F5	TVDD2
F6	VSS
F7	VSS
F8	VDD18
F9	VDD18
F10	VDD18
F11	RXLOS2
F12	RxSCLK3
F13	$\overline{WR}$ / R/$\overline{W}$
F14	$\overline{CS}$
F15	TXSER3

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
F16	ADDR13
G1	RRING2
G2	RGND2
G3	TTIP2
G4	TRING2
G5	TGND2
G6	VDD18
G7	VSS
G8	VSS
G9	VSS
G10	VSS
G11	ADDR14
G12	DATA6
G13	DATA7
G14	DATA5
G15	VDD
G16	ADDR12
H1	RTIP3
H2	RVDD3
H3	TTIP3
H4	TRING3
H5	TVDD3
H6	VDD18
H7	VSS
H8	VSS
H9	VSS
H10	VSS
H11	VDD18
H12	PTYPE2
H13	DATA4
H14	ADDR10
H15	$\overline{INT}$

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
H16	ADDR11
J1	RRING3
J2	RGND3
J3	TTIP4
J4	TRING4
J5	TGND3
J6	VDD18
J7	VSS
J8	VSS
J9	VSS
J10	VSS
J11	VDD18
J12	DATA3
J13	ADDR9
J14	ADDR8
J15	ADDR7
J16	ALE / $\overline{AS}$
K1	RTIP4
K2	RVDD4
K3	TGND4
K4	TVDD4
K5	TVDD5
K6	VDD18
K7	VSS
K8	VSS
K9	VSS
K10	VSS
K11	VDD18
K12	DATA2
K13	ADDR4
K14	ADDR6
K15	ADDR2

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
K16	ADDR5
L1	RRING4
L2	RGND4
L3	TTIP5
L4	TRING5
L5	TGND5
L6	8KEXTOSC
L7	VDD18
L8	VDD18
L9	VDD18
L10	VDD18
L11	ADDR3
L12	DATA1
L13	ADDR0
L14	ADDR1
L15	$\overline{RD}$ / $\overline{DS}$ / $\overline{WE}$
L16	$\overline{RDY}$ / $\overline{DTACK}$
M1	RTIP5
M2	RVDD5
M3	TTIP6
M4	TRING6
M5	TVDD6
M6	VDD
M7	RxSCLK7
M8	RXCASYNC7
M9	VDD
M10	RXSERCLK6
M11	TXSYNC5
M12	PTYPE1
M13	PTYPE0
M14	DATA0
M15	$\overline{ACK1}$

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
M16	PCLK
N1	RRING5
N2	RGND5
N3	TGND6
N4	TVDD7
N5	TGND7
N6	TXMSYNC7
N7	RXCRCSYNC7
N8	TXSYNC6
N9	RXCASYNC6
N10	TXSERCLK5
N11	RXSYNC5
N12	TXSER4
N13	RXSYNC4
N14	VDD
N15	$\overline{ACK0}$
N16	$\overline{REQ0}$
P1	RTIP6
P2	RVDD6
P3	TTIP7
P4	TRING7
P5	TXSER7
P6	TXSERCLK7
P7	RXLOS7
P8	RXSER7
P9	RxSCLK6
P10	TXSER5
P11	RXSER5
P12	RXLOS5
P13	TXMSYNC4
P14	RXSERCLK4
P15	RXSER4

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
P16	RXLOS4
R1	RRING6
R2	RGND6
R3	RGND7
R4	$\overline{RESET}$
R5	E1OSCCLK
R6	RXSERCLK7
R7	RXSYNC7
R8	TXMSYNC6
R9	RXCRCSYNC6
R10	RXLOS6
R11	TXMSYNC5
R12	RXCASYNC5
R13	RXCRCSYNC5
R14	RXCASYNC4
R15	RXCRCSYNC4
R16	$\overline{REQ1}$
T1	RVDD7
T2	RTIP7
T3	RRING7
T4	TXON
T5	T1OSCCLK
T6	TXSYNC7
T7	TXSERCLK6
T8	TXSER6
T9	RXSYNC6
T10	RXSER6
T11	RxSCLK5
T12	RXSERCLK5
T13	TXSYNC4
T14	TXSERCLK4
T15	RxSCLK4

TABLE 2: 256 BALL LIST BY BALL NUMBER

PIN	PIN NAME
T16	VDD

2.0 PIN DESCRIPTIONS

There are six types of pins defined throughout this pin description and the corresponding symbol is presented in table below. The per-channel pin is indicated by the channel number or the letter 'n' which is appended at the end of the signal name, for example, TxSERn, where "n" indicates channels 0 to 7. All output pins are "tri-stated" upon hardware RESET.

SYMBOL	PIN TYPE
I	Input
O	Output
I/O	Bidirectional
GND	Ground
PWR	Power
NC	No Connect

The structure of the pin description is divided into eleven groups, as presented in the table below

TABLE 3: PIN DESCRIPTION STRUCTURE

SECTION	PAGE NUMBER
Transmit System Side Interface	page 13
Receive System Side Interface	page 18
Receive Line Interface	page 23
Transmit Line Interface	page 24
Timing Interface	page 25
JTAG Interface	page 26
Microprocessor Interface	page 26
Power Pins (3.3V)	page 35
Power Pins (1.8V)	page 36
Ground Pins	page 37
No Connect Pins	page 38

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxSER0/ TxPOS0	D11	E10	I	-	**Transmit Serial Data Input (TxSERn)/Transmit Positive Digital Input (TxPOSn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Mode - TxSERn** These pins function as the transmit serial data input on the system side interface, which are latched on the rising edge of the TxSERCLKn pin. Any payload data applied to this pin will be inserted into an outbound DS1/E1 frame and output to the line. In DS1 mode, the framing alignment bits, facility data link bits, CRC-6 bits, and signaling information can also be inserted from this input pin if configured appropriately. In E1 mode, all data intended to be transported via Time Slots 1 through 15 and Time slots 17 through 31 must be applied to this input pin. Data intended for Time Slots 0 and 16 can also be applied to this input pin If configured accordingly. **DS1 or E1 High-Speed Multiplexed Mode* - TxSERn** In this mode, these pins are used as the high-speed multiplexed data input pin on the system side. High-speed multiplexed data of channels 0-3 must be applied to TxSER0 and high-speed multiplexed data of channels 4-7 must be applied to TxSER4 in a byte or bit-interleaved way. The framer latches in the multiplexed data on TxSER0 and TxSER4 using TxMSYNC/TxINCLK and demultiplexes this data into 4 serial streams. The LIU block will then output the data to the line interface using TxSERCLKn. **DS1 or E1 Framer Bypass Mode - TxPOSn** In this mode, TxSERn is used for the positive digital input pin (TxPOSn) to the LIU. ***NOTE:*** 1. **High-speed multiplexed modes include (For T1/E1) 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* 2. *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* 3. *These 8 pins are internally pulled "High" for each channel.*
TxSER1/ TxPOS1	A14	C12			
TxSER2/ TxPOS2	D17	D14			
TxSER3/ TxPOS3	F19	F15			
TxSER4/ TxPOS4	W17	N12			
TxSER5/ TxPOS5	V13	P10			
TxSER6/ TxPOS6	W9	T8			
TxSER7/ TxPOS7	W6	P5			

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxSERCLK0/ TxLINECLK0 TxSERCLK1/ TxLINECLK1 TxSERCLK2/ TxLINECLK2 TxSERCLK3/ TxLINECLK3 TxSERCLK4/ TxLINECLK4 TxSERCLK5/ TxLINECLK5 TxSERCLK6/ TxLINECLK6 TxSERCLK7/ TxLINECLK7	B11 D14 C17 F18 V17 T11 W8 U5	D10 B13 B15 E16 T14 N10 T7 P6	I/O	12	**Transmit Serial Clock (TxSERCLKn)/Transmit Line Clock (TxSERCLKn):** The exact function of these pins depends on the mode of operation selected, as described below. **In Base-Rate Mode (1.544MHz/2.048MHz) - TxSERCLKn:** This clock signal is used by the transmit serial interface to latch the contents on the TxSERn pins into the T1/E1 framer on the rising edge of the TxSERCLKn. These pins can be configured as input or output as described below. **When TxSERCLKn is configured as Input:** These pins will be inputs if the TxSERCLK is chosen as the timing source for the transmit framer. Users must provide a 1.544MHz clock rate to this input pin for T1 mode of operation, and 2.048MHz clock rate in E1 mode. **When TxSERCLKn is configured as Output:** These pins will be outputs if either the recovered line clock or the MCLK PLL is chosen as the timing source for the T1/E1 transmit framer. The transmit framer will output a 1.544MHz clock rate in T1 mode of operation, and a 2.048MHz clock rate in E1 mode. **DS1/E1 High-Speed Backplane Modes* - TxSERCLKn as INPUT ONLY** In this mode, TxSERCLK is an optional clock signal input which is used as the timing source for the transmit line interface, and is only required if TxSERCLK is chosen as the timing source for the transmit framer. If TxSERCLK is chosen as the timing source, system equipment should provide 1.544MHz (For T1 mode) or 2.048MHz (For E1 mode) to the TxSERCLKn pins on each channel. TxSERCLK is not required if either the recovered clock or MCLK PLL is chosen as the timing source of the device. High speed or multiplexed data is latched into the device using the TxMSYNC/TxINCLK high-speed clock signal. **DS1 or E1 Framer Bypass Mode - TxLINECLKn** In this mode, TxSERCLKn is used as the transmit line clock (TxLINECLK) to the LIU. ***NOTE:*** **High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* ***NOTE:*** *These 8 pins are internally pulled "High" for each channel.*

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxSYNC0/ TxNEG0 TxSYNC1/ TxNEG1 TxSYNC2/ TxNEG2 TxSYNC3/ TxNEG3 TxSYNC4/ TxNEG4 TxSYNC5/ TxNEG5 TxSYNC6/ TxNEG6 TxSYNC7/ TxNEG7	A9 A13 D16 E19 T16 U13 V9 W7	C9 B12 A14 E15 T13 M11 N8 T6	I/O	12	**Transmit Single Frame Sync Pulse (TxSYNCn) / Transmit Negative Digital Input (TxNEGn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Base Rate Mode (1.544MHz/2.048MHz) - TxSYNCn:** These TxSYNCn pins are used to indicate the single frame boundary within an outbound T1/E1 frame. In both DS1 or E1 mode, the single frame boundary repeats every 125 microseconds (8kHz). In DS1/E1 base rate, TxSYNCn can be configured as either input or output as described below. **When TxSYNCn is configured as an Input**: Users must provide a signal which must pulse "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 frame. It is imperative that the TxSYNC input signal be synchronized with the TxSERCLK input signal. **When TxSYNCn is configured as an Output:** The transmit T1/E1 framer will output a signal which pulses "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 frame. **DS1/E1 High-Speed Backplane Modes* - TxSYNCn as INPUT ONLY:** In this mode, TxSYNCn must be an input regardless of the clock source that is chosen to be the timing source for the transmit framer. In 2.048MVIP/4.096/8.192MHz high-speed modes, TxSYNCn pins must be pulsed 'High' for one period of TxSERCLK during the first bit of the outbound T1/E1 frame. In HMVIP mode, TxSYNC0 and TxSYNC4 must be pulsed 'High' for 4 clock cycles of the TxMSYNC/TxINCLK signal in the position of the first two and the last two bits of a multiplexed frame. In H.100 mode, TxSYNC0 and TxSYNC4 must be pulsed 'High' for 2 clock cycles of the TxMSYNC/TxINCLK signal in the position of the first and the last bit of a multiplexed frame. **DS1 or E1 Framer Bypass Mode - TxNEGn** In this mode, TxSYNCn is used as the negative digital input pin (TxNEG) to the LIU. ***NOTE:*** **High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* ***NOTE:*** *These 8 pins are internally pulled "Low" for each channel.*

TRANSMIT SYSTEM SIDE INTERFACE

<table>
<tr><th>SIGNAL NAME</th><th>329 PKG BALL#</th><th>256 PKG BALL #</th><th>TYPE</th><th>OUTPUT DRIVE(MA)</th><th>DESCRIPTION</th></tr>
<tr><td>TxMSYNC0/ TxINCLK0
TxMSYNC1/ TxINCLK1
TxMSYNC2/ TxINCLK2
TxMSYNC3/ TxINCLK3
TxMSYNC4/ TxINCLK4
TxMSYNC5/ TxINCLK5
TxMSYNC6/ TxINCLK6
TxMSYNC7/ TxINCLK7</td><td>B10
B14
C18
G16
U16
T13
R8
V6</td><td>D9
A12
C15
E14
P13
R11
R8
N6</td><td>I/O</td><td>12</td><td>
Multiframe Sync Pulse (TxMSYNCn) / Transmit Input Clock (TxINCLKn)
The exact function of these pins depends on the mode of operation selected, as described below.
DS1/E1 Base Rate Mode (1.544MHz/2.048MHz) - TxMSYNCn
In this mode, these pins are used to indicate the multi-frame boundary within an outbound DS1/E1 frame.
In DS1 ESF mode, TxMSYNCn repeats every 3ms.
In DS1 SF mode, TxMSYNCn repeats every 1.5ms.
In E1 mode, TxMSYNCn repeats every 2ms.
If TxMSYNCn is configured as an input, TxMSYNCn must pulse "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 multi-frame. It is imperative that the TxMSYNC input signal be synchronized with the TxSERCLK input signal.
If TxMSYNCn is configured as an output, the transmit section of the T1/E1 framer will output and pulse TxMSYNC "High" for one period of TxSERCLK during the first bit of an outbound DS1/E1 frame.
DS1/E1 High-Speed Backplane Modes* - (TxINCLKn as INPUT ONLY)
In this mode, this pin must be used as the high-speed input clock pin (TxINCLKn) for the backplane interface to latch in high-speed or multiplexed data on the TxSERn pin. The frequency of TxINCLK is presented in the table below.
<table>
<tr><th>OPERATION MODE</th><th>FREQUENCY OF TXINCLK(MHZ)</th></tr>
<tr><td>2.048MVIP non-multiplexed</td><td>2.048</td></tr>
<tr><td>4.096MHz non-multiplexed</td><td>4.096</td></tr>
<tr><td>8.192MHz non-multiplexed</td><td>8.192</td></tr>
<tr><td>12.352MHz Bit-multiplexed (DS1 ONLY)</td><td>12.352</td></tr>
<tr><td>16.384MHz Bit-multiplexed</td><td>16.384</td></tr>
<tr><td>16.384 HMVIP Byte-multiplexed</td><td>16.384</td></tr>
<tr><td>16.384 H.100 Byte-multiplexed</td><td>16.384</td></tr>
</table>
NOTES:
1. *High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.
2. In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don’t care).
3. These 8 pins are internally pulled “Low” for each channel.
</td></tr>
</table>

TRANSMIT SYSTEM SIDE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE(MA)	DESCRIPTION
TxSIG0 TxSIG1 TxSIG2 TxSIG3 TxSIG4 TxSIG5 TxSIG6 TxSIG7	A10 B15 B18 G18 V16 W13 U10 U6		I/O	8	**Transmit Time Slot Octet Identifier Output 0 (TxCHNn_0) / Transmit Serial Signaling Input (TxSIGn):** The exact function of these pins depends on whether or not the transmit framer enables the transmit fractional/signaling interface, as described below: **If transmit fractional/signaling interface is disabled -** - No function **If transmit fractional/signaling interface is enabled - TxSIGn:** These pins can be used to input robbed-bit signaling data to be inserted within an outbound DS1 frame or to input Channel Associated Signaling (CAS) data within an outbound E1 frame, as described below. **T1 Mode:** Signaling data (A,B,C,D) of each channel must be provided on bit 4,5,6,7 of each time slot on the TxSIG pin if 16-code signaling is used. If 4-code signaling is selected, signaling data (A,B) of each channel must be provided on bit 4, 5 of each time slot on the TxSIG pin. If 2-code signaling is selected, signaling data (A) of each channel must be provided on bit 4 of each time slot on the TxSIG pin. **E1 Mode:** Signaling data in E1 mode can be provided on the TxSIGn pins on a time-slot-basis as in T1 mode, or it can be provided on time slot 16 only via the TxSIGn input pins. In the latter case, signaling data (A,B,C,D) of channel 1 and channel 17 must be inserted on the TxSIGn pin during time slot 16 of frame 1, signaling data (A,B,C,D) of channel 2 and channel 18 must be inserted on the TxSIGn pin during time slot 16 of frame 2...etc. The CAS multiframe Alignments bits (0000 bits) and the extra bits/alarm bit (xyxx) must be inserted on the TxSIGn pin during time slot 16 of frame 0. ***NOTE:*** *Transmit fractional interface can be enabled by programming to bit 4 - TxFr1544/TxFr2048 bit from register 0xn120 to '1'.* ***NOTE:*** *These 8 pins are internally pulled "Low" for each channel.*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxSYNC0/ RxNEG0 RxSYNC1/ RxNEG1 RxSYNC2/ RxNEG2 RxSYNC3/ RxNEG3 RxSYNC4/ RxNEG4 RxSYNC5/ RxNEG5 RxSYNC6/ RxNEG6 RxSYNC7/ RxNEG7	A8 C13 C15 E17 T17 U14 T10 T8	B9 A11 A13 C16 N13 N11 T9 R7	I/O	12	**Receive Single Frame Sync Pulse (RxSYNCn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Base Rate Mode (1.544MHz/2.048MHz) - RxSYNCn:** These RxSYNCn pins are used to indicate the single frame boundary within an inbound T1/E1 frame. In both DS1 or E1 mode, the single frame boundary repeats every 125 microseconds (8kHz). In DS1/E1 base rate, RxSYNCn can be configured as either input or output depending on the slip buffer configuration as described below. **When RxSYNCn is configured as an Input**: Users must provide a signal which must pulse "High" for one period of RxSERCLK and repeats every 125μS. The receive serial Interface will output the first bit of an inbound DS1/E1 frame during the provided RxSYNC pulse. ***NOTE:*** *It is imperative that the RxSYNC input signal be synchronized with the RxSERCLK input signal.* **When RxSYNCn is configured as an Output:** The receive T1/E1 framer will output a signal which pulses "High" for one period of RxSERCLK during the first bit of an inbound DS1/E1 frame. **DS1/E1 High-Speed Backplane Modes* - RxSYNCn as INPUT ONLY:** In this mode, RxSYNCn must be an input regardless of the slip buffer configuration. In 2.048MVIP/4.096/ 8.192MHz high-speed modes, RxSYNCn pins must be pulsed 'High' for one period of RxSERCLK during the first bit of the inbound T1/E1 frame. In HMVIP mode, RxSYNCn must be pulsed 'High' for 4 clock cycles of the RxSERCLK signal in the position of the first two and the last two bits of a multiplexed frame. In H.100 mode, RxSYNCn must be pulsed 'High' for 2 clock cycles of the RxSERCLK signal in the position of the first and the last bit of a multiplexed frame. **DS1 or E1 Framer Bypass Mode - RxNEGn** In this mode, RxSYNCn is used as the Receive negative digital output pin (RxNEG) from the LIU. ***NOTE:*** **High-speed backplane modes include (For T1/ E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).* ***NOTE:*** *These 8 pins are internally pulled "Low" for each channel.*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxCRCSYNC0 RxCRCSYNC1 RxCRCSYNC2 RxCRCSYNC3 RxCRCSYNC4 RxCRCSYNC5 RxCRCSYNC6 RxCRCSYNC7	D10 D12 A17 C19 V19 W16 V10 R7	A8 C10 C14 E12 R15 R13 R9 N7	O	12	**Receive Multiframe Sync Pulse (RxCRCSYNCn):** The RxCRCSYNCn pins are used to indicate the receive multi-frame boundary. These pins pulse "High" for one period of RxSERCLK when the first bit of an inbound DS1/E1 Multi-frame is being output on the RxCRCSYNCn pin. • In DS1 ESF mode, RxCRCSYNCn repeats every 3ms • In DS1 SF mode, RxCRCSYNCn repeats every 1.5ms • In E1 mode, RxCRCSYNCn repeats every 2ms.
RxCASYNC0 RxCASYNC1 RxCASYNC2 RxCASYNC3 RxCASYNC4 RxCASYNC5 RxCASYNC6 RxCASYNC7	E10 C14 A16 D19 U17 V15 W10 T9	A9 D11 D13 E13 R14 R12 N9 M8	O	12	**Receive CAS Multiframe Sync Pulse (RxCASYNCn):** **- E1 Mode Only** The RxCASYNCn pins are used to indicate the E1 CAS Multif-frame boundary. These pins pulse "High" for one period of RxSERCLK when the first bit of an E1 CAS Multi-frame is being output on the RxCASYNCn pin.

RECEIVE SYSTEM SIDE INTERFACE

<table>
<tr><th>SIGNAL NAME</th><th>329 PKG BALL#</th><th>256 PKG BALL #</th><th>TYPE</th><th>OUTPUT DRIVE (MA)</th><th>DESCRIPTION</th></tr>
<tr><td>RxSERCLK0/ RxLINECLK0
RxSERCLK1/ RxLINECLK1
RxSERCLK2/ RxLINECLK2
RxSERCLK3/ RxLINECLK3
RxSERCLK4/ RxLINECLK4
RxSERCLK5/ RxLINECLK5
RxSERCLK6/ RxLINECLK6
RxSERCLK7/ RxLINECLK7</td><td>D9
A11
B16
F16
R17
T15
T12
U7</td><td>B8
A10
C13
D15
P14
T12
M10
R6</td><td>I/O</td><td>12</td><td>Receive Serial Clock Signal (RxSERCLKn) / Receive Line Clock (RxLINECLKn):
The exact function of these pins depends on the mode of operation selected, as described below.
In Base-Rate Mode (1.544MHz/2.048MHz) - RxSERCLKn:
These pins are used as the receive serial clock on the system side interface which can be configured as either input or output. The receive serial interface outputs data on RxSERn on the rising edge of RxSERCLKn.
When RxSERCLKn is configured as Input:
These pins will be inputs if the slip buffer on the Receive path is enabled. System side equipment must provide a 1.544MHz clock rate to this input pin for T1 mode of operation, and 2.048MHz clock rate in E1 mode.
When RxSERCLKn is configured as Output:
These pins will be outputs if slip buffer is bypassed. The receive framer will output a 1.544MHz clock rate in T1 mode of operation, and a 2.048MHz clock rate in E1 mode.
DS1/E1 High-Speed Backplane Modes* - (RxSERCLK as INPUT ONLY)
In this mode, this pin must be used as the high-speed input clock for the backplane interface to output high-speed or multiplexed data on the RxSERn pin. The frequency of RxSERCLK is presented in the table below.
<table>
<tr><th>OPERATION MODE</th><th>FREQUENCY OF RXSERCLK(MHZ)</th></tr>
<tr><td>2.048MVIP non-multiplexed</td><td>2.048</td></tr>
<tr><td>4.096MHz non-multiplexed</td><td>4.096</td></tr>
<tr><td>8.192MHz non-multiplexed</td><td>8.192</td></tr>
<tr><td>12.352MHz Bit-multiplexed (DS1 ONLY)</td><td>12.352</td></tr>
<tr><td>16.384MHz Bit-multiplexed</td><td>16.384</td></tr>
<tr><td>16.384 HMVIP Byte-multiplexed</td><td>16.384</td></tr>
<tr><td>16.384 H.100 Byte-multiplexed</td><td>16.384</td></tr>
</table>
NOTES:
1. *High-speed backplane modes include (For T1/E1) 2.048MVIP, 4.096MHz, 8.192MHz, 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.
2. For DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).</td></tr>
</table>

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxSERCLK0/ RxLINECLK0 RxSERCLK1/ RxLINECLK1 RxSERCLK2/ RxLINECLK2 RxSERCLK3/ RxLINECLK3 RxSERCLK4/ RxLINECLK4 RxSERCLK5/ RxLINECLK5 RxSERCLK6/ RxLINECLK6 RxSERCLK7/ RxLINECLK7	D9 A11 B16 F16 R17 T15 T12 U7	B8 A10 C13 D15 P14 T12 M10 R6	I/O	12	**(Continued)** **DS1 or E1 Framer Bypass Mode - RxLINECLKn** In this mode, RxSERCLKn is used as the Receive Line Clock output pin (RxLineClk) from the LIU. ***NOTE:*** *These 8 pins are internally pulled "High" for each channel.*
RxSER0/ RxPOS0 RxSER1/ RxPOS1 RxSER2/ RxPOS2 RxSER3/ RxPOS3 RxSER4/ RxPOS4 RxSER5/ RxPOS5 RxSER6/ RxPOS6 RxSER7/ RxPOS7	D8 C12 B17 B19 V18 V14 W12 V8	B7 B11 B14 B16 P15 P11 T10 P8	O	12	**Receive Serial Data Output (RxSERn):** The exact function of these pins depends on the mode of operation selected, as described below. **DS1/E1 Mode - RxSERn** These pins function as the receive serial data output on the system side interface, which are updated on the rising edge of the RxSERCLKn pin. All the framing alignment bits, facility data link bits, CRC bits, and signaling information will also be extracted to this output pin. **DS1 or E1 High-Speed Multiplexed Mode* - RxSERn** In this mode, these pins are used as the high-speed multiplexed data output pin on the system side. High-speed multiplexed data of channels 0-3 will output on RxSER0 and high-speed multiplexed data of channels 4-7 will output on RxSER4 in a byte or bit-interleaved way. The framer outputs the multiplexed data on RxSER0 and RxSER4 using the high-speed input clock (RxSERCLKn). **DS1 or E1 Framer Bypass Mode** In this mode, RxSERn is used as the positive digital output pin (RxPOSn) from the LIU. ***NOTE:*** **High-speed multiplexed modes include (For T1/E1) 16.384MHz HMVIP, H.100, Bit-multiplexed modes, and (For T1 only) 12.352MHz Bit-multiplexed mode.* ***NOTE:*** *In DS1 high-speed modes, the DS-0 data is mapped into an E1 frame by ignoring every fourth time slot (don't care).*

RECEIVE SYSTEM SIDE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxSig0 RxSig1 RxSig2 RxSig3 RxSig4 RxSig5 RxSig6 RxSig7	A7 B12 C16 D18 U18 W14 V12 U9		O	8	**Receive Serial Signaling Output (RxSIGn):** The exact function of these pins depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled :** -No function **If receive fractional/signaling interface is enabled - RxSIGn:** These pins can be used to output robbed-bit signaling data within an inbound DS1 frame or to output Channel Associated Signaling (CAS) data within an inbound E1 frame, as described below. **T1 Mode:** Signaling data (A,B,C,D) of each channel will be output on bit 4,5,6,7 of each time slot on the RxSIG pin if 16-code signaling is used. If 4-code signaling is selected, signaling data (A,B) of each channel will be output on bit 4, 5 of each time slot on the RxSIG pin. If 2-code signaling is selected, signaling data (A) of each channel will be output on bit 4 of each time slot on the RxSIG pin. **E1 Mode:** Signaling data in E1 mode will be output on the RxSIGn pins on a time-slot-basis as in T1 mode, or it can be output on time slot 16 only via the RxSIGn output pins. In the latter case, signaling data (A,B,C,D) of channel 1 and channel 17 will be output on the RxSIGn pin during time slot 16 of frame 1, signaling data (A,B,C,D) of channel 2 and channel 18 will be output on the RxSIGn pin during time slot 16 of frame 2...etc. The CAS multiframe Alignments bits (0000 bits) and the extra bits/alarm bit (xyxx) will be output on the RxSIGn pin during time slot 16 of frame 0. ***NOTE:*** *Receive Fractional/signaling interface can be enabled by programming to bit 4 - RxFr1544/ RxFr2048 bit from register 0xn122 to '1'.*
RxSCLK0 RxSCLK1 RxSCLK2 RxSCLK3 RxSCLK4 RxSCLK5 RxSCLK6 RxSCLK7	C11 E14 A18 F17 W18 T14 U11 U8	B10 D12 A15 F12 T15 T11 P9 M7	O	8	**Receive Recovered Line Clock Output (RxSCLKn):** The exact function of these pins depends on whether or not the receive framer enables the receive fractional/signaling interface, as described below: **If receive fractional/signaling interface is disabled -** -No function **If receive fractional/signaling interface is enabled - Receive Recovered Line Clock Output (RxSCLKn):** These pins output the recovered T1/E1 line clock (1.544MHz in T1 mode and 2.048MHz in E1 mode) for each channel. ***NOTE:*** *Receive Fractional/Signaling interface can be enabled by programming to bit 4 - RxFr1544/ RxFr2048 bit from register 0xn122 to '1'.*

RECEIVE LINE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RTIP0 RTIP1 RTIP2 RTIP3 RTIP4 RTIP5 RTIP6 RTIP7	C1 E1 H1 K1 M1 P1 T1 W2	B1 D1 F1 H1 K1 M1 P1 T2	I	-	**Receive Positive Analog Input (RTIPn):** RTIP is the positive differential input from the line interface. This input pin, along with the RRING input pin, functions as the “Receive DS1/E1 Line Signal” input for the XRT86VX38A device. The user is expected to connect this signal and the RRING input signal to a 1:1 transformer for proper operation. The center tap of the receive transformer should have a bypass capacitor of 0.1μF to ground (Chip Side) to improve long haul application receive capabilities.
RRING0 RRING1 RRING2 RRING3 RRING4 RRING5 RRING6 RRING7	D1 F1 J1 L1 N1 R1 U1 W3	C1 E1 G1 J1 L1 N1 R1 T3	I	-	**Receive Negative Analog Input (RRINGn):** RRING is the negative differential input from the line interface. This input pin, along with the RTIP input pin, functions as the “Receive DS1/E1 Line Signal” input for the XRT86VX38A device. The user is expected to connect this signal and the RTIP input signal to a 1:1 transformer for proper operation. The center tap of the receive transformer should have a bypass capacitor of 0.1μF to ground (Chip Side) to improve long haul application receive capabilities.
RxLOS0 RxLOS1 RxLOS2 RxLOS3 RxLOS4 RxLOS5 RxLOS6 RxLOS7	B8 B13 D15 E18 U19 U15 V11 V7	A7 C11 F11 D16 P16 P12 R10 P7	O	4	**Receive Loss of Signal Output Indicator (RLOSn):** The XRT86VX38A device will assert this output pin (i.e., toggle it “high”) anytime (and for the duration that) the Receive DS1/E1 Framer or LIU block declares the LOS defect condition. Conversely, the XRT86VX38A wil**l "TRI-State"** this pin anytime (and for the duration that) the Receive DS1/E1 Framer or LIU block is NOT declaring the LOS defect condition. ***NOTE:*** *Since the XRT86VX38A tri-states this output pin (anytime the channel is not declaring the LOS defect condition), the user MUST connect a "pull-down" resistor (ranging from 1K to 10K) to each RxLOS output pin, to pull this output pin to the logic "LOW" condition, whenever the Channel is NOT declaring the LOS defect condition.* This output pin will toggle “High” (declare LOS) if the Receive Framer or the Receive LIU block associated with Channel N determines that an RLOS condition occurs. In other words, this pin is OR-ed with the LIU RLOS and the Framer RLOS bit. If either the LIU RLOS or the Framer RLOS bit associated with channel N pulses high, the corresponding RLOS pin of that particular channel will be set to “High”.

RECEIVE LINE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
RxTSEL	B5	A5	I	-	**Receive Termination Control (RxTSEL):** Upon power up, the receivers are in "High" impedance. Switching to internal termination can be selected through the microprocessor interface by programming the appropriate channel register. However, to switch control to the hardware pin, RxTCNTL must be programmed to "1" in the appropriate global register (0x0FE2). Once control has been granted to the hardware pin, it must be pulled "High" to switch to internal termination. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.* **RxTSEL (pin)** / **Rx Termination** 0 / External 1 / Internal *Note: RxTCNTL (bit) must be set to "1"*

TRANSMIT LINE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	DESCRIPTION
TTIP0 TTIP1 TTIP2 TTIP3 TTIP4 TTIP5 TTIP6 TTIP7	D3 F3 H4 K4 L3 N3 R5 T3	C3 E3 G3 H3 J3 L3 M3 P3	O	**Transmit Positive Analog Output (TTIPn):** TTIP is the positive differential output to the line interface. This output pin, along with the corresponding TRING output pin, function as the Transmit DS1/E1 output signal drivers for the XRT86VX38A device. The user is expected to connect this signal and the corresponding TRING output signal to a 1:2 step up transformer for proper operation. This output pin will be tri-stated whenever the user sets the “TxON” input pin or register bit (0xnF02, bit 3) to “0”. ***NOTE:*** *This pin should have a series line capacitor of 0.68μF for DC blocking purposes.*
TRING0 TRING1 TRING2 TRING3 TRING4 TRING5 TRING6 TRING7	E3 F4 H3 K3 L4 N4 R4 U3	D3 E4 G4 H4 J4 L4 M4 P4	O	**Transmit Negative Analog Output (TRINGn):** TRING is the negative differential output to the line interface. This output pin, along with the corresponding TTIP output pin, function as the Transmit DS1/E1 output signal drivers for the XRT86VX38A device. The user is expected to connect this signal and the corresponding TRING output signal to a 1:2 step up transformer for proper operation. ***NOTE:*** *This output pin will be tri-stated whenever the user sets the “TxON” input pin or register bit (0xnF02, bit 3) to “0”.*

TRANSMIT LINE INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	DESCRIPTION
TxON	W4	T4	I	**Transmitter On** This input pin permits the user to either enable or disable the Transmit Output Driver within the Transmit DS1/E1 LIU Block. If the TxON pin is pulled "Low", all 8 Channels are tri-stated. When this pin is pulled 'High', turning on or off the transmitters will be determined by the appropriate channel registers (address 0x0Fn2, bit 3) **LOW** = Disables the Transmit Output Driver within the Transmit DS1/E1 LIU Block. In this setting, the TTIP and TRING output pins of all 8 channels will be tri-stated. **HIGH** = Enables the Transmit Output Driver within the Transmit DS1/E1 LIU Block. In this setting, the corresponding TTIP and TRING output pins will be enabled or disabled by programming the appropriate channel register. (address 0x0Fn2, bit 3) ***NOTE:*** *Whenever the transmitters are turned off, the TTIP and TRING output pins will be tri-stated.*

TIMING INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
MCLKIN	C8	E6	I	-	**Master Clock Input:** This pin is used to provide the timing reference for the internal master clock of the device. The frequency of this clock is programmable from 1.544MHz to 16.384MHz in register 0x0FE9.
E1OSCCLK	V5	R5	O	8	**Framer E1 Output Clock Reference** This output pin is defaulted to 2.048MHz, but can be programmed to 65.536MHz in register 0x011E.
T1OSCCLK	W5	T5	O	8	**Framer T1 Output Clock Reference** This output pin is defaulted to 1.544MHz, but can be programmed to output 49.408MHz in register 0x011E.
8KEXTOSC	T5	L6	I	-	**External Oscillator Select** For normal operation, this pin should not be used, or pulled "Low". This pin is internally pulled "Low" with a 50kΩ resistor.
ANALOG	E5	B4	O		**Factory Test Mode Pin** ***NOTE:*** *For Internal Use Only*

JTAG INTERFACE

The XRT86VX38A device's JTAG features comply with the IEEE 1149.1 standard. Please refer to the industry specification for additional information on boundary scan operations.

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
TCK	C10	D8	I	-	**Test clock: Boundary Scan Test clock input:** The TCLK signal is the clock for the TAP controller, and it generates the boundary scan data register clocking. The data on TMS and TDI is loaded on the positive edge of TCK. Data is observed at TDO on the falling edge of TCK.
TMS	B7	A6	I	-	**Test Mode Select:** Boundary Scan Test Mode Select input. The TMS signal controls the transitions of the TAP controller in conjunction with the rising edge of the test clock (TCK). ***NOTE:*** *This pin is internally pulled 'high'*
TDI	A5	C8	I	-	**Test Data In:** Boundary Scan Test data input The TDI signal is the serial test data input. ***NOTE:*** *This pin is internally pulled 'high'.*
TDO	D7	B6	O	8	**Test Data Out:** Boundary Scan Test data output The TDO signal is the serial test data output.
TRST	C9	D7	I	-	**Test Reset Input:** The TRST signal (Active Low) asynchronously resets the TAP controller to the Test-Logic-Reset state. ***NOTE:*** *This pin is internally pulled 'high'*
aTEST	C7	C7	I	-	**Factory Test Mode Pin** ***NOTE:*** *This pin is internally pulled 'low', and should be pulled 'low' for normal operation.*

MICROPROCESSOR INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7	N16 P19 K16 L18 J19 H18 H16 G15	M14 L12 K12 J12 H13 G14 G12 G13	I/O	8	**Bidirectional Microprocessor Data Bus** These pins are used to drive and receive data over the bi-directional data bus, whenever the Microprocessor performs READ or WRITE operations with the Microprocessor Interface of the XRT86VX38A device. When DMA interface is enabled, these 8-bit bidirectional data bus is also used by the T1/E1 Framer or the external DMA Controller for storing and retrieving information.

MICROPROCESSOR INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
$\overline{\text{REQ0}}$	T19	N16	O	8	**DMA Cycle Request Output—DMA Controller 0 (Write)**: These output pins are used to indicate that DMA transfers (Write) are requested by the T1/E1 Framer. On the transmit side (i.e., To transmit data from external DMA controller to HDLC buffers within the XRT86VX38A), DMA transfers are only requested when the transmit buffer status bits indicate that there is space for a complete message or cell. The DMA Write cycle starts by T1/E1 Framer asserting the DMA Request ($\overline{\text{REQ0}}$) 'low', then the external DMA controller should drive the DMA Acknowledge ($\overline{\text{ACK0}}$) 'low' to indicate that it is ready to start the transfer. The external DMA controller should place new data on the Microprocessor data bus each time the Write Signal is Strobed low if the $\overline{\text{WR}}$ is configured as a Write Strobe. If $\overline{\text{WR}}$ is configured as a direction signal, then the external DMA controller would place new data on the Microprocessor data bus each time the Read Signal ($\overline{\text{RD}}$) is Strobed low. The Framer asserts this output pin (toggles it "Low") when at least one of the Transmit HDLC buffers are empty and can receive one more HDLC message. The Framer negates this output pin (toggles it "High") when the HDLC buffer can no longer receive another HDLC message.
$\overline{\text{REQ1}}$	R16	R16	O	8	**DMA Cycle Request Output—DMA Controller 1 (Read):** These output pins are used to indicate that DMA transfers (Read) are requested by the T1/E1 Framer. On the receive side (i.e., To transmit data from HDLC buffers within the XRT86VX38A to external DMA Controller), DMA transfers are only requested when the receive buffer contains a complete message or cell. The DMA Read cycle starts by T1/E1 Framer asserting the DMA Request ($\overline{\text{REQ1}}$) 'low', then the external DMA controller should drive the DMA Acknowledge ($\overline{\text{ACK1}}$) 'low' to indicate that it is ready to receive the data. The T1/E1 Framer should place new data on the Microprocessor data bus each time the Read Signal is Strobed low if the $\overline{\text{RD}}$ is configured as a Read Strobe. If $\overline{\text{RD}}$ is configured as a direction signal, then the T1/E1 Framer would place new data on the Microprocessor data bus each time the Write Signal ($\overline{\text{WR}}$) is Strobed low. The Framer asserts this output pin (toggles it "Low") when one of the Receive HDLC buffer contains a complete HDLC message that needs to be read by the µC/µP. The Framer negates this output pin (toggles it "High") when the Receive HDLC buffers are depleted.

MICROPROCESSOR INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
$\overline{INT}$	J18	H15	O	8	**Interrupt Request Output:** This active-low output signal will be asserted when the XRT86VX38A device is requesting interrupt service from the Microprocessor. This output pin should typically be connected to the “Interrupt Request” input of the Microprocessor. The Framer will assert this active "Low" output (toggles it "Low"), to the local µP, anytime it requires interrupt service.
PCLK	P18	M16	I	-	**Microprocessor Clock Input:** This clock input signal is only used if the Microprocessor Interface has been configured to operate in the Synchronous Modes (e.g., Power PC 403 Mode). If the Microprocessor Interface is configured to operate in this mode, then it will use this clock signal to do the following. **1.** To sample the $\overline{CS}$, $\overline{WR}$/R/$\overline{W}$, A[14:0], D[7:0], $\overline{RD}$/$\overline{DS}$ and DBEN input pins, and **2.** To update the state of the D[7:0] and the RDY/DTACK output signals. ***NOTES:*** *1. This pin is inactive if the user has configured the Microprocessor Interface to operate in either the Intel-Asynchronous or the Motorola-Asynchronous Modes. In this case, the user should tie this pin to GND.* When DMA interface is enabled, the PCLK input pin is also used by the T1/E1 Framer to latch in or latch out receive or output data respectively.
PTYPE0 PTYPE1 PTYPE2	P17 N18 K19	M13 M12 H12	I	-	**Microprocessor Type Input:** These input pins permit the user to specify which type of Microprocessor/Microcontroller to be interfaced to the XRT86VX38A device. The following table presents the three different microprocessor types that the XRT86VX38A supports. **µPType2 / µPType1 / µPType0 / MICROPROCESSOR TYPE** 0 0 0 — 68HC11, 8051, 80C188 0 0 1 — MOTOROLA 68K 1 0 1 — IBM POWER PC 403 ***NOTE:*** *These pins are internally pulled “Low” with a 50kΩ resistor.*

MICROPROCESSOR INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
$\overline{\text{RDY}}$/$\overline{\text{DTACK}}$	M16	L16	O	12	**Ready/Data Transfer Acknowledge Output:** The exact behavior of this pin depends upon the type of Microprocessor/Microcontroller the XRT86VX38A has been configured to operate in, as defined by the PTYPE[2:0] pins. **Intel Asynchronous Mode - $\overline{\text{RDY}}$ - Ready Output** Tis output pin will function as the “active-low” READY output. During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic low level, ONLY when the Microprocessor Interface is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic “low” level, then it is now safe for it to move on and execute the next READ or WRITE cycle. If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic “high” level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic low level. **Motorola Asynchronous Mode - $\overline{\text{DTACK}}$ - Data Transfer Acknowledge Output** Tis output pin will function as the “active-low” DTACK output. During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic low level, ONLY when the Microprocessor Interface is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic “low” level, then it is now safe for it to move on and execute the next READ or WRITE cycle. If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic “high” level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic low level.

MICROPROCESSOR INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
$\overline{\text{RDY}}$/$\overline{\text{DTACK}}$	M16	L16	O	12	**(Con't)** **Power PC 403 Mode - RDY Ready Output:** This output pin will function as the "active-high" READY output. During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic high level, ONLY when the Microprocessor Interface is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has sampled this signal being at the logic "high" level upon the rising edge of PCLK, then it is now safe for it to move on and execute the next READ or WRITE cycle. If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "low" level, then the Microprocessor is expected to extend this READ or WRITE cycle, until it samples this output pin being at the logic low level. ***NOTE:*** *The Microprocessor Interface will update the state of this output pin upon the rising edge of PCLK.*
ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 ADDR5 ADDR6 ADDR7 ADDR8 ADDR9 ADDR10 ADDR11 ADDR12 ADDR13 ADDR14	N19 M17 M18 M15 L16 M19 L17 L19 K15 J16 K18 J15 H15 H19 H17	L13 L14 K15 L11 K13 K16 K14 J15 J14 J13 H14 H16 G16 F16 G11	I	-	**Microprocessor Interface Address Bus Input** These pins permit the Microprocessor to identify on-chip registers and Buffer/Memory locations within the XRT86VX38A device whenever it performs READ and WRITE operations with the XRT86VX38A device. ***NOTE:*** *These pins are internally pulled "Low" with a 50kΩ resistor, except ADDR[8:14].*

MICROPROCESSOR INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
ALE / $\overline{AS}$	K17	J16	I	-	**Address Latch Enable Input Address Strobe** The exact behavior of this pin depends upon the type of Microprocessor/Microcontroller the XRT86VX38A has been configured to operate in, as defined by the PTYPE[2:0] pins. **Intel-Asynchronous Mode - ALE** This active-high input pin is used to latch the address (present at the Microprocessor Interface Address Bus pins (A[14:0]) into the XRT86VX38A Microprocessor Interface block and to indicate the start of a READ or WRITE cycle. Pulling this input pin “high” enables the input bus drivers for the Address Bus input pins (A[14:0]). The contents of the Address Bus will be latched into the XRT86VX38A Microprocessor Interface circuitry, upon the falling edge of this input signal. **Motorola-Asynchronous (68K) Mode - $\overline{AS}$** This active-low input pin is used to latch the data residing on the Address Bus, A[14:0] into the Microprocessor Interface circuitry of the XRT86VX38A device. Pulling this input pin “low” enables the input bus drivers for the Address Bus input pins. The contents of the Address Bus will be latched into the Microprocessor Interface circuitry, upon the falling edge of this signal. **Power PC 403 Mode - No Function -Tie to GND:** This input pin has no role nor function and should be tied to GND.
$\overline{CS}$	G19	F14	I	-	**Microprocessor Interface—Chip Select Input:** The user must assert this active low signal in order to select the Microprocessor Interface for READ and WRITE operations between the Microprocessor and the XRT86VX38A on-chip registers and buffer/memory locations.

MICROPROCESSOR INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
$\overline{RD}$/$\overline{DS}$/$\overline{WE}$	N17	L15	I	-	**Microprocessor Interface—Read Strobe Input:** The exact behavior of this pin depends upon the type of Microprocessor/Microcontroller the Framer has been configured to operate in, as defined by the PTYPE[2:0] pins. **Intel-Asynchronous Mode - $\overline{RD}$ - READ Strobe Input:** This input pin will function as the **$\overline{RD}$** (Active Low Read Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the XRT86VX38A device will place the contents of the addressed register (or buffer location) on the Microprocessor Interface Bi-directional data bus (D[7:0]). When this signal is negated, then the Data Bus will be tri-stated. **Motorola-Asynchronous (68K) Mode - $\overline{DS}$ - Data Strobe:** This input pin will function as the $\overline{DS}$ (Data Strobe) input signal. **Power PC 403 Mode - $\overline{WE}$ - Write Enable Input:** This input pin will function as the $\overline{WE}$ (Write Enable) input pin. Anytime the Microprocessor Interface samples this active-low input signal (along with $\overline{CS}$ and $\overline{WR}$/R/$\overline{W}$) also being asserted (at a logic low level) upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents on the Bi-Directional Data Bus (D[7:0]) into the "target" on-chip register or buffer location within the XRT86VX38A device.
$\overline{WR}$ / R/$\overline{W}$	G17	F13	I	-	**Microprocessor Interface—Write Strobe Input** The exact behavior of this pin depends upon the type of Microprocessor/Microcontroller the XRT86VX38A has been configured to operate in, as defined by the PTYPE[2:0] pins. **Intel-Asynchronous Mode - $\overline{WR}$ - Write Strobe Input:** This input pin functions as the $\overline{WR}$ (Active Low WRITE Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the input buffers (associated with the Bi-Directional Data Bus pin, D[7:0]) will be enabled. The Microprocessor Interface will latch the contents on the Bi-Directional Data Bus (into the "target" register or address location, within the XRT86VX38A) upon the rising edge of this input pin. **Motorola-Asynchronous Mode - R/$\overline{W}$ - Read/Write Operation Identification Input Pin:** This pin is functionally equivalent to the "R/$\overline{W}$" input pin. In the Motorola Mode, a "READ" operation occurs if this pin is held at a logic "1", coincident to a falling edge of the RD/$\overline{DS}$ (Data Strobe) input pin. Similarly a WRITE operation occurs if this pin is at a logic "0", coincident to a falling edge of the RD/$\overline{DS}$ (Data Strobe) input pin.

MICROPROCESSOR INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
$\overline{WR}$ / R/$\overline{W}$	G17	F13	I	-	**(Con't)** **Power PC 403 Mode - R/$\overline{W}$ - Read/Write Operation Identification Input:** This input pin will function as the "Read/Write Operation Identification Input" pin. Anytime the Microprocessor Interface samples this input signal at a logic "High" (while also sampling the $\overline{CS}$ input pin "Low") upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents of the Address Bus (A[14:0]) into the Microprocessor Interface circuitry, in preparation for this forthcoming READ operation. At some point (later in this READ operation) the Microprocessor will also assert the $\overline{DBEN/OE}$ input pin, and the Microprocessor Interface will then place the contents of the "target" register (or address location within the XRT86VX38A device) upon the Bi-Directional Data Bus pins (D[7:0]), where it can be read by the Microprocessor. Anytime the Microprocessor Interface samples this input signal at a logic "Low" (while also sampling the $\overline{CS}$ input pin a logic "Low") upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents of the Address Bus (A[14:0]) into the Microprocessor Interface circuitry, in preparation for the forthcoming WRITE operation. At some point (later in this WRITE operation) the Microprocessor will also assert the $\overline{RD/DS/WE}$ input pin, and the Microprocessor Interface will then latch the contents of the Bi-Directional Data Bus (D[7:0]) into the contents of the "target" register or buffer location (within the XRT86VX38A).

MICROPROCESSOR INTERFACE

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	OUTPUT DRIVE (MA)	DESCRIPTION
$\overline{ACK0}$ $\overline{ACK1}$	T18 R19	N15 M15	I	-	**DMA Cycle Acknowledge Input—DMA Controller 0 (Write):** The external DMA Controller will assert this input pin "Low" when the following two conditions are met: **1.** After the DMA Controller, within the Framer has asserted (toggled "Low"), the Req_0 output signal. **2.** When the external DMA Controller is ready to transfer data from external memory to the selected Transmit HDLC buffer. At this point, the DMA transfer between the external memory and the selected Transmit HDLC buffer may begin. After completion of the DMA cycle, the external DMA Controller will negate this input pin after the DMA Controller within the Framer has negated the $\overline{Req\_0}$ output pin. The external DMA Controller must do this in order to acknowledge the end of the DMA cycle. **DMA Cycle Acknowledge Input—DMA Controller 1 (Read):** The external DMA Controller asserts this input pin "Low" when the following two conditions are met: **1.** After the DMA Controller, within the Framer has asserted (toggled "Low"), the Req_1 output signal. **2.** When the external DMA Controller is ready to transfer data from the selected Receive HDLC buffer to external memory. At this point, the DMA transfer between the selected Receive HDLC buffer and the external memory may begin. After completion of the DMA cycle, the external DMA Controller will negate this input pin after the DMA Controller within the Framer has negated the $\overline{Req\_1}$ output pin. The external DMA Controller will do this in order to acknowledge the end of the DMA cycle. ***NOTE:*** *This pin is internally pulled "High" with a 50kΩ resistor.*
$\overline{RESET}$	V4	R4	I	-	**Hardware Reset Input** $\overline{Reset}$ is an active low input. If this pin is pulled "Low" for more than 10μS, the device will be reset. When this occurs, all output will be 'tri-stated', and all internal registers will be reset to their default values.

POWER SUPPLY PINS (3.3V)

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	DESCRIPTION
VDD	A1 A12 A19 B6 B9 E16 F5 J17 P16 R11 R13 R15 R18 T7 U4 V1 W11 W15	A16 E8 E11 G15 M6 M9 N14 T16	PWR	**Framer Block Power Supply (I/O)**
RVDD	C2 E2 G1 J2 L2 N2 P4 U2	B2 D2 F2 H2 K2 M2 P2 T1	PWR	**Receiver Analog Power Supply for LIU Section**
TVDD	D4 G4 J4 K5 M4 N5 R3 T4	D4 F4 F5 H5 K4 K5 M5 N4	PWR	**Transmitter Analog Power Supply for LIU Section**

POWER SUPPLY PINS (1.8V)

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	DESCRIPTION
VDD18	D13 E6 E8 E9 E11 E12 E13 E15 F15 G5 G7 G9 G11 G13 J5 J7 J13 L7 L13 L15 M5 N7 N9 N11 N13 P15 R9 R10 R12 R14 T6	F8 F9 F10 G6 H6 H11 J6 J11 K6 K11 L7 L8 L9 L10	PWR	**Framer Block Power Supply**
DVDD18	B4	C6	PWR	**Digital Power Supply for LIU Section**
AVDD18	D6	C5	PWR	**Analog Power Supply for LIU Section**
VDDPLL18	A2 B2 B3 C4	A3 A4 B3 D5	PWR	**Analog Power Supply for PLL**

GROUND PINS

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	DESCRIPTION
VSS	A3, A6 A15, C5 E7, F2 G8, G10 G12, H5 H7, H8 H9, H10 H11, H12 H13, J8 J9, J10 J11, J12 K7, K8 K9, K10 K11, K12 K13, L8 L9, L10 L11, L12 M7, M8 M9, M10 M11, M12 M13, N8 N10, N12 N15, P2 R6, U12 W1, W19	E7 E9 F6 F7 G7 G8 G9 G10 H7 H8 H9 H10 J7 J8 J9 J10 K7 K8 K9 K10	GND	**Framer Block Ground**
DGND	A4	D6	GND	**Digital Ground for LIU Section**
AGND	C6	B5	GND	**Analog Ground for LIU Section**
RGND	D2 G2 H2 K2 M2 R2 T2 V3	C2 E2 G2 J2 L2 N2 R2 R3	GND	**Receiver Analog Ground for LIU Section**
TGND	E4 G3 J3 L5 M3 P3 P5 V2	E5 F3 G5 J5 K3 L5 N3 N5	GND	**Transmitter Analog Ground for LIU Section**

GROUND PINS

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	DESCRIPTION
GNDPLL	B1 C3 D5	A1 A2 C4	GND	**Analog Ground for PLL**

NO CONNECT PINS

SIGNAL NAME	329 PKG BALL#	256 PKG BALL #	TYPE	DESCRIPTION
NC	F6 F7 F8 F9 F10 F11 F12 F13 F14 G6 G14 H6 H14 J6 J14 K6 K14 L6 L14 M6 M14 N6 N14 P6 P7 P8 P9 P10 P11 P12 P13 P14		NC	**No Connection**

ELECTRICAL CHARACTERISTICS

Absolute Maximums

Power Supply..... VDD_{IO} .. .. -0.5V to +3.465V VDD_{CORE}.....-0.5V to +1.890V		Power Rating fpBGA Package..... 2.4
Storage Temperature .....-65°C to 150°C		Input Logic Signal Voltage (Any Pin) .....-0.5V to + 5.5V
Operating Temperature Range.....-40°C to 85°C		ESD Protection (HBM).....>2000V
Supply Voltage ..... GND-0.5V to +VDD + 0.5V		Input Current (Any Pin) ..... ± 100mA

DC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25°C, VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{LL}	Data Bus Tri-State Bus Leakage Current	-10		+10	µA	
V_{IL}	Input Low voltage			0.8	V	
V_{IH}	Input High Voltage	2.0		VDD	V	
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = -1.6mA
VOH	Output High Voltage	2.4		VDD	V	I_{OH} = 40µA
I_{OC}	Open Drain Output Leakage Current				µA	
I_{IH}	Input High Voltage Current	-10		10	µA	V_{IH} = VDD
I_{IL}	Input Low Voltage Current	-10		10	µA	V_{IL} = GND

XRT86VX38A POWER CONSUMPTION

Test Conditions: TA = 25°C, VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, Internal termination, unless otherwise specified

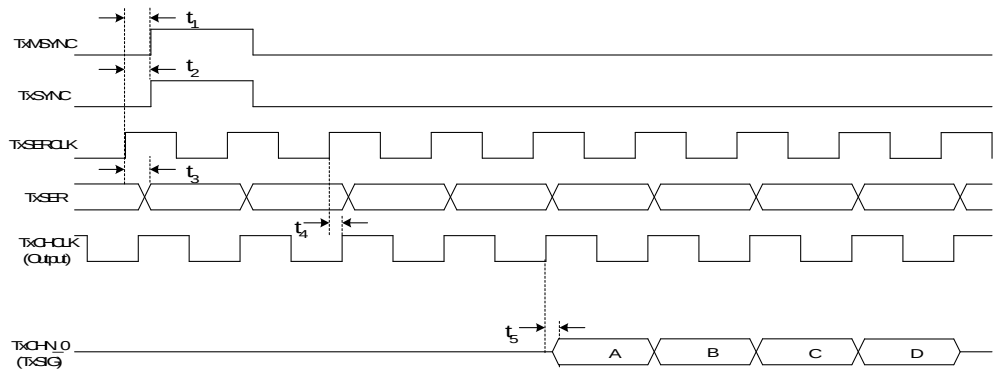
MODE	IMPEDANCE	MIN.	TYP.	MAX.	UNITS	CONDITIONS
T1	100Ω		2.02 1.54		W	All ones Pattern PRBS Pattern
E1	75Ω		1.95 1.57		W	All ones Pattern PRBS Pattern
E1	120Ω		1.77 1.44		W	All ones Pattern PRBS Pattern

NOTE: There are NO power sequence requirements on this device. The VDD_{IO} or VDD_{CORE} are independent and do not have any special timing restrictions.

AC ELECTRICAL CHARACTERISTICS TRANSMIT FRAMER (BASE RATE/NON-MUX)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_1	TxSERCLK to TxMSYNC delay			234	nS	
t_2	TxSERCLK to TxSYNC delay			230	nS	
t_3	TxSERCLK to TxSER data delay			230	nS	
t_4	Rising Edge of TxSERCLK to Rising Edge of TxCH-CLK			13	nS	
t_5	TxSERCLK to TxSIG delay			230	nS	

FIGURE 2. FRAMER SYSTEM TRANSMIT TIMING DIAGRAM (BASE RATE/NON-MUX)



AC ELECTRICAL CHARACTERISTICS RECEIVE FRAMER (BASE RATE/NON-MUX)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RxSERCLK as an Output						
t_8	Rising Edge of RxSERCLK to Rising Edge of RxCASYNC			4	nS	
t_9	Rising Edge of RxSERCLK to Rising Edge of RxCRCSYNC			4	nS	
t_{10}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Output)			4	nS	
t_{11}	Rising Edge of RxSERCLK to Rising Edge of RxSER			6	nS	
RxSERCLK as an Input						

AC ELECTRICAL CHARACTERISTICS RECEIVE FRAMER (BASE RATE/NON-MUX)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{13}	Rising Edge of RxSERCLK to Rising Edge of RxCASYNC			8	nS	
t_{14}	Rising Edge of RxSERCLK to Rising Edge of RxCRCSYNC			8	nS	
t_{15}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Output)			10	nS	
t_{15}	Rising Edge of RxSERCLK to Rising Edge of RxSYNC (RxSYNC as Input)			230	nS	
t_{16}	Rising Edge of RxSERCLK to Rising Edge of RxSER			10	nS	

FIGURE 3. FRAMER SYSTEM RECEIVE TIMING DIAGRAM (RXSERCLK AS AN OUTPUT)

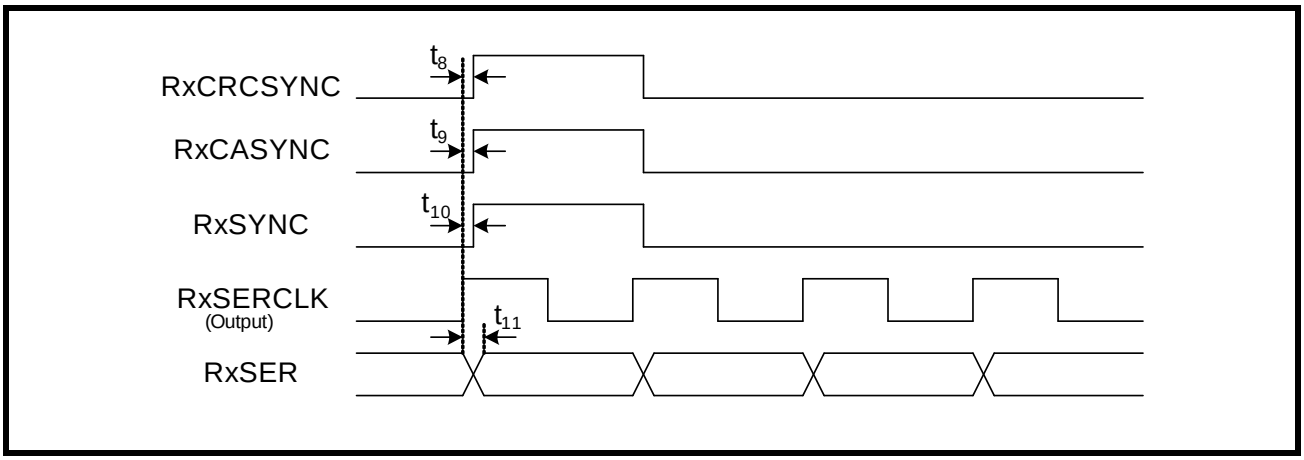
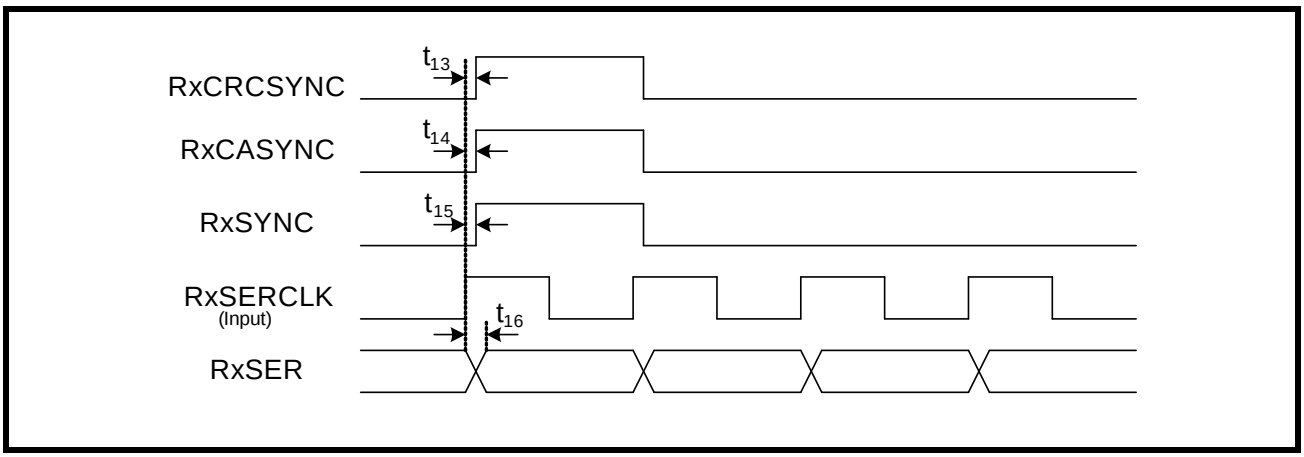


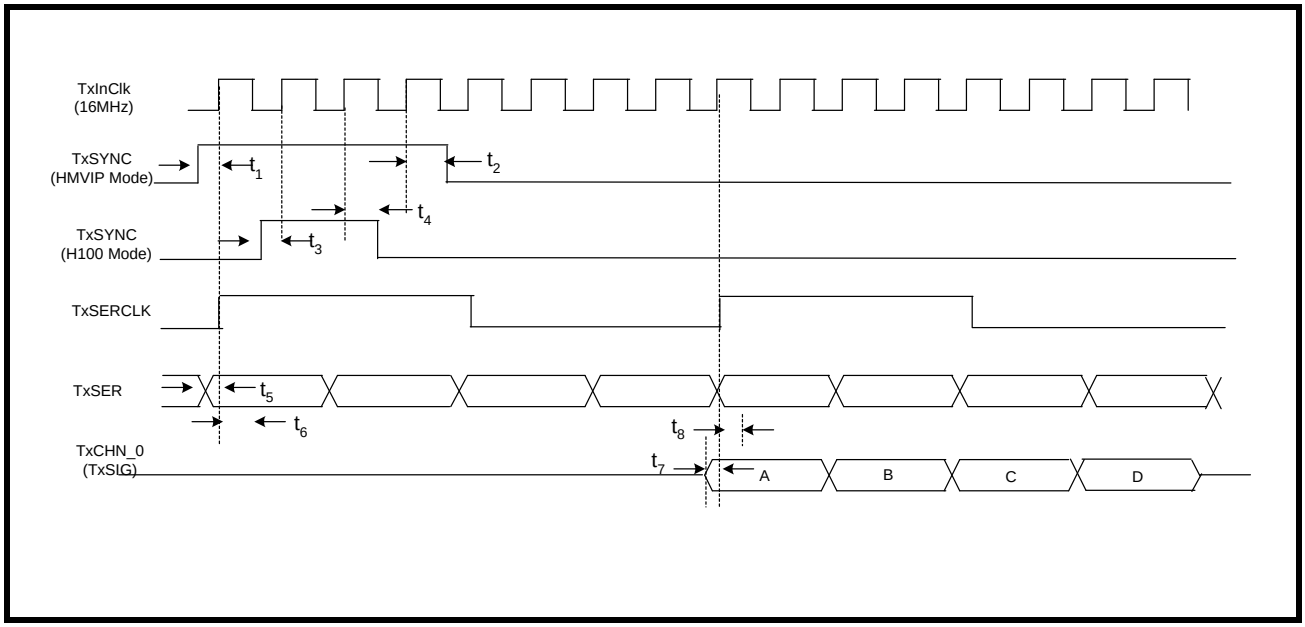
FIGURE 4. FRAMER SYSTEM RECEIVE TIMING DIAGRAM (RXSERCLK AS AN INPUT)



AC ELECTRICAL CHARACTERISTICS TRANSMIT FRAMER (HMVIP/H100 MODE)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_1	TxSYNC Setup Time - HMVIP Mode	7			nS	
t_2	TxSYNC Hold Time - HMVIP Mode	4			nS	
t_3	TxSYNC Setup Time - H100 Mode	7			nS	
t_4	TxSYNC Hold Time - H100 Mode	4			nS	
t_5	TxSER Setup Time - HMVIP and H100 Mode	6			nS	
t_6	TxSER Hold Time - HMVIP and H100 Mode	3			nS	
t_7	TxSIG Setup Time - HMVIP and H100 Mode	6			nS	
t_8	TxSIG Hold Time - HMVIP and H100 Mode	3			nS	

FIGURE 5. FRAMER SYSTEM TRANSMIT TIMING DIAGRAM (HMVIP AND H100 MODE)



NOTE: *Setup and Hold time is not valid from TxInClk to TxSERCLK as TxInClk is used as the timing source for the back plane interface and TxSERCLK is used as the timing source on the line side.*

AC ELECTRICAL CHARACTERISTICS RECEIVE FRAMER (HMVIP/H100 MODE)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_1	RxSYNC Setup Time - HMVIP Mode	4			nS	
t_2	RxSYNC Hold Time - HMVIP Mode	3			nS	
t_3	RxSYNC Setup Time - H100 Mode	5			nS	
t_4	RxSYNC Hold Time - H100 Mode	3			nS	
t_5	Rising Edge of RxSERCLK to Rising Edge of RxSER delay			11	nS	

NOTE: *Both RxSERCLK and RxSYNC are inputs*

FIGURE 6. FRAMER SYSTEM RECEIVE TIMING DIAGRAM (HMVIP/H100 MODE)

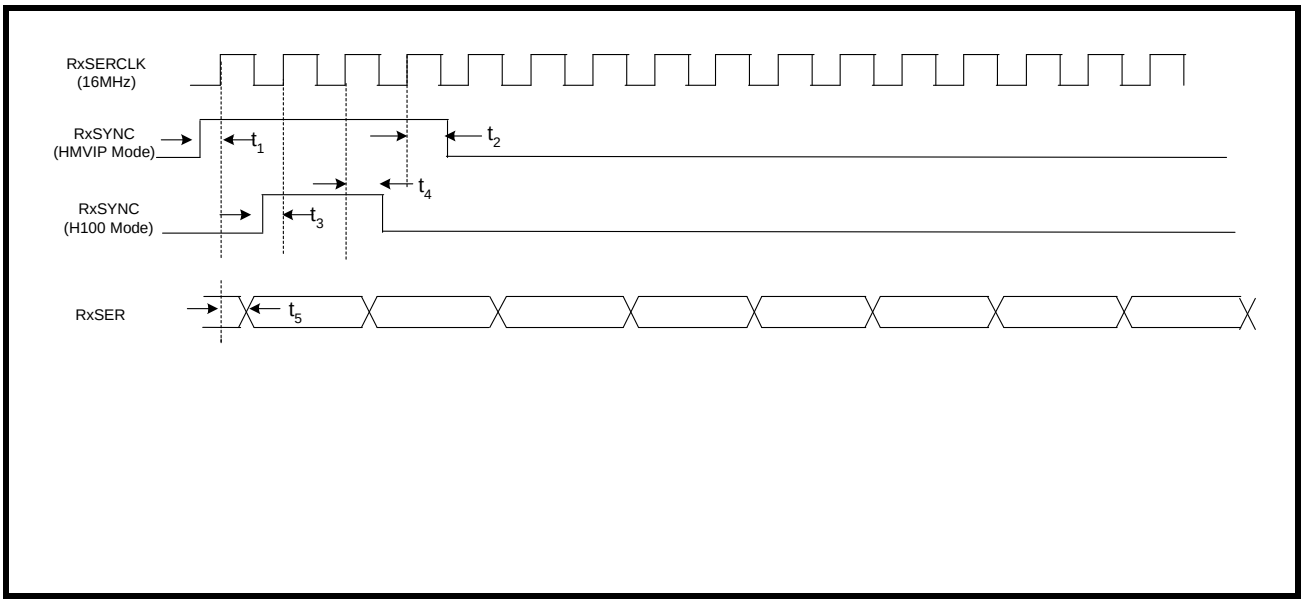


TABLE 4: E1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A= -40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Receiver loss of signal: Number of consecutive zeros before RLOS is set Input signal level at RLOS RLOS De-asserted	 15 12.5	 32 20		 dB % ones	Cable attenuation @1024kHz ITU-G.775, ETSI 300 233
Receiver Sensitivity (Short Haul with cable loss)	11			dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application.
Receiver Sensitivity (Long Haul with cable loss)	0		43	dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application.
Input Impedance		15		kΩ	
Input Jitter Tolerance: 1 Hz 10kHz-100kHz	 37 0.3			 UIpp UIpp	 ITU G.823
Recovered Clock Jitter Transfer Corner Frequency Peaking Amplitude	 -	 20	 0.5	 kHz dB	 ITU G.736
Jitter Attenuator Corner Frequency (-3dB curve) (JABW=0) (JABW=1)	-	10 1.5	-	Hz Hz	ITU G.736
Return Loss: 51kHz - 102kHz 102kHz - 2048kHz 2048kHz - 3072kHz	 12 8 8	 -	 -	 dB dB dB	 ITU-G.703

TABLE 5: T1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Receiver loss of signal:					
Number of consecutive zeros before RLOS is set		175			
Input signal level at RLOS	15	20	-	dB	Cable attenuation @772kHz
RLOS Clear	12.5	-	-	% ones	ITU-G.775, ETSI 300 233
Receiver Sensitivity (Short Haul with cable loss)	12	-		dB	With nominal pulse amplitude of 3.0V for 100Ω termination
Receiver Sensitivity (Long Haul with cable loss)		-			With nominal pulse amplitude of 3.0V for 100Ω termination
Normal	0		36	dB	
Extended	0		45	dB	
Input Impedance		15	-	kΩ	
Jitter Tolerance:					
1Hz	138	-	-	UIpp	AT&T Pub 62411
10kHz - 100kHz	0.4	-	-		
Recovered Clock Jitter					
Transfer Corner Frequency	-	10	-	KHz	TR-TSY-000499
Peaking Amplitude	-		0.1	dB	
Jitter Attenuator Corner Frequency (-3dB curve)	-	6		Hz	AT&T Pub 62411
Return Loss:					
51kHz - 102kHz	-	14	-	dB	
102kHz - 2048kHz	-	20	-	dB	
2048kHz - 3072kHz	-	16	-	dB	

TABLE 6: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
AMI Output Pulse Amplitude:					1:2 transformer
75Ω Application	2.13	2.37	2.60	V	
120Ω Application	2.70	3.00	3.30	V	
Output Pulse Width	224	244	264	ns	
Output Pulse Width Ratio	0.95	-	1.05	-	ITU-G.703
Output Pulse Amplitude Ratio	0.95	-	1.05	-	ITU-G.703

TABLE 6: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Jitter Added by the Transmitter Output	-	0.025	0.05	UIpp	Broad Band with jitter free TCLK applied to the input.
Output Return Loss: 51kHz -102kHz 102kHz-2048kHz 2048kHz-3072kHz	 15 9 8	 - - -	 - - -	 dB dB dB	 ETSI 300 166

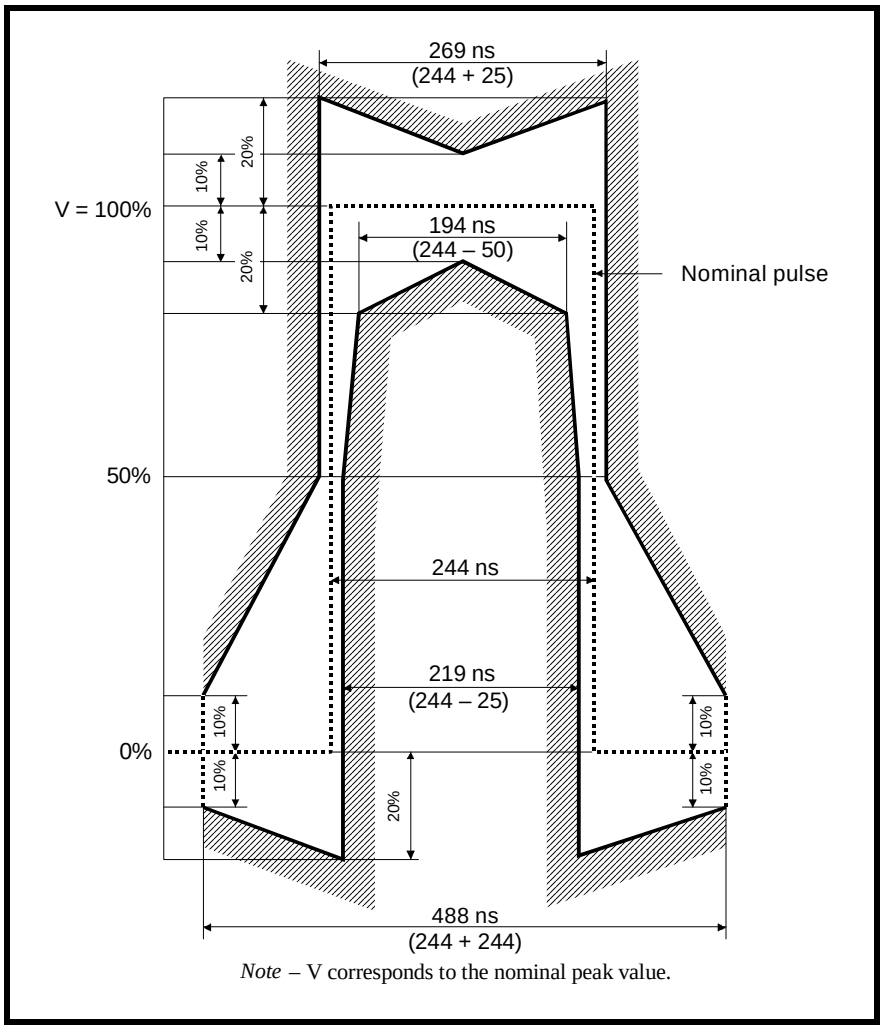
TABLE 7: E1 TRANSMIT RETURN LOSS REQUIREMENT

FREQUENCY	RETURN LOSS ETS 300166
51-102kHz	6dB
102-2048kHz	8dB
2048-3072kHz	8dB

TABLE 8: T1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=-40° to 85°C, unless otherwise specified					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
AMI Output Pulse Amplitude:	2.4	3.0	3.60	V	1:2 transformer measured at DSX-1.
Output Pulse Width	338	350	362	ns	ANSI T1.102
Output Pulse Width Imbalance	-	-	20	-	ANSI T1.102
Output Pulse Amplitude Imbalance	-	-	±200	mV	ANSI T1.102
Jitter Added by the Transmitter Output	-	0.025	0.05	UIpp	Broad Band with jitter free TCLK applied to the input.
Output Return Loss: 51kHz -102kHz 102kHz-2048kHz 2048kHz-3072kHz	 - - -	 17 12 10	 - - -	 dB dB dB	

FIGURE 7. ITU G.703 PULSE TEMPLATE



Note – V corresponds to the nominal peak value.

TABLE 9: TRANSMIT PULSE MASK SPECIFICATION

Test Load Impedance	75Ω Resistive (Coax)	120Ω Resistive (twisted Pair)
Nominal Peak Voltage of a Mark	2.37V	3.0V
Peak voltage of a Space (no Mark)	0 ± 0.237V	0 ± 0.3V
Nominal Pulse width	244ns	244ns
Ratio of Positive and Negative Pulses Imbalance	0.95 to 1.05	0.95 to 1.05

FIGURE 8. ITU G.703 SECTION 13 SYNCHRONOUS INTERFACE PULSE TEMPLATE

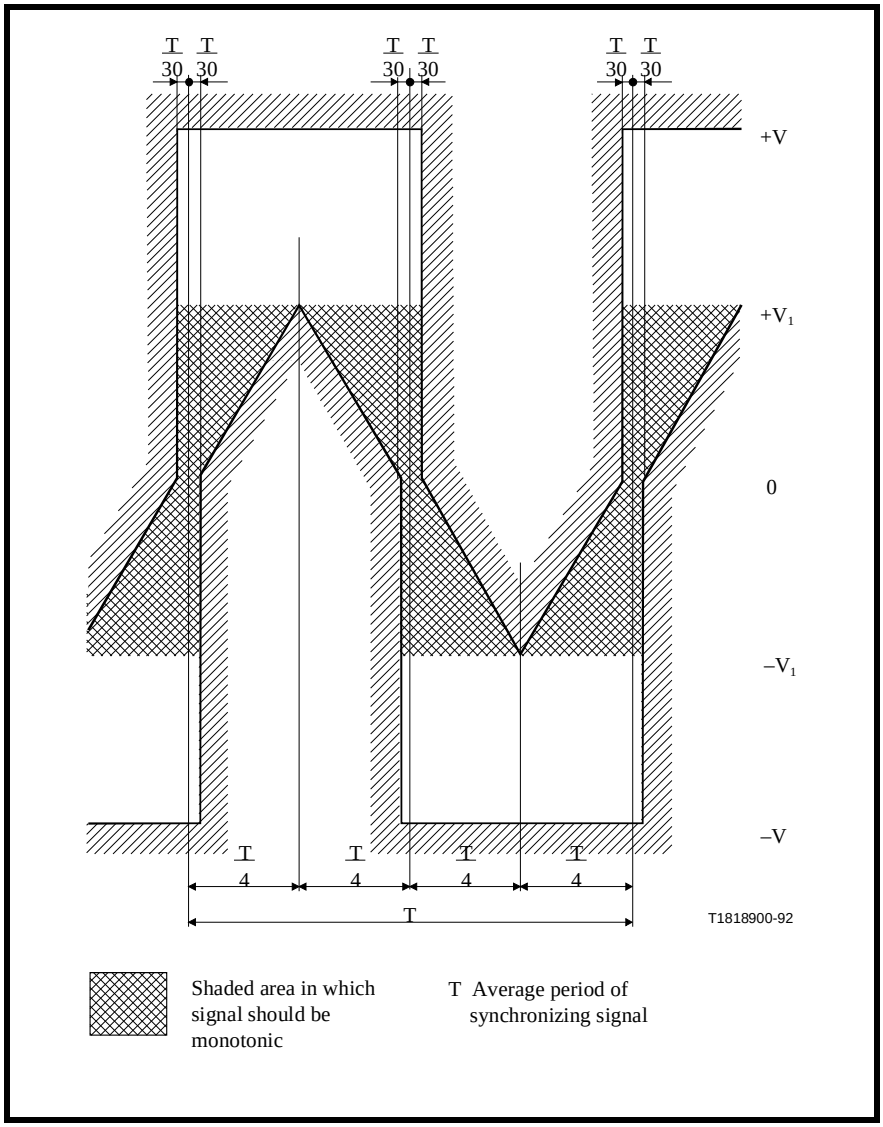


TABLE 10: E1 SYNCHRONOUS INTERFACE TRANSMIT PULSE MASK SPECIFICATION

Test Load Impedance	75Ω Resistive (Coax)	120Ω Resistive (twisted Pair)
Maximum Peak Voltage of a Mark	1.5V	1.9V
Minimum Peak Voltage of a Mark	0.75V	1.0V
Nominal Pulse width	244ns	244ns

FIGURE 9. DSX-1 PULSE TEMPLATE (NORMALIZED AMPLITUDE)

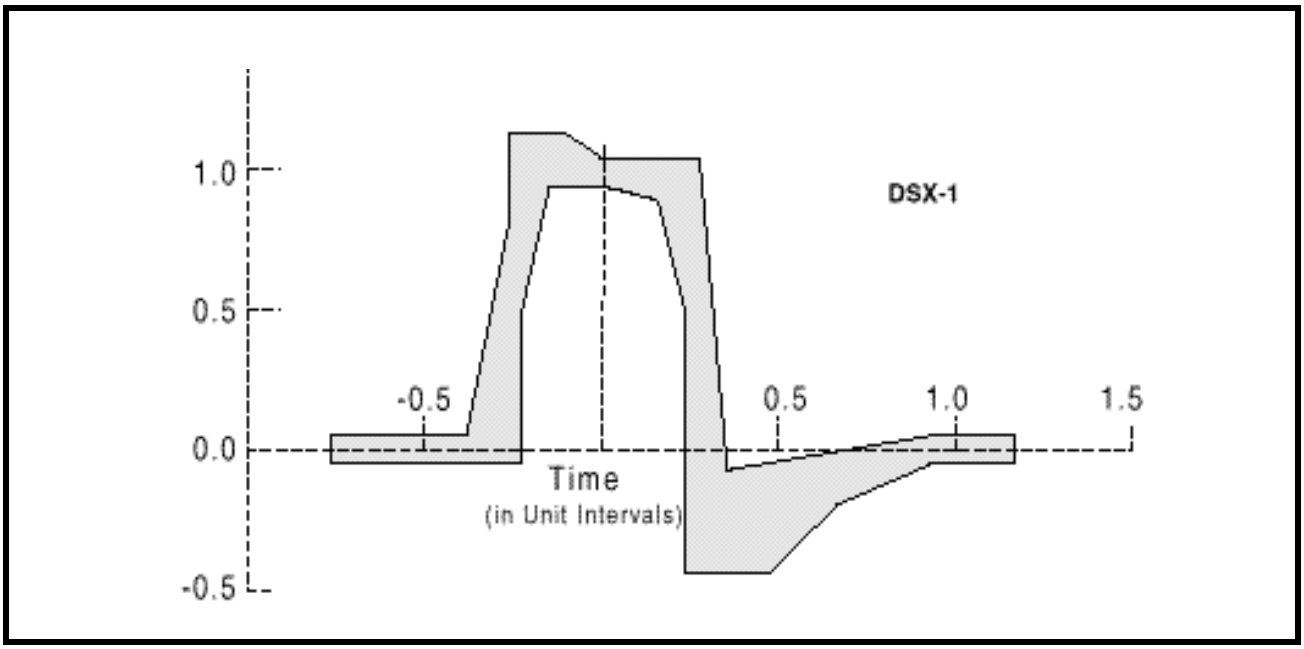


TABLE 11: DSX1 INTERFACE ISOLATED PULSE MASK AND CORNER POINTS

MINIMUM CURVE		MAXIMUM CURVE	
TIME (UI)	NORMALIZED AMPLITUDE	TIME (UI)	NORMALIZED AMPLITUDE
-0.77	-.05V	-0.77	.05V
-0.23	-.05V	-0.39	.05V
-0.23	0.5V	-0.27	.8V
-0.15	0.95V	-0.27	1.15V
0.0	0.95V	-0.12	1.15V
0.15	0.9V	0.0	1.05V
0.23	0.5V	0.27	1.05V
0.23	-0.45V	0.35	-0.07V
0.46	-0.45V	0.93	0.05V
0.66	-0.2V	1.16	0.05V
0.93	-0.05V		
1.16	-0.05V		

TABLE 12: AC ELECTRICAL CHARACTERISTICS

VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, TA=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
MCLKIN Clock Duty Cycle		40	-	60	%
MCLKIN Clock Tolerance		-	±50	-	ppm

MICROPROCESSOR INTERFACE I/O TIMING

INTEL INTERFACE TIMING - ASYNCHRONOUS

The signals used for the Intel microprocessor interface are: Address Latch Enable (ALE), Read Enable ($\overline{RD}$), Write Enable ($\overline{WR}$), Chip Select ($\overline{CS}$), Address and Data bits. The microprocessor interface uses minimum external glue logic and is compatible with the timings of the 8051 or 80188 family of microprocessors. The ALE signal can be tied 'HIGH' if this signal is not available, and the corresponding timing interface is shown in **Figure 11** and **Table 14.**

FIGURE 10. INTEL µP INTERFACE TIMING DURING PROGRAMMED I/O READ AND WRITE OPERATIONS WHEN ALE IS NOT TIED 'HIGH'

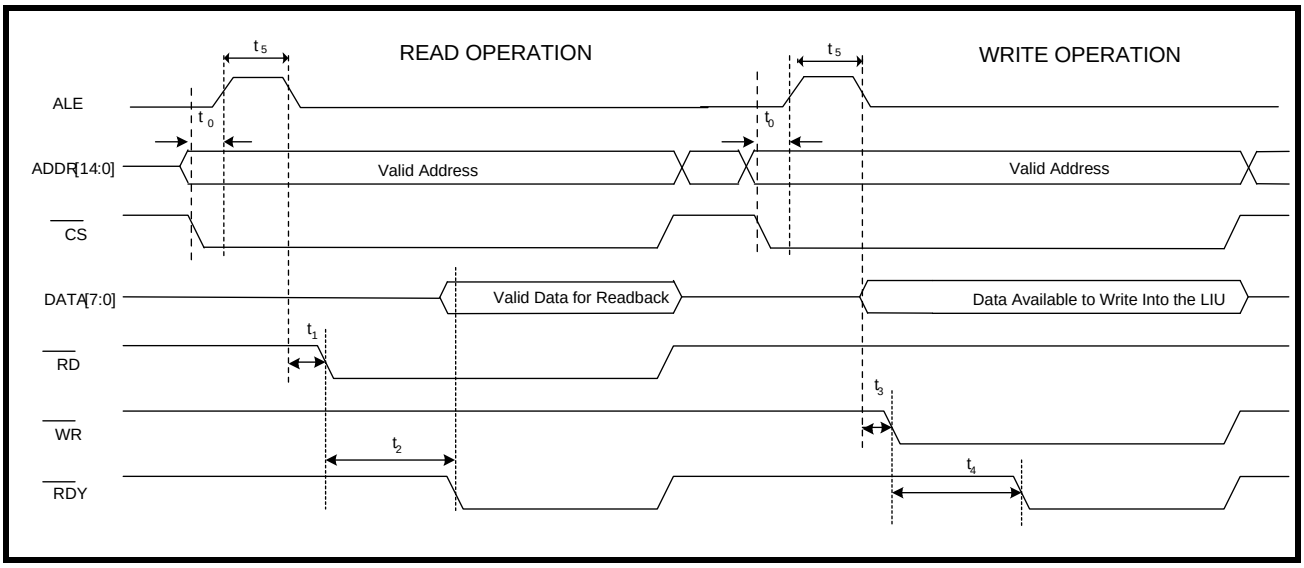


TABLE 13: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge and ALE Rising Edge	0	-	ns
t_1	ALE Falling Edge to $\overline{RD}$ Assert	5	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	320	ns
NA	$\overline{RD}$ Pulse Width (t_2)	320	-	ns
t_3	ALE Falling Edge to $\overline{WR}$ Assert	5	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	320	ns
NA	$\overline{WR}$ Pulse Width (t_4)	320	-	ns
t_5	ALE Pulse Width(t_5)	10		ns

FIGURE 11. INTEL µP INTERFACE TIMING DURING PROGRAMMED I/O READ AND WRITE OPERATIONS WHEN ALE IS TIED 'HIGH'

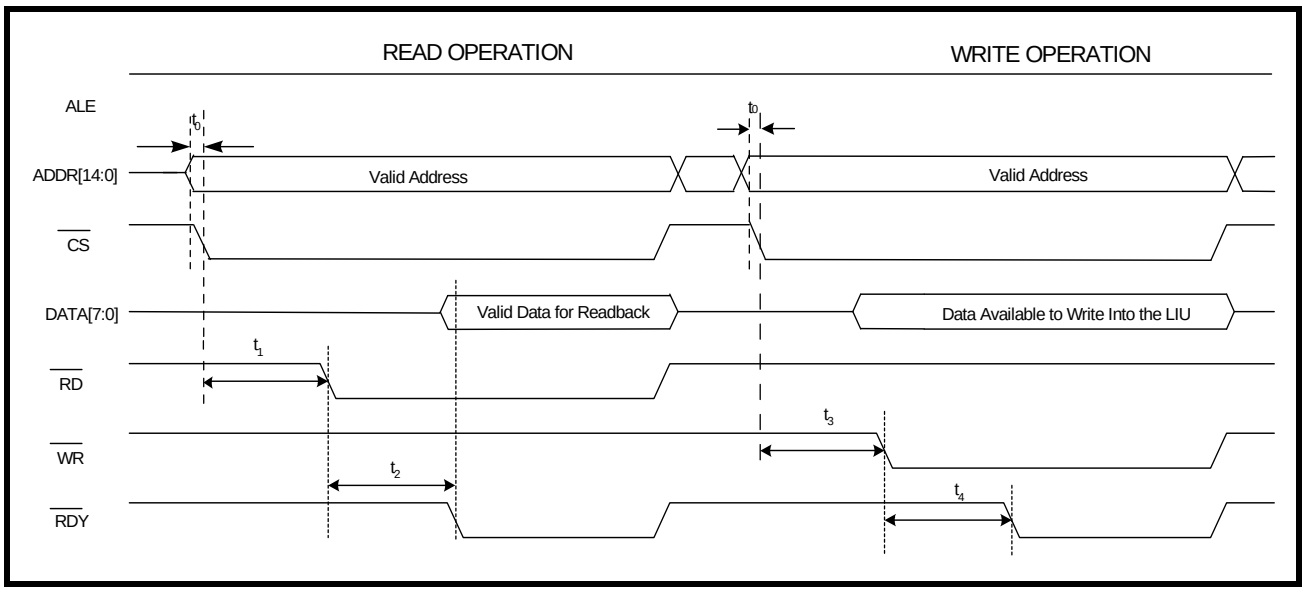


TABLE 14: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{RD}$ Assert	0	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	320	ns
NA	$\overline{RD}$ Pulse Width (t_2)	320	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{WR}$ Assert	0	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	320	ns
NA	$\overline{WR}$ Pulse Width (t_4)	320	-	ns

MOTOROLA ASYNCHRONOUS INTERFACE TIMING

The signals used in the Motorola microprocessor interface mode are: Address Strobe (AS), Data Strobe ($\overline{DS}$), Read/Write Enable (R/$\overline{W}$), Chip Select ($\overline{CS}$), Address and Data bits. The interface is compatible with the timing of a Motorola 68000 microprocessor family. The interface timing is shown in **Figure 12**. The I/O specifications are shown in **Table 15**.

FIGURE 12. MOTOROLA ASYNCHRONOUS MODE INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

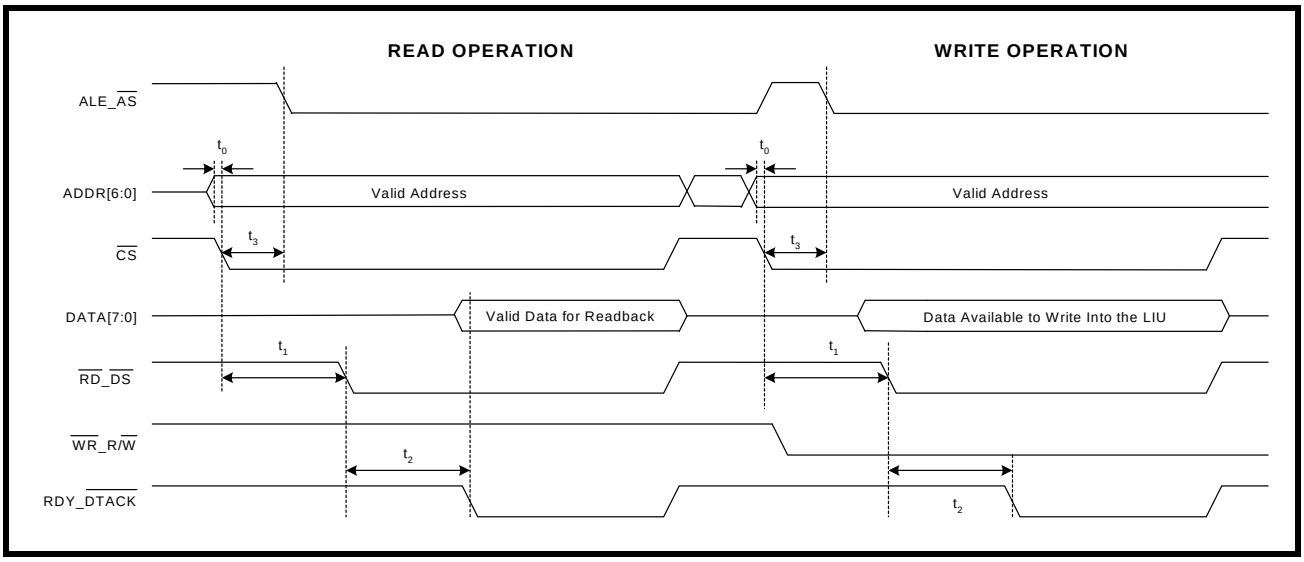


TABLE 15: MOTOROLA ASYNCHRONOUS MODE MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{DS}$ (Pin $\overline{RD}\_\overline{DS}$) Assert	0	-	ns
t_2	$\overline{DS}$ Assert to $\overline{DTACK}$ Assert	-	320	ns
NA	$\overline{DS}$ Pulse Width (t_2)	320	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{AS}$ (Pin ALE_AS) Falling Edge	0	-	ns

POWER PC 403 SYCHRONOUS INTERFACE TIMING

The signals used in the Power PC 403 Synchronus microprocessor interface mode are: Address Strobe (AS), Microprocessor Clock (uPCLK), Data Strobe ($\overline{DS}$), Read/Write Enable (R/$\overline{W}$), Chip Select ($\overline{CS}$), Address and Data bits. The interface timing is shown in **Figure 13**. The I/O specifications are shown in **Table 16**.

FIGURE 13. POWER PC 403 INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

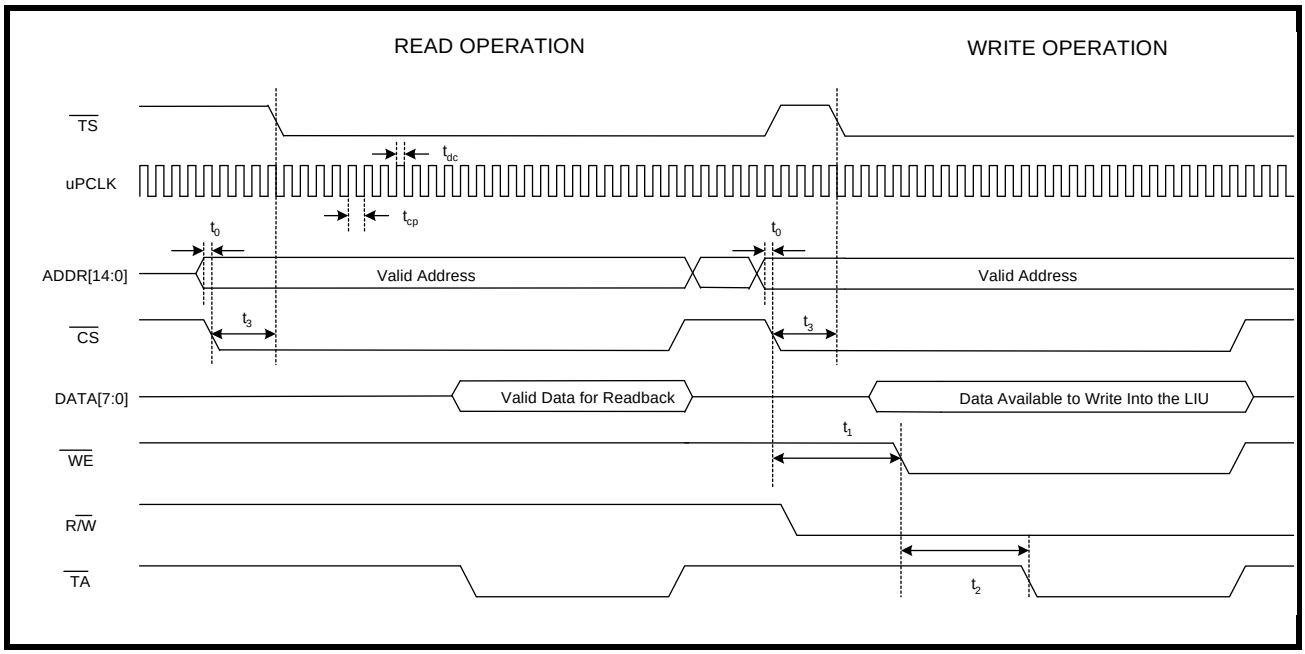


TABLE 16: POWER PC 403 MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

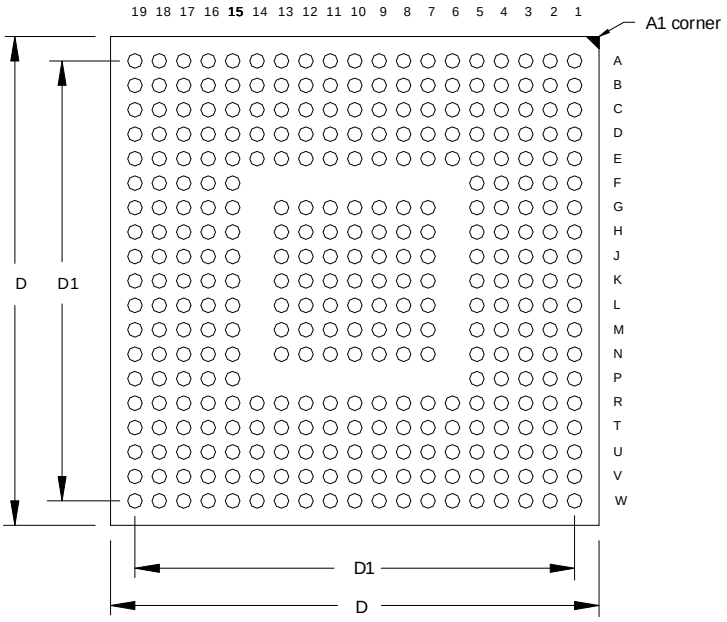
SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{WE}$ Assert	0	-	ns
t_2	$\overline{WE}$ Assert to $\overline{TA}$ Assert	-	320	ns
NA	$\overline{WE}$ Pulse Width (t_2)	320	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{TS}$ Falling Edge	0	-	
t_{dc}	µPCLK Duty Cycle	40	60	%
t_{cp}	µPCLK Clock Period	20	-	ns

ORDERING INFORMATION

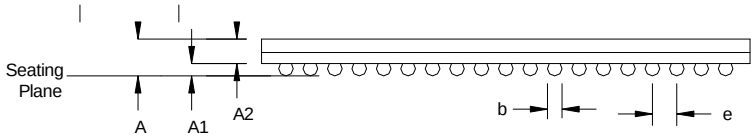
PRODUCT NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86VX38AIB329	329 Fine Pitch Ball Grid Array	-40°C to +85°C
XRT86VX38AIB256	256 Fine Pitch Ball Grid Array	-40°C to +85°C

PACKAGE DIMENSIONS FOR 329 FINE PITCH BALL GRID ARRAY

329 Fine Pitch Ball Grid Array
(17.0 mm x 17.0 mm, fpBGA)
Rev. 1.00



(A1 corner feature is mfger option)

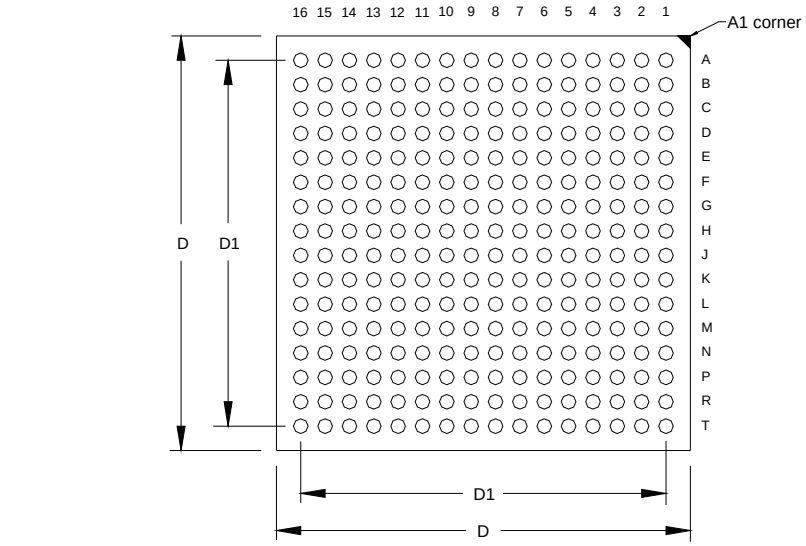


Note: The control dimension is in millimeter.

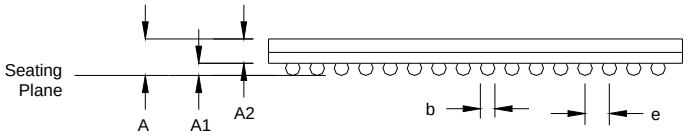
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.056	0.067	1.43	1.71
A1	0.010	0.014	0.26	0.36
A2	0.046	0.053	1.17	1.35
D	0.663	0.675	16.85	17.15
D1	0.567 BSC		14.40 BSC	
b	0.014	0.018	0.36	0.46
e	0.031 BSC		0.80 BSC	

PACKAGE DIMENSIONS FOR 256 FINE PITCH BALL GRID ARRAY

256 Fine Pitch Ball Grid Array
(17.0 mm x 17.0 mm, fpBGA)
Rev. 1.00



(A1 corner feature is mfger option)



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.058	0.070	1.48	1.78
A1	0.013	0.017	0.33	0.43
A2	0.045	0.053	1.15	1.35
D	0.661	0.677	16.80	17.20
D1	0.591 BSC		15.00 BSC	
b	0.020	0.024	0.50	0.60
e	0.039 BSC		1.00 BSC	

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Datasheet July 2013.

Send your technical inquiry with technical details to our email hotline: commtechsupport@exar.com.

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
1.0.0	July 2013	Initial release of XRT86VX38A Hardware Description