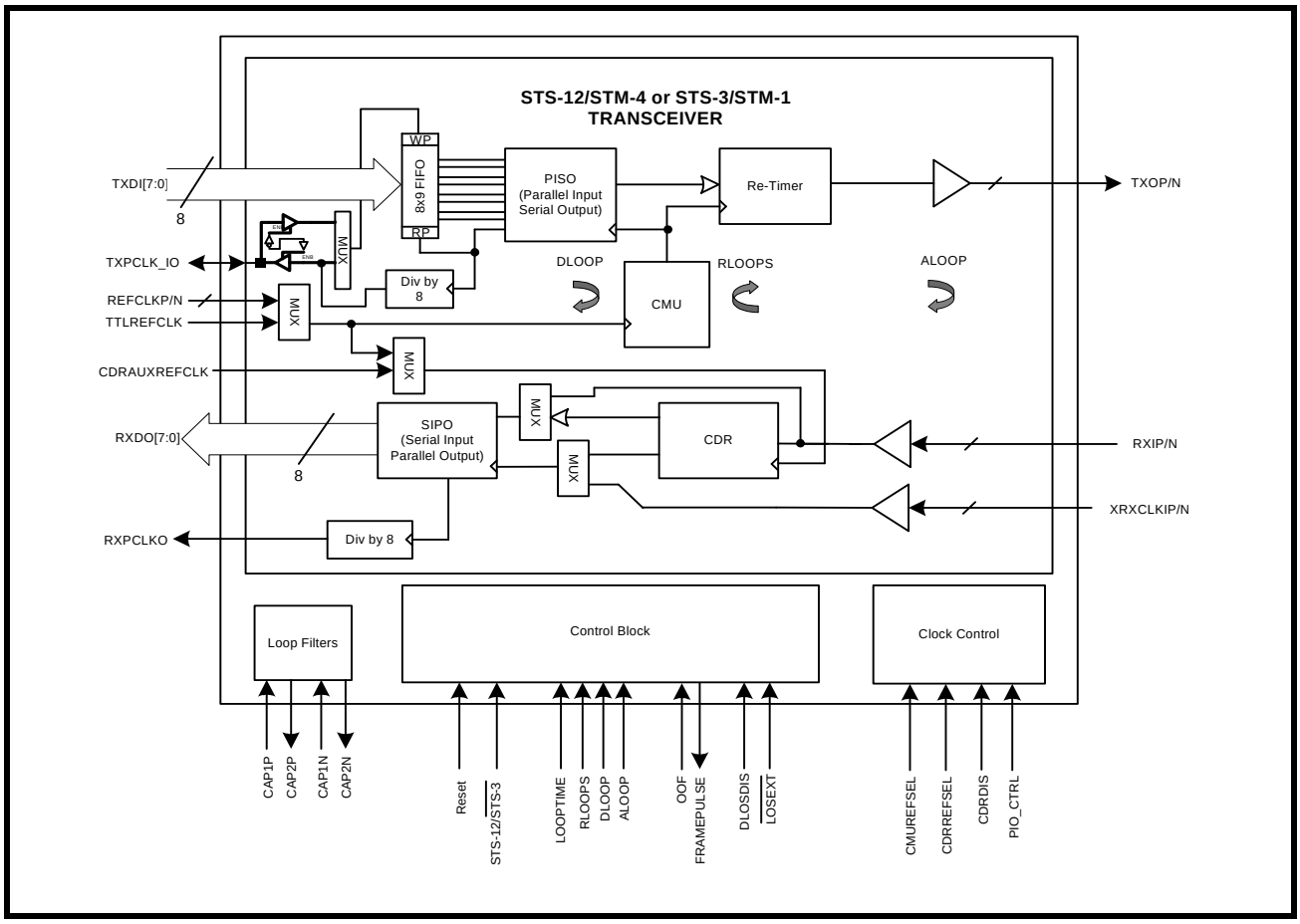
GENERAL DESCRIPTION

The XRT91L30 is a fully integrated SONET/SDH transceiver for SONET/SDH 622.08 Mbps STS-12/STM-4 or 155.52 Mbps STS-3/STM-1 applications. The transceiver includes an on-chip Clock Multiplier Unit (CMU), which uses a high frequency Phase-Locked Loop (PLL) to generate the high-speed transmit serial clock from a slower external clock reference. It also provides Clock and Data Recovery (CDR) function by synchronizing its on-chip Voltage Controlled Oscillator (VCO) to the incoming serial data stream. The internal CDR unit can be disabled and bypassed in lieu of an externally recovered received clock from the optical module. Either the internally recovered clock or the externally recovered clock can be used for loop timing applications. The chip provides serial-to-parallel and parallel-to-serial converters using an 8-bit wide LVTTL system interface in both receive and transmit directions. The transmit section includes an option to accept a parallel clock signal from the framer/mapper to synchronize the transmit section timing. The device can internally monitor Loss of Signal (LOS) condition and automatically mute received data upon LOS. An on-chip SONET/SDH frame byte and boundary detector and frame pulse generator offers the ability recover SONET/SDH framing and to byte align the receive serial data stream into the 8-bit parallel bus.

APPLICATIONS

- SONET/SDH-based Transmission Systems
- Add/Drop Multiplexers
- Cross Connect Equipment
- ATM and Multi-Service Switches, Routers and Switch/Routers
- DSLAMS
- SONET/SDH Test Equipment
- DWDM Termination Equipment

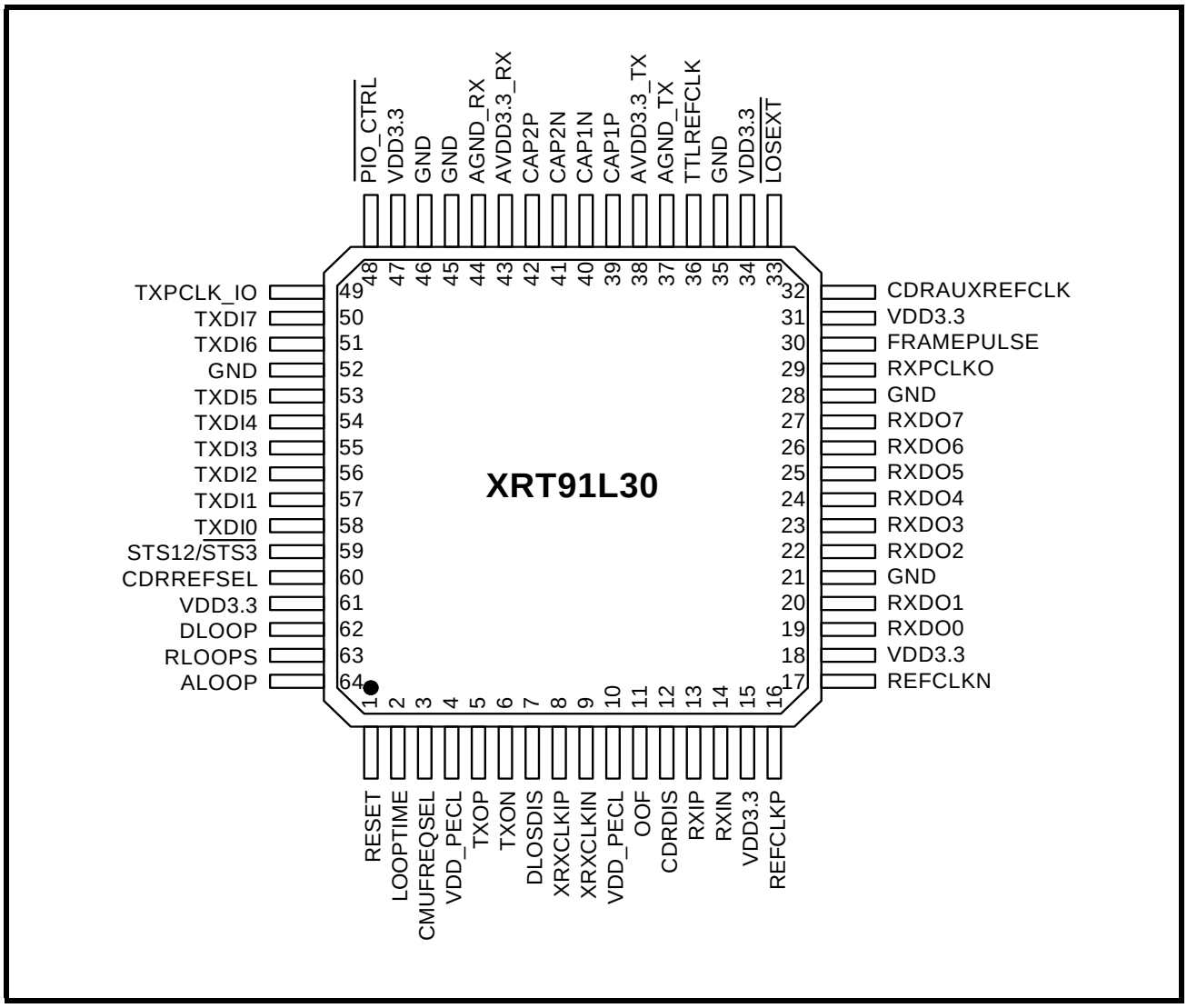
FIGURE 1. BLOCK DIAGRAM OF XRT91L30



FEATURES

- Targeted for SONET STS-12/STS-3 and SDH STM-4/STM-1 Applications
- Selectable full duplex operation between STS-12/STM-4 standard rate of 622.08 Mbps or STS-3/STM-1 155.52 Mbps
- Single-chip fully integrated solution containing parallel-to-serial converter, clock multiplier unit (CMU), serial-to-parallel converter, clock data recovery (CDR) functions, and a SONET/SDH frame and byte boundary detection circuit
- Ability to disable and bypass onchip CDR for external based received reference clock recovery thru Differential LVPECL input pins XRXCLKIP/N
- 8-bit LVTTL parallel data bus paths running at 77.76 Mbps in STS-12/STM-4 or 19.44 Mbps in STS-3/STM-1 mode of operation
- Uses Differential LVPECL or Single-Ended LVTTL CMU reference clock frequencies of either 19.44 MHz or 77.76 MHz for both STS-12/STM-1 or STS-3/STM-1 operations
- Optional use of 77.76 MHz Single-Ended LVTTL input for independent CDR reference clock operation
- Able to Detect and Recover SONET/SDH frame boundary and byte align received data on the parallel bus
- Diagnostics features include LOS monitoring and automatic received data mute upon LOS
- Provides Local, Remote and Split Loop-Back modes as well as Loop Timing mode
- Optional flexibility to re-configure the transmit parallel bus clock output to a clock input and accept timing signal from the framer/mapper device to permit the framer/mapper device time domain to be synchronized with the transceiver transmit timing.
- Meets Telcordia, ANSI and ITU-T G.783 and G.825 SDH jitter requirements including T1.105.03 - 2002 SONET Jitter Tolerance specification, Bellcore TR-NWT-000253 and GR-253-CORE, GR-253 ILR SONET Jitter specifications.
- Complies with ANSI/TIA/EIA-644 and IEEE P1596.3 3.3V LVDS standard, 3.3V LVPECL, and JESD 8-B LVTTL and LVCMOS standard.
- Operates at 3.3V Core with 3.3V I/O
- Less than 660mW in STS-3/STM-1 mode or 800mW in STS-12/STM-4 mode Typical Power Dissipation
- Package: 10 x 10 x 2.0 mm 64-pin QFP

FIGURE 2. 64 QFP PIN OUT OF THE XRT91L30 (TOP VIEW)



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT91L30IQ	64 Pin Lead QFP	-40°C to +85°C

TABLE OF CONTENTS

PIN DESCRIPTIONS

HARDWARE CONTROL

<table>
<tr><th>NAME</th><th>LEVEL</th><th>TYPE</th><th>PIN</th><th>DESCRIPTION</th></tr>
<tr><td>RESET</td><td>LVTTL</td><td>I</td><td>1</td><td>Master Reset Input
Active "High." When this pin is pulled "High" , the internal state machines are set to their default state.
"Low" = Normal Operation
"High" = Master Hardware Reset</td></tr>
<tr><td>STS12/$\overline{\text{STS3}}$</td><td>LVTTL</td><td>I</td><td>59</td><td>Data Rate Selection
Selects SONET/SDH transmission and reception speed rate
"Low" = STS-3/STM-1 155.52 Mbps
"High" = STS-12/STM-4 622.08 Mbps</td></tr>
<tr><td>CMUFREQSEL</td><td>LVTTL</td><td>I</td><td>3</td><td>Clock Multiplier Unit Reference Frequency Select
This pin is used to select the frequency of the REFCLKP/N or TTLREFCLK input to the CMU.
"Low" = 77.76 MHz reference clock
"High" = 19.44 MHz reference clock
<table>
<tr><th>CMU-FREQSEL</th><th>STS12/$\overline{\text{STS3}}$</th><th>REFCLKP/N OR TTLREFCLK REFERENCE FREQUENCY</th><th>DATA RATE</th></tr>
<tr><td>0</td><td>0</td><td>77.76 MHz</td><td>STS-3/STM-1 155.52 Mbps</td></tr>
<tr><td>0</td><td>1</td><td>77.76 MHz</td><td>STS-12/STM-4 622.08 Mbps</td></tr>
<tr><td>1</td><td>0</td><td>19.44 MHz</td><td>STS-3/STM-1 155.52 Mbps</td></tr>
<tr><td>1</td><td>1</td><td>19.44 MHz</td><td>STS-12/STM-4 622.08 Mbps</td></tr>
</table>
NOTE: REFCLKP/N or TTLREFCLK input should be generated from an LVPECL/LVTTL crystal oscillator which has a frequency accuracy better than 20ppm in order for the transmitted data rate frequency to have the necessary accuracy required for SONET systems..</td></tr>
</table>

NAME	LEVEL	TYPE	PIN	DESCRIPTION
CDRREFSEL	LVTTL	I	60	**Clock and Data Recover Unit Reference Frequency Select** Selects the Clock and Data Recovery Unit reference frequency based on the table below. "Low" = CDR uses CMU's reference clock "High" = CDR reference clock from CDRAUXREFCLK **CDRREFSEL** / **STS12/STS3** / **CDRAUXREFCLK FREQUENCY** / **DATA RATE** **0** — CDR uses CMU's reference clock (see CMUFREQSEL pin) **1** / **0** / 77.76 MHz / STS-3/STM-1 155.52 Mbps **1** / **1** / 77.76 MHz / STS-12/STM-4 622.08 Mbps ***NOTE:*** *CDRAUXREFCLK requires accuracy of 77.76 MHz +/- 500ppm.*
LOOPTIME	LVTTL	I	2	**Loop Timing Mode** When the loop timing mode is activated the external reference clock to the input of the Retimer is replaced with the high-speed recovered receive clock from the CDR. "Low" = Disabled "High" = Loop timing Activated
CDRDIS	LVTTL	I	12	**Clock and Data Recovery Unit Disable** Active "High." Disables internal Clock and Data Recovery unit. Received serial data bypasses the integrated CDR block. RXINP/N is then sampled on the rising edge of externally recovered differential clock XRXCLKIP/N coming from the optical module. "Low" = Internal CDR unit is Enabled "High" = Internal CDR unit is Disabled and Bypassed
$\overline{\text{PIO\_CTRL}}$	LVTTL	I	48	**Transmit Parallel Clock Directional Control** **Transmit Parallel Clock Output Operation** If this pin is asserted "High", TXPCLK_IO is a parallel bus clock output. Data on the TXDI[7:0] must be synchronously applied prior to the sampling by the PISO at the rising edge of TXPCLK_IO clock output driven by the XRT91L30. **Alternate Transmit Parallel Clock Input Operation** Asserting this control pin "Low" or if left unconnected, it configures TXPCLK_IO to serve as a parallel bus clock input rather than a parallel bus clock output and permits the XRT91L30 to accept the external clock input. Data on the TXDI[7:0] is then sampled at the rising edge of the TXPCLK_IO clock input driven by the framer/mapper device. "Low" = TXPCLK_IO is a Parallel Clock Input. "High" = TXPCLK_IO is a Parallel Clock Output. ***NOTE:*** *Parallel Clock Input operation has the advantage of permitting the framer/mapper device timing to be synchronized with the transceiver transmitter timing.* This pin is provided with an internal pull-down.

NAME	LEVEL	TYPE	PIN	DESCRIPTION
RLOOPS	LVTTL	I	63	**Serial Remote Loopback** The serial remote loopback mode interconnects the receive serial data input to the transmit serial data output. If serial remote loopback is enabled, the 8-bit parallel transmit data input is ignored while the 8-bit parallel receive data output is maintained. "Low" = Disabled "High" = Serial Remote Loopback Mode Enabled ***NOTE:*** *DLOOP and RLOOPS can be enabled simultaneously to achieve a SPLIT loopback diagnostic feature in normal operation.*
DLOOP	LVTTL	I	62	**Digital Local Loopback** The digital local loopback mode interconnects the 8-bit parallel transmit data input and TxCLK to the 8-bit parallel receive data output and RxCLK respectively while maintaining the transmit serial data output. If digital local loopback is enabled, the receive serial data input is ignored. "Low" = Disabled "High" = Digital Local Loopback Mode Enabled ***NOTE:*** *DLOOP and RLOOPS can be enabled simultaneously to achieve a SPLIT loopback diagnostic feature in normal operation.*
ALOOP	LVTTL	I	64	**Analog Local Loopback** This loopback feature serializes the 8-bit parallel transmit data input and presents the data to the transmit serial output and in addition it also internally routes the serialized data back to the Clock and Data Recovery block for serial to parallel conversion. The received serial data input is ignored. "Low" = Disabled "High" = Analog Local Loopback Mode Enabled

TRANSMITTER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
TXDI0 TXDI1 TXDI2 TXDI3 TXDI4 TXDI5 TXDI6 TXDI7	LVTTL	I	58 57 56 55 54 53 51 50	**Transmit Parallel Data Input** **Transmit Parallel Clock Output Operation** The 77.76 Mbps (STS-12/STM-4) / 19.44 Mbps (STS-3/STM-1) 8-bit parallel transmit data should be applied to the transmit parallel bus and simultaneously referenced to the rising edge of the TXPCLK_IO clock output. The 8-bit parallel interface is multiplexed into the transmit serial output interface with the MSB first (TXDI[7:0]). **Alternate Transmit Parallel Clock Input Operation** When operating is this mode, TXPCLK_IO is no longer a parallel clock output reference but reverses direction and serves as the parallel transmit clock input reference for the PISO (Parallel Input to Serial Output) block. The 77.76 Mbps (STS-12/STM-4) / 19.44 Mbps (STS-3/STM-1) 8-bit parallel transmit data should be applied to the transmit parallel bus and simultaneously referenced to the rising edge of the TXPCLK_IO clock input.
TXOP TXON	LVPECL Diff	O	5 6	**Transmit Serial Data Output** The transmit serial data stream is generated by multiplexing the 8-bit parallel transmit data input into a 622.08 Mbps STS-12/STM-4 or 155.52 Mbps STS-3/STM-1 serial data stream.
TXPCLK_IO	LVTTL	I/O	49	**Transmit Parallel Clock Input/Output (77.76/19.44 MHz)** **Transmit Parallel Clock Output Operation** When the $\overline{\text{PIO\_CTRL}}$ pin 48 is asserted "High," this pin will output a 77.76 MHz (STS-12/STM-4) or 19.44 MHz (STS-3/STM-1) clock output reference for the 8-bit parallel transmit data input TXDI[7:0]. This clock is used by the framer/mapper device to present the TXDI[7:0] data which the XRT91L30 will latch on the rising edge of this clock. This enables the framer/mapper device and the XRT91L30 transceiver to be in synchronization. **Alternate Transmit Parallel Clock Input Operation** When the $\overline{\text{PIO\_CTRL}}$ pin 48 is asserted "Low," this pin will accept a 77.76 MHz (STS-12/STM-4) or 19.44 MHz (STS-3/STM-1) clock input reference for the 8-bit parallel transmit data input TXDI[7:0]. The XRT91L30 will latch data at TXDI[7:0] on the rising edge of this clock. This has the enormous advantage of enabling the framer/mapper device transmit timing to be synchronized with the transceiver transmit timing.

TRANSMITTER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
REFCLKP REFCLKN	LVPECL Diff	I	16 17	**Reference Clock Input (77.76 MHz or 19.44 MHz)** This differential clock input reference is used for the transmit clock multiplier unit (CMU) and clock data recovery (CDR) to provide the necessary high speed clock reference for this device. It will accept either a 77.76 MHz or a 19.44 MHz Differential LVPECL clock source. Pin CMUFREQSEL determines the value used as the reference. See Pin CMUFREQSEL for more details. REFCLKP/N inputs are internally biased to 1.65V. ***NOTE:*** *In the event that TTLREFCLK LVTTL input is used instead of these differential inputs for clock reference, the REFCLKP should be tied to ground.*
TTLREFCLK	LVTTL	I	36	**TTL Reference Clock Input (77.76 MHz or 19.44 MHz)** This optional LVTTL clock input reference is used for the transmit clock multiplier unit (CMU) and clock data recovery (CDR) to provide the necessary high speed clock reference for this device rather than a differential clock source. It will accept either a 77.76 MHz or a 19.44 MHz LVTTL clock source. Pin CMUFREQSEL determines the value used as the reference. See Pin CMUFREQSEL for more details. ***NOTE:*** *In the event that REFCLKP/N differential inputs are used instead of this LVTTL input for clock reference, the TTLREFCLK should be tied to ground.*

RECEIVER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
RXDO0 RXDO1 RXDO2 RXDO3 RXDO4 RXDO5 RXDO6 RXDO7	LVTTL	O	19 20 22 23 24 25 26 27	**Receive Parallel Data Output** 77.76 Mbps (STS-12/STM-4) / 19.44 Mbps (STS-3/STM-1) 8-bit parallel receive data output is updated simultaneously on the rising edge of the RXPCLKO output. The 8-bit parallel interface is de-multiplexed from the receive serial data input MSB first (RXDO[7:0]). The XRT91L30 will output the data on the falling edge of this clock.
RXIP RXIN	Diff LVPECL	I	13 14	**Receive Serial Data Input** The differential receive serial data stream of 622.08 Mbps STS-12/STM-1 or 155.52 Mbps STS-3/STM-1 is applied to these input pins.
XRXCLKIP XRXCLKIN	Diff LVPECL	I	8 9	**External Recovered Receive Clock Input** The differential receive serial data stream of 622.08 Mbps STS-12/STM-1 or 155.52 Mbps STS-3/STM-1 is sampled on the rising edge of this externally recovered differential clock coming from the optical module. It is used when the internal CDR unit is disabled and bypassed by the CDRDIS pin. ***NOTE:*** *In the event that XRXCLKIP/N differential input pins are unused, XRXCLKIP should be tied to VCC with a 1k Ohm pull-up and XRXCLKIN should be tied to Ground with a 1k Ohm pull-down.*
RXPCLKO	LVTTL	O	29	**Receive Parallel Clock Output (77.76 MHz or 19.44 MHz)** 77.76 MHz (STS-12/STM-4) or 19.44 MHz (STS-3/STM-1) clock output reference for the 8-bit parallel receive data output RXDO[7:0]. The parallel received data output bus will be updated on the falling edge of this clock.
CDRAUX- REFCLK	LVTTL	I	32	**Clock and Data Recovery Auxillary Reference Clock** 77.76 MHz ± 500 ppm auxillary reference clock for the CDR. ***NOTE:*** *In the event that CDRAUXREFCLK LVTTL input pin is unused, CDRAUXREFCLK should be tied to ground.*
OOF	LVTTL	I	11	**Out of Frame Input Indicator** This level sensitive input pin is used to initiate frame detection and byte alignment recovery when OOF is declared by the downstream device. When this pin is held High, FRAME-PULSE will pulse for a single RXPCLKO period upon the detection of every third frame alignment A2 byte in the incoming SONET/SDH Frame. "Low" = Normal Operation "High" = OOF Indication initiating frame detection and byte boundary recovery and activating FRAMEPULSE
FRAMEPULSE	LVTTL	O	30	**Sonet Frame Alignment Pulse** This pin will generate a single pulse for an RXPCLKO clock period upon the detection of the third frame alignment A2 byte whenever the OOF input pin is held High. The parallel received data output bus will then be byte aligned to this newly recovered SONET/SDH frame.

NAME	LEVEL	TYPE	PIN	DESCRIPTION
CAP1P CAP2P	Analog	-	39 42	**CDR Non-polarized External Filter Capacitor** C1 = 0.47µF ± 10% tolerance (Isolate from noise and place close to pin)
CAP1N CAP2N	Analog	-	40 41	**CDR Non-polarized External Filter Capacitor** C2 = 0.47µF ± 10% tolerance (Isolate from noise and place close to pin)
DLOSDIS	LVTTL	I	7	**LOS (Los of Signal) Detect Disable** Disables internal LOS monitoring and automatic muting of RXDO[7:0] upon LOS detection. LOS is declared when a string of 128 consecutive zeros occur on the line. LOS condition is cleared when the 16 or more pulse transitions is detected for 128 bit period sliding window. "Low" = Monitor and Mute received data upon LOS declaration "High" = Disable internal LOS monitoring
$\overline{\text{LOSEXT}}$	SE-LVPECL	I	33	**LOS or Signal Detect Input from Optical Module** Active "Low." When active, this pin will force the received data output bus RXDO[7:0] to a logic state of '0.' "Low" = Forced LOS "High" = Normal Operation

POWER AND GROUND

NAME	TYPE	PIN	DESCRIPTION
VDD3.3	PWR	15, 18, 31, 34, 47, 61	**3.3V CMOS Power Supply** VDD3.3 should be isolated from the Analog VDD power supplies. For best results, use a ferrite bead along with an internal power plane separation. The VDDD3.3 power supply pins should have bypass capacitors to the nearest ground.
AVDD3.3_TX	PWR	38	**Analog 3.3V Transmitter Power Supply** AVDD3.3_TX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD3.3_TX power supply pins should have bypass capacitors to the nearest ground.
AVDD3.3_RX	PWR	43	**Analog 3.3V Receiver Power Supply** AVDD3.3_RX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD3.3_RX power supply pins should have bypass capacitors to the nearest ground.
VDD_LVPECL	PWR	4, 10	**3.3V Input/Output LVPECL Bus Power Supply** These pins require a 3.3V potential voltage for properly biasing the Differential LVPECL input and output pins.
AGND_TX	PWR	37	**Transmitter Analog Ground for 3.3V Analog Power Supplies** It is recommended that all ground pins of this device be tied together.

NAME	TYPE	PIN	DESCRIPTION
AGND_RX	PWR	44	**Receiver Analog Ground for 3.3V Analog Power Supplies** It is recommended that all ground pins of this device be tied together.
GND	GND	21, 28, 35, 45, 46, 52	**Power Supply and Thermal Ground** It is recommended that all ground pins of this device be tied together.

1.0 FUNCTIONAL DESCRIPTION

The XRT91L30 transceiver is designed to operate with a SONET Framer/ASIC device and provide a high-speed serial interface to optical networks. The transceiver converts 8-bit parallel data running at 77.76 Mbps (STS-12/STM-4) or 19.44 Mbps (STS-3/STM-1) to a serial Differential LVPECL bit stream at 622.08 Mbps or 155.52 Mbps and vice-versa. It implements a clock multiplier unit (CMU), SONET/SDH serialization/de-serialization (SerDes), receive clock and data recovery (CDR) unit and a SONET/SDH frame and byte boundary detection circuit. The transceiver is divided into Transmit and Receive sections and is used to provide the front end component of SONET equipment, which includes primarily serial transmit and receive functions.

1.1 STS-12/STM-4 and STS-3/STM-1 Mode of Operation

Functionality of the transceiver can be configured by using the appropriate signal level on the STS-12/$\overline{\text{STS-3}}$ pin. STS-3/STM-1 mode is selected by pulling STS-12/$\overline{\text{STS-3}}$ "Low" as described in the Hardware Pin Descriptions. However, if STS-12/STM-4 mode is desired, it is selected by pulling STS-12/$\overline{\text{STS-3}}$ "High." Therefore, the following sections describe the functionality rather than how each function is controlled. The Hardware Pin Descriptions and describe device configuration.

1.2 Clock Input Reference for Clock Multiplier (Synthesizer) Unit

The XRT91L30 can accept both a 19.44 MHz or a 77.76 MHz Differential LVPECL clock input at REFCLKP/N or a Single-Ended LVTTL clock at TTLREFCLK as its internal timing reference for generating higher speed clocks. The REFCLKP/N or TTLREFCLK input should be generated from an LVPECL/LVTTL crystal oscillator which has a frequency accuracy better than 20ppm in order for the transmitted data rate frequency to have the necessary accuracy required for SONET systems. The reference clock can be provided with one of two frequencies chosen by CMUFREQSEL. The reference frequency options for the XRT91L30 are listed in Table 1.

TABLE 1: CMU REFERENCE FREQUENCY OPTIONS (DIFFERENTIAL OR SINGLE-ENDED)

CMUFREQSEL	STS12/$\overline{\text{STS3}}$	REFCLKP/N OR TTLREFCLK REFERENCE FREQUENCY	DATA RATE
0	**0**	77.76 MHz	STS-3/STM-1 155.52 Mbps
0	**1**	77.76 MHz	STS-12/STM-4 622.08 Mbps
1	**0**	19.44 MHz	STS-3/STM-1 155.52 Mbps
1	**1**	19.44 MHz	STS-12/STM-4 622.08 Mbps

1.3 Data Latency

Due to different operating modes and data logic paths through the device, there is an associated latency from data ingress to data egress. Table 2 specifies the data latency for a typical path.

TABLE 2: DATA INGRESS TO DATA EGRESS LATENCY

MODE OF OPERATION	DATA PATH	CLOCK REFERENCE	RANGE OF CLOCK CYCLES
Thru-mode	MSB at RXIP/N to data on RXDO[7:0]	Recoved RXIP/N Clock	25 to 35
Serial Remote Loopback	MSB at RXIP/N to MSB at TXOP/N	Recoved RXIP/N Clock	2 to 4

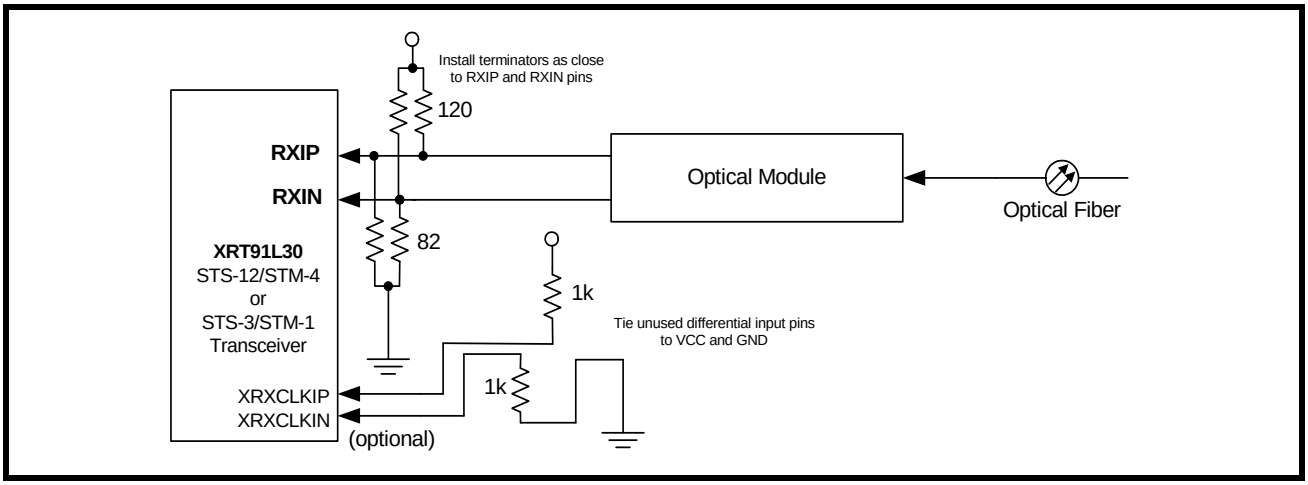
2.0 RECEIVE SECTION

The receive section of XRT91L30 include the inputs RXIP/N, followed by the clock and data recovery unit (CDR) and receive serial-to-parallel converter. The receiver accepts the high speed Non-Return to Zero (NRZ) serial data at 622.08 Mbps or 155.52 Mbps through the input interfaces RXIP/N. The clock and data recovery unit recovers the high-speed receive clock from the incoming scrambled NRZ data stream. The recovered serial data is converted into an 8-bit-wide, 77.76 Mbps or 19.44 Mbps parallel data and presented to the RXDO[7:0] parallel interface. This parallel interface is designed for Single-Ended LVTTL operation. A divide-by-8 version of the high-speed recovered clock RXPCLKOP/N, is used to synchronize the transfer of the 8-bit RXDO[7:0] data with the receive portion of the framer/mapper device. Upon initialization or loss of signal or loss of lock, the external reference clock signal of 19.44 MHz or 77.76 MHz is used to start-up the clock recovery phase-locked loop for proper operation. In certain applications, the CDR block on the XRT91L30 can be disabled and bypassed by enabling the CDRDIS pin to permit the flexibility of using an externally recovered receive clock thru the XRXCLKIP/N pins.

2.1 Receive Serial Input

The receive serial inputs are applied to RXIP/N. The receive serial inputs can be AC or DC coupled to an optical module or an electrical interface. A simplified DC coupling block diagram is shown in Figure 3.

FIGURE 3. RECEIVE SERIAL INPUT INTERFACE BLOCK



NOTE: *Some optical modules integrate AC coupling capacitors within the module. AC or DC coupling is largely specific to system design and optical module of choice.*

2.2 Recieve Serial Data Input Timing

The received High-Speed Serial Differential Data Input must adhere to the set-up and hold time timing specifications below.

FIGURE 4. RECEIVE HIGH-SPEED SERIAL DATA INPUT TIMING DIAGRAM

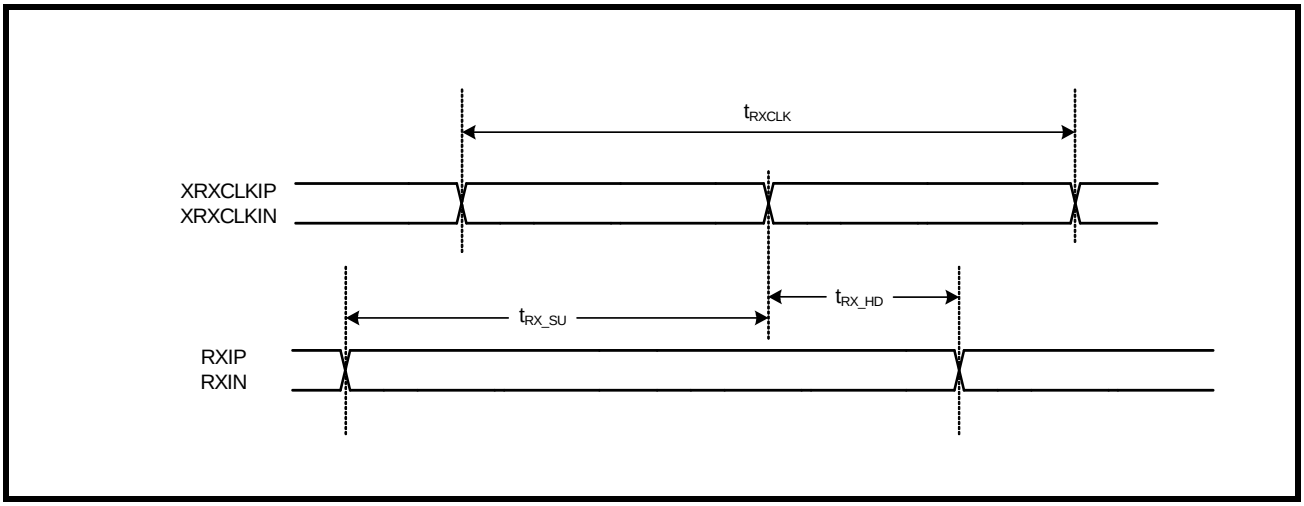


TABLE 3: RECEIVE HIGH-SPEED SERIAL DATA INPUT TIMING (STS-12/STM-4 OPERATION)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{RXCLK}	Receive external recovered clock period		1.608		ns
t_{RX_SU}	Serial data setup time with respect to XRXCLKIP/N	400			ps
t_{RX_HD}	Serial data hold time with respect to XRXCLKIP/N	100			ps

TABLE 4: RECEIVE HIGH-SPEED SERIAL DATA INPUT TIMING (STS-3/STM-1 OPERATION)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{RXCLK}	Receive external recovered clock period		6.43		ns
t_{RX_SU}	Serial data setup time with respect to XRXCLKIP/N	1.5			ns
t_{RX_HD}	Serial data hold time with respect to XRXCLKIP/N	1.5			ns

2.3 Receive Clock and Data Recovery

The clock and data recovery (CDR) unit accepts the high speed NRZ serial data from the Differential LVPECL receiver and generates a clock that is the same frequency as the incoming data. The clock recovery can either utilize the transmitter's CMU reference clock from either REFCLKP/N or TTLREFCLK or it can use independent clock source CDRAUXREFCLK to train and monitor its clock recovery PLL. Initially upon startup, the PLL locks to the local reference clock within ±500 ppm. Once this is achieved, the PLL then attempts to lock onto the incoming receive data stream. Whenever the recovered clock frequency deviates from the local reference clock frequency by more than approximately ±500 ppm, the clock recovery PLL will switch and lock back onto the local reference clock. Whenever a Loss of Lock or a Loss of Signal event occurs, the CDR will continue to supply a receive clock (based on the local reference) to the framer/mapper device. When the LOSEXT is asserted by the optical module or when LOS is detected, the receive parallel data output will be forced to a logic zero state for the entire duration that a LOS condition is detected. This acts as a receive data mute upon LOS function to prevent random noise from being misinterpreted as valid incoming data. When the LOSEXT becomes inactive and the recovered clock is determined to be within ±500 ppm accuracy with respect to the local reference source and LOS is no longer declared, the clock recovery PLL will switch and lock back onto the incoming receive data stream. Table 5 shows Clock and Data Recovery reference clock settings. Table 6 specifies the Clock and Data Recovery Unit performance characteristics.

TABLE 5: CLOCK DATA RECOVERY UNIT REFERENCE CLOCK SETTINGS

CMUFREQSEL	CDRREFSEL	STS12/$\overline{\text{STS3}}$	REFCLKP/N[1] OR TTLREFCLK[1] FREQUENCY (MHZ)	CDRAUXREFCLK[2] FREQUENCY (MHZ)	CDR OUTPUT FREQUENCY (MHZ)
0	**0**	**0**	77.76 MHz	not used	155.52
0	**0**	**1**	77.76 MHz	not used	622.08
1	**0**	**0**	19.44 MHz	not used	155.52
1	**0**	**1**	19.44 MHz	not used	622.08
X	**1**	**0**	not referenced by CDR	77.76 MHz	155.52
X	**1**	**1**	not referenced by CDR	77.76 MHz	622.08

[1]Requires frequency accuracy better than 20ppm in order for the transmitted data rate frequency to have the necessary accuracy required for SONET systems.

[2]CDRAUXREFCLK requires accuracy of 77.76 MHz +/- 500ppm.

TABLE 6: CLOCK AND DATA RECOVERY UNIT PERFORMANCE

NAME	PARAMETER	MIN	TYP	MAX	UNITS
REF_{DUTY}	Reference clock duty cycle	40		60	%
REF_{JIT}	Reference clock jitter (rms) with 19.44 MHz reference[1]			5	ps
REF_{JIT}	Reference clock jitter (rms) with 77.76 MHz reference[1]			13	ps
REF_{TOL}	Reference clock frequency tolerance[2]	-20		+20	ppm
TOL_{JIT}	Input jitter tolerance with 1 MHz < f < 20 MHz PRBS pattern	0.3	0.4		UI
$OCLK_{FREQ}$	Frequency output	620		624	MHz
$OCLK_{DUTY}$	Clock output duty cycle	40		60	%

Jitter specification is defined using a 12kHz to 1.3/5MHz LP-HP single-pole filter.

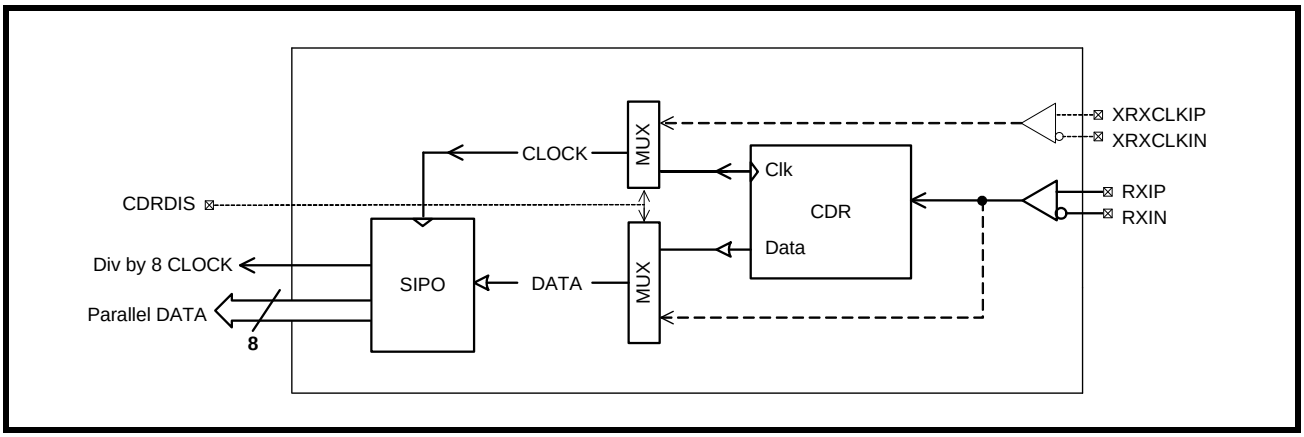
[1]These reference clock jitter limits are required for the outputs to meet SONET system level jitter requirements (<10 mUI_{rms}).

[2]Required to meet SONET output frequency stability requirements.

2.3.1 Internal Clock and Data Recovery Bypass

Optionally, the internal CDR unit can be disabled and bypassed in lieu of an externally recovered clock. Asserting the CDRDIS "High" disables the internal Clock and Data Recovery unit and the received serial data bypasses the integrated CDR block. RXINP/N is then sampled on the rising edge of the externally recovered differential clock XRXCLKIP/N coming from the optical module or an external clock recovery unit. Figure 5 shows the possible internal paths of the recovered clock and data.

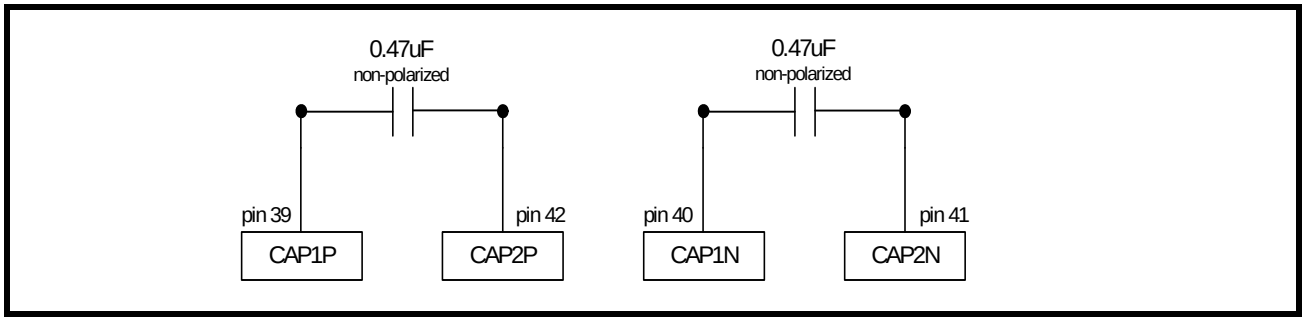
FIGURE 5. INTERNAL CLOCK AND DATA RECOVERY BYPASS



2.4 External Receive Loop Filter Capacitors

These 0.47µF non-polarized external loop filter capacitors provide the necessary components to achieve the required receiver jitter performance. They must be well isolated to prohibit noise entering the CDR block and should be placed as close to the pins as much as possible. Figure 6 shows the pin connections and external loop filter components. These two non-polarized capacitors should be of +/- 10% tolerance.

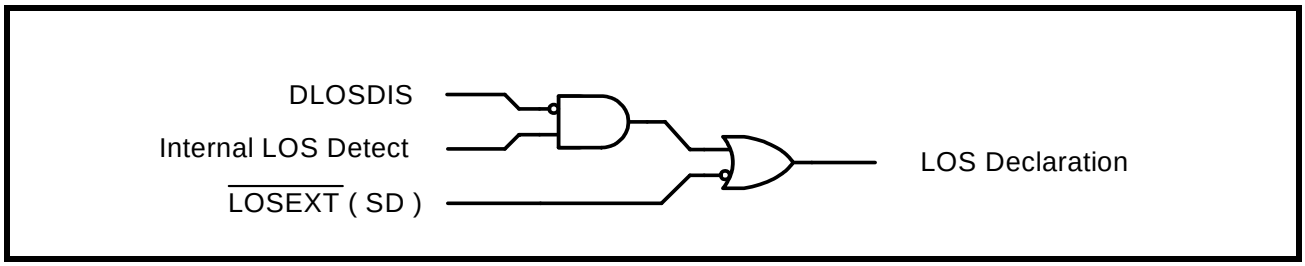
FIGURE 6. EXTERNAL LOOP FILTERS



2.5 Loss Of Signal

XRT91L30 supports internal Loss of Signal detection (LOS) and external LOS detection. The internal Loss of Signal Detector monitors the incoming data stream and if the incoming data stream has no transition continuously for more than 128 bit periods, Loss of Signal is declared. This LOS detection will be removed when the circuit detects 16 transitions in a 128 bit period sliding window. Pulling the corresponding DLOSDIS signal to a high level will disable the internal LOS detection circuit. The external LOS function is supported by the LOSEXT input. The Single-Ended LVPECL input usually comes from the optical module through an output usually called “SD” or “FLAG” which indicates the lack or presence of optical power. Depending on the manufacturer of these devices the polarity of this signal can be either active "Low" or active "High." LOSEXT is an active "Low" signal requiring a low level to assert or invoke a forced LOS. The external LOSEXT input pin and internal LOS detector are Logically OR’ed to control detection and declaration of Loss of Signal. Whenever LOS is internally detected or an external LOS is asserted thru the LOSEXT pin, the XRT91L30 will automatically force the receive parallel data output to a logic state "0" for the entire duration that a LOS condition is declared. This acts as a receive data mute upon LOS function to prevent random noise from being misinterpreted as valid incoming data.

FIGURE 7. LOS DECLARATION CIRCUIT



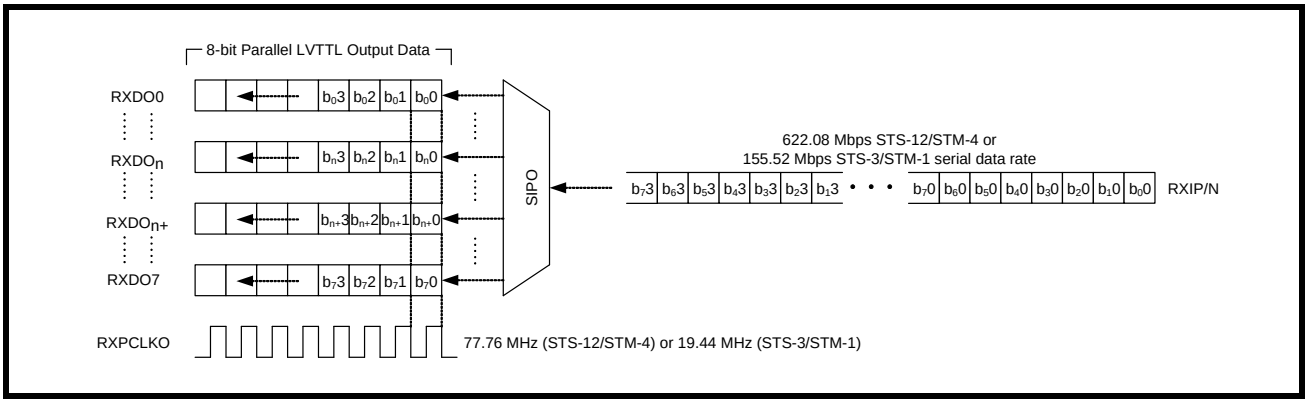
2.6 SONET Frame Boundary Detection and Byte Alignment Recovery

A Frame and Byte Boundary Detection circuit searches the incoming data channel for three consecutive A1 (0xF6 Hex) bytes followed by three consecutive A2 (0x28 Hex) bytes. The detector operates under the control of the OOF (Out of Frame) signals provided from the SONET Framer. Detection is enabled when OOF is held "High" and remains active until OOF goes "Low." When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming receive data stream. The receive serial-to-parallel converter block uses the located byte boundary to assemble the incoming data stream into bytes for output on the parallel data output bus RXDO[7:0]. The frame boundary is reported on the frame pulse (FRAMEPULSE) output at the onset of detecting the third A2 byte pattern when any serial 48-bit pattern matching the framing pattern is detected on the incoming data stream. While in the pattern search and detection state and so long is OOF is active, the frame pulse (FRAMEPULSE) output is activated for one byte clock cycle (RXPCLKO = 12.86 ns pulse duration for STS-12/STM-4 or 51.44 ns pulse duration for STS-3/STM-1) anytime a 48-bit pattern matching the framing pattern is detected on the incoming data stream. Once the SONET Framer Overhead Circuitry has verified that frame and byte synchronization are correct, the OOF input pin should be de-asserted by the SONET Framer to disable the XRT91L30 frame search process from trying to synchronize repeatedly and to de-activate FRAMEPULSE. When the XRT91L30's framing pattern detection is disabled upon the de-assertion of OOF input pin from the SONET Framer, the byte boundary will lock to the detected location and will remain locked to that location found when detection was previously enabled.

2.7 Receive Serial Input to Parallel Output (SIPO)

During STS-12/STM-4 operation, the SIPO is used to convert the 622.08 Mbps serial data input to 77.76 Mbps parallel data output which can interface to a SONET Framer/ASIC. If the XRT91L30 is operating in STS-3/STM-1, the SIPO will convert the 155.52 Mbps serial data input to 19.44 Mbps parallel data output. The SIPO bit de-interleaves the serial data input into an 8-bit parallel output to RXDO[7:0]. A simplified block diagram is shown in Figure 8. XRT91L30 clocks data out on RXDO[7:0] at the falling edge of RXPCLKO.

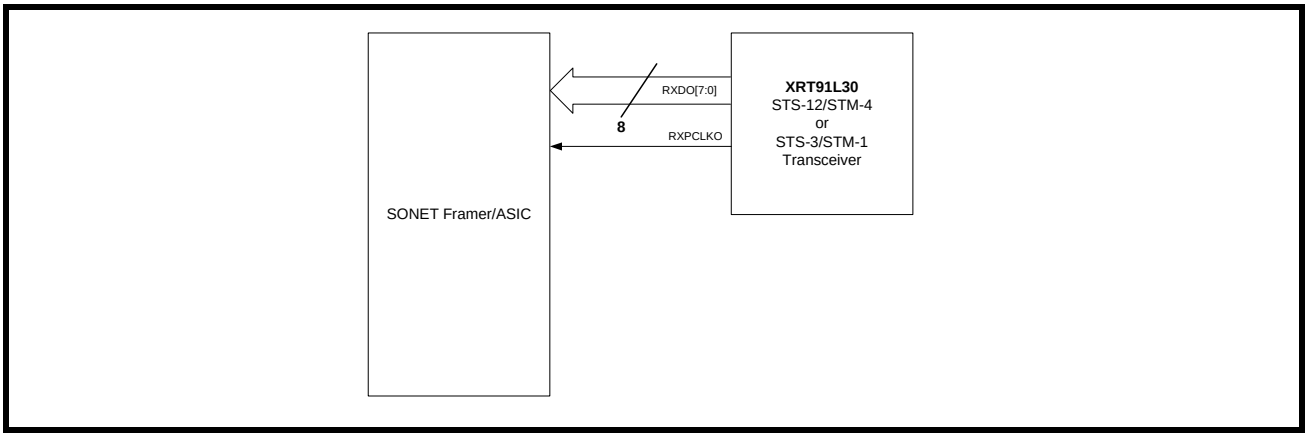
FIGURE 8. SIMPLIFIED BLOCK DIAGRAM OF SIPO



2.8 Receive Parallel Output Interface

The 8-bit Single-Ended LVTTL running at 77.76 Mbps (STS-12/STM-4) or 19.44 Mbps (STS-3/STM-1) parallel data output of the receive path is used to interface to a SONET Framer/ASIC synchronized to the recovered clock. A simplified block diagram is shown in Figure 9.

FIGURE 9. RECEIVE PARALLEL OUTPUT INTERFACE BLOCK



2.9 Disable Parallel Receive Data Output Upon LOS

The parallel receiver outputs are automatically pulled "Low" or forced to a logic state of "0" during a LOS condition to prevent data chattering unless LOS detection is disabled by asserting DLOSDIS and keeping LOSEXT input pin "high." In addition, the user can also assert LOSEXT input pin from the optical module to force an LOS and mute the parallel receiver outputs as well.

2.10 Receive Parallel Data Output Timing

The receive parallel data output from the STS-12/STM-4 or STS-3/STM-1 receiver will adhere to the setup and hold times shown in Figure 10 ,Table 7, and Table 8. Table 9 shows the PECL and TTL output timing specifications.

FIGURE 10. RECEIVE PARALLEL OUTPUT TIMING

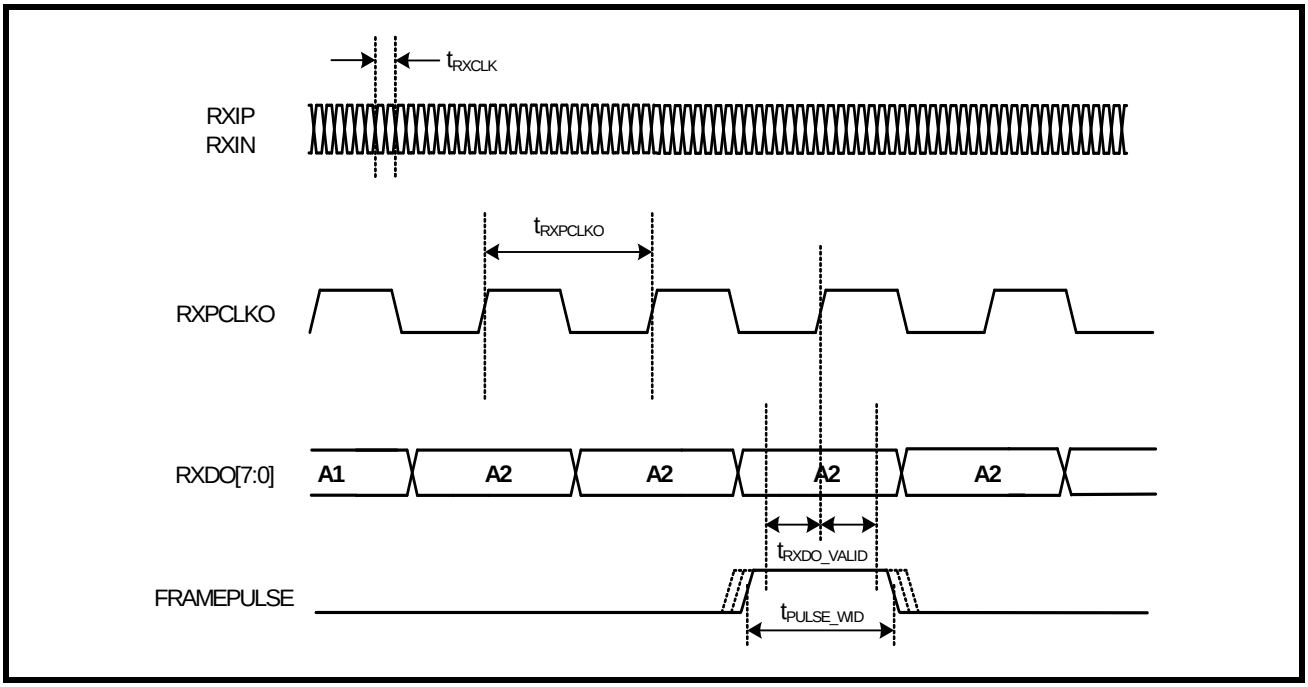


TABLE 7: RECEIVE PARALLEL DATA OUTPUT TIMING (STS-12/STM-4 OPERATION)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{RXCLK}	Receive high-speed serial clock period		1.608		ns
$t_{RXPCLKO}$	Receive parallel data output byte clock period		12.86		ns
t_{RXDO_VALID}	Time the data is valid on RXDO[7:0] and FRAMEPULSE before and after the rising edge of RXPCLKO	4			ns
t_{PULSE_WID}	Pulse width of frame detection pulse on FRAMEPULSE		12.86		ns

TABLE 8: RECEIVE PARALLEL DATA OUTPUT TIMING (STS-3/STM-1 OPERATION)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{RXCLK}	Receive high-speed serial clock period		6.43		ns
$t_{RXPCLKO}$	Receive parallel data output byte clock period		51.44		ns
t_{RXDO_VALID}	Time the data is valid on RXDO[7:0] and FRAMEPULSE before and after the rising edge of RXPCLKO	22			ns
t_{PULSE_WID}	Pulse width of frame detection pulse on FRAMEPULSE		51.44		ns

TABLE 9: PECL AND TTL RECEIVE OUTPUTS TIMING SPECIFICATION

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{R_PECL}	PECL output rise time (20% to 80%)		350		ps
t_{F_PECL}	PECL output fall time (80% to 20%)		350		ps
t_{R_TTL}	TTL output rise time (10% to 90%)		2		ns
t_{F_TTL}	TTL output fall time (90% to 10%)		1.5		ns

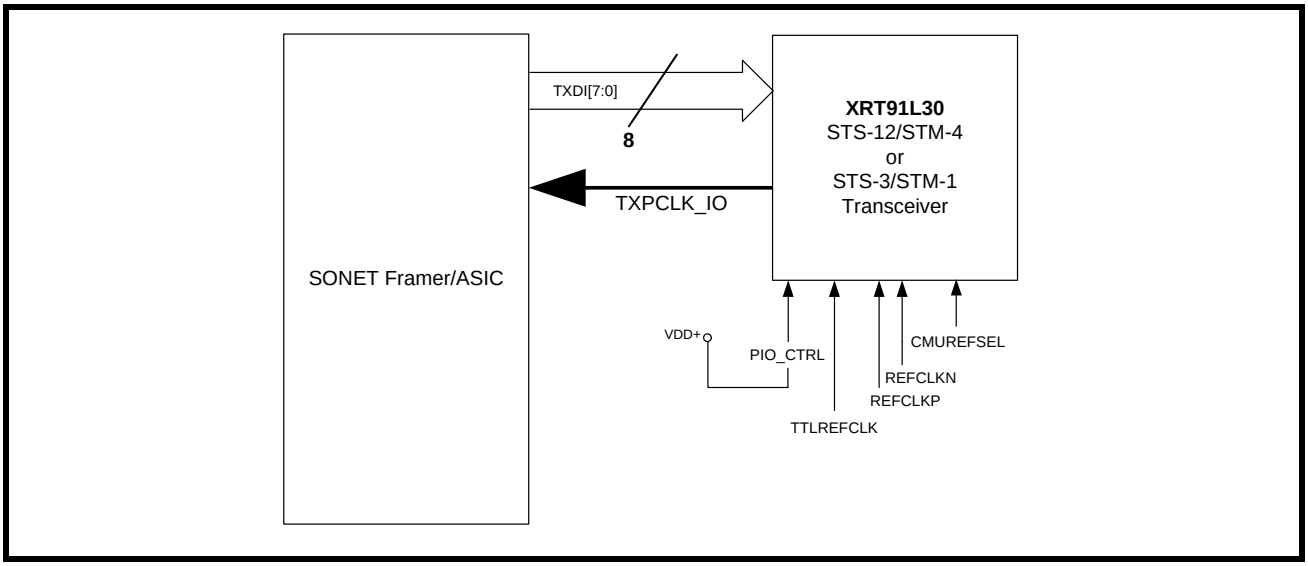
3.0 TRANSMIT SECTION

The transmit section of the XRT91L30 accepts 8-bit parallel data and converts it to serial Differential LVPECL data output intented to interface to an optical module. It consists of an 8-bit parallel Single-Ended LVTTL interface, Parallel-to-Serial Converter, a clock multiplier unit (CMU), a Low Voltage Positive-referenced Emitter-Coupled Logic (LVPECL) differential line driver, and Loop Timing modes. The LVPECL serial data output rate is 622.08 Mbps for STS-12/STM-4 applications and 155.52 Mbps for STS-3/STM-1 applications. The high frequency serial clock is synthesized by a PLL, which uses a low frequency clock as its input reference. In order to synchronize the data transfer process, the synthesized 622.08 MHz for STS-12/STM-4 or 155.52 MHz STS-3/STM-1 serial clock output is divided by eight and the 77.76 MHz (STS-12/STM-4) or 19.44 MHz (STS-3/STM-1) clock respectively is presented to the framer/mapper device to be used as its timing source.

3.1 Transmit Parallel Input Interface

The parallel data from an framer/mapper device is presented to the XRT91L30 through an 8-bit Single-Ended LVTTL parallel bus interface TXDI[7:0]. To directly interface to the XRT91L30, the SONET Framer/ASIC must be synchronized to the same timing source TXPCLK_IO in presenting data on the parallel bus interface. The data must meet setup and hold times with respect to TXPCLK_IO. This clock output source is used to synchronize the SONET Framer/ASIC to the XRT91L30. The framer/mapper device should use TXPCLK_IO as its timing source so that parallel data is phase aligned with the serial transmit data. The data is latched into a parallel input register on the rising edge of TXPCLK_IO. TXPCLK_IO is derived from a divide-by-8 of the high speed synthesized clock resulting in a 77.76/ 19.44 MHz Single-Ended LVTTL clock output source to be used by the framer/mapper device for parallel bus synchronization. A simplified block diagram of the transmit parallel bus clock output system interface is shown in Figure 11.

FIGURE 11. TRANSMIT PARALLEL INPUT INTERFACE BLOCK



3.2 Transmit Parallel Data Input Timing

When applying parallel data input to the transmitter, the setup and hold times should be followed as shown in Figure 12 and Table 10, Table 11.

FIGURE 12. TRANSMIT PARALLEL INPUT TIMING

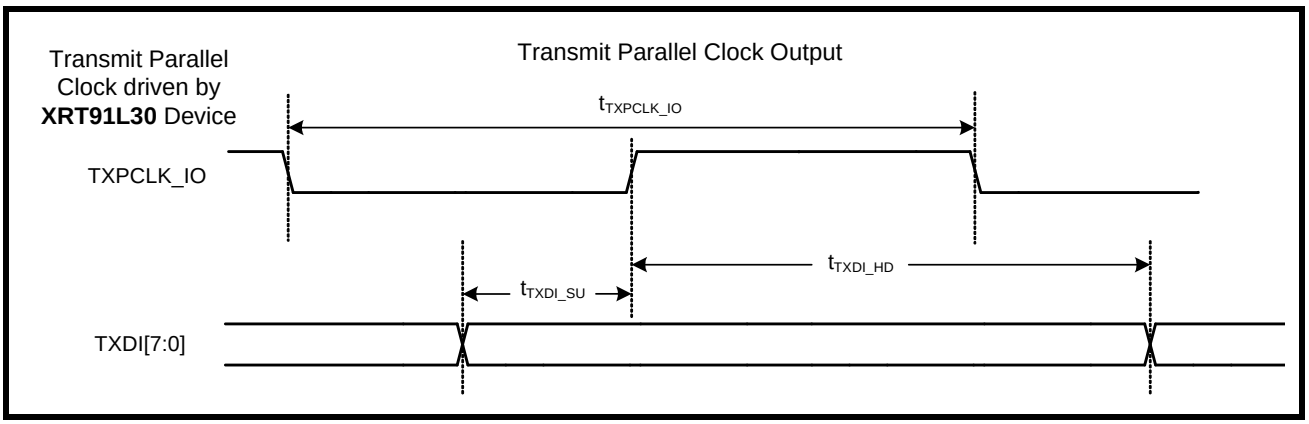


TABLE 10: TRANSMIT PARALLEL DATA INPUT TIMING (STS-12/STM-4 OPERATION)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{TXPCLK_IO}	Transmit Clock **Output** period		12.86		ns
t_{TXDI_SU}	Transmit data setup time with respect to TXPCLK_IO	2.0			ns
t_{TXDI_HD}	Transmit data hold time with respect to TXPCLK_IO	1.0			ns

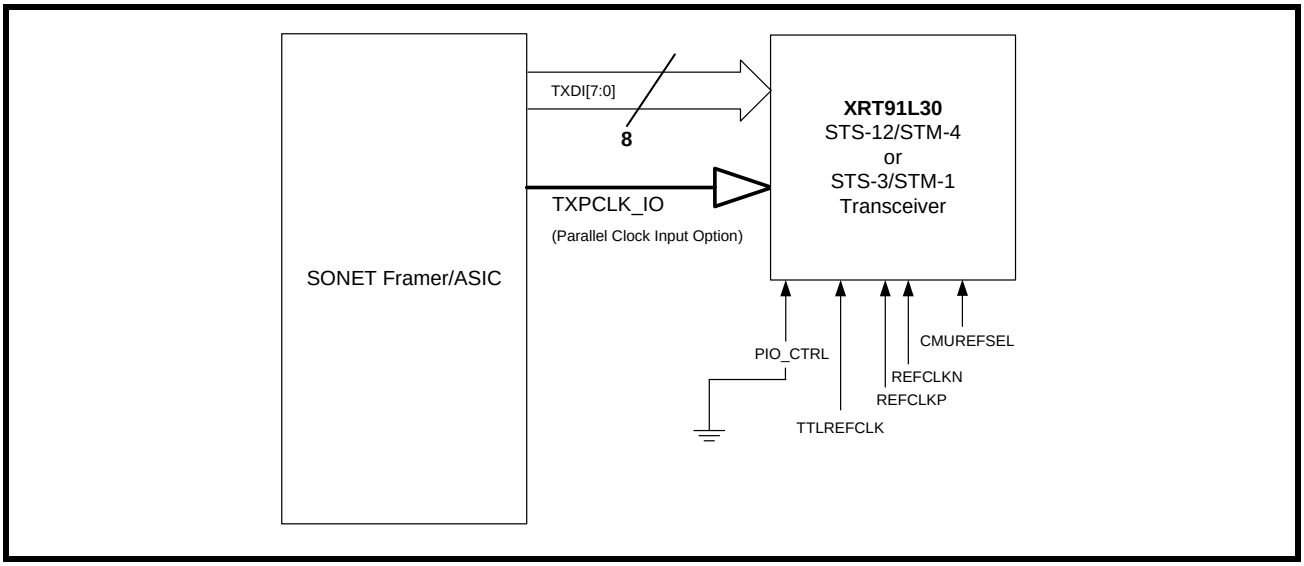
TABLE 11: TRANSMIT PARALLEL DATA INPUT TIMING (STS-3/STM-1 OPERATION).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{TXPCLK_IO}	Transmit Clock **Output** period		51.44		ns
t_{TXDI_SU}	Transmit data setup time with respect to TXPCLK_IO	2.0			ns
t_{TXDI_HD}	Transmit data hold time with respect to TXPCLK_IO	1.0			ns

3.3 Alternate Transmit Parallel Bus Clock Input Option

To decouple transmit parallel clock domains of the framer/mapper device and the XRT91L30 transceiver and to eliminate difficult timing issues between them, the transmit parallel clock TXPCLK_IO can also be optionally configured as a clock input. Rather than provide a transmit parallel clock output reference to the framer/mapper device, the XRT91L30 can instead accept a reference transmit parallel clock input signal from the framer/mapper device to sample the transmit parallel bus. When PIO_CTRL pin 48 is asserted "Low," TXPCLK_IO switches into a clock input and the XRT91L30 will now sample data on the transmit parallel bus TXDI[7:0] based on TXPCLK_IO clock input reference coming from the framer/mapper device. The use of the alternate transmit parallel bus clock input option permits the system to tolerate an arbitrary amount of phase mismatch and jitter between framer/mapper transmit parallel clock timing and transceiver transmit timing. Figure 13 provides a detailed overview of the alternate transmit parallel bus clock input system interface.

FIGURE 13. ALTERNATE TRANSMIT PARALLEL INPUT INTERFACE BLOCK (PARALLEL CLOCK INPUT OPTION)



3.4 Alternate Transmit Parallel Data Input Timing

When applying parallel data input to the transmitter in the alternate transmit parallel bus clock input mode of operation, the setup and hold times should be followed as shown in Figure 14 and Table 12, Table 13.

FIGURE 14. ALTERNATE TRANSMIT PARALLEL INPUT TIMING

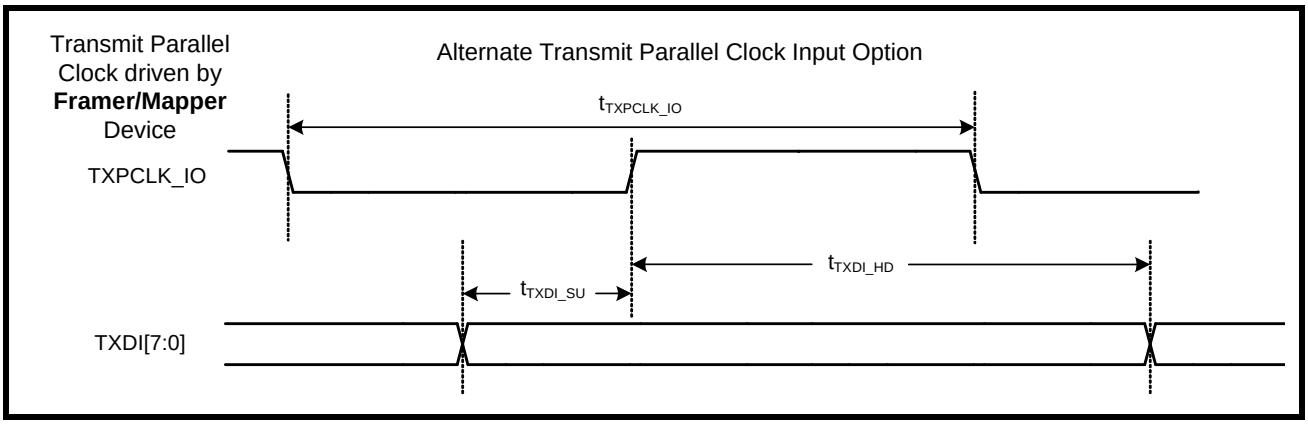


TABLE 12: ALTERNATE TRANSMIT PARALLEL DATA INPUT TIMING (STS-12/STM-4 OPERATION)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{TXPCLK_IO}	Transmit Clock **Input** period		12.86		ns
t_{TXDI_SU}	Transmit data setup time with respect to TXPCLK_IO	2.0			ns
t_{TXDI_HD}	Transmit data hold time with respect to TXPCLK_IO	1.0			ns

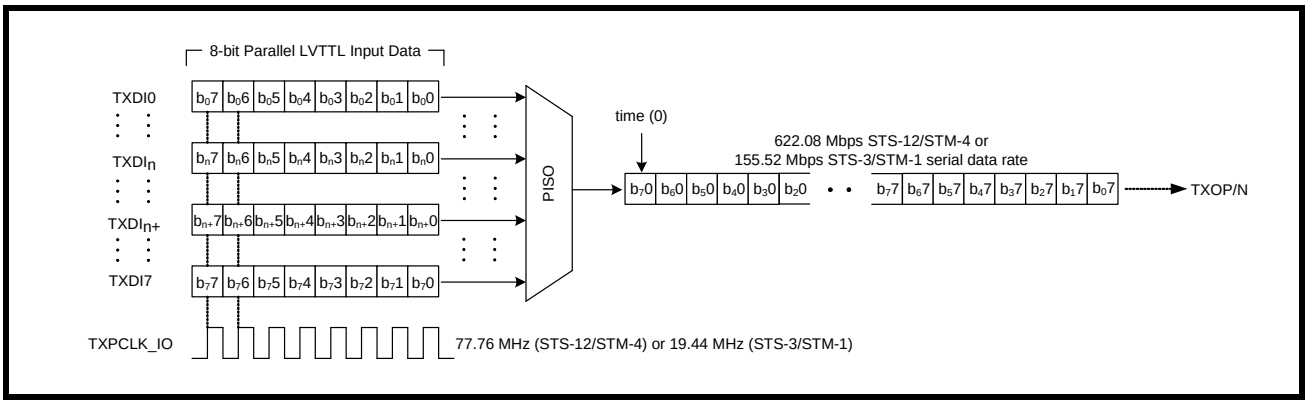
TABLE 13: ALTERNATE TRANSMIT PARALLEL DATA INPUT TIMING (STS-3/STM-1 OPERATION).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{TXPCLK_IO}	Transmit Clock **Input** period		51.44		ns
t_{TXDI_SU}	Transmit data setup time with respect to TXPCLK_IO	2.0			ns
t_{TXDI_HD}	Transmit data hold time with respect to TXPCLK_IO	1.0			ns

3.5 Transmit Parallel Input to Serial Output (PISO)

The PISO is used to convert 77.76 Mbps or 19.44 Mbps parallel data input to 622.08 Mbps STS-12/STM-1 or 155.52 Mbps STS-3/STM-1 serial data output respectively, which can interface to an optical module. The PISO bit interleaves parallel data input into a serial bit stream taking the first bit from TXDI7, then the first bit from TXDI6, and so on as shown in Figure 15.

FIGURE 15. SIMPLIFIED BLOCK DIAGRAM OF PISO



3.6 Clock Multiplier Unit (CMU) and Re-Timer

The clock synthesizer uses a 77.76 MHz or a 19.44 MHz reference clock to generate the 622.08 MHz (for STS-12/STM-4) or 155.52 MHz (for STS-3/STM-1) SONET/SDH transmit serial data rate frequency. Differential LVPECL input REFCLKP/N accepts a clock reference of 77.76 MHz or 19.44 MHz to synthesize a high speed 622.08 MHz clock for STS-12/STM-4 or 155.52 MHz clock for STS-3/STM-1 applications. Optionally, if a Differential LVPECL clock source is not available, TTLREFCLK can accept an LVTTL clock signal. The clock synthesizer uses a PLL to lock-on to the differential input REFCLKP/N or Single-Ended input TTLREFCLK reference clock. The REFCLKP/N input should be generated from an LVPECL crystal oscillator which has a frequency accuracy better than 20ppm in order for the transmitted data rate frequency to have the necessary accuracy required for SONET systems. If the TTLREFCLK reference clock is used, the TTLREFCLK reference input should be tied to a LVTTL crystal oscillator with 20ppm accuracy. The two reference clocks are XNOR'ed and the choice between the LVPECL and LVTTL clocks are controlled tying either REFCLKP or TTLREFCLK to ground. Table 1, on page 12 shows the CMU reference clock frequency settings. Table 14 specifies the Clock Multiplier Unit performance characteristics.

TABLE 14: CLOCK MULTIPLIER UNIT PERFORMANCE

NAME	PARAMETER	MIN	TYP	MAX	UNITS
REF_{DUTY}	Reference clock duty cycle	40		60	%
REF_{JIT}	Reference clock jitter (rms) with 19.44 MHz reference[1]			5	ps
REF_{JIT}	Reference clock jitter (rms) with 77.76 MHz reference[1]			13	ps
REF_{TOL}	Reference clock frequency tolerance[2]	-20		+20	ppm
$ECLK_{JIT}$	STS-3/STM-1 Electrical Clock output jitter (rms) with 19.44 MHz reference		1		mUI_{rms}
$ECLK_{JIT}$	STS-12/STM-4 Electrical Clock output jitter (rms) with 19.44 MHz reference		5		mUI_{rms}
$ECLK_{JIT}$	STS-3/STM-1 Electrical Clock output jitter (rms) with 77.76 MHz reference		2		mUI_{rms}
$ECLK_{JIT}$	STS-12/STM-4 Electrical Clock output jitter (rms) with 77.76 MHz reference		4		mUI_{rms}
$OCLK_{FREQ}$	Frequency output	620		624	MHz
$OCYC_{DUTY}$	Clock output duty cycle ('1010' data pattern)	45		55	%

Jitter specification is defined using a 12kHz to 1.3/5MHz LP-HP single-pole filter.

[1]These reference clock jitter limits are required for the outputs to meet SONET system level jitter requirements (<10 mUI_{rms}).

[2]Required to meet SONET output frequency stability requirements.

3.7 Loop Timing and Clock Control

Two types of loop timing are possible in the XRT91L30.

In the internal loop timing mode, loop timing is controlled by the LOOPTIME pin. This mode is selected by asserting the LOOPTIME signal to a high level. When the loop timing mode is activated, the CMU synthesized hi-speed reference clock input to the Retimer is replaced with the hi-speed internally recovered receive clock coming from the CDR. Under this condition both the transmit and receive sections are synchronized to the internally recovered receive clock. Loop time mode directly locks the Retimer to the recovered receive clock.

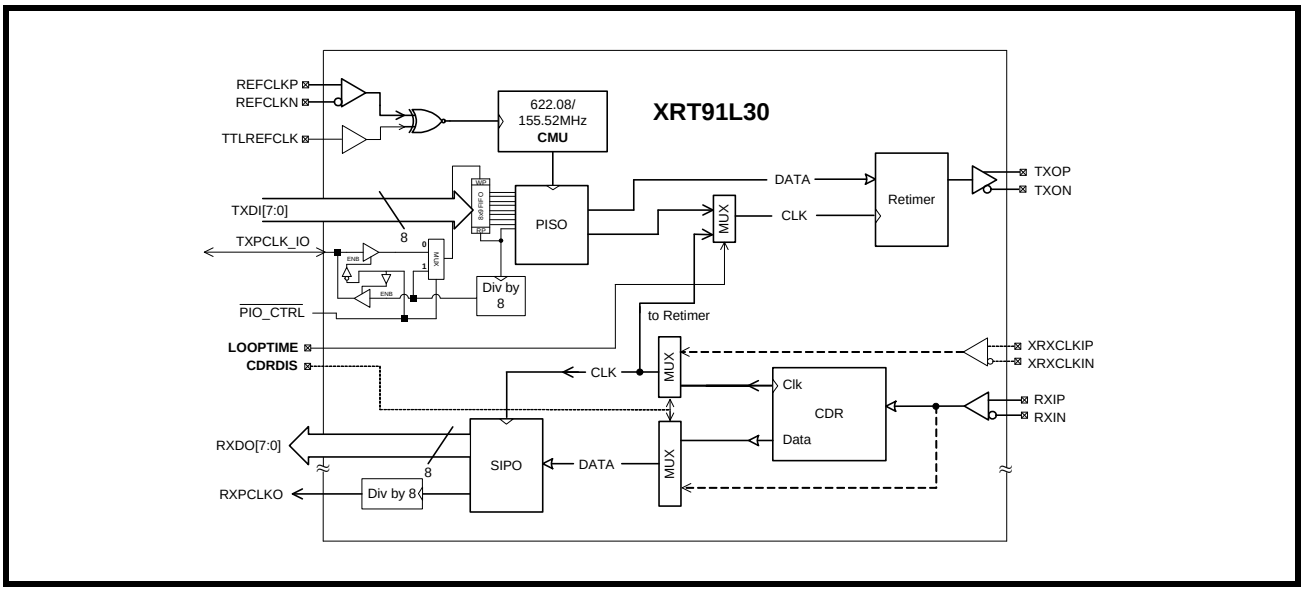
In external loop timing mode, the XRT91L30 allows the user the flexibility of using an externally recovered receive clock for retiming the high speed serial data. First, the CDRDIS input pin should be set high. By doing so, the internal CDR is disabled and bypassed and the XRT91L30 will sample the incoming high speed serial data on RXIP/N with the externally recovered receive clock connected to the XRXCLKIP/N inputs. In this state, the receive clock de-jittering and recovery is done externally and fed thru XRXCLKIP/N and the XRT91L30 will sample RXIP/N on the rising edge of XRXCLKIP/N. Secondly, the LOOPTIME pin must also be set high in order to select the externally recovered receive clock on XRXCLKIP/N as the reference clock source for the transmit serial data output stream TXOP/N.

Table 15 provides configuration for selecting the loop timing and clock recovery modes. The use of the on-chip CDR or an external recovered clock in loop timing applications is shown in Figure 16.

TABLE 15: LOOP TIMING AND CLOCK RECOVERY CONFIGURATIONS

CDRDIS	LOOPTIME	TRANSMIT CLOCK SOURCE	RECEIVE CLOCK SOURCE
0	**0**	Clock Multiplier Unit	CDR Enabled. Clock and Data recovery by internal CDR
0	**1**	Internal CDR	CDR Enabled. Clock and Data recovery by internal CDR
1	**0**	Clock Multiplier Unit	CDR Disabled. Externally recovered Receive Clock from XRXCLKIP/N 622.08/155.52 Mbps data on RXIP/N sampled at rising edge of XRXCLKIP/N
1	**1**	External CDR thru XRXCLKIP/N	CDR Disabled. Externally recovered Receive Clock from XRXCLKIP/N 622.08/155.52 Mbps data on RXIP/N sampled at rising edge of XRXCLKIP/N

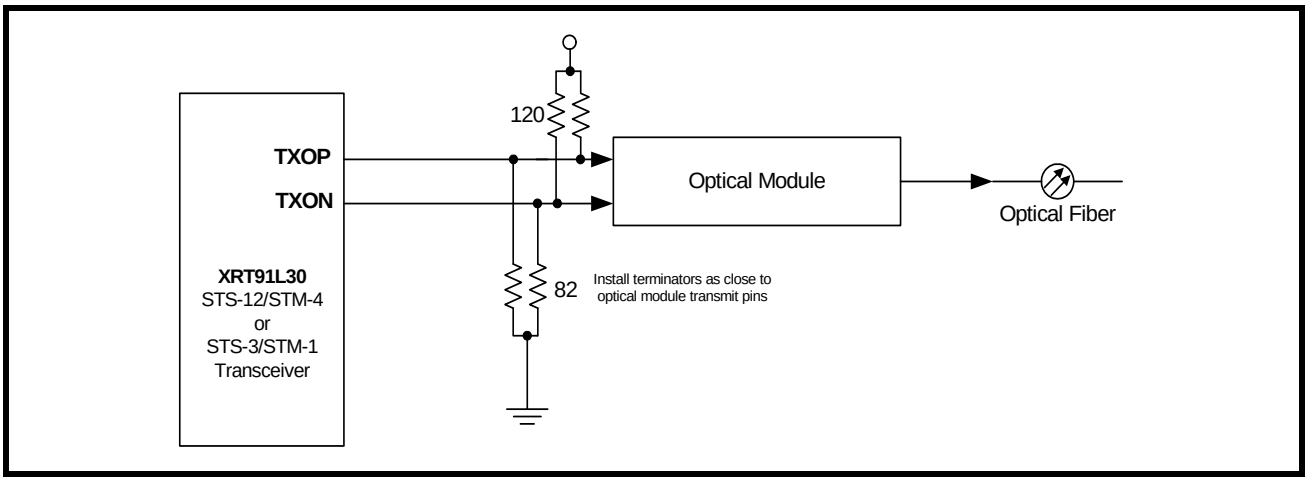
FIGURE 16. LOOP TIMING MODE USING INTERNAL CDR OR AN EXTERNAL RECOVERED CLOCK



3.8 Transmit Serial Output Control

The 622.08 Mbps STS-12/STM-4 or 155.52 Mbps STS-3/STM-1 transmit serial output is avaliable on TXOP/N pins. The transmit serial output can be AC or DC coupled to an optical module or electrical interface. A simplified DC coupling block diagram is shown in Figure 17.

FIGURE 17. TRANSMIT SERIAL OUTPUT INTERFACE BLOCK



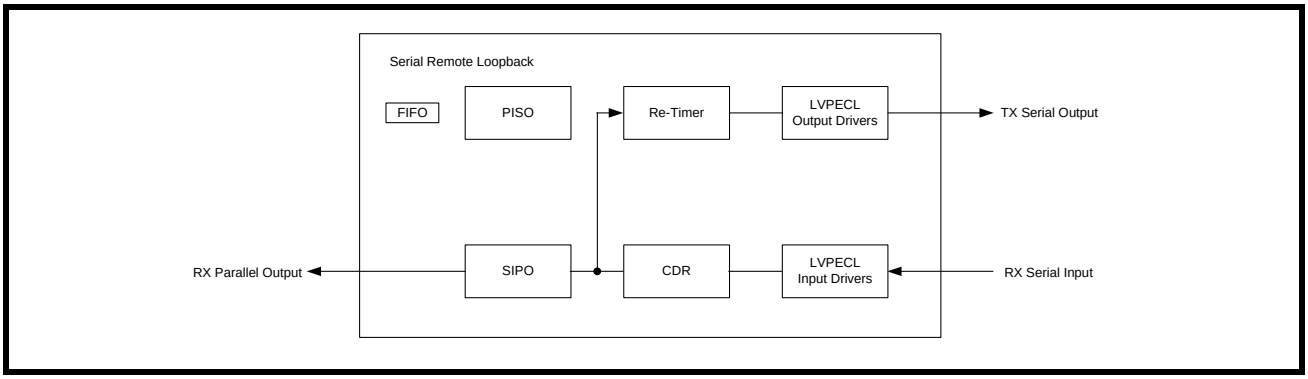
NOTE: *Some optical modules integrate AC coupling capacitors within the module. AC or DC coupling is largely specific to system design and optical module of choice.*

4.0 DIAGNOSTIC FEATURES

4.1 Serial Remote Loopback

The serial remote loopback function is activated by setting RLOOPS "High". When serial remote loopback is activated, the high-speed serial receive data from RXIP/N is presented at the high speed transmit output TXOP/N, and the high-speed recovered clock is selected and presented to the high-speed transmit clock input of the Retimer. During serial remote loopback, the high-speed receive data (RXIP/N) is also converted to parallel data and presented at the low-speed receive parallel interface RXDO[7:0]. The recovered receive clock is also divided by 8 and presented at the low-speed clock output RXPCLKO to synchronize the transfer of the 8-bit received parallel data. A simplified block diagram of serial remote loopback is shown in Figure 18.

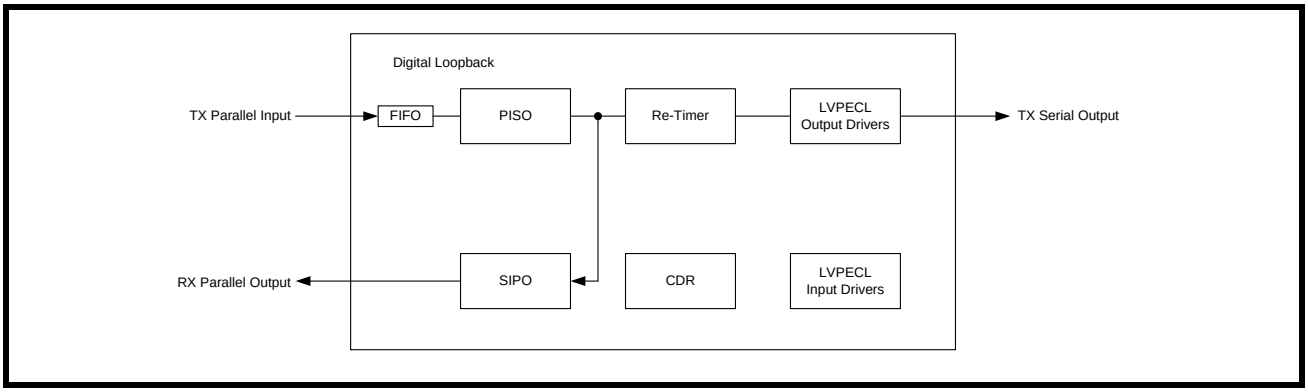
FIGURE 18. SERIAL REMOTE LOOPBACK



4.2 Digital Local Loopback

The digital local loopback is activated when the DLOOP signal is set "High." When digital local loopback is activated, the high-speed data from the output of the parallel to serial converter is looped back and presented to the high-speed input of the receiver serial to parallel converter. The CMU output is also looped back to the receive section and is used to synchronize the transfer of the data through the receiver. In Digital loopback mode, the transmit data from the transmit parallel interface TXDI[7:0] is serialized and presented to the high-speed transmit output TXOP/N using the high-speed 622.08/155.52 MHz transmit clock generated from the clock multiplier unit and presented to the input of the Retimer and SIPO. A simplified block diagram of digital loopback is shown in Figure 19.

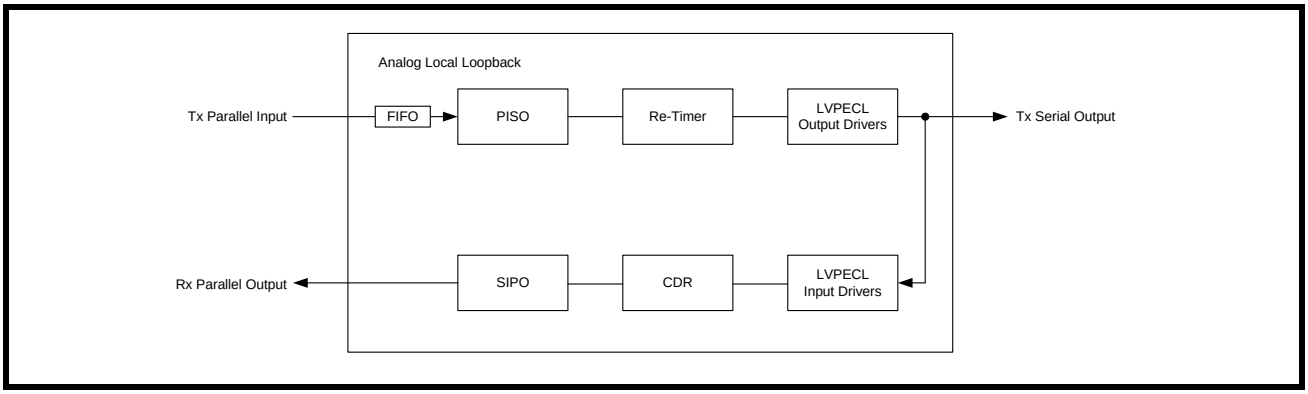
FIGURE 19. DIGITAL LOCAL LOOPBACK



4.3 Analog Local Loopback

Analog Local Loopback (ALOOP) controls a more comprehensive version of digital local loopback in which the point where the transmit data is looped back is moved all the way back to the high-speed receive I/O. The transmit data from the transmit parallel interface TXDI[7:0] is serialized and presented to the high-speed transmit output TXOP/N using the high-speed 622.08/155.52 MHz transmit clock generated from the clock multiplier unit. In addition, the high-speed transmit data TXOP/N is looped back to the receive clock and data recovery unit, replacing the RXIP/N. The signal is then processed by the CDR, and is sent through the serial to parallel converter and presented at the low-speed receive parallel interface RXDO[7:0]. ALOOP is invoked by asserting the ALOOP pin "High." A simplified block diagram of parallel remote loopback is shown in Figure 20.

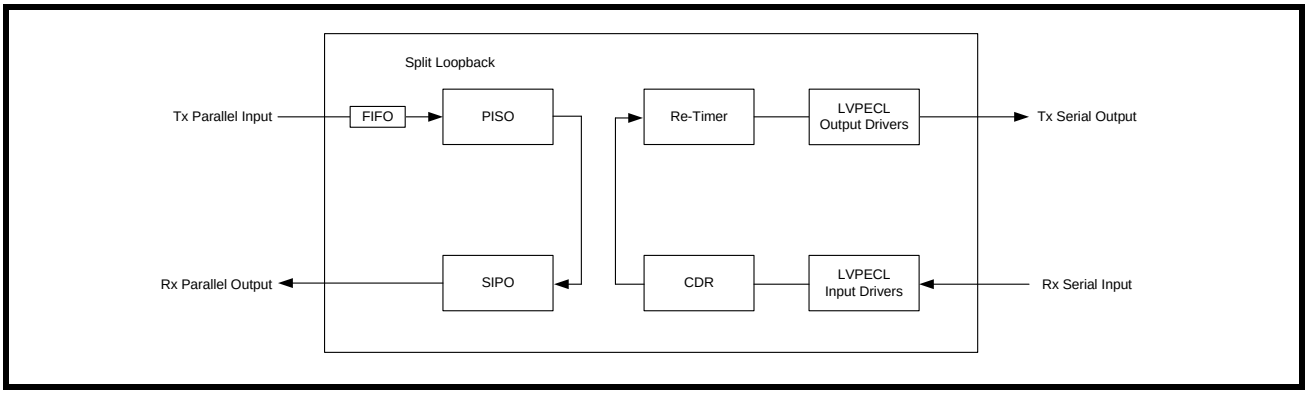
FIGURE 20. ANALOG LOCAL LOOPBACK



4.4 Split Loopback

The serial remote loopback and the digital local loopback can be combined to form a split loopback. The output of the parallel to serial converter is looped back and presented to the high-speed input of the receiver serial to parallel converter. The high-speed serial receive data from RXIP/N is presented at the high speed transmit output TXOP/N, and the high-speed recovered clock is selected to re-time the high speed transmit data output. A simplified block diagram of parallel remote loopback is shown in Figure 21.

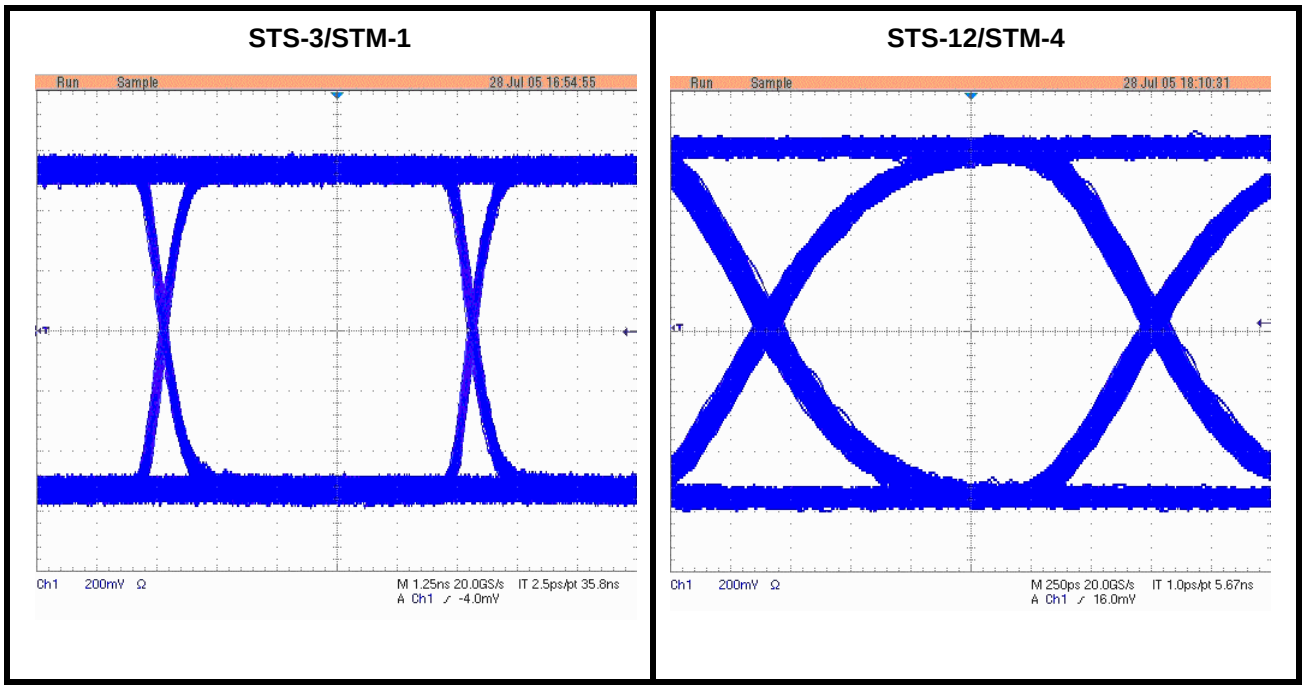
FIGURE 21. SPLIT LOOPBACK



4.5 Eye Diagram

The XRT91L30 Eye diagram illustrates the transmit serial output signal integrity and quality.

FIGURE 22. TRANSMIT ELECTRICAL OUTPUT EYE DIAGRAM



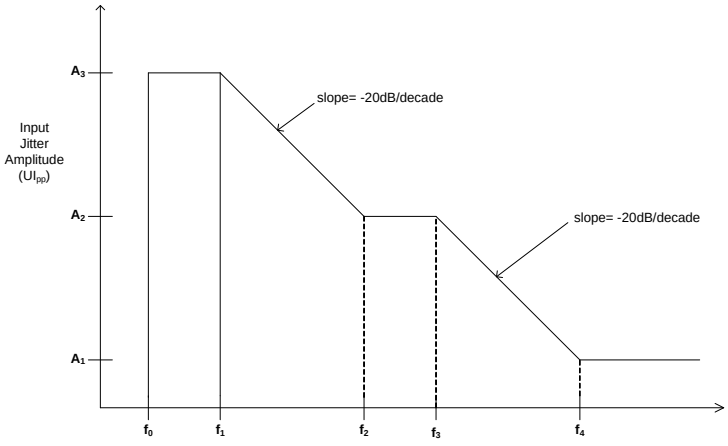
4.6 SONET Jitter Requirements

SONET equipment jitter requirements are specified for the following three types of jitter. The definitions of each of these types of jitter are given below. SONET equipment jitter requirements are specified for the following three types of jitter.

4.6.1 Jitter Tolerance:

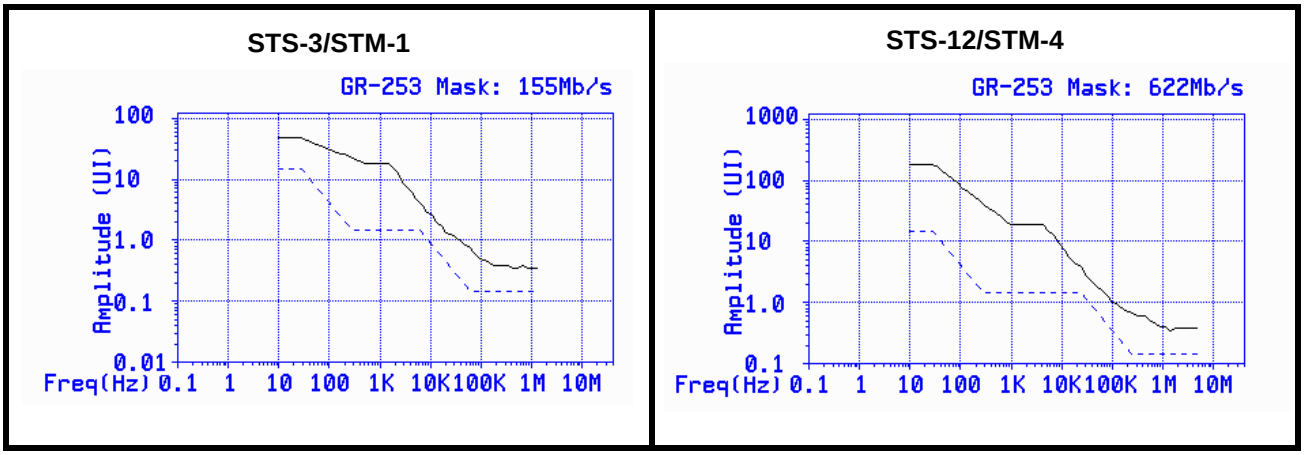
Jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied on the input OC-N equipment interface that causes an equivalent 1dB optical power penalty. OC-1/STS-1, OC-3/STS-3, OC-12 and OC-48 category II SONET interfaces should tolerate, the input jitter applied according to the mask of Figure 23, with the corresponding parameters specified in the figure.

FIGURE 23. GR-253 JITTER TOLERANCE MASK



OC-N/STS-N LEVEL	F0 (HZ)	F1 (HZ)	F2 (HZ)	F3 (HZ)	F4 (HZ)	A1 (UIPP)	A2 (UIPP)	A3 (UIPP)
1	10	30	300	2K	20K	0.15	1.5	15
3	**10**	**30**	**300**	**6.5K**	**65K**	**0.15**	**1.5**	**15**
12	**10**	**30**	**300**	**25K**	**250K**	**0.15**	**1.5**	**15**
48	10	600	6000	100K	1000K	0.15	1.5	15

FIGURE 24. XRT91L30 MEASURED JITTER TOLERANCE



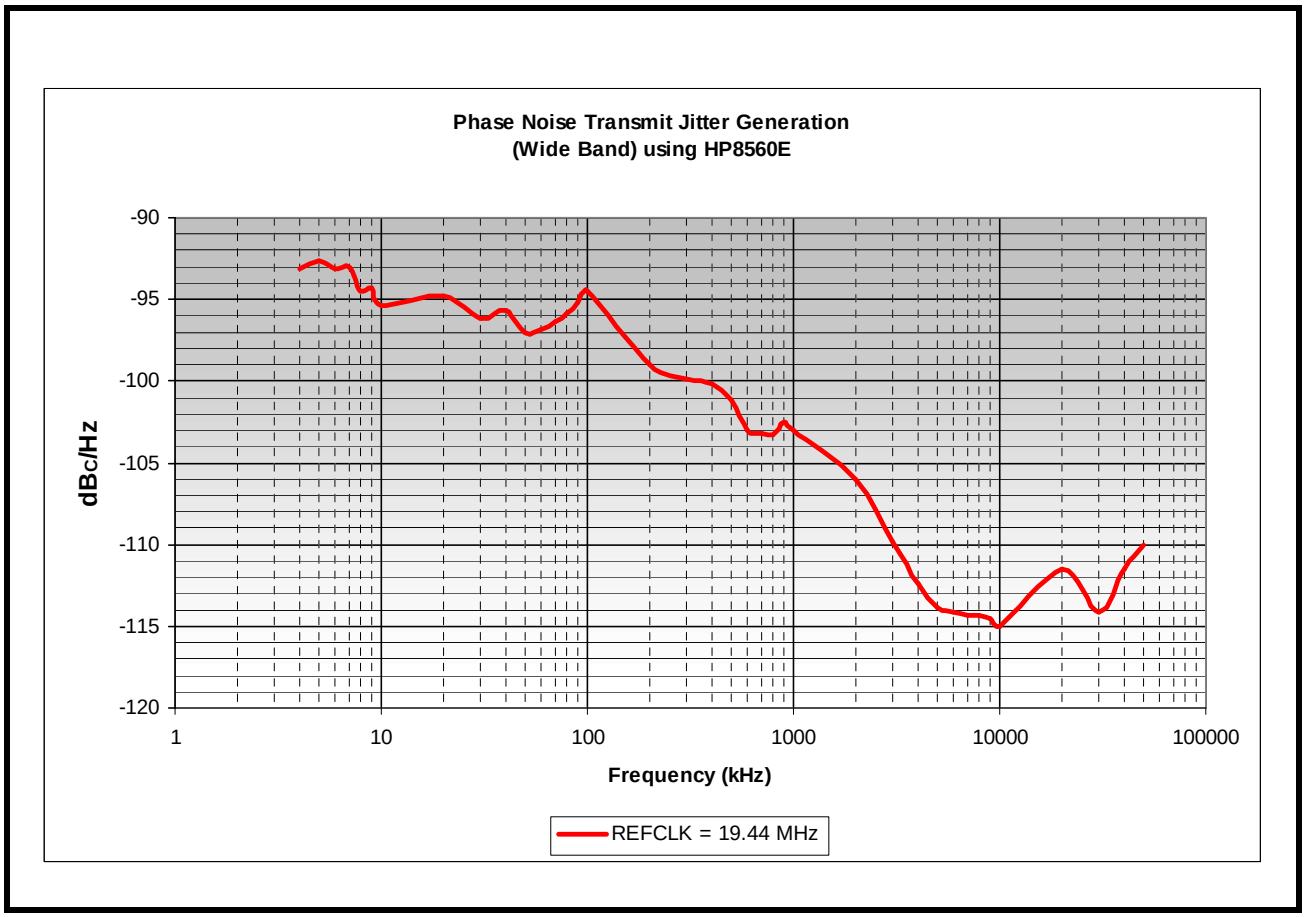
4.6.2 Jitter Generation

Jitter generation is defined as the amount of jitter at the STS-N output in the absence of applied input jitter. The Bellcore and ITU requirement for this type jitter is 0.01UI rms measured with a specific band-pass filter.

For more information on these specifications refer to Bellcore TR-NWT-000253 sections 5.6.2-5 and GR-253-CORE section 5.6.

Phase noise plot shows the power of the noise with respect to the carrier power. When this curve is integrated in the frequency band of interest, the outcome is the noise power. Jitter generation in rms is then derived by factoring with the appropriate period for the clock cycle.

FIGURE 25. XRT91L30 MEASURED ELECTRICAL PHASE NOISE TRANSMIT JITTER GENERATION AT 622.08 MBPS STS-12/STM4 USING '1010' OUTPUT PATTERN



5.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Thermal Resistance of QFP Package.....Θ_{jA} = 45℃/W		Operating Temperature Range.....-40℃ t o 85℃
Thermal Resistance of QFP Package.....Θ_{jC} = 12℃/W		Case Temperature under bias.....-55℃ to 125℃
ESD Protection (HBM).....>2000V		Storage Temperature .....-65℃ to 150℃

ABSOLUTE MAXIMUM POWER AND INPUT/OUTPUT RATINGS

SYMBOL	TYPE	PARAMETER	MIN.	TYP.	MAX.	UNITS
$VDD_{3.3}$		CMOS Digital Power Supply	-0.5		6.0	V
VDD_{LVPECL}		PECL I/O Power Supply	-0.5		6.0	V
$AVDD_{\_IO}$		3.3V Analog I/O and Power Supply	-0.5		6.0	V
	LVPECL	DC logic signal input voltage	-0.5		VDD_{LVPECL} +0.5	V
	LVTTL	DC logic signal input voltage	-0.5		5.5	V
	LVTTL	DC logic signal output voltage	-0.5		$VDD_{3.3}$ +0.5	V
	LVPECL	Input current	-100		100	mA
	LVTTL	Input current	-100		100	mA

NOTE: *Stresses listed under Absolute Maximum Power and I/O ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods will severely affect device reliability.*

POWER AND CURRENT DC ELECTRICAL CHARACTERISTICS

Test Conditions: VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	TYPE	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$VDD_{3.3}$		Power Supply Voltage	3.135	3.3	3.465	V	
$AVDD_{3.3}$		Transmit Power Supply Voltage (AVDD3.3_TX)	3.135	3.3	3.465	V	
$AVDD_{3.3}$		Receiver Power Supply Voltage (AVDD3.3_RX)	3.135	3.3	3.465	V	
VDD_{LVPECL}		PECL I/O Power Supply Voltage	3.135	3.3	3.465	V	
I_{DD-OC3}		Total Power Supply Current		200		mA	
$I_{DD-OC12}$		Total Power Supply Current		242		mA	
P_{DD-OC3}		Total Power Consumption		660		mW	
$P_{DD-OC12}$		Total Power Consumption		800		mW	

LVPECL AND LVTTL LOGIC SIGNAL DC ELECTRICAL CHARACTERISTICS

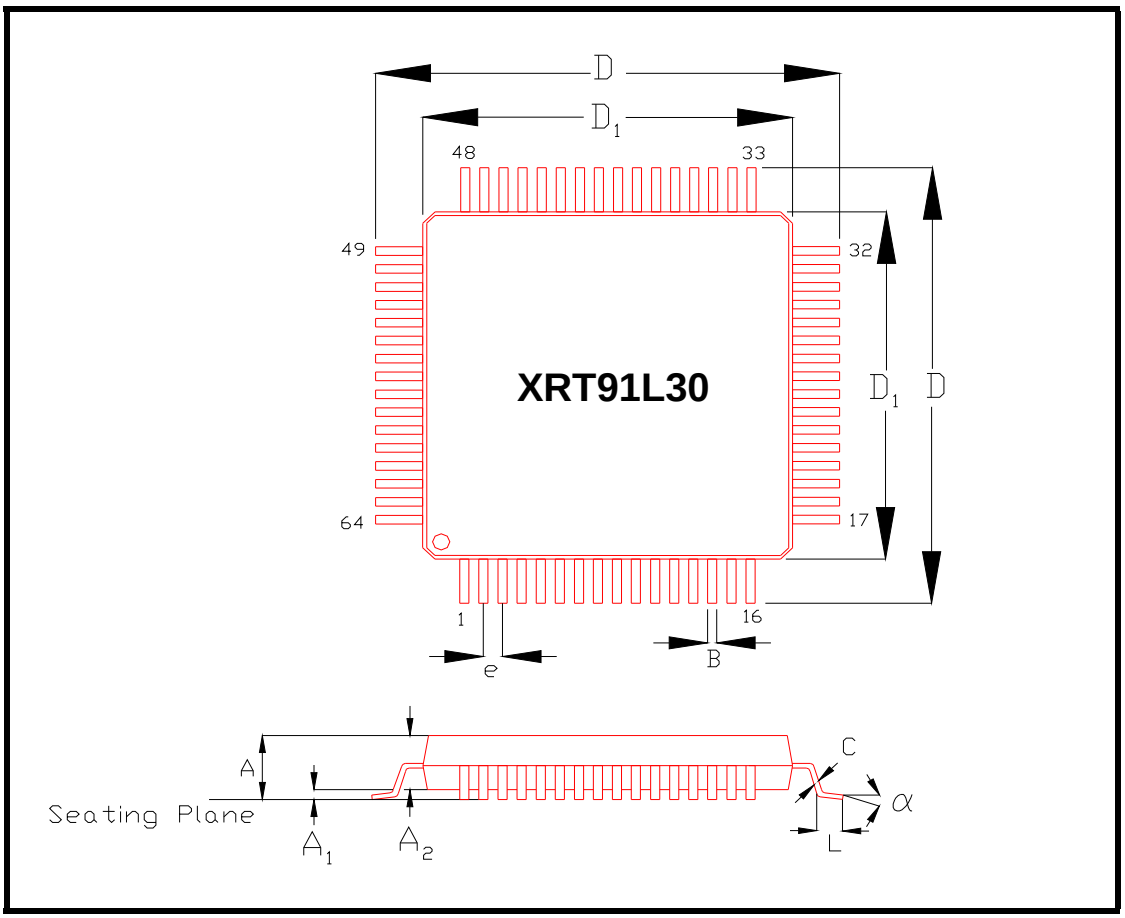
Test Conditions: VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	TYPE	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{OH}	LVPECL	Output High Voltage			VDD_{LVPECL} - 0.9	V	
V_{OL}	LVPECL	Output Low Voltage	0.7			V	
V_{OCOMM}	LVPECL	Output Common Mode Voltage	1.1		VDD_{LVPECL} - 1.3	V	
V_{ODIFF}	LVPECL	Output Differential Voltage	600		1300	mV	Terminate with 50Ω to VDD_{LVPECL}- 2.0
V_{IH}	LVPECL	Input High Voltage	VDD_{LVPECL} - 0.9		VDD_{LVPECL} - 0.3	V	For Single-Ended
V_{IL}	LVPECL	Input Low Voltage	0		VDD_{LVPECL} - 1.72	V	For Single-Ended
V_{IDIFF}	LVPECL	Input PECL Differential Voltage	400		1600	mV	
V_{ICOMM}	LVPECL	Input PECL Common Mode Voltage	1.5 - $\Delta V_{IN}/2$		VDD_{LVPECL} -1.0 -$\Delta V_{IN}/2$	V	
V_{OH}	LVTTL	Output High Voltage	2.0			V	I_{OH} = -1.0mA
V_{OL}	LVTTL	Output Low Voltage	0		0.8	V	I_{OH} = 1.0mA
V_{IH}	LVTTL	Input High Voltage	2.0			V	
V_{IL}	LVTTL	Input Low Voltage	0		0.8	V	
I_{IH}	LVTTL	Input High Current		50	500	µA	2.0V<V_{IN}<5.5V V_{IN}=2.4V typical
I_{IL}	LVTTL	Input Low Current			-500	µA	-0.5V<V_{IN}<0.8V

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT91L30IQ	64-pin Plastic Quad Flat Pack (10.0 x 10.0 x 2.0 mm, QFP)	-40°C to +85°C

PACKAGE DIMENSIONS



Note: The control dimension is in millimeters.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.072	0.096	1.82	2.45
A1	0.010	0.020	0.25	0.50
A2	0.071	0.087	1.80	2.20
B	0.007	0.011	0.17	0.27
C	0.004	0.009	0.11	0.23
D	0.510	0.530	12.95	13.45
D1	0.390	0.398	9.90	10.10
e	0.0197 BSC		0.50 BSC	
L	0.029	0.041	0.73	1.03
α	0°	7°	0°	7°

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.0	January 2005	First draft of XRT91L30 datasheet.
P1.0.1	February 2005	Preliminary limited release version of XRT91L30 datasheet.
P1.0.2	February 2005	Corrected package type to IQ. Changed MHz to Mbps in PISO and SIPO section.
P1.0.3	March 2005	1.CAP1,CAP2,CAP3,CAP4 pin names changed to CAP1P, CAP2P, CAP1N, CAP2N respectively. 2.Added “Section 2.3.1, Internal Clock and Data Recovery Bypass” on page 16 4.Corrected external receive loop filter capacitors from 0803 to 0603 industry size in Section 2.4,External Receive Loop Filter Capacitors. 5.Corrected LOOPTIME bit description. 6.Enhanced " Section 2.2,Recieve Serial Data Input Timing, Section 2.3,Receive Clock and Data Recovery. 7.Enhanced Section 3.2,Transmit Parallel Data Input Timing, Section 3.6,Clock Multiplier Unit (CMU) and Re-Timer, and Section 3.7,Loop Timing and Clock Control. 8.Enhanced Loopback diagrams on "Section 4.0,diagnostic features."
P1.0.4	May 2005	1.Added $\overline{\text{PIO\_CTRL}}$ pin description. 2.Removed support for pull-ups and pull-downs on all control input pins except $\overline{\text{PIO\_CTRL}}$. 3.Added internal biasing notes in REFCLKP/N pin description. 4.Corrected V_{OCOMM}, V_{IH}, and V_{IDIFF}, V_{ICOMM} in LVPECL electrical characteristics table. 5.Corrected typo "TXDOP/N" in table 2. 6.Added FIFO and $\overline{\text{PIO\_CTRL}}$ control block in pertinent diagrams. 7.Revised Transmit Parallel Input Interface and added Transmit FIFO section. 8.Added Receive Jitter Tolerance parameter in CDR unit performance table.
P1.0.5	August 2005	1.Updated performance numbers. Removed TBD’s.
P1.0.6	September 2005	1.Updated transmit parallel clock timing information. 2.Fig. 3 RXIP/N and Fig. 17 TXOP/N changed to DC coupling.
P1.0.7	October 2005	1.Added intructions for unused pins in pin description and diagrams. 2.Removed external loop filter 0603 capacitor size requirement.
P1.0.8	January 2006	1.Changed TXPCLK_IO setup time (t_{TXDI_SU}) to 2ns. 2.Corrected RXDO[7:0] pin description to "update on falling edge". 3.Removed subscript on TXPCLK_IO in Table 10, Table 11, Table 12, & Table 13. 4.Revised standards compliance list on page 2. 5.Changed CAP1P, CAP2P, CAP1N, CAP2N pin description title. 6.Revised Section 4.5 and 4.6.1. 7.Removed TA = 25℃ test condition from electrical characteristics table.

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Datasheet January 2006.