FEATURES

- Performs clock and data recovery for selectable data of 622.08 Mbps (STS-12/STM-4) or 155.52 Mbps (STS-3/STM-1) NRZ data
- Meets Telcordia, ANSI and ITU-T G.783 and G.825 SDH jitter requirements including T1.105.03 - 2002 SONET Jitter Tolerance specification, and GR-253 CORE, GR-253 ILR SONET Jitter specifications.
- LOCK is a status output that monitors data run length and frequency drift away from the reference clock
- Data is resampled at the output
- Active High Signal Detect (SIGD) LVPECL input
- Low jitter, high-speed outputs support LVPECL and low-power LVDS termination
- 19.44 MHz reference frequency LVTTL input
- Low power: 215 mW typical
- 3.3V power supply
- 20-pin TSSOP package
- Requires one external capacitor
- PLL bypass operation facilitates board debug process
- ESD greater than 2kV on all pins
- Enhanced Jitter performance
- Meets both Jitter tolerance and generation requirements

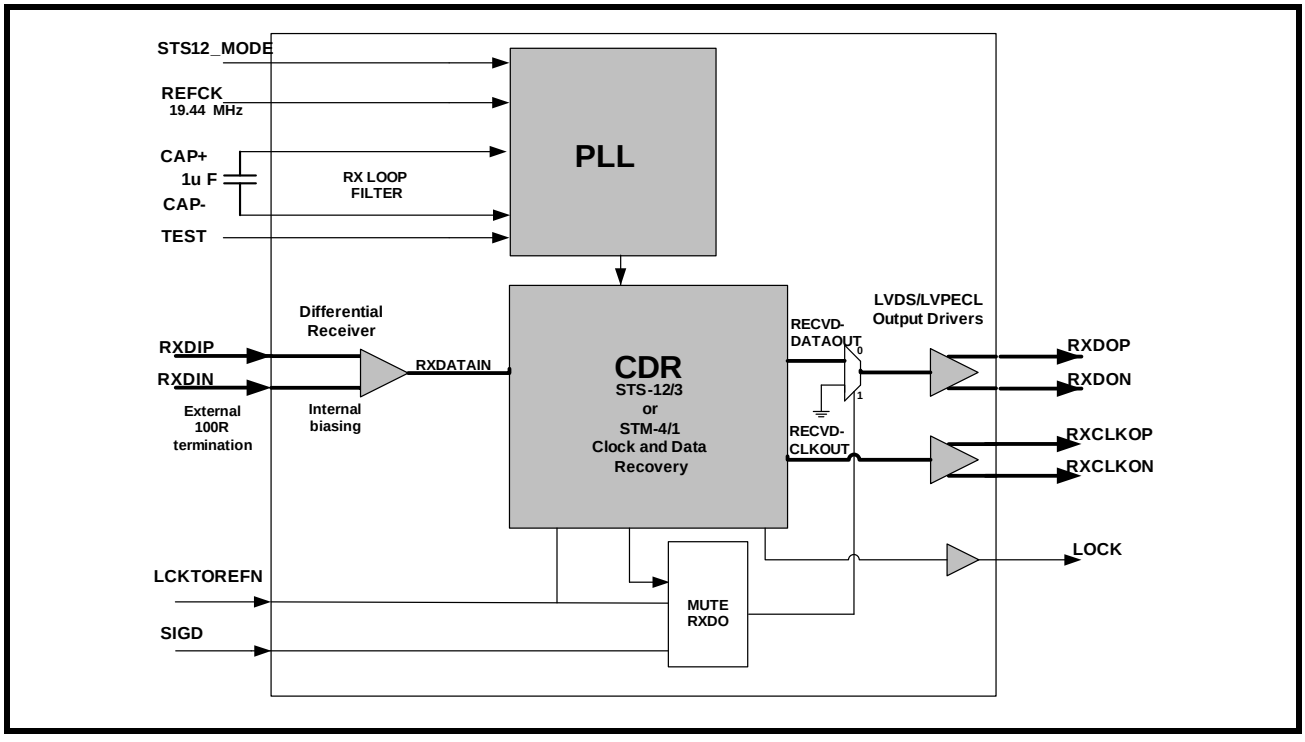
APPLICATIONS

- SONET/SDH-based Transmission Systems
- DSLAMS and Add/Drop Multiplexers
- Cross Connect Equipment
- ATM and Multi-Service Switches, Routers and Switch/Routers
- DWDM Termination Equipment

GENERAL DESCRIPTION

The XRT91L33A is a fully integrated multirate Clock and Data Recovery (CDR) device for SONET/SDH 622.08 Mbps STS-12/STM-4 or 155.52 Mbps STS-3/ STM-1 applications. The device provides Clock and Data Recovery (CDR) function by synchronizing its on-chip Voltage Controlled Oscillator (VCO) to the incoming serial scrambled non-return to zero (NRZ) data stream. Figure 1 shows the block diagram of the XRT91L33A.

FIGURE 1. BLOCK DIAGRAM OF XRT91L33A



CLOCK AND DATA RECOVERY OVERVIEW

The clock and data recovery (CDR) unit accepts high speed NRZ serial data from the Differential receiver and generates a clock with a frequency equal to that of the incoming data. The CDR block uses a reference clock to train and monitor its clock recovery PLL. Upon startup, the PLL locks to the local reference clock. Once this is achieved, the PLL attempts to lock onto the incoming receive serial data stream. Whenever the recovered clock frequency deviates from the local reference clock frequency by more than approximately ±500 ppm, the clock recovery PLL will switch and lock back onto the local reference clock and declare a Loss of Lock. Whenever a Loss of Lock or a Loss of Signal event occurs, the CDR will continue to supply a recovered clock (based on the local reference) to the framer/mapper device. An LOS condition occurs when either SIGD or LCKTOREFN is low. In this case, the receive serial data output is forced to a logic zero state for the entire duration of the LOS condition. This acts as a receive data mute upon LOS function to prevent random noise from being misinterpreted as valid incoming data. When SIGD becomes active again, the recovered clock is determined to be within ±500 ppm accuracy with respect to the local reference source and LOS is no longer declared, the clock recovery PLL will switch and lock back onto the incoming receive serial data stream.

FIGURE 2. 20 PIN TSSOP OF XRT91L33A (TOP VIEW)

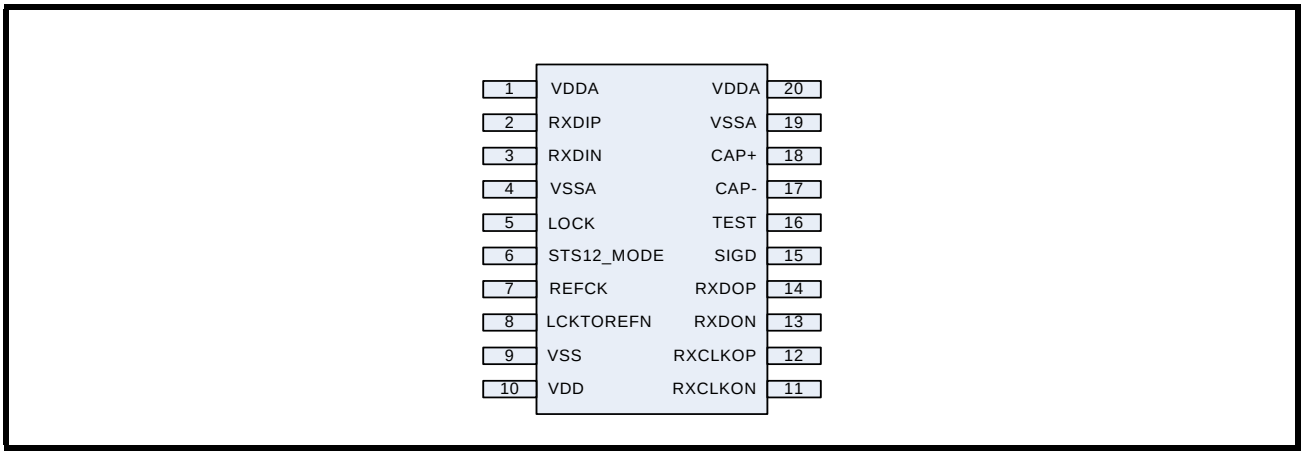


TABLE 1: ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT91L33AIG-F	20-Pin TSSOP Lead-Free Package	-40°C to +95°C

1.0 PIN DESCRIPTIONS

TABLE 2: PIN DESCRIPTION TABLE

NAME	LEVEL	TYPE	PIN	DESCRIPTION
VDDA	PWR	PWR	1	3.3V Power supply
RXDIP	LVDS/PECL	I	2	Positive side of receive data input. The high-speed output clock (RXCLKOP/N) is recovered from this high-speed differential input data.
RXDIN	LVDS/PECL	I	3	Negative side of receive data input. The high-speed output clock (RXCLKOP/N) is recovered from this high-speed differential input data.
VSSA	PWR	PWR	4	Ground pin
LOCK	LVPECL	O	5	Active HIGH to indicate that the PLL is locked to serial data input and valid clock and data are present at the serial outputs (RXDOP/N and RXCLKOP/N). The LOCK will go inactive under the following conditions: • If SIGD is set LOW • If LCKTOREFN is set LOW • If the VCO has drifted away from the local reference clock, REFCK, by more than +/- 500 ppm
STS12_MODE	LVTTL	I	6	STS-12 or STS-3 mode selection. Set HIGH to select the STS-12 operation. Set LOW for STS-3 operation
REFCK	LVTTL	I	7	Local 19.44 MHz reference clock input for the CDR. REFCK is used for the PLL phase adjustment during power up. It also serves as a stable clock source in the absence of serial input data.
LCKTOREFN	LVTTL	I	8	Lock to REFCK input. When set LOW, this pin causes the output clock, RXCLKOP/N to be held within +/- 500ppm of the input reference clock REFCL and forces the RXDOP/N to a low state.
VSS	PWR	PWR	9	Ground pin
VDD	PWR	PWR	10	3.3V power supply
RXCLKON	LVDS/ LVPECL	O	11	High-speed clock output, negative. This clock is recovered from the receive data input (RXDIP/N) and supports either LVDS or LVPECL termination
RXCLKOP	LVDS/ LVPECL	O	12	High-speed clock output, positive This clock is recovered from the receive data input (RXDIP/N) and supports either LVDS or LVPECL. termination
RXDON	LVDS/ LVPECL	O	13	High-speed output, negative This is the retimed version of the recovered data stream from RXDIP/N and can be in either LVDS or LVPECL termination
RXDOP	LVDS/ LVPECL	O	14	High-speed output, positive. This is the retimed version of the recovered data stream from RXDIP/N and can be in either LVDS or LVPECL termination

NAME	LEVEL	TYPE	PIN	DESCRIPTION
SIGD	LVPECL	I	15	Signal detect. SIGD should be connected to the SIGD output on the optical module. SIGD is active HIGH. When SIGD is set HIGH, it means there is sufficient optical power. When SIGD is LOW, this indicates an LOS condition, the RXCLKOP/N output signal will be held to within +/- 500 ppm of the REFCK input. Additionally, the RXDOP/N will be held in the LOW state.
TEST	LVTTL	I	16	Three-level input: Set to VSS for normal operation, VDD for improved Jitter transfer characteristics and 1.4V for bypass mode (used for production testing). Note: To improve Jitter transfer, set the TEST pin to VDD.
CAP-	Analog	I	17	Negative side of the external loop filter. The loop filter capacitor should be connected to these pins. The capacitor value should be 1.0 μF +/- 10%
CAP+	Analog	I	18	Positive side of the external loop filter. The loop filter capacitor should be connected to these pins. The capacitor value should be 1.0 μF +/- 10%.
VSSA	PWR	PWR	19	Ground pin
VDDA	PWR	PWR	20	3.3V power supply

2.0 FUNCTIONAL DESCRIPTION

The XRT91L33A CDR is designed to operate with a SONET Framer/ASIC device and provide a high-speed serial clock and data recovery interface to optical networks. The CDR receives a differential NRZ serial bit stream running at STS-12/STM-4 or STS-3/STM-1 and generates recovered serial clock and data via differential LVDS/LVPECL drivers.

2.1 Reference Clock Input

The XRT91L33A accepts a 19.44 MHz LVTTL clock input at REFCK. The REFCK should be generated from a source that has a frequency accuracy better than ±100ppm in order for the CDR Loss of Lock detector to have the necessary accuracy required for SONET systems.

2.2 Receive Clock and Data Recovery

The clock and data recovery (CDR) unit accepts the high-speed NRZ serial data from the Differential receiver and generates a clock that is the same frequency as the incoming data. The clock recovery block utilizes the reference clock from REFCK to train and monitor its clock recovery PLL. Upon startup, the PLL locks to the local reference clock. Once this is achieved, the PLL then attempts to lock onto the incoming receive serial data stream. Whenever the recovered clock frequency deviates from the local reference clock frequency by more than approximately ±500ppm, the clock recovery PLL will switch to the local reference clock, declare a Loss of Lock and output a LOW level signal on the LOCK output pin. Whenever a Loss of Lock (LOL) or a Loss of Signal (LOS) event occurs, the CDR will continue to supply a receive clock (based on the local reference).

2.3 External Receive Loop Filter Capacitor

For STS12/STM4 and STS3/STM1 operation, the XRT91L33A uses a 1.0uF external loop filter capacitor to achieve the required receiver jitter performance. It must be well isolated to prohibit noise entering the CDR block and should be placed as close to the pins as possible. The non-polarized capacitor should be of ±10% tolerance. Use type X7R or X5R capacitors for improved stability over temperature.

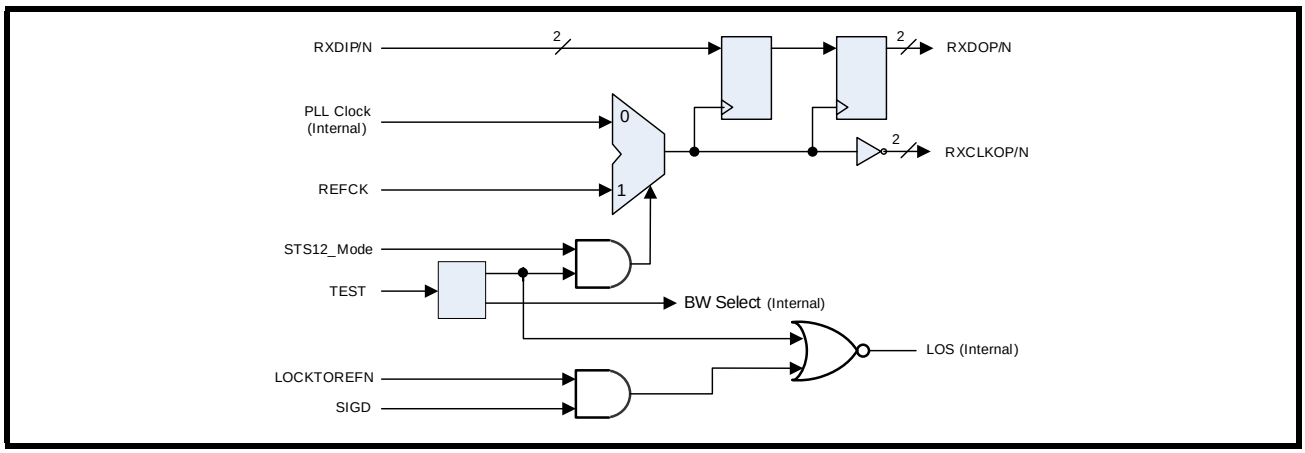
2.4 STS-12/STM-4 and STS-3/STM-1 Mode of Operation

The VCO output signal is fed into a programmable frequency divider allowing one to properly set the PLL operating frequency corresponding to the desired data rate. For 622.08 Mbps signal STS12_MODE is set HIGH and for 155.52 Mbps, STS12_MODE is set LOW.

2.5 Signal Detection

XRT91L33A has two control pins that are used to indicate an LOS condition (Loss Of Signal). The SIGD pin is a LVPECL input and the LCKTOREFN pin is a LVTTL input. They are internally connected as shown in Figure 3. If either of these two inputs goes LOW and TEST is LOW or HIGH, XRT91L33A will enter a Loss of Signal (LOS) state, and will mute the RXDOP/N. During the LOS state, XRT91L33A will also maintain RXCLKOP/N within ±500ppm of the input reference clock, REFCK. Most optical modules have an SIGD output. This SIGD output indicates that there is sufficient optical power and is typically active HIGH. If the SIGD output on the optical module is LVPECL, it should be connected directly to the SIGD input of XRT91L33A, and the LCKTOREFN input should be tied HIGH. If the SIGD output is LVTTL, it should be connected directly to the LCKTOREFN input and the SIGD input should be tied HIGH. The SIGD and LCKTOREFN inputs also can be used for other applications when it is required to hold RXCLKOP/N output within ±500ppm of the input reference clock and mute the serial data output lines.

FIGURE 3. CONTROL DIAGRAM FOR SIGNAL DETECTION CIRCUIT AND PLL TEST OPERATION



2.6 Lock Detection

XRT91L33A features a PLL lock detection circuit. The lock detect (LOCK) output goes HIGH to indicate that the PLL is locked to the serial data input and valid data and clock are present at the high-speed differential output. The LOCK output will go LOW if either the LOCKTOREFN or the SIGD input is forced LOW. Additionally, LOCK will also go low if the incoming data frequency is more than +/-500ppm away from the reference clock frequency (REFCK x 32 in OC12 mode, REFCK x 8 in OC3 mode). When LOCK output is driven LOW, the VCO is forced to lock to REFCK and then released to lock on the incoming data. If the incoming data frequency remains outside the +/-500ppm window, the training mode is repeated. Debounce logic stabilizes the LOCK output pin to stay LOW for incoming frequencies well beyond the +/-500ppm window.

2.7 Test Pin Functionality

The TEST pin on the XRT91L33A is a three-level control input - VDD, VSS and 1.4V. This pin determines the test (bypass) mode operation and controls the bandwidth of the PLL. Pulling this pin low sets the high bandwidth operation and is used for normal operation. Pulling this pin high sets the low bandwidth operation that is used for improved SONET jitter transfer performance. Applying 1.4V to the input configures the device into a bypass mode for use in production test.

2.7.1 Normal Operation

If the Test pin is held low the part functions normally with similar performance to the XRT91L33A. The PLL bandwidth is configured for high bandwidth.

2.7.2 Improved Jitter Transfer Operation

If the Test pin is held high the part optimizes the SONET jitter transfer performance. This mode is offered for applications where the jitter transfer characteristics are more critical. The PLL bandwidth is configured for low bandwidth.

2.7.3 Bypass Mode Operation

If TEST is set to 1.4V and STS12_MODE pin is set to logic HIGH, XRT91L33A will bypass the PLL and present an inverted version of the REFCK to the clock output RXCLKOP/N. REFCK's rising edge is used to capture the input data and transmit data to RXDOP/N. This bypass test operation can be used to facilitate board level debugging process.

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TABLE 3: SIGNAL DETECT AND TEST PIN OPERATION CONTROL

STS12_MODE	TEST	LCKTOREFN	SIGD	RXDO	RXCLKO
1	**1 or 0**	1	1	RXDI	PLL clock
1	**1 or 0**	1	0	Muted	PLL clock
1	**1 or 0**	0	1	Muted	PLL clock
1	**1 or 0**	0	0	Muted	PLL clock
1	**1.4V**	X	X	RXDI	REFCK
0	**1 or 0**	1	1	RXDI	PLL clock
0	**1 or 0**	1	0	Muted	PLL clock
0	**1 or 0**	0	1	Muted	PLL clock
0	**1 or 0**	0	0	Muted	PLL clock
0	**1.4V**	X	X	Not allowed	Not allowed

3.0 ELECTRICAL CHARACTERISTICS

3.1 Absolute Maximum RATINGS

TABLE 4: ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
V_{DD}	Power supply voltage, referenced to GND	-0.5	4.0	V
	DC input voltage (LVPECL, LVTTL)	-0.5	VDD+0.5	V
	Output current (LVDS or LVPECL)	-50	+50	mA
T_S	Storage Temperature	-65	150	°C
V_{ESD}	Electrostatic discharge voltage, human body model	-2000	2000	V

3.2 Operating Conditions

TABLE 5: RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNITS
V_{DD}	Power supply voltage	3.135	3.3	3.465	V
Temp	Operating Temperature under bias [1]	-40		95	°C
I_{DD}	Power supply current (outputs unterminated)		71	80	mA
P_D	Power dissipation (outputs unterminated)		234	277	mW

1. Lower limit of specification is ambient temperature, and upper limit is case temperature.

3.3 LVPECL Single Ended Input and Output DC characteristics

TABLE 6: LVPECL SINGLE ENDED INPUTS AND OUTPUTS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH voltage	V_{DD}-1.125		V_{DD}-0.5	V	Guaranteed input HIGH voltage
V_{IL}	Input LOW voltage	V_{DD}-2.0		V_{DD}-1.5	V	Guaranteed input LOW voltage
I_{IH}	Input HIGH current	-0.5		10	µA	$V_{IN} = V_{DD}$ - 0.5V
I_{IL}	Input LOW current	-0.5		10	µA	$V_{IN}=V_{DD}$-2.0V
V_{OL}	Output LOW voltage	V_{DD}-2.0		V_{DD}-1.8	V	50Ω to (V_{DD}-2.0V)
V_{OH}	Output HIGH voltage	V_{DD}-1.25		V_{DD}-0.67	V	50Ω to (V_{DD}-2.0V)

3.4 LVPECL Differential Input and Output DC characteristics

TABLE 7: LVPECL DIFFERENTIAL INPUTS AND OUTPUTS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH voltage	V_{DD}-1.75		V_{DD}-0.4	V	Guaranteed input HIGH voltage
V_{IL}	Input LOW voltage	V_{DD}-2.0		V_{DD}-0.7	V	Guaranteed input LOW voltage
I_{IH}	Input HIGH current	-0.5		10	µ A	$V_{IN\ DIFF}$ =0.5V
I_{IL}	Input LOW current	-0.5		10	µA	$V_{IN\ DIFF}$ =0.5V
V_{IDIFF}	Input PECL Differential Voltage, peak-to-peak swing (see Figure 4)	250			mV	
V_{OCM}	Output Common-Mode Voltage	0.8	1.35	1.7	V	50Ω to (V_{DD}-2.0V)
V_{ODIFF}	Output LVPECL Differential Voltage, peak-to-peak swing (see Figure 4)	800		1700	mV	50Ω to (V_{DD}-2.0V)

FIGURE 4. DIFFERENTIAL VOLTAGE SWING DEFINITIONS (INPUT OR OUTPUT) FOR CLOCK AND DATA

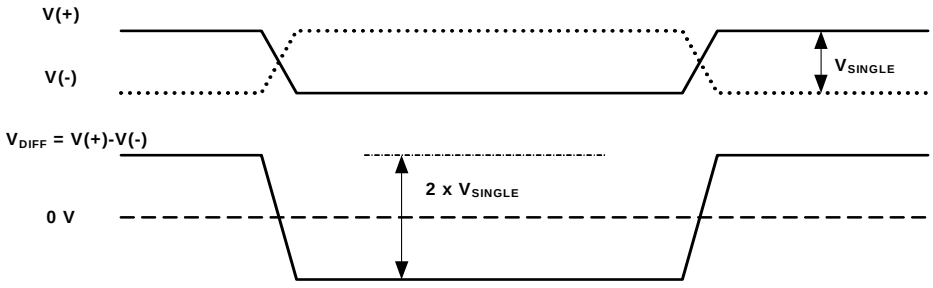


TABLE 8: LVDS OUTPUTS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{OCM}	Output common-mode voltage	1.0	1.35	1.7	V	100Ω between RXDOP/N and RXCLKP/N
V_{ODIFF}	Output LVDS Differential Voltage, peak-to-peak Swing (see Figure 4)	700		1700	mV	100Ω between RXDOP/N and RXCLKP/N

TABLE 9: LVTTL INPUTS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH voltage	2.0		V_{DD}	V	
V_{IL}	Input LOW voltage	0		0.8	V	
I_{IH}	Input HIGH current	-50		50	μA	VIN = 2.75 V, V_{DD} = Maximum
I_{IL}	Input LOW current	-50		50	μA	VIN = 0.5 V, V_{DD} = Maximum

3.5 AC Characteristics

TABLE 10: PERFORMANCE SPECIFICATIONS

Test Condition: VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
f	VCO center frequency		622.08		MHz	
f_{TOL}	CDR's reference clock frequency	-250		250	ppm	
fT_{REF_CLK}	OC-12/STS-12 capture range	-500		500	ppm	with respect to the fixed reference frequency
$CLKOUT_{DC}$	Clock output duty cycle	45		55	% UI	20% minimum transition density
t_{LOCK}	OC-12/STS-12 acquisition lock time			16	μs	Valid REFCK and device already powered up
t_{LOCK_R}, t_{LOCK_F}	LOCK output rise and fall time			500	ps	10% to 90%, with 100Ω and 5 pF capacitive equivalent load
J_{GEN_CLCK}	RXCLKOP/N jitter generation		0.005	0.01	U_{Irms}	
J_{TOL}	OC-12/STS-12 jitter tolerance	0.40	0.5		UI	Sinusoidal input jitter of RXDIP/N from 250 KHz to 5MHz

4.0 JITTER PERFORMANCE

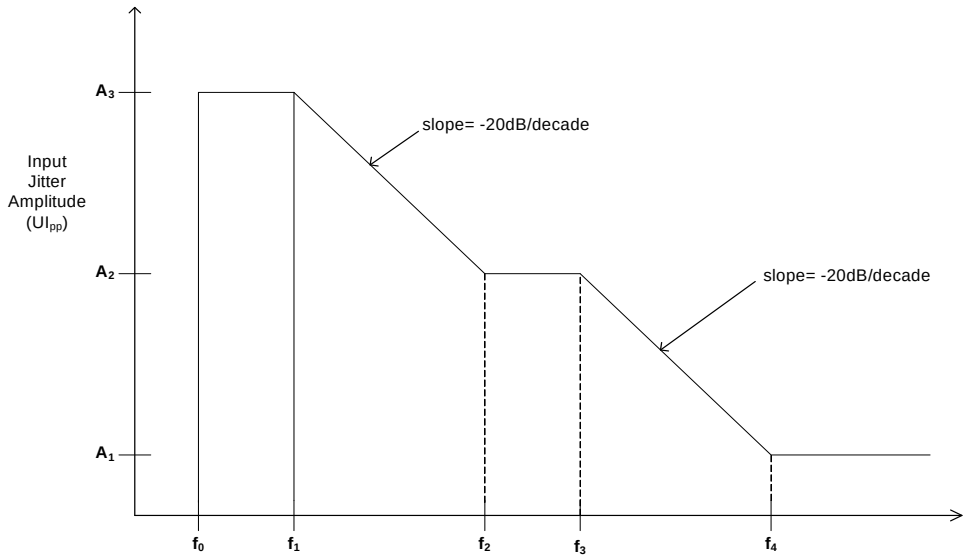
4.1 SONET Jitter Requirements

SONET receive equipment jitter requirements are specified jitter tolerance and jitter transfer. The definitions of each of these types of jitter are given below.

4.1.1 Rx Jitter Tolerance:

OC-3/STM-1, and OC-12/STM-4 category II SONET interfaces should tolerate, the input jitter applied according to the mask of **Figure 5**, with the corresponding specified parameters. Jitter measurements are done with standard SONET/SDH testers such as Acterna ANT20 as well as Agilent Omniber testers.

FIGURE 5. GR-253/G.783 JITTER TOLERANCE MASK



OC-N STM-X LEVEL	F0 (HZ)	F1 (HZ)	F2 (HZ)	F3 (HZ)	F4 (HZ)	A1 (UIPP)	A2 (UIPP)	A3 (UIPP)
OC1/STS1 STM0	**10**	**30**	**300**	**2K**	**20K**	**0.15**	**1.5**	**15**
OC3/STS3 STM1	**10**	**30**	**300**	**6.5K**	**65K**	**0.15**	**1.5**	**15**
OC12/STS12 STM4	**10**	**30**	**300**	**25K**	**250K**	**0.15**	**1.5**	**15**

FIGURE 6. XRT91L33A JITTER TOLERANCE AT 155 MBPS OC3/STM-1 (LOW BANDWIDTH)

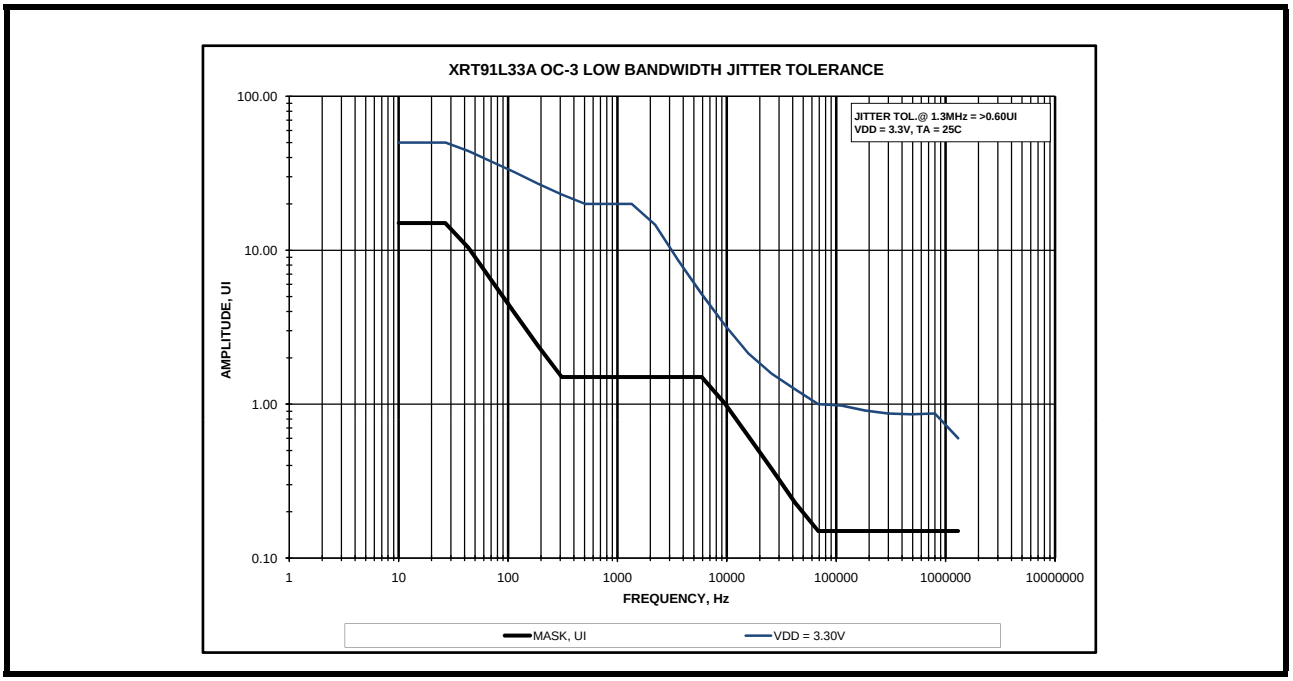


FIGURE 7. XRT91L33A JITTER TOLERANCE AT 155 MBPS OC3/STM-1 (HIGH BANDWIDTH)

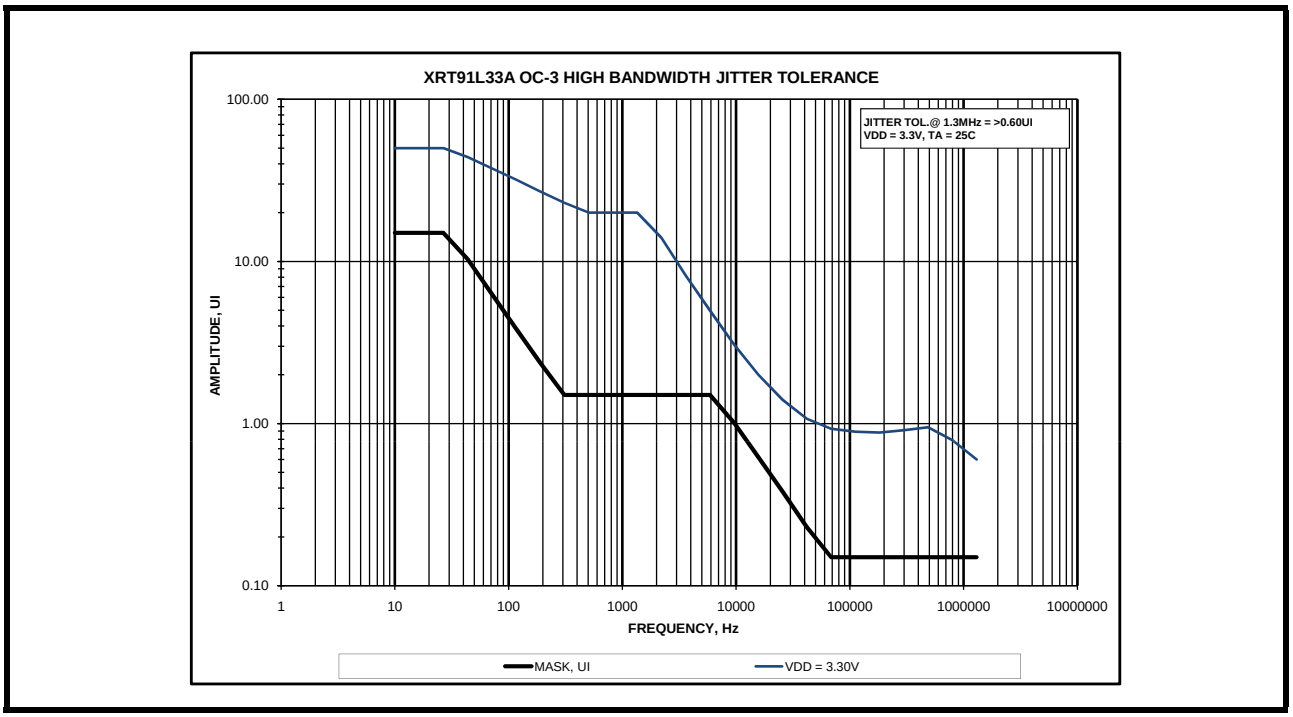


FIGURE 8. XRT91L33A JITTER TOLERANCE AT 622 MBPS OC12/STM-4 (LOW BANDWIDTH)

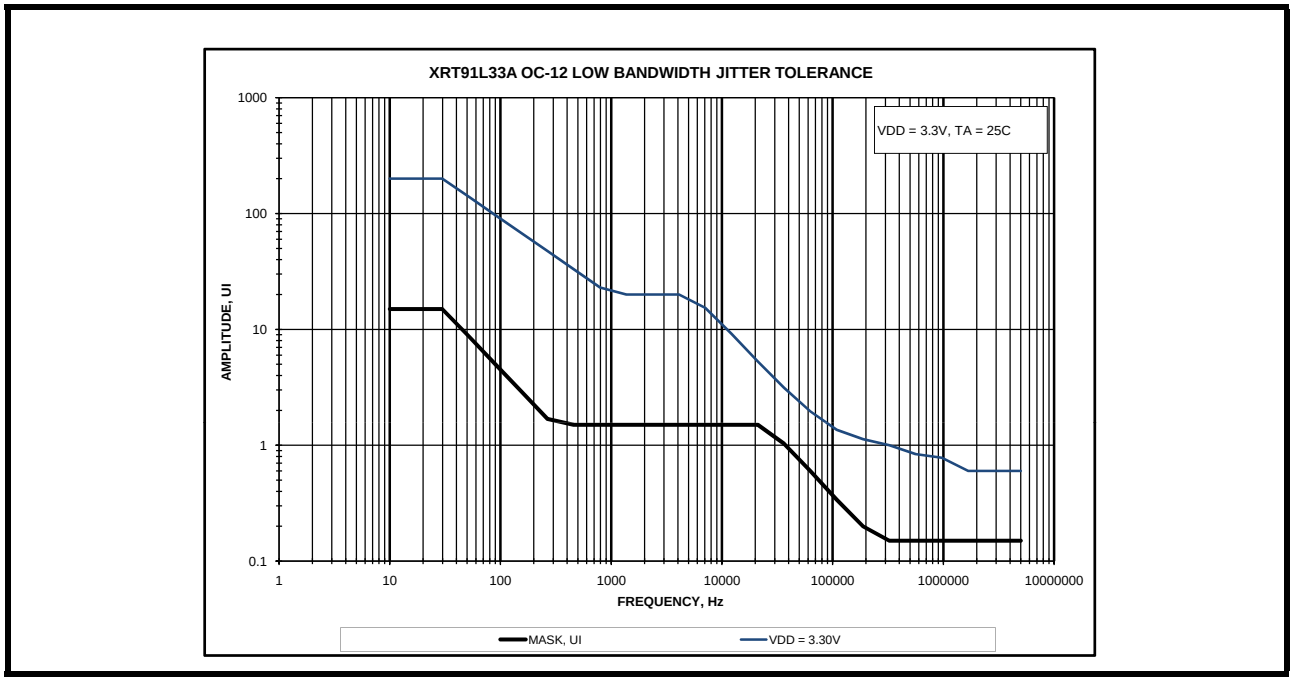
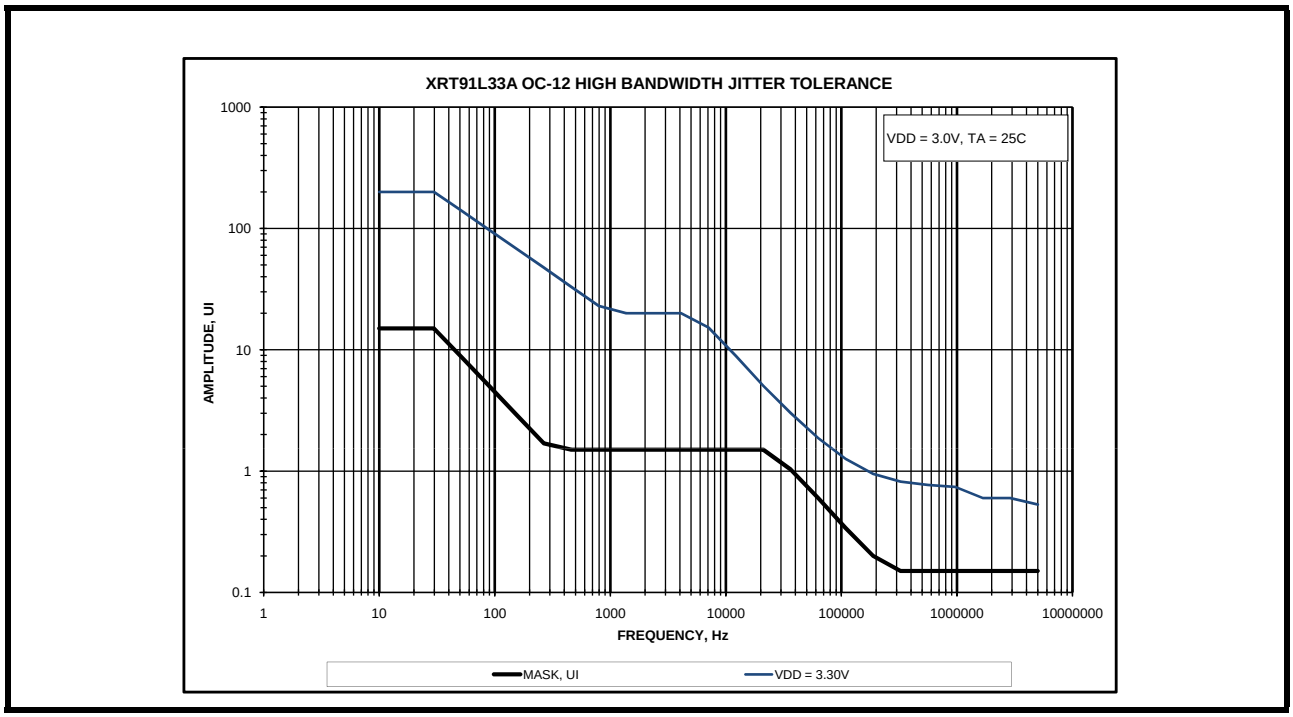


FIGURE 9. XRT91L33A JITTER TOLERANCE AT 622 MBPS OC12/STM-4 (HIGH BANDWIDTH)



4.1.2 Jitter Generation

Maximum jitter generation is less than 0.01 UI rms within the SONET/SDH band, when rms jitter of less than 14 ps (OC-12) or 56 ps (OC-3) is presented to the serial data inputs.

4.1.3 Jitter Transfer

When in the Low Bandwidth mode (Test pin = VDD) the XRT91L33A does meet the jitter transfer requirement in the ITU standard.

FIGURE 10. XRT91L33A JITTER TRANSFER AT 155 MBPS OC3/STM-1 (LOW BANDWIDTH)

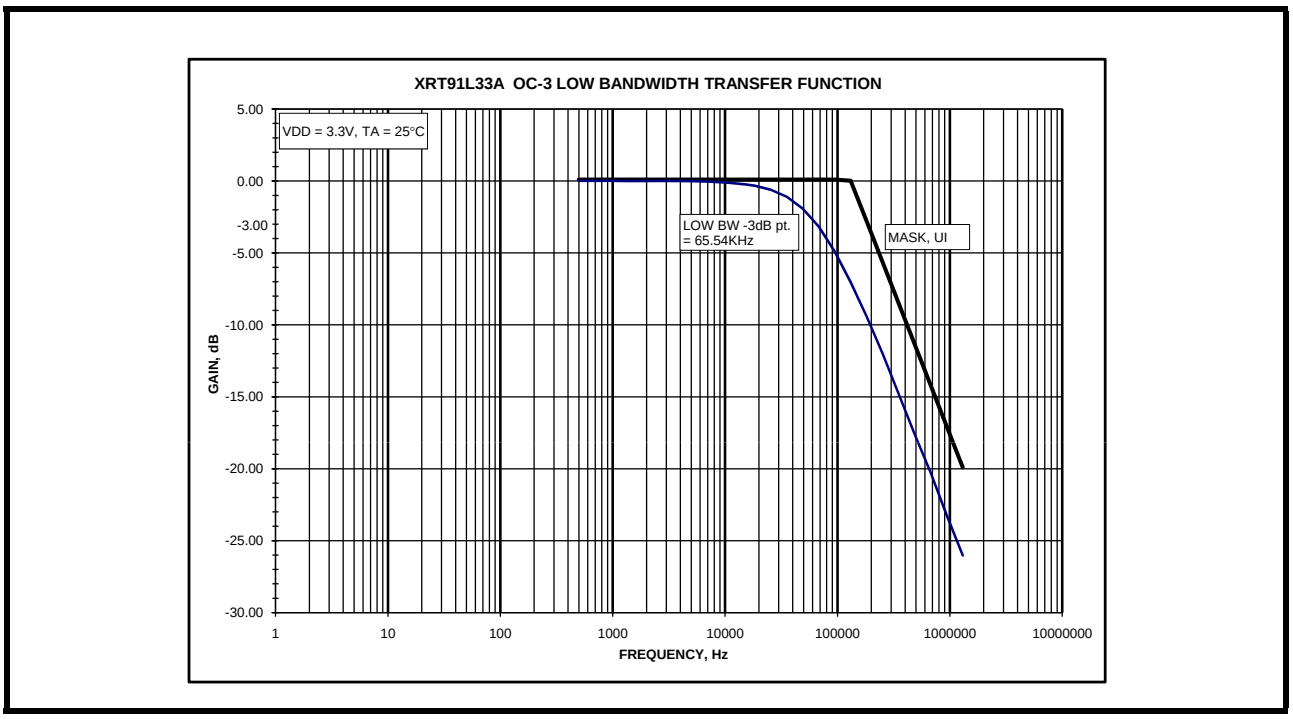
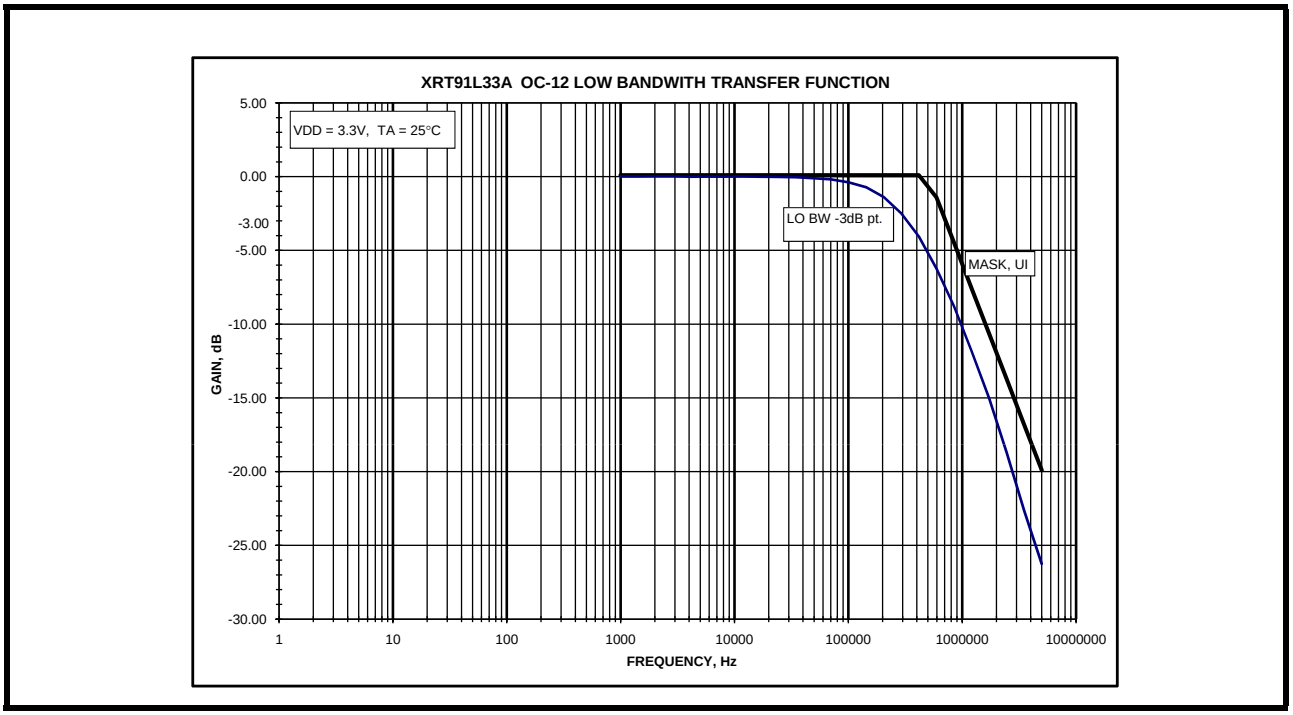


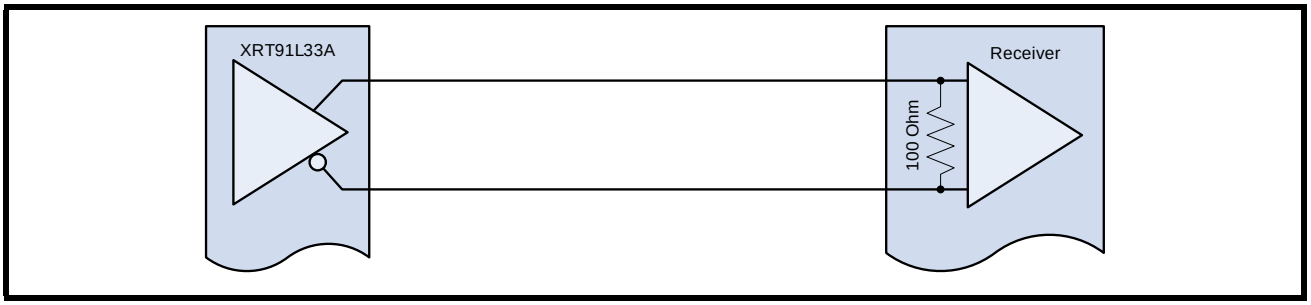
FIGURE 11. XRT91L33A JITTER TRANSFER AT 622 MBPS OC12/STM-4 (LOW BANDWIDTH)



5.0 HIGH-SPEED OUTPUTS

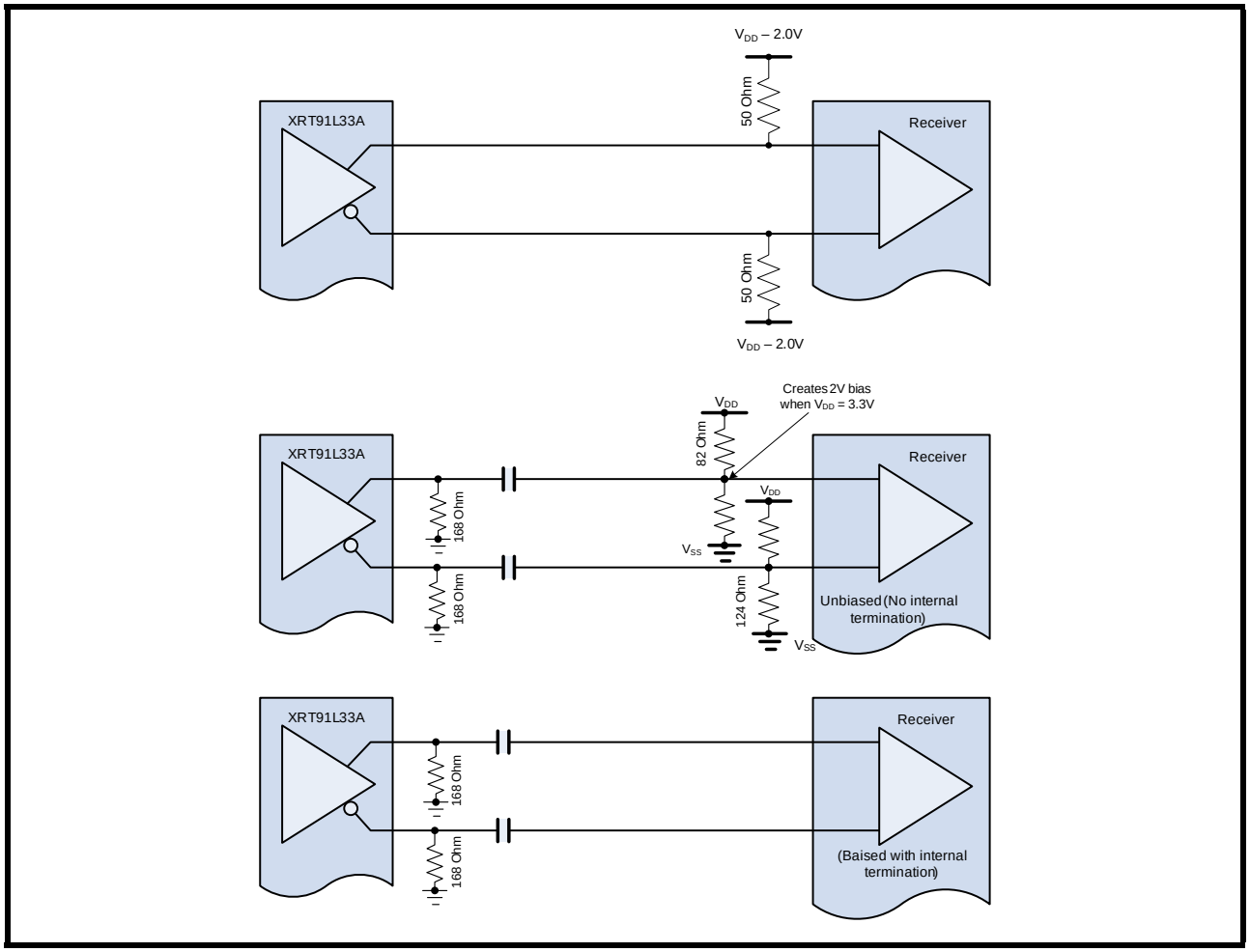
The high-speed output buffers, RXDOP/N and RXCLKOP/N can be terminated as either LVDS or LVPECL outputs. In LVDS mode, the transmission lines must be routed with 100 Ω differential impedance and terminated at the receive end with a line-to-line 100Ω resistor (See **Figure 12**).

FIGURE 12. HIGH SPEED OUTPUTS, LVDS TERMINATION



For LVPECL connections, the transmission line must be terminated with 50Ω pull-down resistors near the receiving end or an equivalent circuit. (See **Figure 13**)

FIGURE 13. HIGH-SPEED OUTPUTS, LVPECL TERMINATION OPTIONS



6.0 RESAMPLED DATA AND CLOCK OUTPUTS

It is recommended that the retimed data output be captured with the rising edge of the clock output as shown in Figure 14. Data valid time is longer for OC-3/STS-3 mode of operation than that of OC-12/STS-12. Data valid time before the output clock's rising edge is the available setup time (t_{SU}), while the data valid time after the clock's rising edge is the available hold time (t_H).

FIGURE 14. OUTPUT DATA AND CLOCK AFTER RESAMPLING

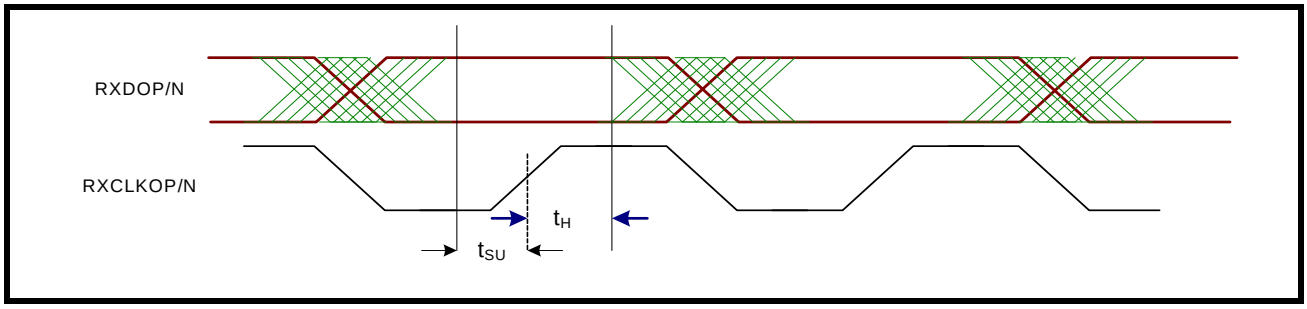


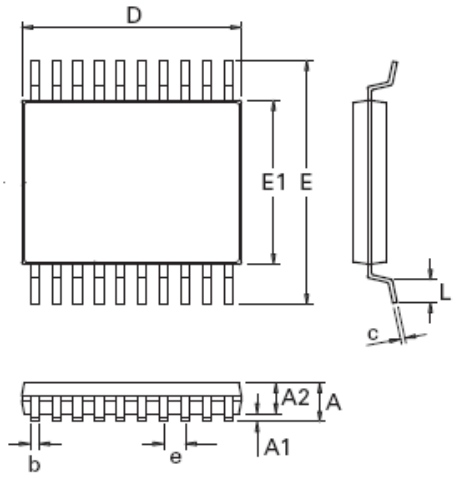
TABLE 11: OUTPUT TIMING

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT	CONDITION
t_{SU}	Available setup time	450		ps	STS-12 operation (622.08 MHz)
		2.0		ns	STS-3 operation (155.52 MHz)
t_H	Available hold time	650		ps	STS-12 operation (622.08 MHz)
		3.0		ns	STS-3 operation (155.52 MHz)

7.0 PACKAGE DIMENSIONS

20 pin Surface mount TSSOP

Package outline



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	-	1.20	-	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
D	6.40	6.60	0.252	0.260
E	6.40 BSC		0.252 BSC	
L	0.45	0.75	0.018	0.030
e	0.65 BSC		0.026 BSC	
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008

Note: Controlling dimensions are in millimeters. Approximate dimensions are provided in inches

Nominal weight

Nominal weight per device 69mg.

TABLE 12: REVISION HISTORY

REVISION #	DATE	DESCRIPTION
1.0.0	March 2010	Initial release of Final Product Datasheet
1.0.1	June 2010	Changed the maximum temperature to 95^{O}C, updated the typical IDD and typical power values in the electrical table.