3A Synchronous Rectified Step Down Converter

■ General Description

The XT1720 is a monolithic synchronous high-efficiency DC/DC buck converter delivers up to 3A of output current. The device operates from an input voltage of 2.5V to 8 V and provides an output voltage from 0.8V to VIN, making the XT1720 ideal for on-board post-regulation applications. The XT1720 operate at a wide switching frequency range from 300KHz to 1.5MHz with an efficiency of up to 94%. The high operating frequency minimizes the size of external components.

Internal soft-start control circuitry reduces inrush current. Short-circuit and thermal-overload protections improve design reliability.

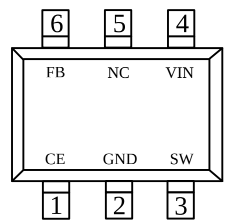
The XT1720 are available in a space-saving SOT-23-6 package.

■ Features

- Ceramic Input and Output Capacitors
- Efficiency Up to 94%
- Guaranteed 3A Output Current
- Operate from 2.5V to 8V Supply
- Adjustable Output from 0.8V to VIN
- Internal Soft-Start
- Short-Circuit and Thermal-Overload Protection
- RoHS Compliant

■ Package

- **SOT-23-6**

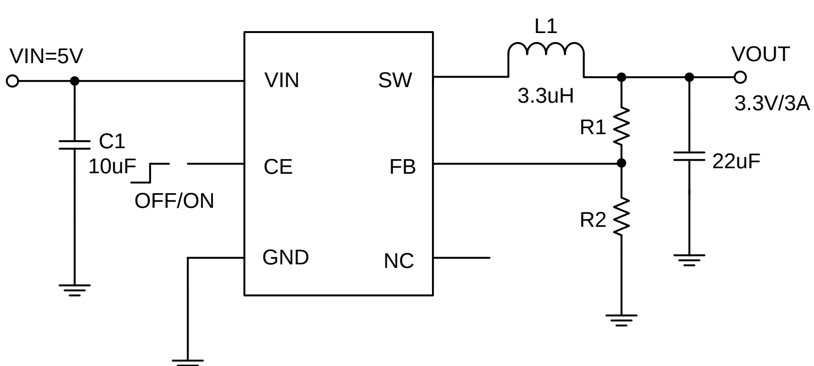


SOT-23-6L
(Top View)

■ Applications

- FPGA,ASIC,DSP POWER SUPPLICES
- LCD TV
- Green Electronics/Appliances
- Notebook Computers
- Set-Top box
- Cellular Base Stations
- Networking and Telecommunications

■ Typical Application Circuit



$V_{OUT}=0.6V\times(1+R_1/R_2)$

■ Ordering Information

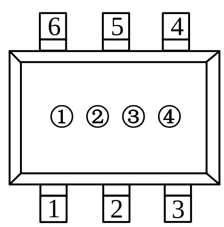
XT1720 ①②③④⑤

Designator	Represents	Symbol	Description
① ②	Output Voltage	25-50/AD	Output Voltage: e.g. 33= 3.3V etc. Adjustable version: ①② fixed as AD
③	Frequency	M	1.5MHZ
④	Package	M	SOT-23-6
⑤	Device Orientation	S	Embossed Tape :Standard Feed
		R	Embossed Tape :Reverse Feed

■ Functional Pin Description

Pin Number	Pin Name	Function
1	CE	Chip Enable pin. Active high. Internal pull high for auto start up.
2	GND	Ground Pin.
3	SW	Switch Pin.
4	VIN	Input Power Supply Pin.
5	NC	Not connect.
6	FB	Feedback Pin. VOUT=0.6V×(1+R1/R2).

■ Marking Rule



SOT-23-6L
(Top View)

① Represents the product name

Symbol	Product Name
2	XT1720◆◆◆◆◆

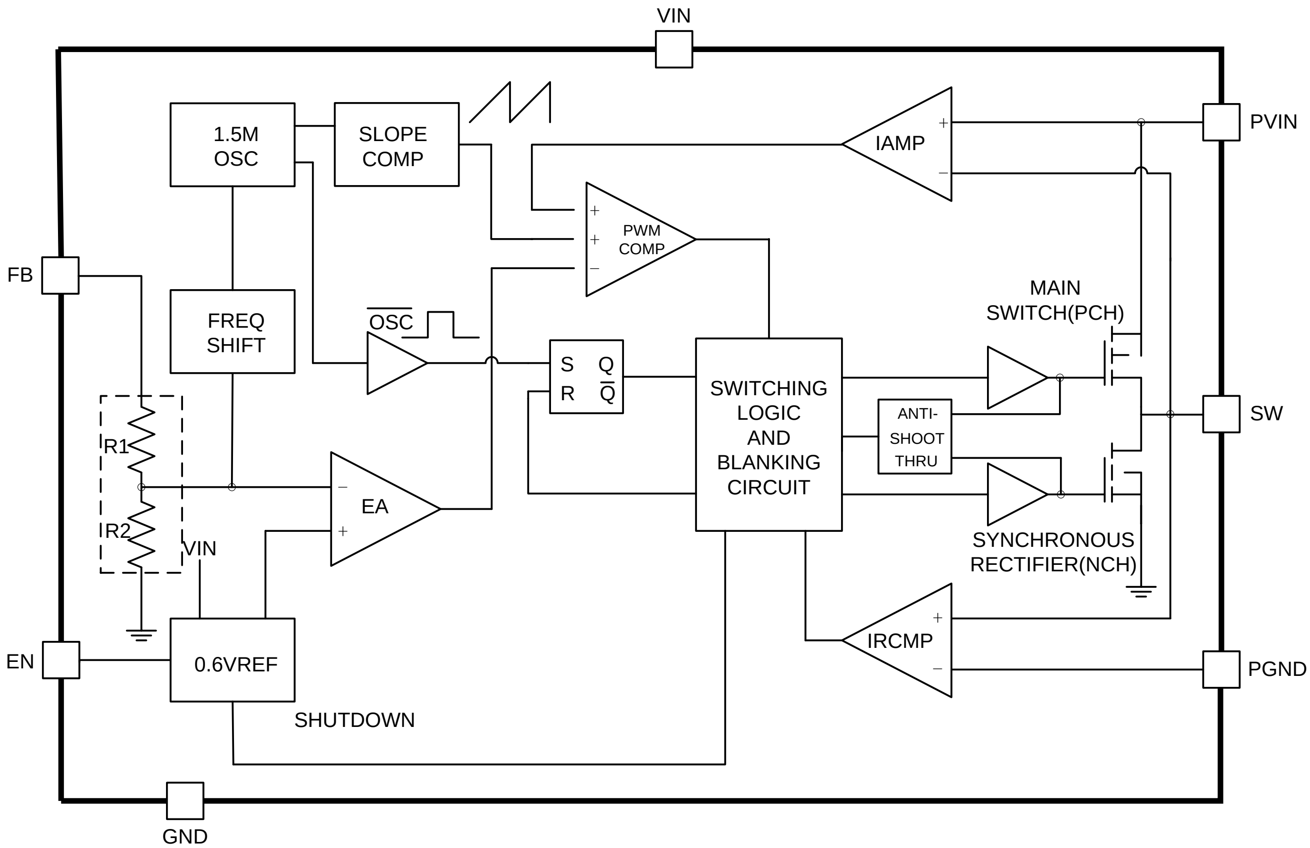
② ③ Represents the output voltage

Designator	Represents	Symbol	Description
② ③	Output Voltage	25-50/AD	Output Voltage: e.g. 33= 3.3V etc. Adjustable version: ②③ fixed as AD

④ Represents the assembly lot No.

0-9，A-Z; 0-9，A-Z mirror writing，repeated（G，I，J，O，Q，W exception）

■ Function Block Diagram



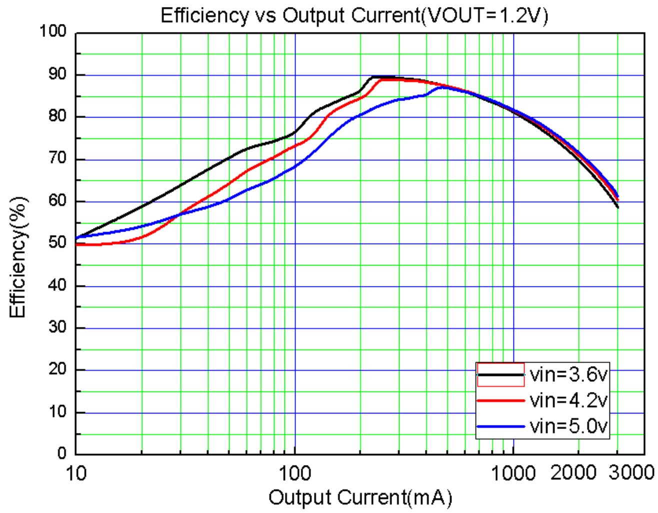
■ Absolute Maximum Ratings

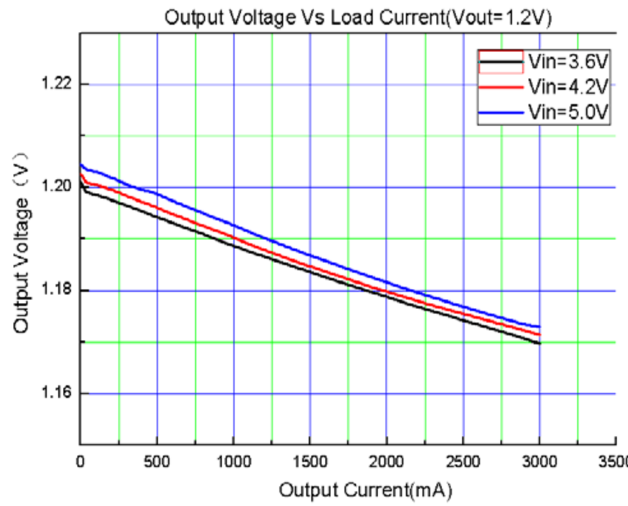
Parameter	Symbol	Maximum Rating		Unit
Input Voltage	V_{IN}	V_{SS}-0.3～V_{SS}+8		V
	V_{LX}	Vss-0.3~V_{IN}+0.7		
	$V_{CE.FB,SW}$	V_{SS}-0.3～V_{IN}+0.3		
Power Dissipation	P_D	SOT-23-6	250	mW
Operating Ambient Temperature	Topr	-40～+85		°C
Storage Temperature	Tstg	-40～+125		
Reflow Temperature(soldeing,10s)	Trefl	250		

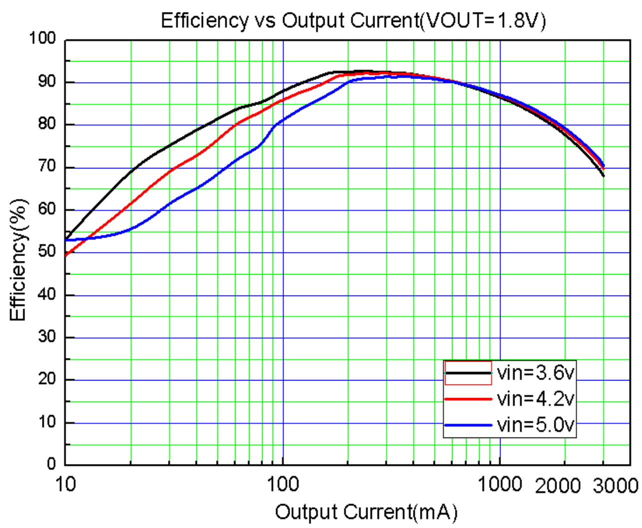
■ Electrical Characteristics

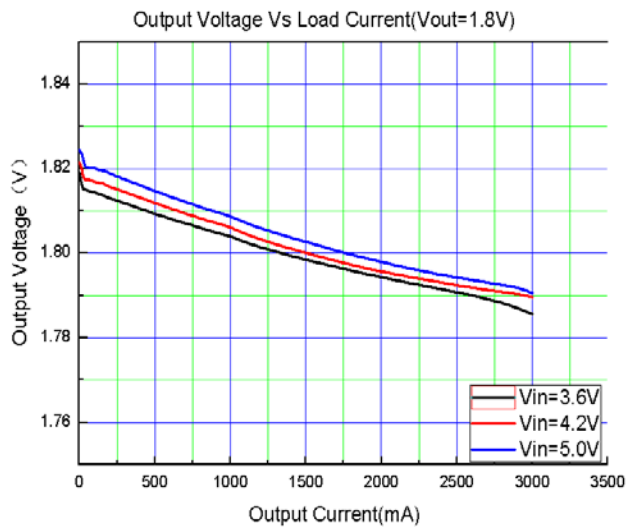
Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Range		3		8	V
Input UVLO		2	2.3	2.6	V
Quiescent Current	V_{FB} = 1V (no switching)	—	460	550	uA
	V_{EN} = 0V	—	0	+1	uA
FB Pin Voltage		0.588	0.6	0.612	V
FB Pin Current		-50	0	+50	nA
Load Regulation	0A < IOUT < 3A		0.3		%
Line Regulation	3.3V < VIN < 5V		0.17		%
EN Pin Voltage High		0.9			V
EN Pin Voltage Low				0.75	V
EN Pin Leakage Current	VEN=3V		0.1	1	uA
Switching Frequency		1.4	1.5	1.6	MHz
Current Limit		3.5	4.0	4.5	A
Maximum Duty				100	%
Minimum Duty		0			%
Minimum On Time			180		nS
Error Amp Transconductance		300	400	500	umho
P-Switch Leakage Current	VLX = 0V, VEN = 0V		0.1	20	uA
P-Switch RDS(ON)	ILX = 150mA		130	200	mΩ
N-Switch RDS(ON)	ILX = 150mA		110	180	mΩ
Thermal Shutdown Protection	Rising		160		℃
	Hysteresis		-20		℃

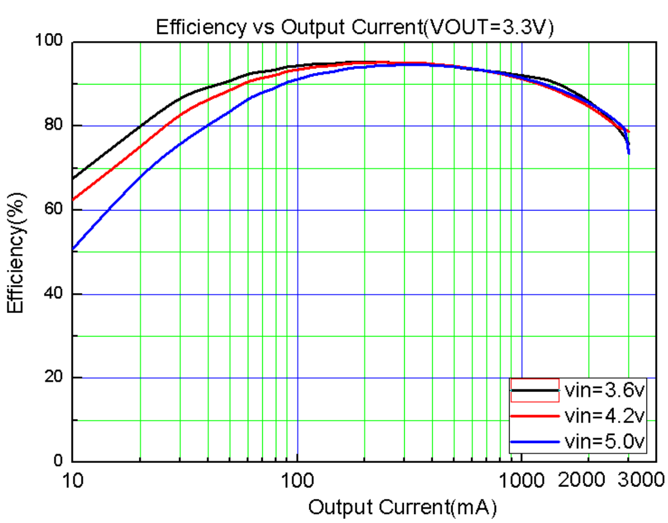
■ Typical Performance Characteristic

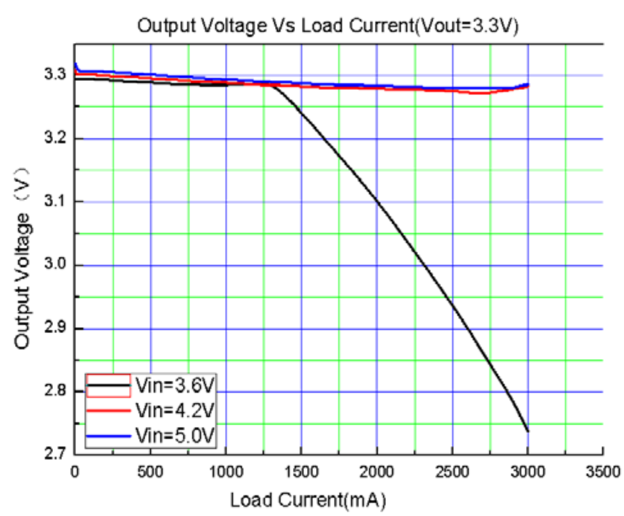


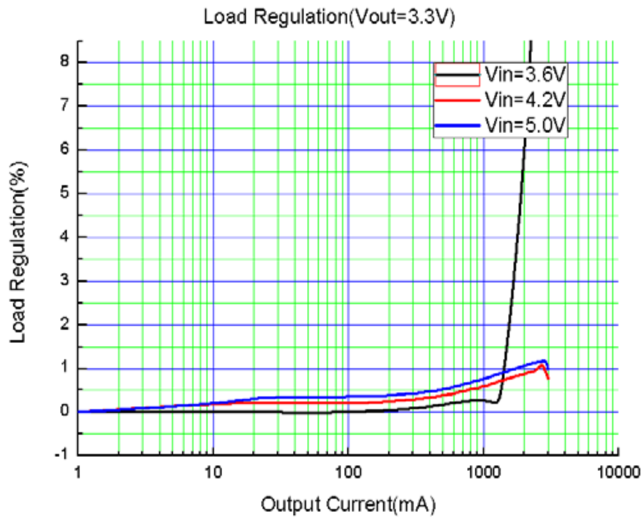


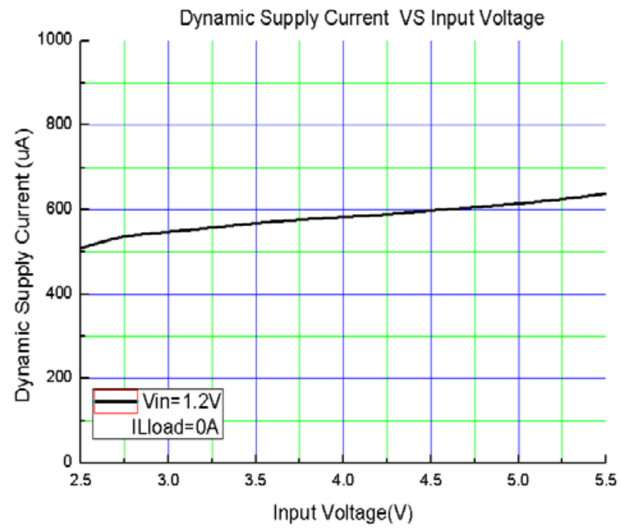


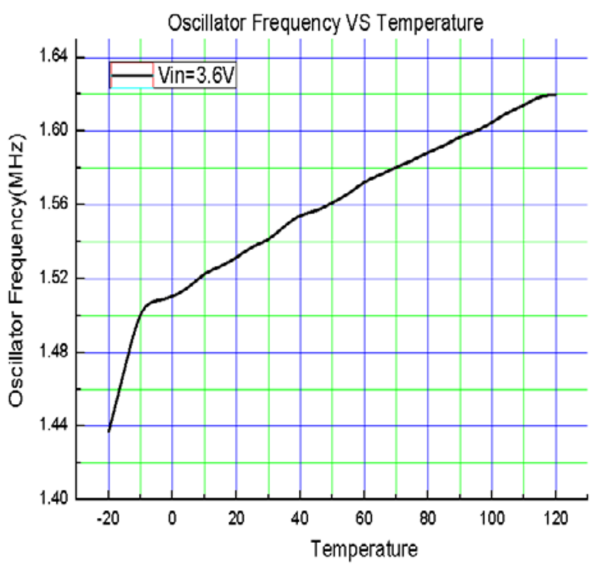


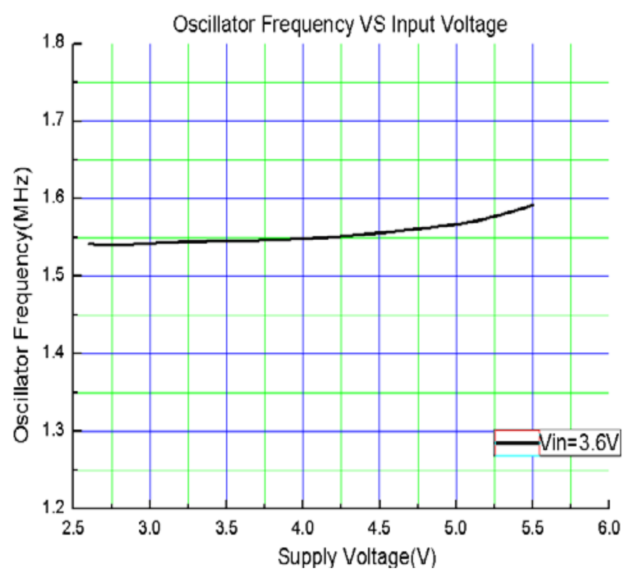





Load Regulation(Vout=3.3V)
Vin=3.6V
Vin=4.2V
Vin=5.0V
Load Regulation(%)
Output Current(mA)
8
7
6
5
4
3
2
1
0
-1
1
10
100
1000
10000


Dynamic Supply Current VS Input Voltage
Dynamic Supply Current (uA)
Input Voltage(V)
Vin=1.2V
ILload=0A
1000
800
600
400
200
0
2.5
3.0
3.5
4.0
4.5
5.0
5.5


Oscillator Frequency VS Temperature
Vin=3.6V
Oscillator Frequency(MHz)
Temperature
1.64
1.60
1.56
1.52
1.48
1.44
1.40
-20
0
20
40
60
80
100
120


Oscillator Frequency VS Input Voltage
Oscillator Frequency(MHz)
Supply Voltage(V)
Vin=3.6V
1.8
1.7
1.6
1.5
1.4
1.3
1.2
2.5
3.0
3.5
4.0
4.5
5.0
5.5
6.0

Application Information

Inductor Selection

For most applications, the value of the inductor will fall in the range of 3.3µH to 22µH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher VIN or VOUT also increase the ripple current ΔI_L:

$$\Delta I_L = \frac{1}{f \times L} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$C_{IN} \text{requires} I_{RMS} \cong I_{QMAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

$$\Delta V_{OUT} \cong \Delta I_L\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

$$V_{OUT} = 0.6 \times \left[1 + \frac{R1}{R2}\right] \text{Volt}$$

where f=switching frequency, L=inductance. A reasonable inductor current ripple is usually set as 1/3 to 1/10 of maximum out current.

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. For better efficiency, choose a low DCR inductor.

Capacitor Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle VOUT/VIN. To prevent large voltage transients, a low ESR input capacitor sized for maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{requires} I_{RMS} \cong I_{QMAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

$$\Delta I_L = \frac{1}{f \times L} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

This formula has a maximum at VIN=2VOUT, where IRMS=IOUT/2. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief.

The selection of COUT is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for COUT has been met, the RMS current rating generally far exceeds the IRIPPLE(P-P) requirement.

The output ripple ΔVOUT is determined by:

$$\Delta V_{OUT} \cong \Delta I_L\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

$$\Delta I_L = \frac{1}{f \times L} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔIL increases with input voltage.

Nowadays, higher value, lower cost ceramic capacitors are becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the XT1720's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for given value and size.

Output Voltage Programming

The output voltage of the XT1720 is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.6 \times \left[1 + \frac{R1}{R2}\right] \text{Volt}$$

Some standard value of R1, R2 for most commonly used output voltage values are listed in Table 1.

V_{OUT}(V)	R_1(kΩ)	R_2(kΩ)
1.1	7.5	15
1.2	10	10
1.5	15	10
1.8	30	15
2.5	76	24
3.3	108	24

Loop Compensation

The XT1720 employs peak current mode control for easy use and fast transient response. Peak current mode control eliminates the double pole effect of the output L-C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole can be calculated by:

$$f_{p1} = \frac{1}{2\pi \times C_{OUT} \times R_L}$$

$$f_{Z1} = \frac{1}{2\pi \times C_{OUT} \times ESR_{COUT}}$$

$$f_{p2} = \frac{1}{2\pi \times C_C \times (R_C + \frac{A_{EA}}{G_{EA}})} \cong \frac{G_{EA}}{2\pi \times C_C \times A_{EA}}$$

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

$$R_C = f_C \times \frac{V_{OUT}}{V_{FB}} \times \frac{2\pi \times C_{OUT}}{G_{EA} \times G_{CS}}$$

$$C_C = \frac{C_{OUT} \times R_L}{R_C}$$

$$R_{LX} = (R_{DS}(ON))D + (R_D(F)(1 - D)$$

The zero is a ESR zero due to output capacitor and its ESR. It can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_{OUT} \times ESR_{COUT}}$$

Where COUT is the output capacitor; RL is load resistance; ESRCOUT is the equivalent series resistance of output capacitor.

The compensation design is to shape the converter close loop transfer function to get desired gain and phase. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In the XT1720, FB pin and COMP pin are the inverting input and the output of internal transconductance error amplifier (EA). A series RC and CC compensation network connected to COMP pin provides one pole and one zero:

for RC <<AEA/GEA

$$f_{p2} = \frac{1}{2\pi \times C_C \times (R_C + \frac{A_{EA}}{G_{EA}})} \cong \frac{G_{EA}}{2\pi \times C_C \times A_{EA}}$$

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

where GEA is the error amplifier transconductance
AEA is the error amplifier voltage gain
RC is the compensation resistor
CC is the compensation capacitor

The desired crossover frequency fC of the system is defined to be the frequency where the control loop has unity gain. It is also called the bandwidth of the converter. In general, a higher bandwidth means faster response to load transient. However, the bandwidth should not be too high because of system stability concern. When designing the compensation loop, converter stability under all line and load condition must be considered. Usually, it is recommended to set the bandwidth to be less than 1/10 of switching frequency.

Using selected crossover frequency, fC, to calculate RC:

$$R_C = f_C \times \frac{V_{OUT}}{V_{FB}} \times \frac{2\pi \times C_{OUT}}{G_{EA} \times G_{CS}}$$

where GCS = 2 A/V is the current sense circuit transconductance.

The compensation capacitor CC and resistor RC together make zero. This zero is put somewhere close to the pole fP1 of selected frequency. CC is selected by:

$$C_C = \frac{C_{OUT} \times R_L}{R_C}$$

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, VOUT immediately shifts by an amount equal to (ΔILOAD×ESR), where ESR is the effective series resistance of COUT. ΔILOAD also begins to charge or discharge COUT, which generates a feedback error signal. The regulator loop then acts to return VOUT to its steady-state value. During this recovery time VOUT can be monitored for overshoot or ringing that would indicate a stability problem.

Efficiency Considerations

Although all dissipative elements in the circuit produce losses, one major source usually account for most of the losses in XT1720 circuits: I^2R losses. The I^2R loss dominates the efficiency loss at medium to high load currents. The I^2R losses are calculated from the resistances of the internal switches, RLX, and external inductor RL. In continuous mode, the average output current flowing through inductor L is "chopped" between the main switch and the external diode. Thus the series resistance looking into the LX pin is a function of internal high-side switch's RDS(ON), external low-side diode's forward resistance RD(F) and the duty cycle (D) as follows:

$$R_{LX} = (R_{DS}(ON))D + (R_D(F)(1 - D)$$

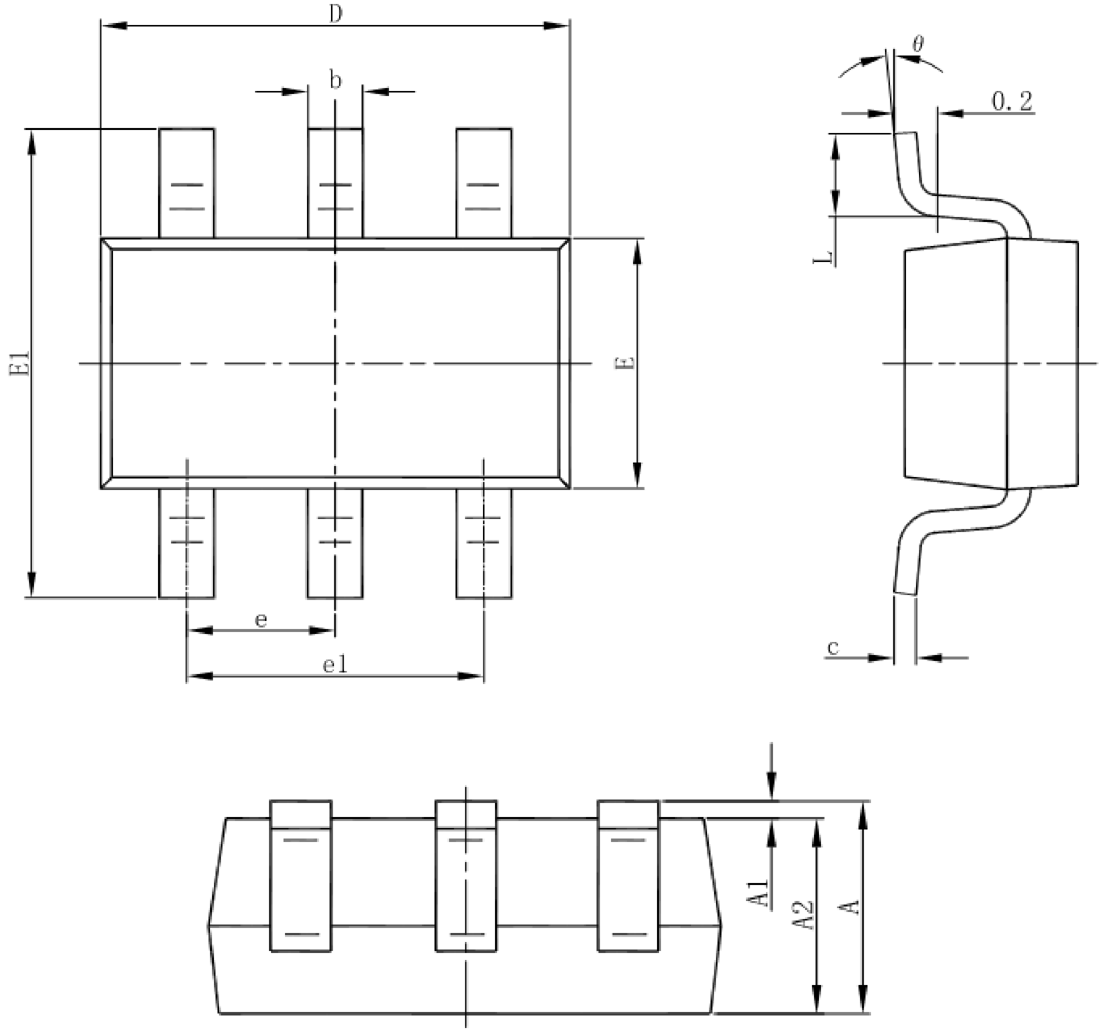
Thus, to obtained I^2R losses, simply add RLX to RL and multiply the result by the square of the average output current. Other losses including CIN and COUT ESR dissipative losses and inductor core losses generally account for less than 2% total additional loss.

Thermal considerations

In most application the XT1720 does not dissipate much heat due to its high efficiency. But, in applications where the XT1720 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 140°C, both power switches will be turned off and the LX node will become high impedance.

Package Information

- **SOT-23-6**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°