8MHz PWM Synchronous Buck Regulator with LDO Standby Mode

■ General Description

The XT1780 is a high efficiency 8MHz pulse width modulated (PWM) synchronous buck (step-down) regulator that features a LOWQ LDO standby mode that draws only 25μA of quiescent current. The XT1780 allows an ultra-low noise, small size, and high efficiency solution for portable power applications.

In PWM mode, the XT1780 operates with a constant frequency 8MHz PWM control. Under light load conditions, such as in system sleep or standby modes, the PWM switching operation can be disabled to reduce switching losses. In this light load LDO mode, the LDO maintains the output voltage and draws only 25μA of quiescent current. The LDO mode of operation saves battery life while not introducing spurious noise and high ripple as experienced with pulse skipping or bursting mode regulators.

The XT1780 operates from a 2.7V to 5.5V input voltage and features internal power MOSFETs that can supply up to 800mA output current in PWM mode. It can operate with a maximum duty cycle of 100% for use in low-dropout conditions.

The XT1780 is available in the DFN3×3-10 package with a junction operating range from －40°C to +125°C.

■ Applications

- 2.7 to 5.5V supply/input voltage
- Light load LDO mode
- 25μA quiescent current
- Low noise, 75μVrms
- 8MHz PWM mode
- Output current to 800mA
- >90% efficiency
- 100% maximum duty cycle
- Adjustable output voltage option down to 1V
- Fixed output voltage options available
- Ultra-fast transient response
- Uses a tiny 0.47μH inductor
- Enables sub 1mm profile solution
- Fully integrated MOSFET switches
- Micropower shutdown
- Thermal shutdown and current limit protection
- Pb-free DFN3×3-10 package
- –40°C to +125°C junction temperature range

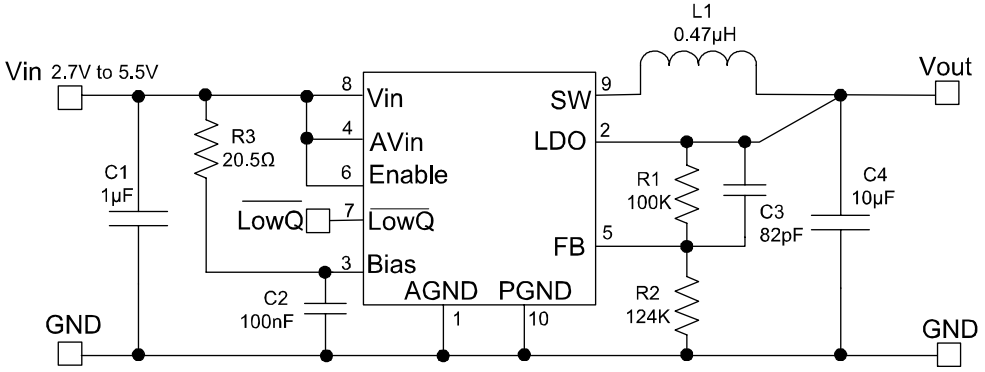
■ Features

- Cellular phones
- PDAs
- USB peripherals

■ Package

- DFN3×3-10

■ Typical Application Circuit



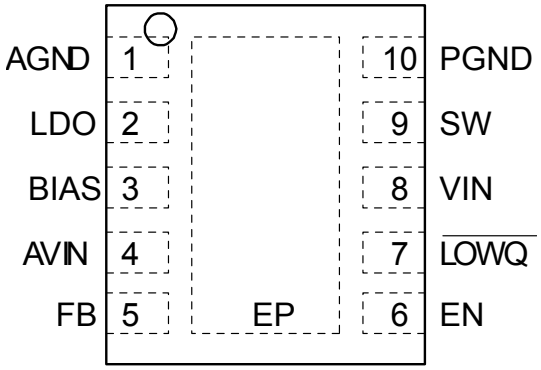
Adjustable Output Buck Regulator

■ Ordering Information

XT1780 ①②③

Designator	Symbol	Description
①	A	Output Voltage adjustable
②	M	Package Types: DFN3×3-10
③	S	Embossed Tape :Standard Feed
	R	Embossed Tape :Reverse Feed

■ Pin Assignment



10-Pin 3mm x 3mm (DFN)

■ Functional Pin Description

Pin Number	Pin Name	Function Description
1	AGND	Analog (signal) Ground.
2	LDO	LDO Output (Output): Connect to VOUT for LDO mode operation.
3	BIAS	Internal circuit bias supply. Must be filtered from input voltage through an RC lowpass filter with a cut off frequency $\geq \frac{1}{2\pi(20.5\Omega)(100nF)}$
4	AVIN	Analog Supply/Input Voltage (Input): Supply voltage for the analog control circuitry and LDO input power. Requires bypass capacitor to GND.
5	FB	Feedback. Input to the error amplifier. For the Adjustable option, connect to the external resistor divider network to set the output voltage. For fixed output voltage options, connect to VOUT and an internal resistor network sets the output voltage.
6	EN	Enable (Input). Logic low will shut down the device, reducing the quiescent current to less than 5μA.
7	$\overline{\text{LOWQ}}$	Enable LDO Mode (Input): Logic low enables the internal LDO and disables the PWM operation. Logic high enables the PWM mode and disables the LDO mode.
8	VIN	Supply/Input Voltage (Input): Supply voltage for the internal switches and drivers.
9	SW	Switch (Output): Internal power MOSFET output switches.
10	PGND	Power Ground.
EP	GND	Ground, backside pad.

■ Functional Description

- **VIN**

VIN provides power to the MOSFETs for the switch mode regulator section, along with the current limiting sensing. Due to the high switching speeds, a 1μF capacitor is recommended close to VIN and the power ground (PGND) pin for bypassing. Please refer to layout recommendations.

- **AVIN**

Analog VIN (AVIN) provides power to the LDO section. AVIN and VIN must be tied together. Careful layout should be considered to ensure high frequency switching noise caused by VIN is reduced before reaching AVIN.

- **LDO**

The LDO pin is the output of the linear regulator and should be connected to the output. In LDO mode (LOWQ<1.5V), the LDO provides the output voltage. In PWM mode (LOWQ>1.5V), the LDO pin is high impedance.

- **EN**

The enable pin provides a logic level control of the output. In the off state, supply current of the device is greatly reduced (typically <1μA). Also, in the off state, the output drive is placed in a "tri-stated" condition, where both the high side P-channel Mosfet and the low-side N-channel are in an “off” or non-conducting state. Do not drive the enable pin above the supply voltage.

- **$\overline{\text{LOWQ}}$**

The LOWQ pin provides a logic level control between the internal PWM mode and the low noise linear regulator mode. With LOWQ pulled low (<0.5V), quiescent current of the device is greatly reduced by switching to a low noise linear regulator mode that has a typical I_Q of 25μA. In linear (LDO) mode, the output can deliver 60mA of current to the output. By placing $\overline{\text{LOWQ}}$ high (>1.5V), this transitions the device into a constant frequency PWM buck regulator mode. This allows the device the ability to efficiently deliver up to 800mA of output current at the same output voltage.

- **BIAS**

The BIAS pin supplies the power to the internal power to the control and reference circuitry. The bias is powered from the input voltage through an RC lowpass filter. The RC lowpass filter frequency must be $\geq \frac{1}{2\pi(20.5\Omega)(100nF)}$

- **FB**

The feedback pin (FB) provides the control path to control the output. For adjustable versions, a resistor divider connecting the feedback to the output is used to adjust the desired output voltage. The output voltage is calculated as follows:

$$V_{OUT} = V_{REF} \times (\frac{R1}{R2} + 1)$$ where V_{REF} is equal to 1.0V.

A feed forward capacitor is recommended for most designs using the adjustable output voltage option. To reduce battery current draw, a 100K feedback resistor is recommended from the output to the FB pin (R1). Also, a feedforward capacitor should be connected between the output and feedback (across R1). The large resistor value and the parasitic capacitance of the FB pin can cause a high frequency pole that can reduce the overall system phase margin. By placing a feedforward capacitor, these effects can be significantly reduced. Typically an 82pF small ceramic capacitor is recommended.

- **SW**

The switch (SW) pin connects directly to the inductor and provides the switching current necessary to operate in PWM mode. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes.

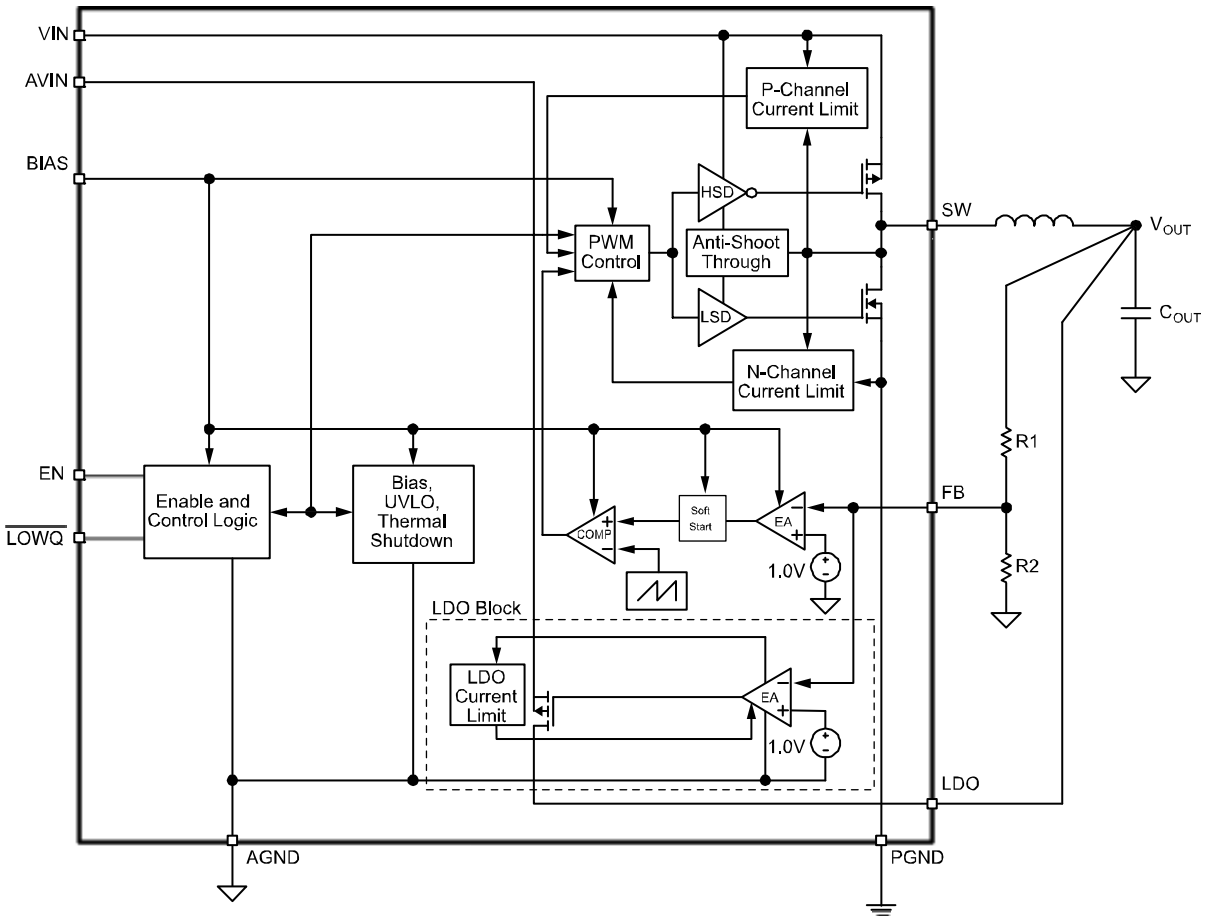
- **PGND**

Power ground (PGND) is the ground path for the high current PWM mode. The current loop for the power ground should be as small as possible and separate from the Analog ground (AGND) loop. Refer to the layout considerations for more details.

- **AGND**

Signal ground (AGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the Power ground (PGND) loop. Refer to the layout considerations for more details.

■ Function Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Typical	Unit
Input voltage	V_{IN}	6.0	V
Output switch voltage	V_{SW}	6.0	V
Output switch current	I_{SW}	2	A
Logic input voltage	V_{EN},V_{LOWQ}	-0.3 to V_{IN}	V
Storage temperature	Ts	-60 to 150	°C
ESD rating	V_{ESD}	3K	V
Supply voltage	V_{IN}	+2.7 to +5.5	V
Logic input voltage	V_{EN},V_{LOWQ}	-0.3 to V_{IN}	V
Junction temperature	T_J	-40 to +125	°C
Junction thermal resistance	θ_{JA}	60	°C/W

■ Electrical Characteristics

V_{IN}=V_{EN}=V_{LOWQ}=3.6V；L=0.47μH；C_{OUT}=10μF;T_A=25℃，unless noted. Bold values indicate -40℃≤TJ≤＋125℃

Parameter	Test condition	Min	Typ	Max	Units
Supply voltage range		2.7		5.5	V
Under-voltage lockout threshold	(turn-on)	2.45	2.55	2.65	V
ULVO hysteresis			200		mV
Quiescent current, PWM mode	V_{FB}=0.9*V_{NOM}(not switching)		890	1000	μA
Quiescent current, LDO mode	V_{OWQ}=0V;I_{OUT}= 0mA		25	29	μA
Shutdown Current	V_{EN}=0V		0..01	5	μA
[Adjustable] Feedback voltage	±2%(over temperature)	0.98	1	1.02	V
FB Pin input current			1		nA
Current Limit in PWM mode	V_{FB}=0.9*VNOM	0.8	1	1.85	A
Output voltage line regulation	V_{OUT}>2V;V_{IN}=V_{OUT}+300mV to 5.5V;I_{LOAD}=100mA $V_{OUT<}$2V;V_{IN}=2.7 V to 5.5V;I_{LOAD}=100mA		0.13		%
Output voltage load regulation, PWM mode	200mA<I_{LOAD}<300mA		0.2	0.8	%
Output voltage load regulation, LDO mode	100μA<I_{LOAD}<50mA V_{LOWQ}=0V		0.5	1	%
Maximum duty cycle	V_{FB}≤0.4V	100			%
PWM switch on-resistance	I_{SW}=50mA V_{FB}=0.7V_{FB_NOM}(High side switch) I_{SW}=-50mA V_{FB}=1.1V_{FB_NOM}(Low side switch)		0.4 0.35		Ω
Oscillator frequency		7.2	8	8.8	MHz
$\overline{LOWQ}$ threshold voltage		0.8	1.0	1.3	V
$\overline{LOWQ}$ input current			0.1	2	μA
Enable threshold		0.8	1.0	1.3	V
Enable input current			0.1	2	μA
LDO dropout voltage	I_{OUT}=50mA		110		mV
Output voltage noise	$L_{\overline{OWQ}}$=0V;C_{OUT}=10μF,10Hz to 100KHz		75		μVrms
LDO current limit	$L_{\overline{OWQ}}$=0V;Vout=0V (LDO Mode)	50	80		mA
Over-Temperature shutdown			160		℃
Over-Temperature hysteresis			20		℃

Notes:1. Exceeding the absolute maximum rating may damage the device.

2. The device is not guaranteed to function outside its operating rating.

3. Devices are ESD sensitive. Handling precautions recommended. Human body model: 1.5kΩ in series with 100pF.

4. Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal value that is initially measured at a 1V differential. For outputs below 2.7V, the dropout voltage is the input-to-output voltage differential with a minimum input voltage of 2.7V.

■ Application Information

The XT1780 is a 800mA PWM power supply that utilizes a LDO light load mode to maximize battery efficiency in light load conditions. This is achieved with a $\overline{\text{LOWQ}}$ control pin that when pulled low, shuts down all the biasing and drive current for the PWM regulator, drawing only 25μA of operating current. This allows the output to be regulated through the LDO output, capable of providing 60mA of output current. This method has the advantage of producing a clean, low current, ultra-low noise output in LDO mode. During LDO mode, the SW node becomes high impedance, blocking current flow. Other methods of reducing quiescent current, such as pulse frequency modulation (PFM), or bursting techniques, create large amplitude, low frequency ripple voltages that can be detrimental to system operation.

When more than 60mA is required, the $\overline{\text{LOWQ}}$ pin can be forced high, causing the XT1780 to enter PWM mode. In this case, the LDO output makes a "hand-off" to the PWM regulator with virtually no variation in output voltage. The LDO output then turns off allowing up to 800mA of current to be efficiently supplied through the PWM output to the load.

- **Input Capacitor**

A minimum 1μF ceramic is recommended on the VIN pin for bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore, not recommended.

A minimum 1μF is recommended close to the VIN and PGND pins for high frequency filtering. Smaller case size capacitors are recommended due to their lower ESR and ESL. Please refer to layout recommendation section of data sheet for proper layout of the input capacitor.

- **Output Capacitor**

The XT1780 is optimized for a 10μF output capacitor. A larger value can be used to improve transient response. The XT1780 utilizes type III internal compensation and utilizes an internal high frequency zero to compensate for the double pole roll off of the LC filter. For this reason, larger output capacitors can create instabilities. X5R or X7R dielectrics are recommended for the output capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore, not recommended.

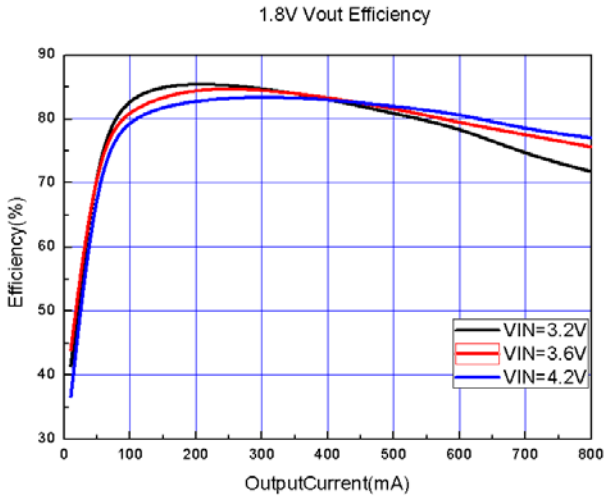
In addition to a 10μF, a small 10nF is recommended close to the load for high frequency filtering. Smaller case size capacitors are recommended due to there lower ESR and ESL.

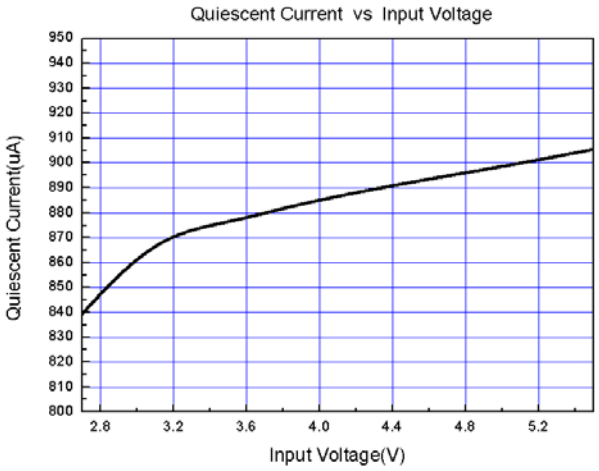
- **Inductor Selection**

The XT1780 is designed for use with a 0.47μH inductor. Proper selection should ensure the inductor can handle the maximum average and peak currents required by the load. Maximum current ratings of the inductor are generally given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure that the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor. Peak inductor current can be calculated as follows: $I_{PK} = I_{OUT} + \frac{V_{OUT}(1-\frac{V_{OUT}}{V_{IN}})}{2 \times f \times L}$

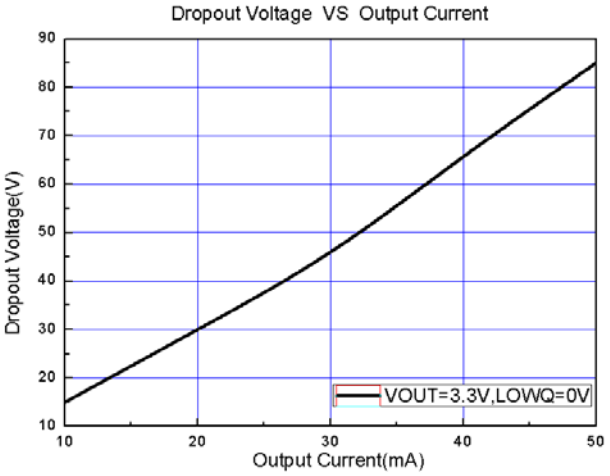
■ Typical Performance Characteristics

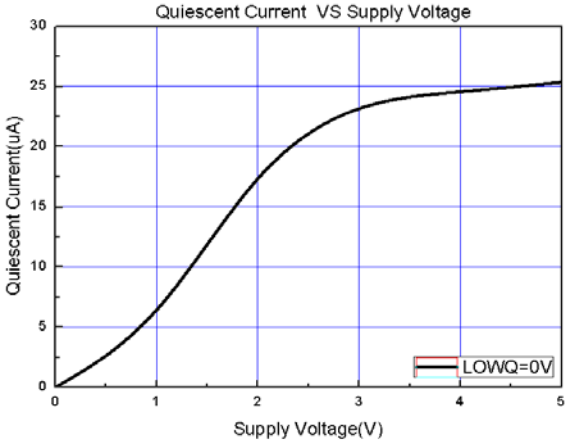
DC-DC



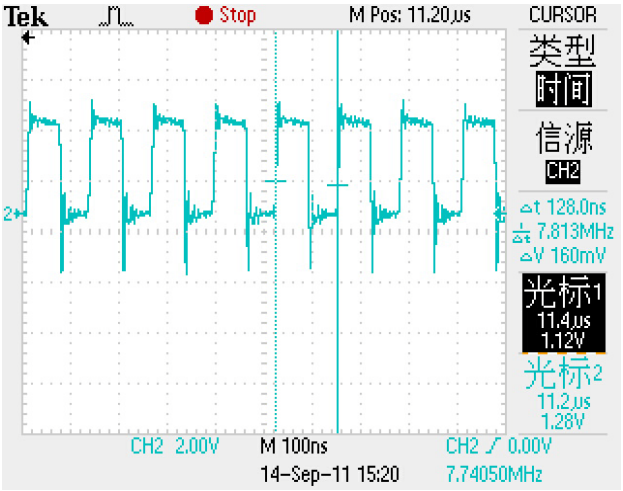


LDO

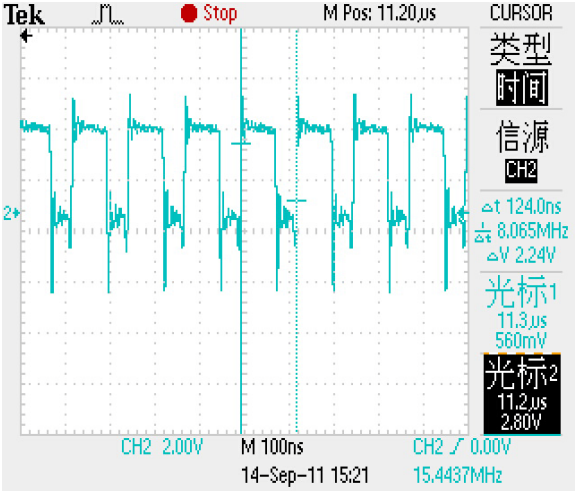




VIN=3.6V,ILOAD=100mA

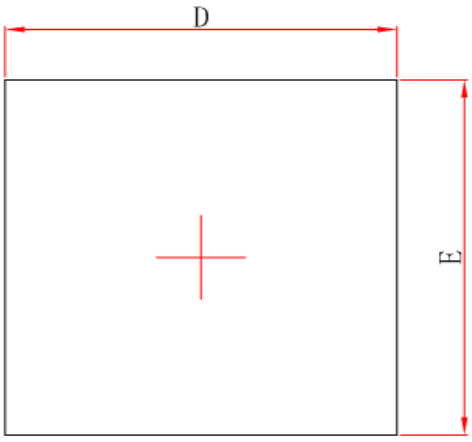


VIN=3.6V,ILOAD=800mA

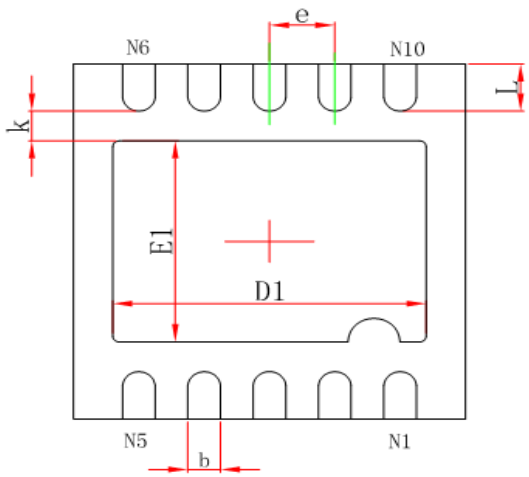


■ Package Information

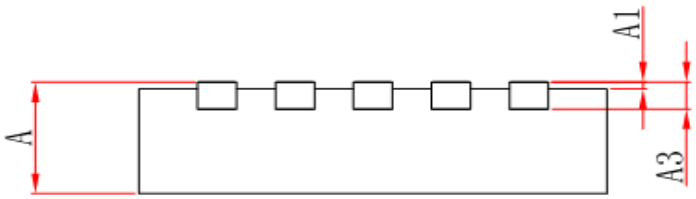
- **DFN3×3-10**



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	2.300	2.500	0.091	0.098
E1	1.600	1.800	0.063	0.071
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.020TYP.	
L	0.300	0.500	0.012	0.020