XT25F128B

Quad IO Serial NOR Flash
Datasheet

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Serial NOR Flash Memory

128 Megabits 3.3V Quad I/O Serial Flash Memory with 4KB Uniform Sector

- **128M -bit Serial Flash**
  - 16, 384K-byte
  - 256 bytes per programmable page
- **Support SFDP & Unique ID**
- **Standard, Dual, Quad SPI**
  - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
  - Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#
  - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3
  - QPI: SCLK, CS#, IO0, IO1, IO2, IO3
- **Flexible Architecture**
  - Sector of 4K-byte
  - Block of 32/64k-byte
- **Advanced security Features**
  - 4*256-Byte Security Registers With OTP Lock
- **Software/Hardware Write Protection**
  - Write protect all/portion of memory via soft-ware
  - Enable/Disable protection with WP# Pin
  - Top or Bottom, Sector or Block selection
- **Package Options**
  - See 1.1 Available Ordering OPN
  - All Pb-free packages are compliant RoHS, Halo-gen-Free and REACH.
- **Temperature Range & Moisture Sensitivity Level**
  - Industrial Level Temperature. (-40℃ to +85℃), MSL3
- **Low Power Consumption**
  - 30mA maximum active current
  - 0.1uA typical power down current
- **Single Power Supply Voltage: Full voltage range: 2.70~3.60V**
- **Typical 100,000 Program/Erase Cycle**
- **High Speed Clock Frequency**
  - 108MHz for fast read with 30PF load
  - Dual Output Data transfer up to 216Mbits/s
  - Quad I/O Data transfer up to 432Mbits/s
  - QPI Mode Data transfer up to 288Mbits/s
  - Continuous Read With 8/16/32/64-byte Wrap
- **Program/Erase Speed**
  - Page Program time: 0.3ms typical
  - Sector Erase time: 80ms typical
  - Block Erase time: 0.15/0.2s typical
  - Chip Erase time: 35s typical

CONTENTS

1. GENERAL DESCRIPTION 3

1.1. AVAILABLE ORDERING OPN 3
1.2. CONNECTION DIAGRAM 3
1.3. PIN DESCRIPTION 5
1.4. BLOCK DIAGRAM 6

2. MEMORY ORGANIZATION 7

3. DEVICE OPERATION 8

4. DATA PROTECTION 10

5. STATUS REGISTER 13

6. COMMANDS DESCRIPTION 15

6.1. WRITE ENABLE (WREN) (06H) 19
6.2. WRITE ENABLE FOR VOLATILE STATUS REGISTER (50H) 19
6.3. WRITE DISABLE (WRDI) (04H) 20
6.4. READ STATUS REGISTER (RDSR) (05H OR 35H) 21
6.5. WRITE STATUS REGISTER (WRSR) (01H) 22
6.6. READ DATA BYTES (READ) (03H) 23
6.7. READ DATA BYTES AT HIGHER SPEED (FAST READ) (0BH) 24
6.8. DUAL OUTPUT FAST READ (3BH) 25
6.9. QUAD OUTPUT FAST READ (6BH) 26
6.10. DUAL I/O FAST READ (BBH) 26
6.11. QUAD I/O FAST READ (EBH) 28
6.12. QUAD I/O WORD FAST READ (E7H) 30
6.13. SET BURST WITH WRAP (77H) 31
6.14. PAGE PROGRAM (PP) (02H) 32
6.15. QUAD PAGE PROGRAM (QPP) (32H) 33
6.16. SECTOR ERASE (SE) (20H) 35
6.17. 32KB BLOCK ERASE (BE) (52H) 36
6.18. 64KB BLOCK ERASE (BE) (D8H) 37
6.19. CHIP ERASE (CE) (60/C7H) 38
6.20. DEEP POWER-DOWN (DP) (B9H) 39
6.21. RELEASE FROM DEEP POWER-DOWN AND READ DEVICE ID (RDI) (ABH) 40
6.22. READ MANUFACTURE ID/ DEVICE ID (REMS) (90H) 41
6.23. READ MANUFACTURE ID/ DEVICE ID DUAL I/O (92H) 43
6.24. READ MANUFACTURE ID/ DEVICE ID QUAD I/O (94H) 44
6.25. READ IDENTIFICATION (RDID) (9FH) 44
6.26. GLOBAL BLOCK/SECTOR LOCK (7EH) OR UNLOCK (98H) 45
6.27. INDIVIDUAL BLOCK/SECTOR LOCK (36H)/UNLOCK (39H)/READ (3DH) 47
6.28. ERASE SECURITY REGISTERS (44H) 49
6.29. PROGRAM SECURITY REGISTERS (42H) 49
6.30. READ SECURITY REGISTERS (48H) 50
6.31. SET READ PARAMETERS (C0H) 51
6.32. BURST READ WITH WRAP (0CH) 52
6.33. ENABLE QPI (38H) 52
6.34. CONTINUOUS READ MODE RESET (CRMR) (FFH)/ DISABLE QPI (FFH) 53
6.35. ENABLE RESET (66H) AND RESET (99H) 54
6.36. READ SERIAL FLASH DISCOVERABLE PARAMETER (5AH) 55
6.37. READ UNIQUE ID (5AH) 56

7. ELECTRICAL CHARACTERISTICS 61

7.1. POWER-ON TIMING 61

7.2. INITIAL DELIVERY STATE 61
7.3. DATA RETENTION AND ENDURANCE 61
7.4. LATCH UP CHARACTERISTICS 61
7.5. ABSOLUTE MAXIMUM RATINGS 62
7.6. CAPACITANCE MEASUREMENT CONDITION 62
7.7. DC CHARACTERISTICS 63
7.8. AC CHARACTERISTICS 64

8. ORDERING INFORMATION 67

9. PACKAGE INFORMATION 68

9.1. PACKAGE SOP8 208MIL 68
9.2. PACKAGE SOP16 300MIL 69
9.3. PACKAGE DFN8 (4X4X0.85) MM 70
9.4. PACKAGE WSON (6X5) MM 71
9.5. PACKAGE BGA (8X6) MM 72

10. REVISION HISTORY 73

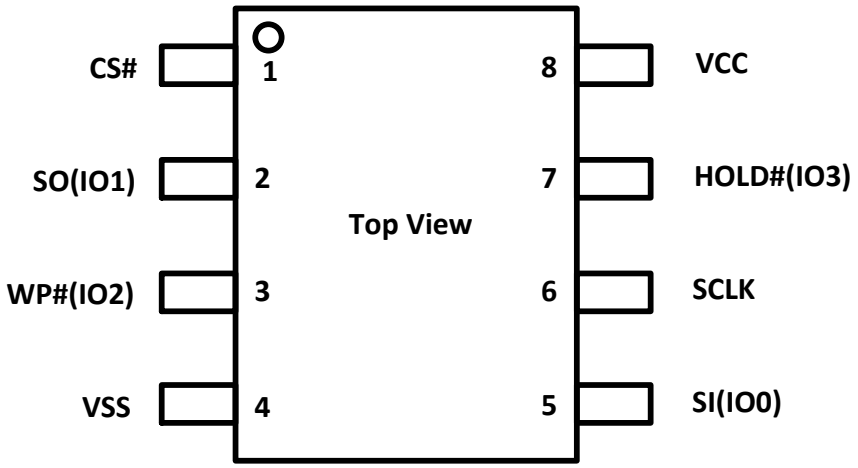
1. GENERAL DESCRIPTION

The XT25F128B (128M-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), Dual and Quad SPI. The Dual Output data is transferred with speed up to 216Mbits/s and the Quad I/O & Quad output data is transferred with speed up to 432Mbits/s.

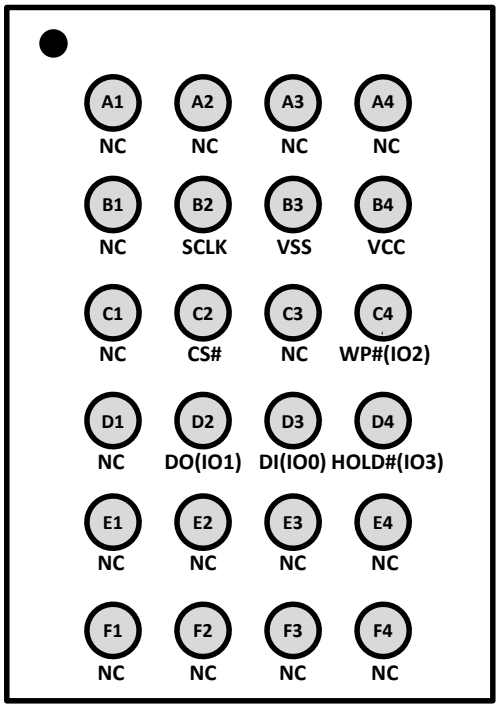
1.1. Available Ordering OPN

OPN	Package Type	Package Carrier
XT25F128BSSIGU	SOP8 208mil	Tube
XT25F128BSSIGT	SOP8 208mil	Tape & Reel
XT25F128BWOIGT	WSON8 6x5mm	Tape & Reel
XT25F128BDHIGT	DFN8 4x4mm	Tape & Reel
XT25F128BBGIGA	24-ball TFBGA	Tray
XT25F128BSFIGU	SOP16 300mil	Tube
XT25F128BSFIGT	SOP16 300mil	Tape & Reel

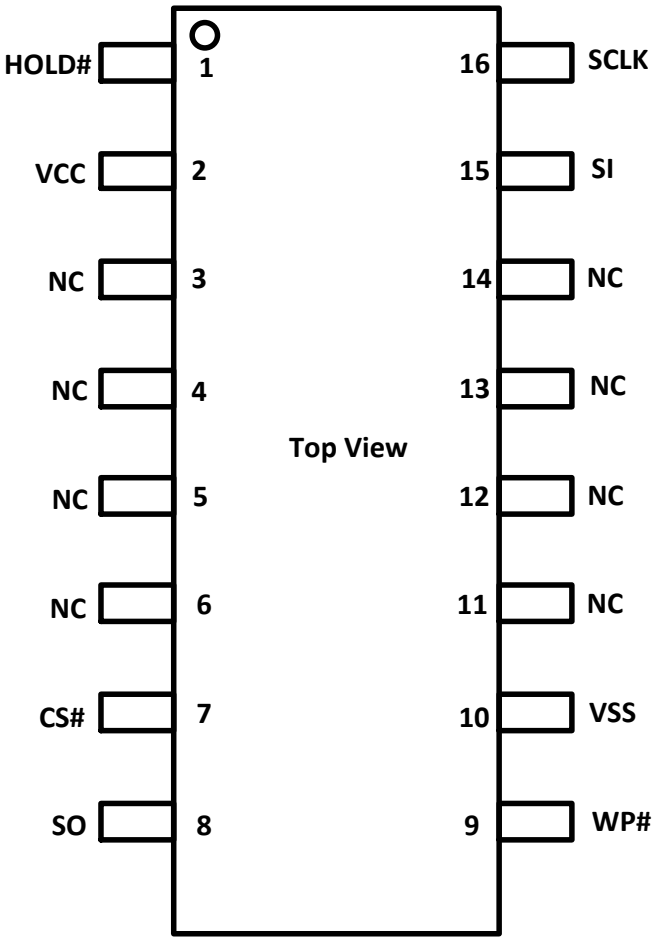
1.2. Connection Diagram



8 – LEAD SOP/DFN8/WSON8



24-ball TFBGA



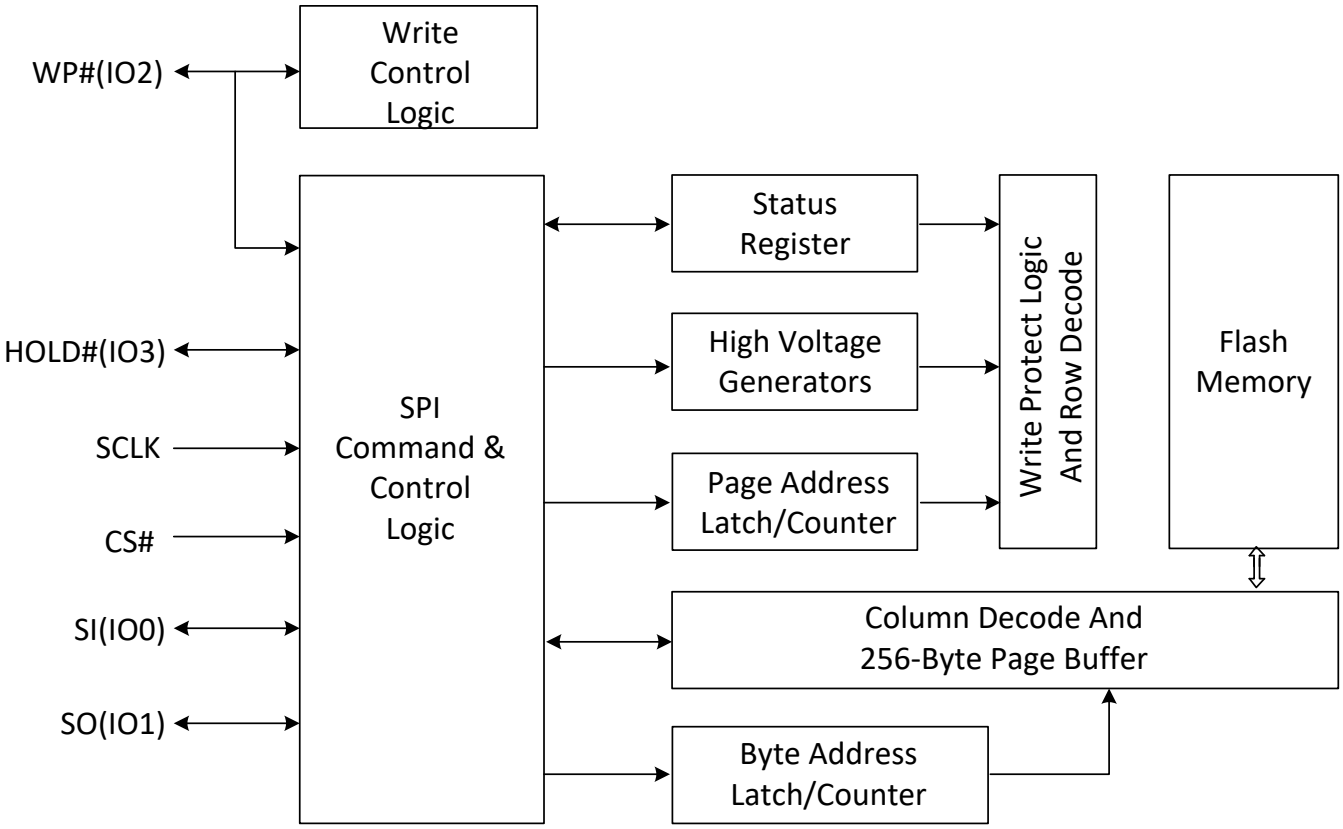
16-PIN SOP

Note: Only for 16-PIN SOP special order, Pin 3 is RESET# pin. Please contact XTX-tech for detail.

1.3. Pin Description

Pin Name	I/O	Description
CS#	I	Chip Select Input
SO(IO1)	I/O	Data Output(Data Input Output1)
WP#(IO2)	I/O	Write Protect Input(Data Input Output2)
VSS		Ground
SI(IO0)	I/O	Data Input(DataInputOutput0)
SCLK	I	Serial Clock Input
HOLD# (IO3)	I/O	Hold Input(Data Input Output3)
VCC		Power Supply

1.4. Block Diagram



2. MEMORY ORGANIZATION

XT25F128B

Each Device has	Each block has	Each sector has	Each page has	Remark
16M	64K/32K	4K	256	bytes
64K	256/128	16	-	pages
4K	16/8	-	-	sectors
256/512	-	-	-	blocks

UNIFORM BLOCK SECTOR ARCHITECTURE

XT25F128B 64Kbytes Block Sector Architecture

Block	Sector	Address range	
255	4095	FFF000H	FFFFFFH
	……	……	……
	4080	FF0000H	FF0FFFH
254	4079	FEF000H	FEFFFFH
	……	……	……
	4064	FE0000H	FE0FFFH
……	……	……	……
	……	……	……
	……	……	……
……	……	……	……
	……	……	……
	……	……	……
2	47	02F000H	02FFFFH
	……	……	……
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	……	……	……
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	……	……	……
	0	000000H	000FFFH

3. DEVICE OPERATION

SPI Mode

Standard SPI

The XT25F128B features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK. Note: “WP#” & “HOLD#” pin require external pull-up.

Dual SPI

The XT25F128B supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3BH and BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1. Note: “WP#” & “HOLD#” pin require external pull-up.

Quad SPI

The XT25F128B supports Quad SPI operation when using the “Quad Output Fast Read”,” Quad I/O Fast Read”, “Quad I/O Word Fast Read” (6BH, EBH, E7H) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be set.

QPI

The XT25F128B supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enable the QPI (38H)” command. The QPI mode utilizes all four IO pins to input the command code. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given times. “Enable the QPI (38H)” and “Disable the QPI (FFH)” commands are used to switch between these two modes. Upon power-up and after software reset using “Reset (99H)” command, the default state of the device is Standard/Dual/Quad SPI mode. The QPI mode requires the non-volatile Quad Enable bit (QE) in Status Register to be set.

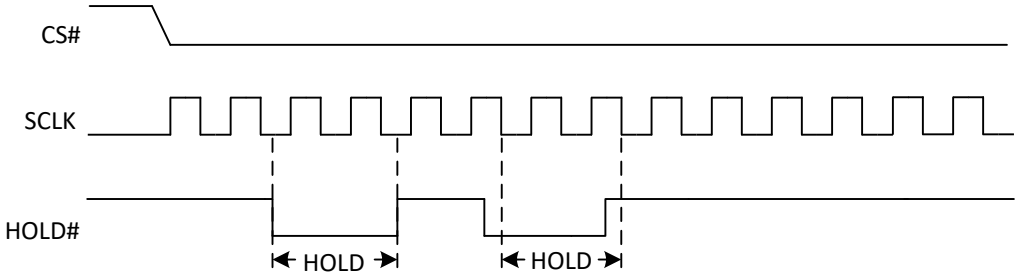
Hold

The HOLD# signal goes low to stop any serial communications with the device, but doesn’t stop the on going operation of writing status register, programming, or erasing which was in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

Both SI and SCLK don’t care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

Figure1.Hold Condition



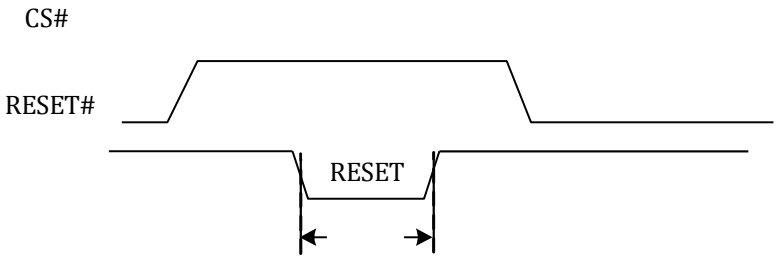
RESET

The RESET# pin allows the device to be reset by the control. Only available on the SOP16 package, a dedicated RESET# pin is provided and it is independent of QE bit setting.

The RESET# pin goes low for a period of tRLRH or longer will reset the flash. After the reset cycle, the flash will be at the following states:

- Standby mode
- All the volatile bits will return to the default status as power on.

Figure1a.Reset Condition



4. DATA PROTECTION

The XT25F128B provide the following data protection methods:

- Write Enable (WREN) command: The WREN command sets the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  - **POWER-UP**
  - **WRITE DISABLE (WRDI)**
  - **WRITE STATUS REGISTER (WRSR)**
  - **PAGE PROGRAM (PP)**
  - **SECTOR ERASE (SE) / BLOCK ERASE (BE) / CHIP ERASE (CE)**
- Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, BP0) bits define the section of the memory array that can be read only.
- Hardware Protection Mode: WP# goes low protect the BP0~BP4 bits and SRP bit.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command.

Table1.0 XT25F128B Protected area size (CMP=0)

Status Register Content					Memory Content			
BP4	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	252 to 255	FC0000H-FFFFFFH	256KB	Upper 1/64
0	0	0	1	0	248 to 255	F80000H-FFFFFFH	512KB	Upper 1/32
0	0	0	1	1	240 to 255	F00000H-FFFFFFH	1MB	Upper 1/16
0	0	1	0	0	224 to 255	E00000H-FFFFFFH	2MB	Upper 1/8
0	0	1	0	1	192 to 255	C00000H-FFFFFFH	4MB	Upper 1/4
0	0	1	1	0	128 to 255	800000H-FFFFFFH	8MB	Upper 1/2
0	1	0	0	1	0 to 3	000000H-03FFFFH	256KB	Lower 1/64
0	1	0	1	0	0 to 7	000000H-07FFFFH	512KB	Lower 1/32
0	1	0	1	1	0 to 15	000000H-0FFFFFH	1MB	Lower 1/16
0	1	1	0	0	0 to 31	000000H-1FFFFFH	2MB	Lower 1/8
0	1	1	0	1	0 to 63	000000H-3FFFFFH	4MB	Lower 1/4
0	1	1	1	0	0 to 127	000000H-7FFFFFH	8MB	Lower 1/2
X	X	1	1	1	0 to 255	000000H-FFFFFFH	16MB	ALL
1	0	0	0	1	255	FFF000H-FFFFFFH	4KB	Top Block
1	0	0	1	0	255	FFE000H-FFFFFFH	8KB	Top Block
1	0	0	1	1	255	FFC000H-FFFFFFH	16KB	Top Block
1	0	1	0	X	255	FF8000H-FFFFFFH	32KB	Top Block
1	0	1	1	0	255	FF8000H-FFFFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H-007FFFH	32KB	Bottom Block
1	1	1	1	0	0	000000H-007FFFH	32KB	Bottom Block

Table1.1 XT25F128B Protected area size (CMP=1)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	0 to 255	000000H-FFFFFFH	ALL	ALL
0	0	0	0	1	0 to 251	000000H-FBFFFFH	16128KB	Lower 63/64
0	0	0	1	0	0 to 247	000000H-F7FFFFH	15872KB	Lower 31/32
0	0	0	1	1	0 to 239	000000H-EFFFFFH	15MB	Lower 15/16
0	0	1	0	0	0 to 223	000000H-DFFFFFH	14MB	Lower 7/8
0	0	1	0	1	0 to 191	000000H-BFFFFFH	12MB	Lower 3/4
0	0	1	1	0	0 to 127	000000H-7FFFFFH	8MB	Lower 1/2
0	1	0	0	1	4 to 255	040000H-FFFFFFH	16128KB	Upper 63/64
0	1	0	1	0	8 to 255	080000H-FFFFFFH	15872KB	Upper 31/32
0	1	0	1	1	16 to 255	100000H-FFFFFFH	15MB	Upper 15/16
0	1	1	0	0	32 to 255	200000H-FFFFFFH	14MB	Upper 7/8
0	1	1	0	1	64 to 255	400000H-FFFFFFH	12MB	Upper 3/4
0	1	1	1	0	128 to 255	800000H-FFFFFFH	8MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 255	000000H-FFEFFFH	16380KB	L-4095/4096
1	0	0	1	0	0 to 255	000000H-FFDFFFH	16376KB	L-2047/2048
1	0	0	1	1	0 to 255	000000H-FFBFFFH	16368KB	L-1023/1024
1	0	1	0	X	0 to 255	000000H-FF7FFFH	16352KB	L-511/512
1	0	1	1	0	0 to 255	000000H-FF7FFFH	16352KB	L-511/512
1	1	0	0	1	0 to 255	001000H-FFFFFFH	16380KB	U-4095/4096
1	1	0	1	0	0 to 255	002000H-FFFFFFH	16376KB	U-2047/2048
1	1	0	1	1	0 to 255	004000H-FFFFFFH	16368KB	U-1023/1024
1	1	1	0	X	0 to 255	008000H-FFFFFFH	16352KB	U-511/512
1	1	1	1	0	0 to 255	008000H-FFFFFFH	16352KB	U-511/512

Table1.2 XT25F128B Individual Block Protection (WPS=1)

Block	Sector	Address range		Individual Block Lock Operation
255	4095	FFF000H	FFFFFFH	32 Sectors(Top/Bottom)/254 Blocks Block Lock: 36H+Address Block Unlock: 39H+Address Read Block Lock: 3DH+Address Global Block Lock: 7EH Global Block Unlock: 98H
	……	……	……	
	4080	FF0000H	FF0FFFH	
254	4079	FEF000H	FEFFFFH	
	……	……	……	
	4064	FE0000H	FE0FFFH	
……	……	……	……	
	……	……	……	
	……	……	……	
……	……	……	……	
	……	……	……	
	……	……	……	
2	47	02F000H	02FFFFH	
	……	……	……	
	32	020000H	020FFFH	
1	31	01F000H	01FFFFH	
	……	……	……	
	16	010000H	010FFFH	
0	15	00F000H	00FFFFH	
	……	……	……	
	0	000000H	000FFFH	

5. STATUS REGISTER

S15	S14	S13	S12	S11	S10	S9	S8
Reserved	CMP	Reserved	WPS	LB1	LB0	QE	SRP1

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	BP4	BP3	BP2	BP1	BP0	WEL	WIP

The status and control bits of the Status Register are as follows:

WIP bit.

The Write In Progress (WIP) bit indicates whether the memory is busy in programing/erasing/writing status register progress. When WIP bit sets to 1, that means the device is busy in programing/erasing/writing status register progress, when WIP bit sets to 0, that means the device is not in programing/erasing/writing status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, then Write Status Register, Program or Erase command will be accepted. when set to 0 the internal Write Enable Latch is reset, then no Write Status Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits.

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size and location of the flash memory to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1) becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written when the Hardware Protected mode has not been set. The Chip Erase (CE) command will be executed if the Block Protect (BP2, BP1, BP0) bits are 0 and CMP=0 or the Block Protect (BP2, BP1, BP0) bits are 1 and CMP=1.

SRP1, SRP0 bits.

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the type of write protection: software protection, hardware protection, power supply lock-down or one-time programmable protection.

SRP1	SRP0	WP#	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
0	1	0	Hardware Protected	WP#=0, the Status Register locked and cannot be written until the next power-up.
0	1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.
1	0	X	Power Supply Lock-Down(1)(2)	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle.
1	1	X	One-Time Program(2)	Status Register is permanently protected and cannot be written to.

NOTE:
1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available on special order (XT25F128BxxSx). Please contact XTX for details.

QE bit.

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# pin are enable. When the QE pin is set to 1, IO2 and IO3 pins will be enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the WP# or HOLD# pins are tied directly to the power supply or ground).

LB1, LB0, bits.

The LB1, LB0, bits are non-volatile One Time Program (OTP) bits in Status Register (S11-S10) that provide the write protect control and status to the Security Registers. The default state of LB1-LB0 are 0, the security registers are unlocked. The LB1-LB0 bits can be set to 1 individually using the Write Register instruction. The LB1-LB0 bits are One Time Programmable. Once LB0 or LB1 is set to 1, the corresponding Security Register page 1 or page 2 will become permanently lock for read-only and non-erasable, while if Any of the LB bits are is set to 1, then all 4 pages of the Security Register will become permanently lock for read-only non-erasable.

CMP bit.

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status register Memory Protection table for details. The default setting is CMP=0.

WPS

The WPS Bit is used to select which Write Protect scheme should be used. When WPS=0, the device will use the combination of CMP, BP (4:0) bits to protect a specific area of the memory array. When WPS=1, the device will utilize the Individual Block Locks to protect any individual sector or block. The default value for all Individual Block Lock bits is 1 upon device power on or after reset.

6. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, the most significant bit will be the first bit on SI, each bit will be latched on the following rising edge of SCLK.

See Table2, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table2. Commands

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	n-Bytes
Write Enable	06H						
Write Enable for Volatile Status Register	50H						
Write Disable	04H						
Read Status Register	05H	(S7-S0)					(continuous)
Read Status Register-1	35H	(S15-S8)					(continuous)
Write Status Register	01H	(S7-S0)	(S15-S8)				(continuous)
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)		(continuous)
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)	(continuous)
Dual I/O Fast Read	BBH	A23-A8(2)	A7-A0 M7-M0(2)	(D7-D0)(1)			(continuous)
Quad Output Fast Read	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(3)	(continuous)
Quad I/O Fast Read	EBH	A23-A0 M7-M0(4)	dummy(5)	(D7-D0)(3)			(continuous)
Quad I/O Word Fast Read	E7H	A23-A0 M7-M0(4)	dummy(6)	(D7-D0)(3)			(continuous)
Continuous Read Reset	FFH						
Page Program	02H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	
Quad Page Program	32H	A23-A16	A15-A8	A7-A0	(D7-D0)(3)		
Sector Erase	20H	A23-A16	A15-A8	A7-A0			
Block Erase(32KB)	52H	A23-A16	A15-A8	A7-A0			
Block Erase(64KB)	D8H	A23-A16	A15-A8	A7-A0			

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	n-Bytes
Chip Erase	C7/60H						
Enable QPI	38H						
Set Burst with Wrap	77H	dummy	dummy	dummy	W6-W4		
Deep Power-Down	B9H						
Release From Deep Power-Down, And Read Device ID	ABH	dummy	dummy	dummy	(ID7-DID0)		(continuous)
Release From Deep Power-Down	ABH						
Manufacturer/Device ID	90H	A23-A16	A15-A8	A7-A0	(MID7-MID0)	(DID7-DID0)	(continuous)
Manufacturer/Device ID by Dual I/O	92H	A23-A8	A7-A0, M[7:0]	(M7-M0) (ID7-ID0)			(continuous)
Manufacturer/Device ID by Quad I/O	94H	A23-A0, M[7:0]	dummy	(M7-M0) (ID7-ID0)			
Read Serial Flash Discov-erable Parameters	5AH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Read Unique ID	5AH	00h	00h	94h	dummy	(D7-D0)	(continuous)
Read Identification	9FH	(M7-M0)	(ID15-ID8)	(ID7-ID0)			(continuous)
Erase Security Regis-ter(8)	44H	A23-A16	A15-A8	A7-A0			
Program Security Regis-ter(8)	42H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	
Read Security Register(8)	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	
Enable Reset	66H						
Reset	99H						
Individual Block Lock	36H	A23-A16	A15-A8	A7-A0			
Individual Block Unlock	39H	A23-A16	A15-A8	A7-A0			
Read Block Lock	3DH	A23-A16	A15-A8	A7-A0			
Global Block Lock	7EH						
Global Block Unlock	98H						

Table2a. Commands (QPI)

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6
Clock Number	**（0,1）**	**（2,3）**	**（4,5）**	**（6,7）**	**（8,9）**	**（10,11**
Write Enable	06H					
Write Enable for Volatile Status Register	50H					
Write Disable	04H					
Read Status Register	05H	(S7-S0)				
Read Status Register-1	35H	(S15-S8)				
Write Status Register	01H	(S7-S0)	(S15-S8)			
Page Program	02H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)
Sector Erase	20H	A23-A16	A15-A8	A7-A0		
Block Erase(32KB)	52H	A23-A16	A15-A8	A7-A0		
Block Erase(64KB)	D8H	A23-A16	A15-A8	A7-A0		
Chip Erase	C7/60H					
Deep Power-Down	B9H					
Set Read Parameters	C0H	P7-P0				
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Burst Read with Wrap	0CH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Quad I/O Fast Read	EBH	A23-A0 M7-M0(4)	dummy(5)	(D7-D0)(3)		
Release from Deep Power-Down, And Read Device ID(10)	ABH	dummy	dummy	dummy * N	(ID7-ID0)	
Manufacturer/Device ID(11)	90H	dummyx2	00H	dummy * N	MID7~MID0	(ID7-ID0)
Disable QPI	FFH					
Enable Reset	66H					
Reset	99H					
Individual Block Lock	36H	A23-A16	A15-A8	A7-A0		
Individual Block Unlock	39H	A23-A16	A15-A8	A7-A0		
Read Block Lock	3DH	A23-A16	A15-A8	A7-A0		
Global Block Lock	7EH					
Global Block Unlock	98H					
Read Serial Flash Discovera-ble Parameter	5AH					

NOTE:

1. Dual Output data

   IO0 = (D6, D4, D2, D0)

   IO1 = (D7, D5, D3, D1)

2. Dual Input Address

   IO0 = A22, A20, A18, A16, A14, A12, A10, A8,A6, A4, A2, A0, M6, M4, M2, M0

IO1 = A23, A21, A19, A17, A15, A13, A11, A9,A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data
   IO0 = (D4, D0, ...)
   IO1 = (D5, D1, ...)
   IO2 = (D6, D2, ...)
   IO3 = (D7, D3, ...)
4. Quad Input Address
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3
5. Quad I/O Fast Read Data
   IO0 = (x, x, x, x, D4, D0,…)
   IO1 = (x, x, x, x, D5, D1,…)
   IO2 = (x, x, x, x, D6, D2,…)
   IO3 = (x, x, x, x, D7, D3,…)
6. Quad I/O Word Fast Read Data
   IO0 = (x, x, D4, D0,…)
   IO1 = (x, x, D5, D1,…)
   IO2 = (x, x, D6, D2,…)
   IO3 = (x, x, D7, D3,…)
7. Quad I/O Word Fast Read Data: the lowest address bit must be 0.
8. Security Registers Address:
   Security Register0: A23-A16=00H, A15-A8=00H, A7-A0= Byte Address;
   Security Register1: A23-A16=00H, A15-A8=01H, A7-A0= Byte Address;
   Security Register2: A23-A16=00H, A15-A8=02H, A7-A0= Byte Address;
   Security Register3: A23-A16=00H, A15-A8=03H, A7-A0= Byte Address.
9. QPI Command, Address, Data input/output format:
   CLK# = 0 1 2 3 4 5 6 7 8 9 10 11
   IO0 = C4, C0, A20, A16, A12, A8, A4, A0, D4, D0, D4, D0
   IO1 = C5, C1, A21, A17, A13, A9, A5, A1, D5, D1, D5, D1
   IO2 = C6, C2, A22, A18, A14, A10, A6, A2, D6, D2, D6, D2
   IO3 = C7, C3, A23, A19, A15, A11, A7, A3, D7, D3, D7, D4
10. QPI mode: Release from Deep Power-Down, And Read Device ID (ABH)
    N dummy cycles should be inserted before ID read cycle, refer to C0H command
11. QPI mode: Manufacturer/Device ID (90H)
    N dummy cycles should be inserted before ID read cycle, refer to C0H command

Table of ID Definitions:

XT25F128B

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	0B	40	18
90H	0B		17
ABH			17

6.1. Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) command. The Write Enable (WREN) command sequence: CS# goes low→Sending the Write Enable command→CS# goes high.

Figure2.Write Enable Sequence Diagram

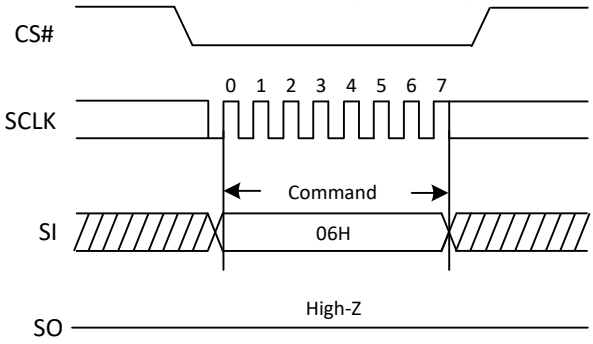
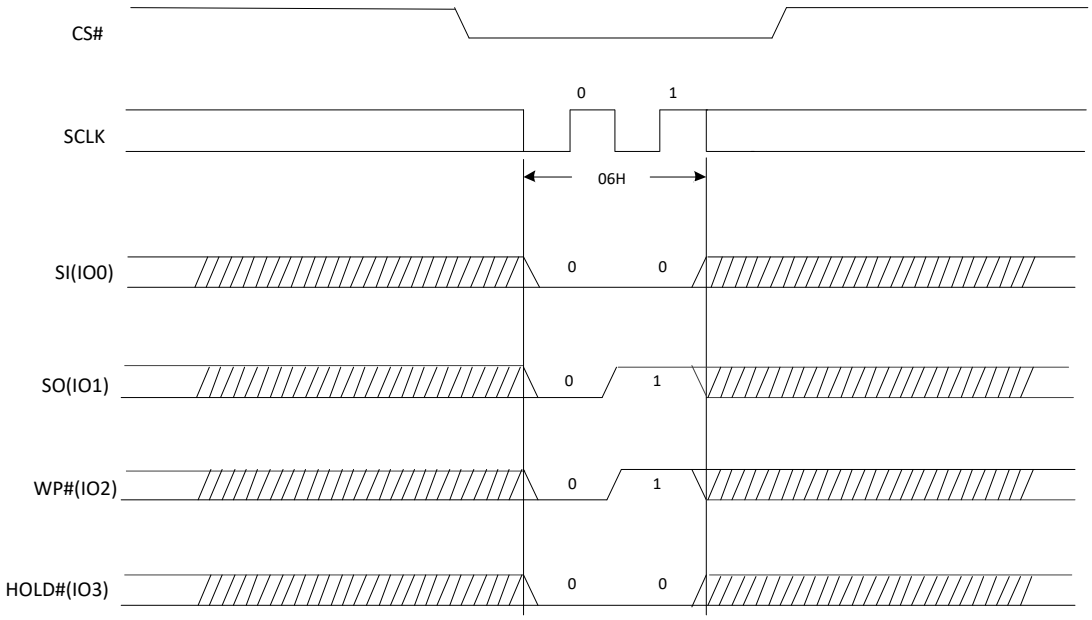


Figure2a. Write Enable Sequence Diagram (QPI)



6.2. Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

Figure3.Write Enable for Volatile Status Register Sequence Diagram

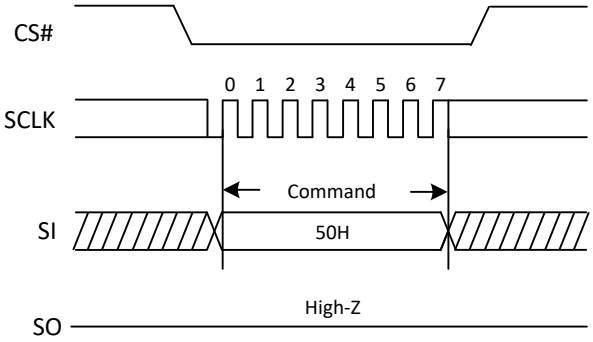
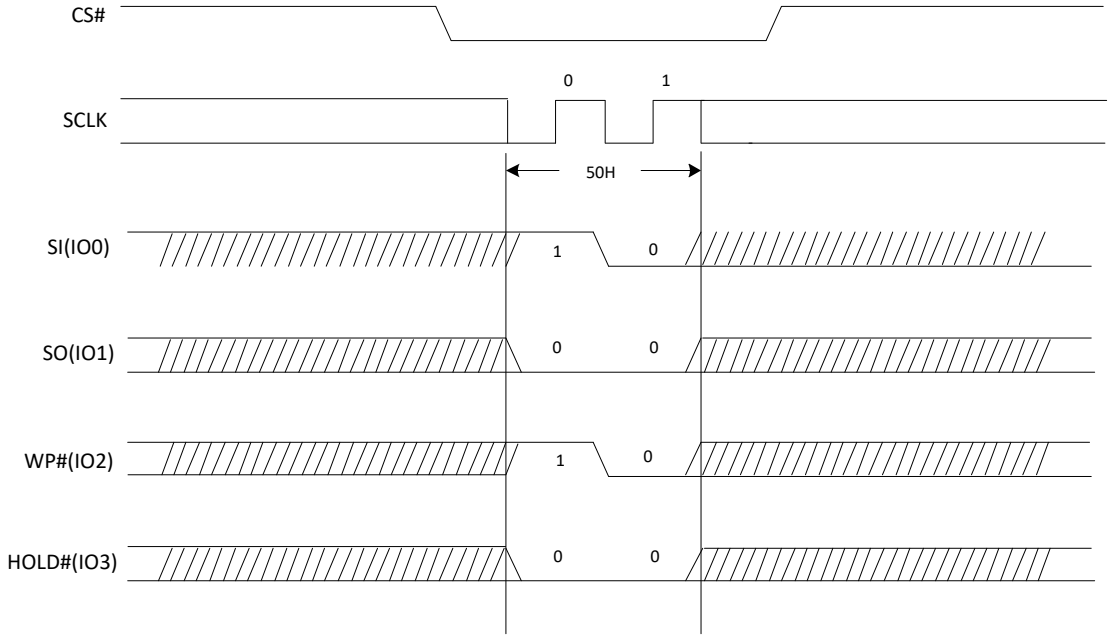


Figure3a. Write Enable for Volatile Status Register Sequence Diagram (QPI)



6.3. Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low→Sending the Write Disable command→CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

Figure4.Write Disable Sequence Diagram

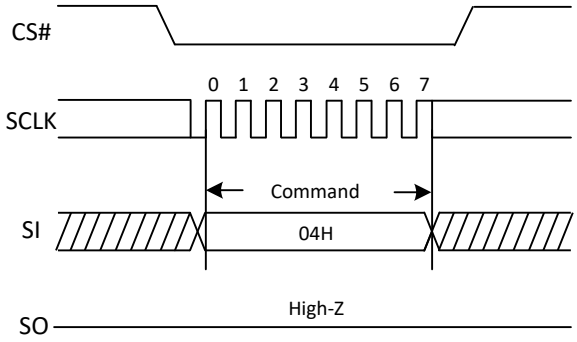
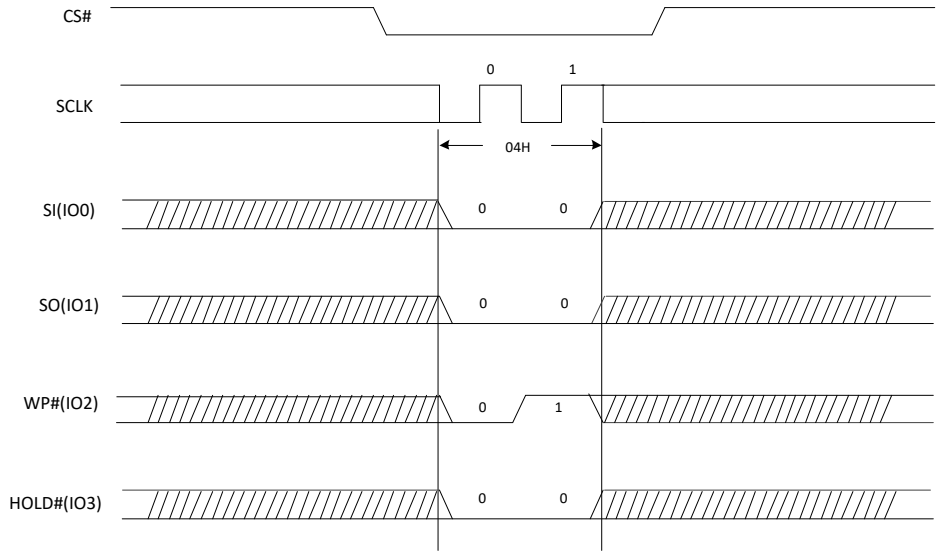


Figure4a. Write Disable Sequence Diagram (QPI)



6.4. Read Status Register (RDSR) (05H or 35H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register can be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code “05H”, the SO will output Status Register bits S7~S0. The command code “35H”, the SO will output Status Register bits S15~S8.

Figure5. Read Status Register Sequence Diagram

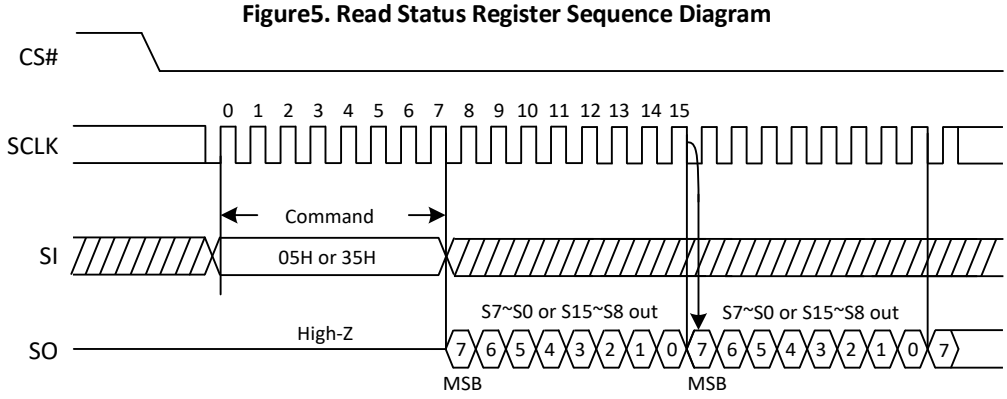
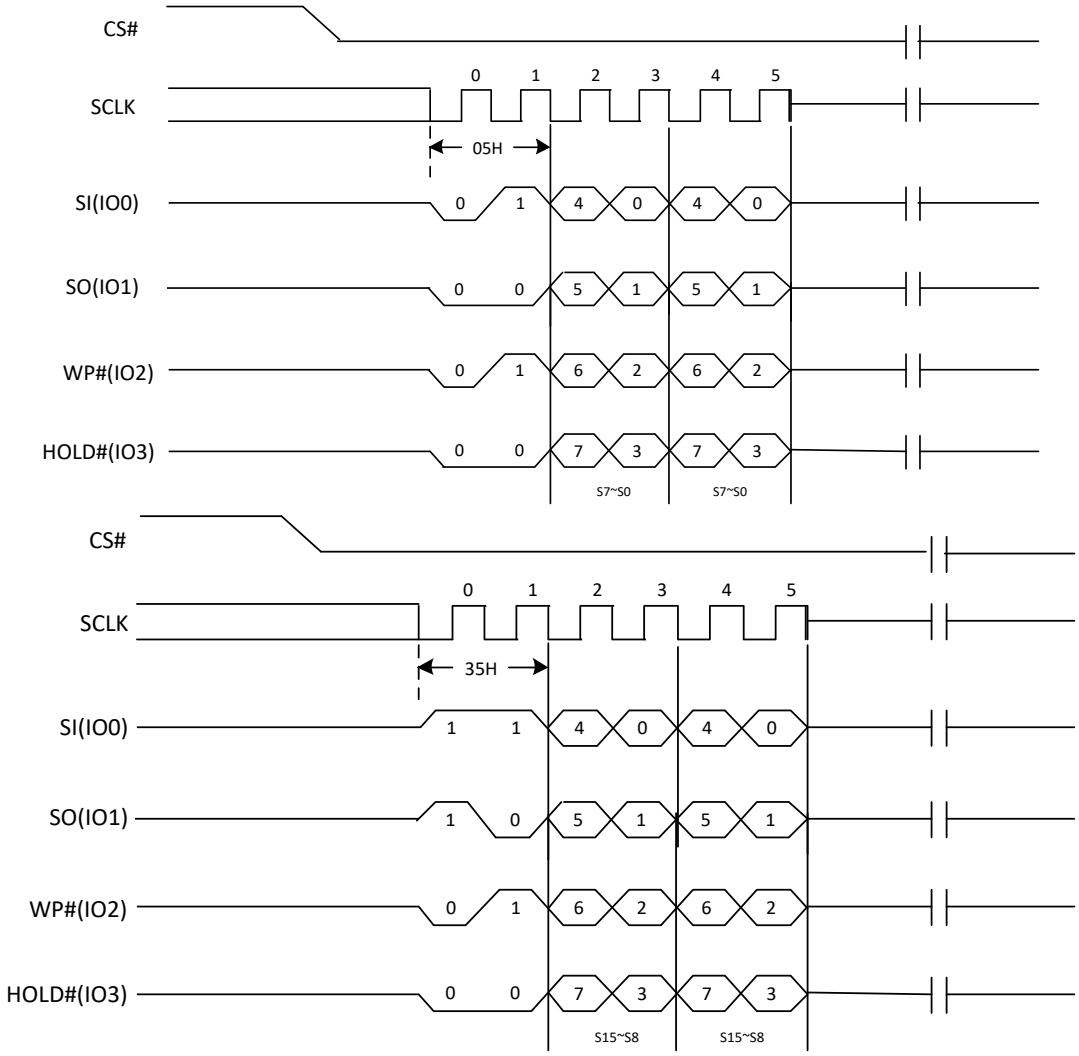


Figure5a. Read Status Register Sequence Diagram (QPI)



6.5. Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S15, S1 and S0 of the Status Register. CS# must be driven high after the eighth or sixteen bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. If CS# is driven high after eighth bit of the data byte, the CMP and QE bit will be cleared to 0. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table1. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

Figure6.Write Status Register Sequence Diagram

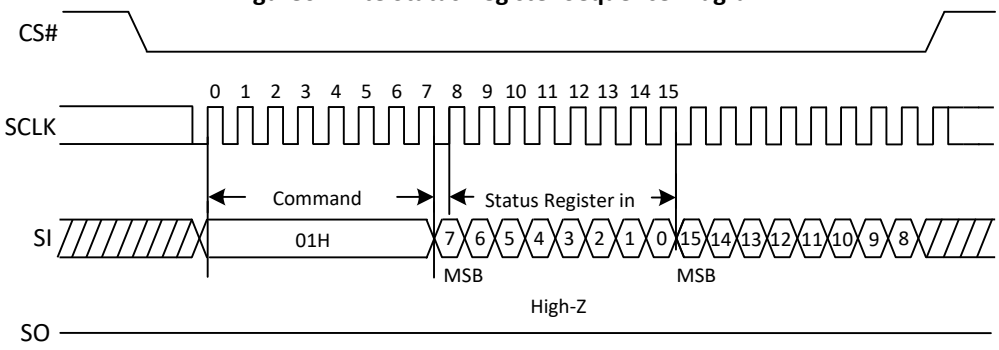
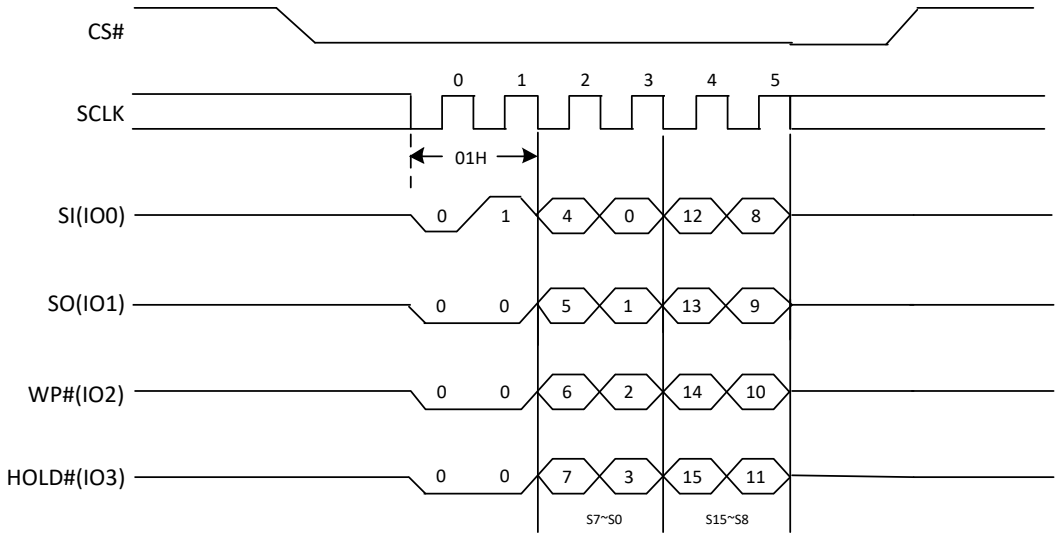


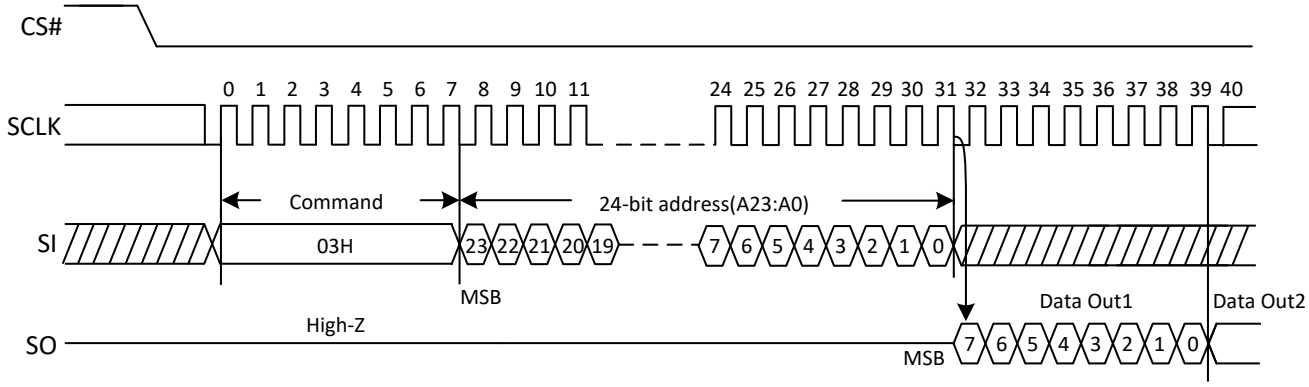
Figure6a. Write Status Register Sequence Diagram (QPI)



6.6. Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The first byte can be addressed at any location and the address is automatically incremented to the next address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

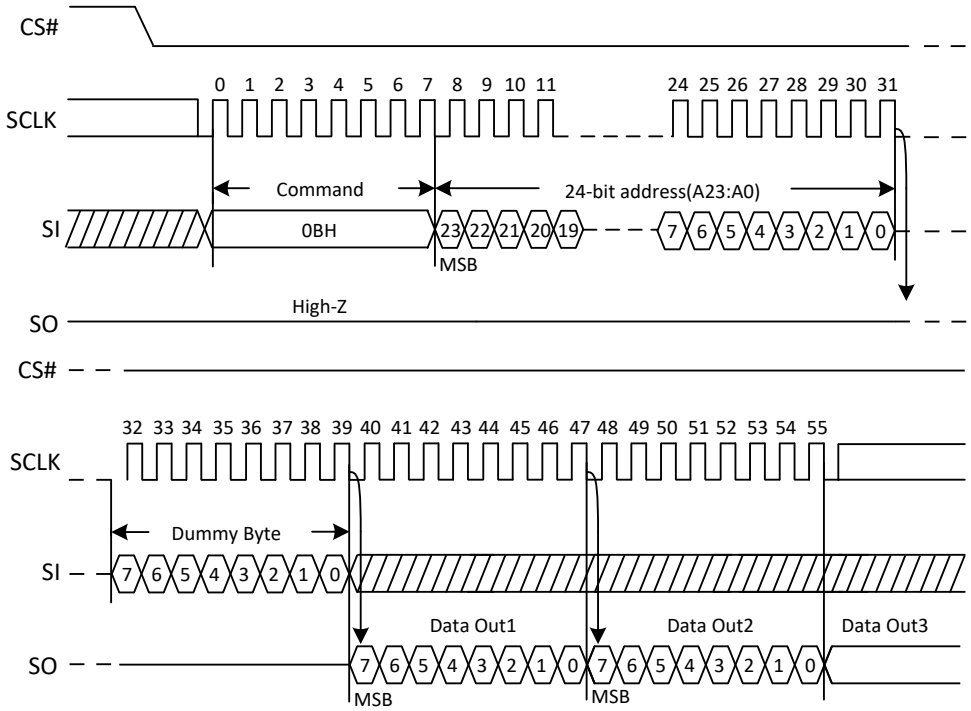
Figure7.Read Data Bytes Sequence Diagram



6.7. Read Data Bytes At Higher Speed (Fast Read) (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte can be addressed at any location and the address is automatically incremented to the next address after each byte of data is shifted out.

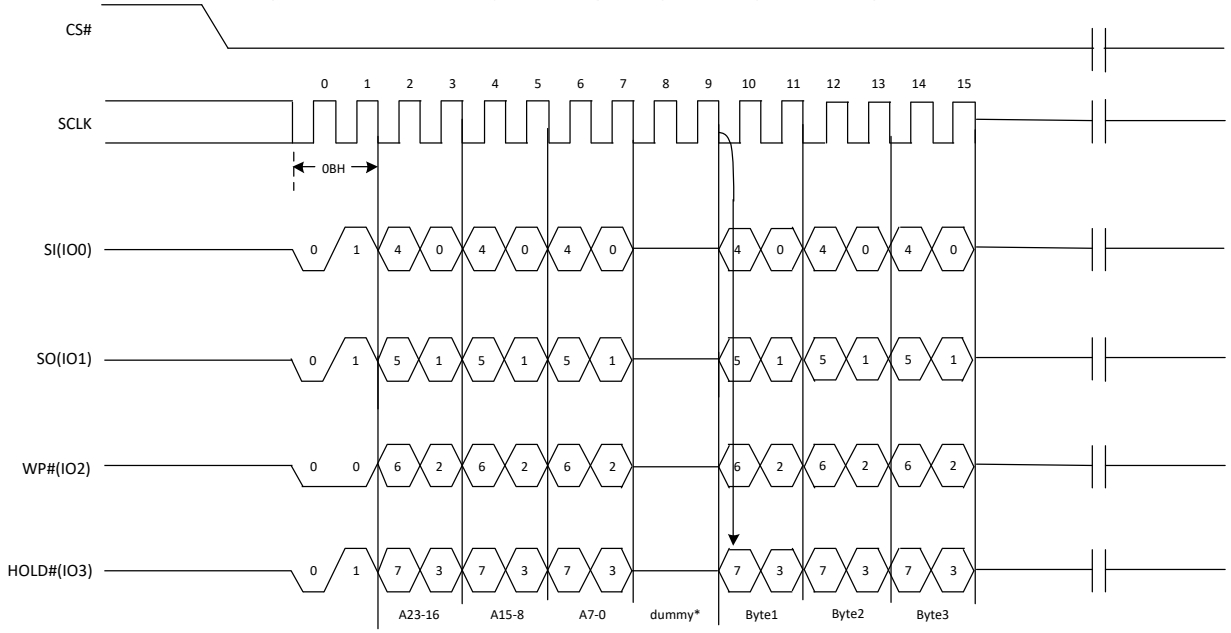
Figure8.Read Data By test Higher Speed Sequence Diagram



Fast Read (0BH) in QPI mode

The Fast Read command is also supported in QPI mode. In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8. When the dummy cycle is configured to 4, addr [0] input must be 0.

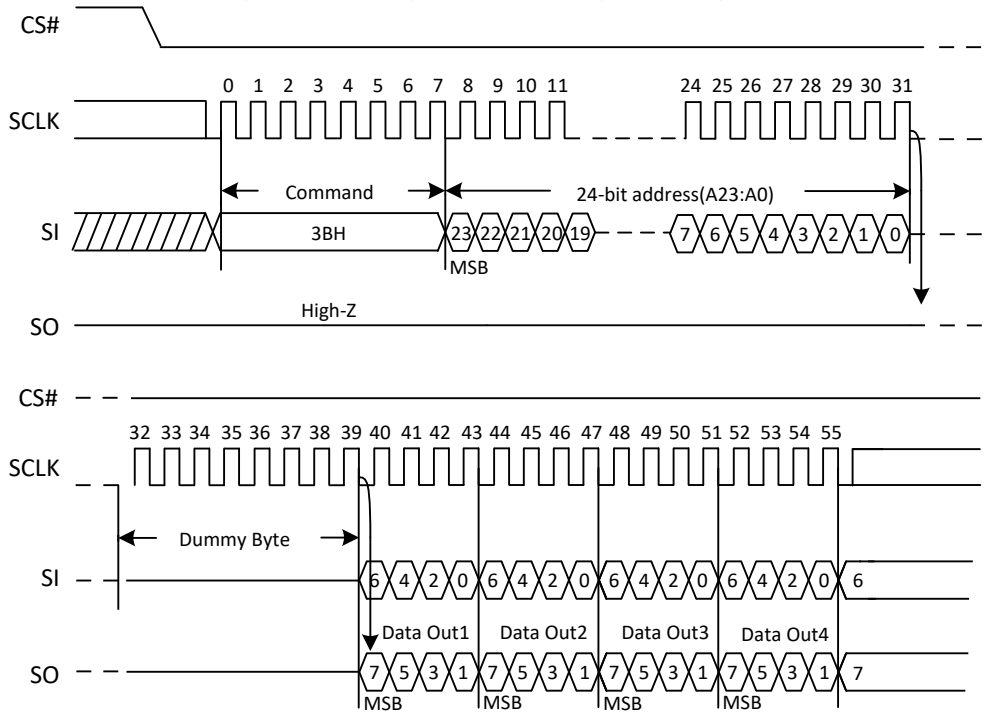
Figure8a. Read Data Bytes at Higher Speed Sequence Diagram (QPI)



6.8. Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in Figure9. The first byte can be addressed at any location and the address is automatically incremented to the next address after each byte of data is shifted out.

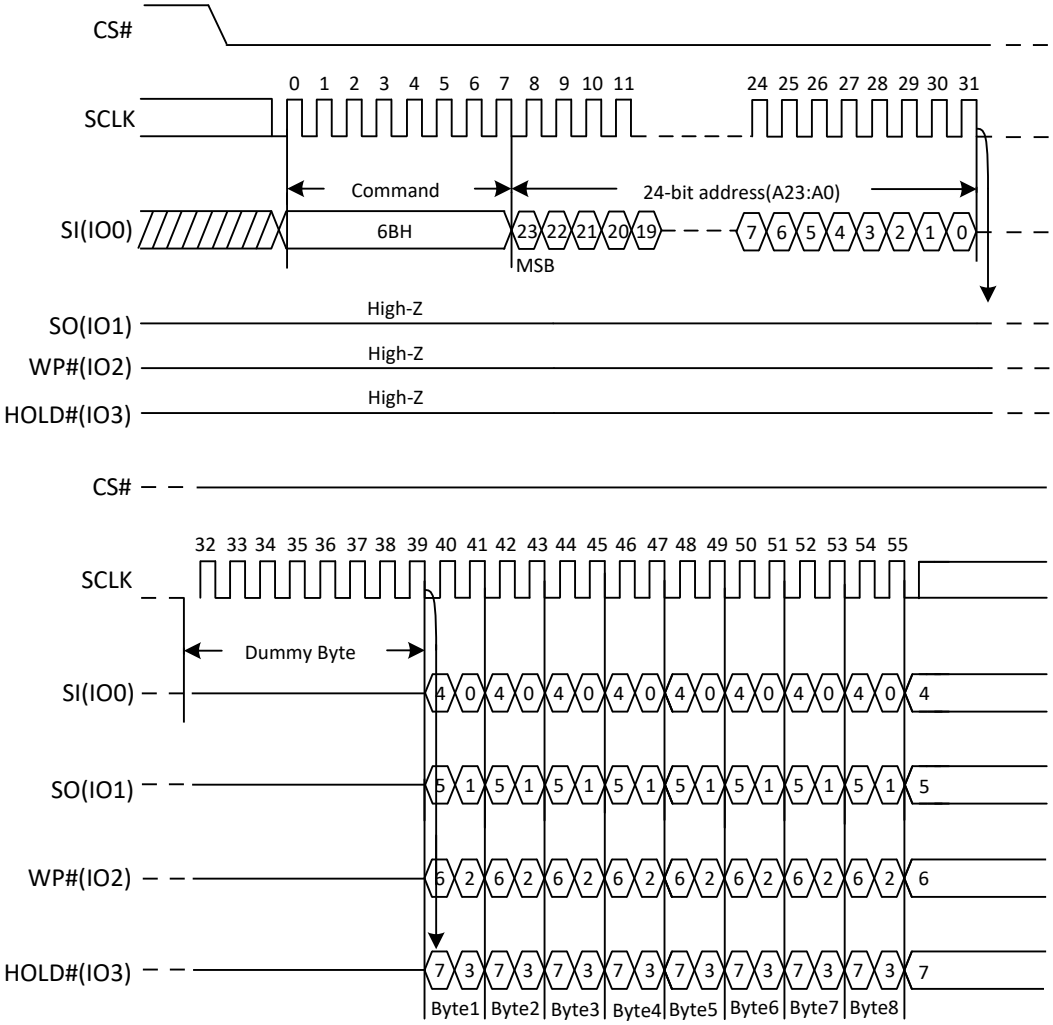
Figure9.Dual Output Fast Read Sequence Diagram



6.9. Quad Output Fast Read (6BH)

The Quad Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown in Figure10. The first byte addressed can be at any location and the address is automatically incremented to the next address after each byte of data is shifted out.

Figure 10.Quad Output Fast Read Sequence Diagram



6.10. Dual I/O Fast Read (BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in Figure11. The first byte can be addressed at any location and the address is automatically incremented to the next address after each byte of data is shifted out.

Dual I/O Fast Read with “Continuous Read Mode”

The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5- 4) =(1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in Figure12. If the “Continuous Read Mode” bits (M5- 4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5- 4) before issuing normal command.

Figure11.Dual I/O Fast Read Sequence Diagram (M5-4≠(1,0))

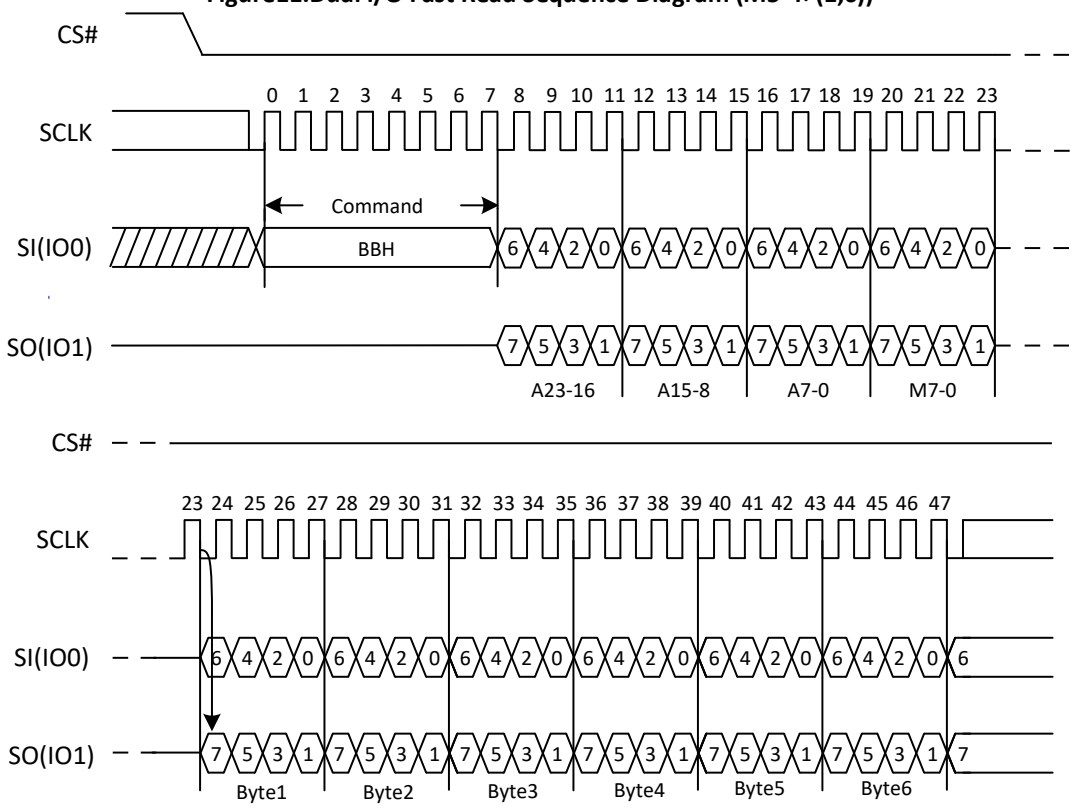
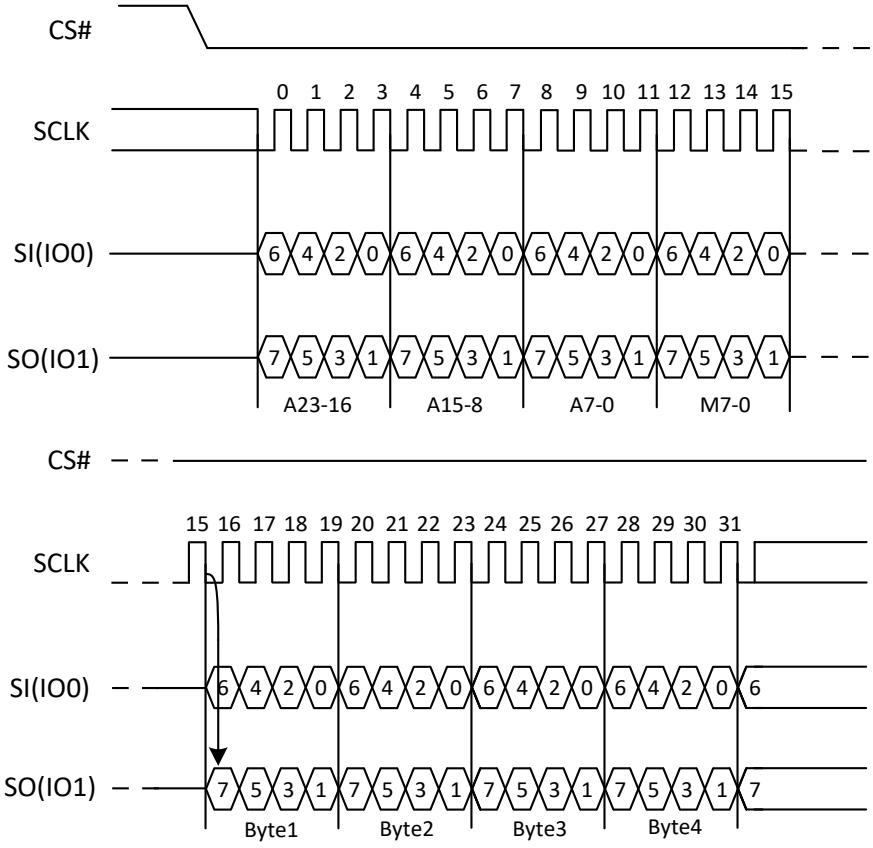


Figure12.Dual I/O Fast Read Sequence Diagram (M5-4=(1,0))



6.11. Quad I/O Fast Read (EBH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The command sequence is shown in Figure13. The first byte can be addressed at any location and the address is automatically incremented to the next address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command.

Quad I/O Fast Read with “Continuous Read Mode”

The Quad I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) =(1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. The command sequence is shown in Figure14. If the “Continuous Read Mode” (M5- 4) do not equal (1, 0), the next command requires the first EBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5- 4) before issuing normal command.

Figure13.Quad I/O Fast Read Sequence Diagram (M5-4≠(1,0))

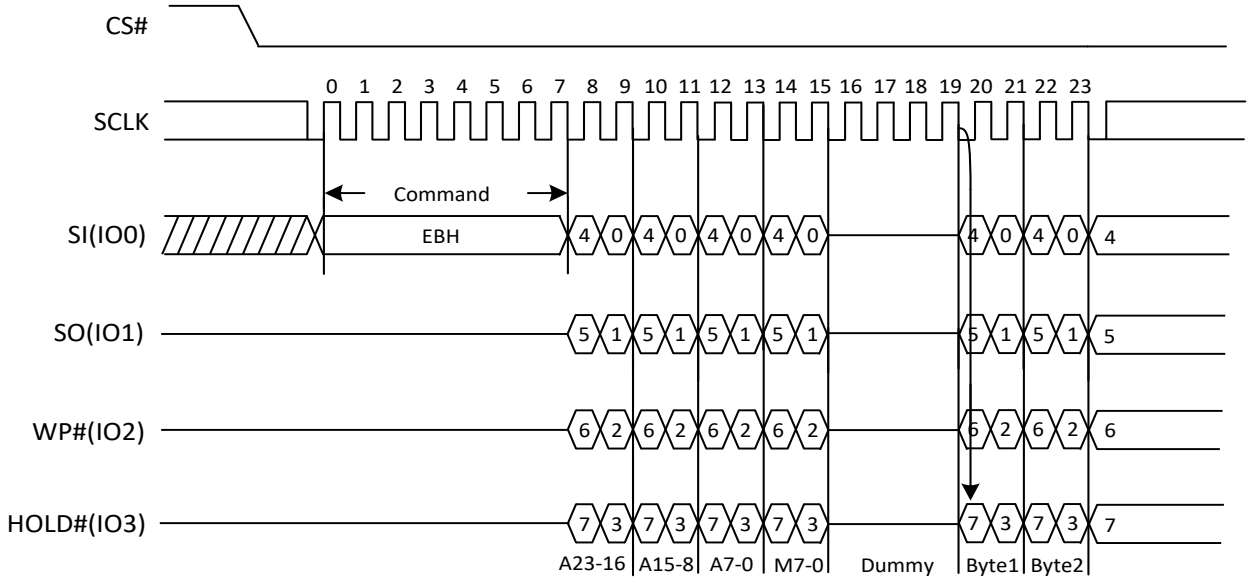
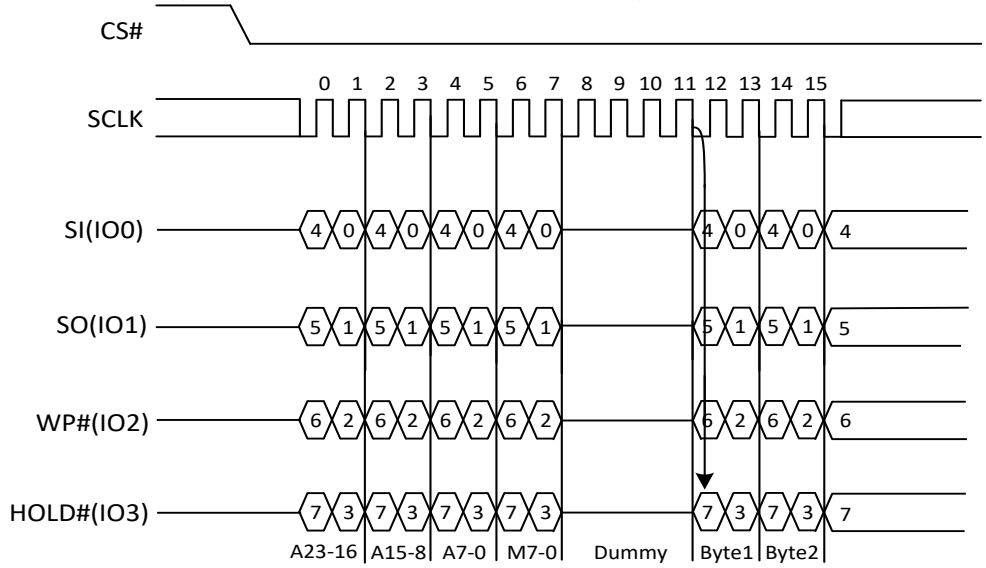


Figure14.Quad I/O Fast Read Sequence Diagram (M5-4=(1,0))



Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

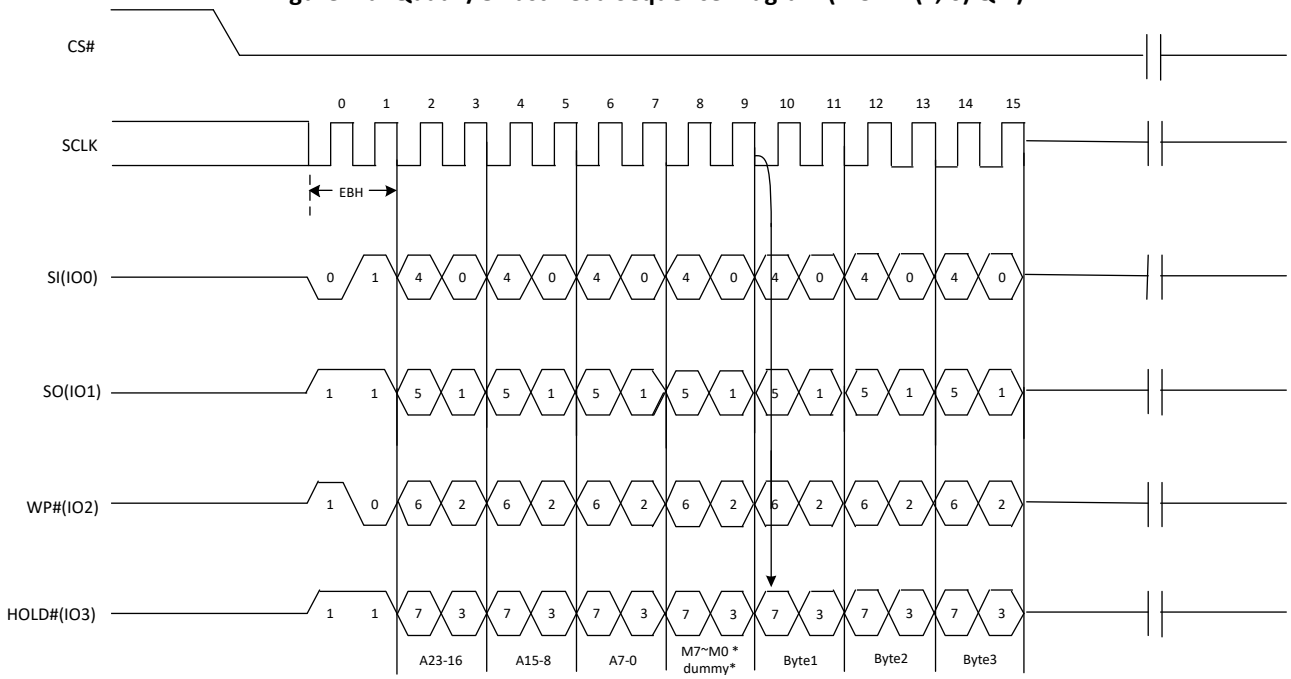
The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to EBH. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following EBH commands. When "Wrap Around" is enabled, the data being accessed can be limited to an 8/16/32/64-byte section within a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

Quad I/O Fast Read (EBH) in QPI mode

The Quad I/O Fast Read command is also supported in QPI mode. See Figure 14a. In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4/6/8. When the dummy cycle is configured to 4, addr[0] input must be 0. In QPI mode, the "Continuous Read Mode" bits M7-M0 are also considered as dummy clocks. "Continuous Read Mode" feature is also available in QPI mode for Quad I/O Fast Read command. "Wrap Around" feature is not available in QPI mode for Quad I/O Fast Read command. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0CH) command must be used.

Figure14a. Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0) QPI)



6.12. Quad I/O Word Fast Read (E7H)

The Quad I/O Word Fast Read command is similar to the Quad I/O Fast Read command except that the lowest address bit (A0) must equal 0 and only 2-dummy clock. The command sequence is shown in followed Figure15. The first byte can be addressed at any location. The address is automatically incremented to the next address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Word Fast read command.

Quad I/O Word Fast Read with "Continuous Read Mode"

The Quad I/O Word Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5- 4) = (1, 0), then the next Quad I/O Word Fast Read command (after CS# is raised and then lowered) does not require the E7H command code. The command sequence is shown in Figure15. If the "Continuous Read Mode" bits (M5- 4) do not equal (1, 0), the next command requires the first E7H command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M7-0) before issuing normal command.

Figure15.Quad I/O Word Fast Read Sequence Diagram (M5-4≠(1,0))

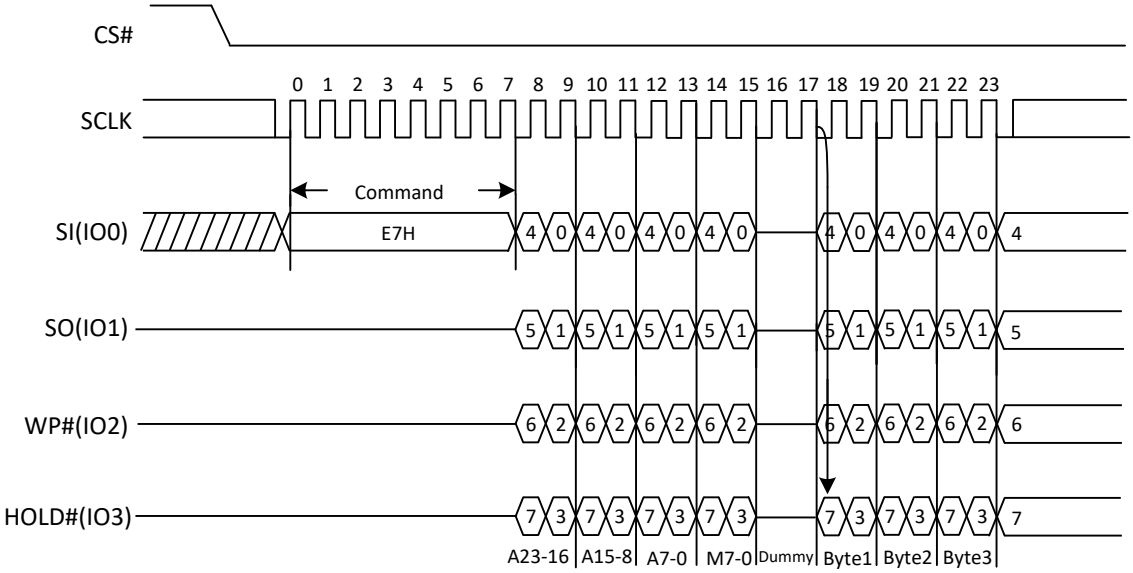
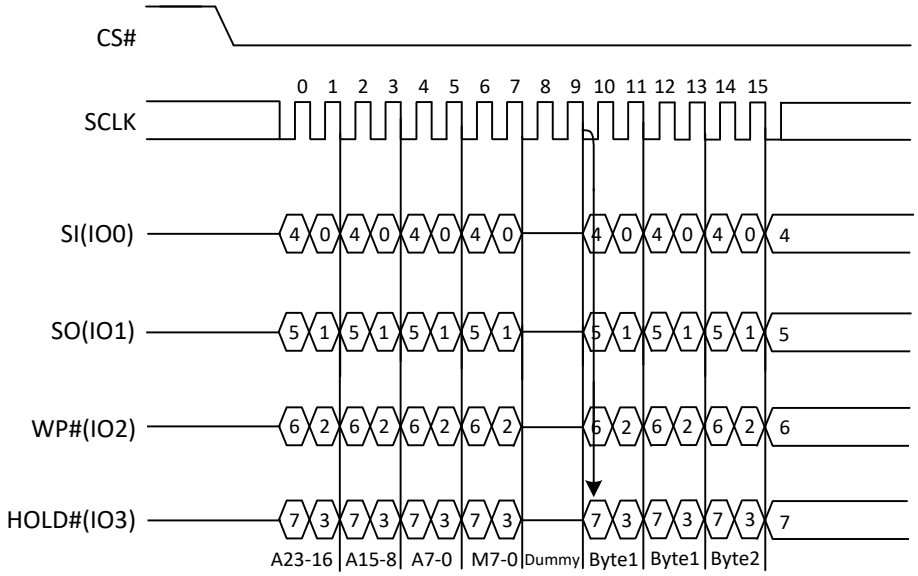


Figure15a.Quad I/O Word Fast Read Sequence Diagram (M5-4=(1,0))



Quad I/O Word Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Quad I/O Word Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to E7H. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following E7H commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section within a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until CS# is pulled high to terminate the command. The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

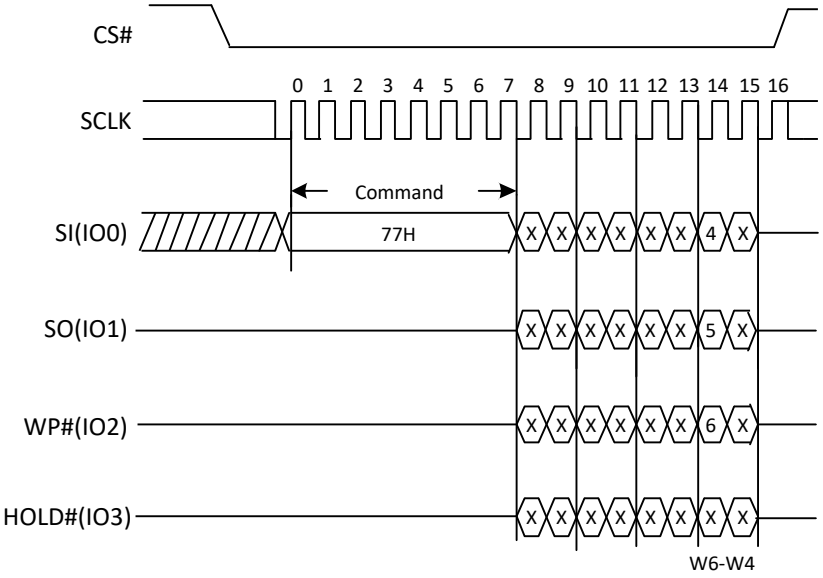
6.13. Set Burst with Wrap (77H)

The Set Burst with Wrap command is used in conjunction with "Quad I/O Fast Read" and "Quad I/O Word Fast Read" command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode. The Set Burst with Wrap command sequence: CS# goes low →Send Set Burst with Wrap command →Send 24 dummy bits →Send 8 bits "Wrap bits"→CS# goes high

W6,W5	W4=0		W4=1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0, 0	Yes	8-byte	No	N/A
0, 1	Yes	16-byte	No	N/A
1, 0	Yes	32-byte	No	N/A
1, 1	Yes	64-byte	No	N/A

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following "Quad I/O Fast Read" and "Quad I/O Word Fast Read" command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1. In QPI mode, the "Burst Read with Wrap (0CH)" command should be used to perform the Read Operation with "Wrap Around" feature. The Wrap Length set by W5-W6 in Standard SPI mode is still valid in QPI mode and can also be re-configured by "Set Read Parameters (C0H) command.

Figure16. Set Burst with Wrap Sequence Diagram



6.14. Page Program (PP) (02H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low→sending Page Program command→3-byte address on SI→at least 1 byte data on SI→ CS# goes high. The command sequence is shown in Figure17. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) will not be executed.

Figure17.PageProgramSequenceDiagram

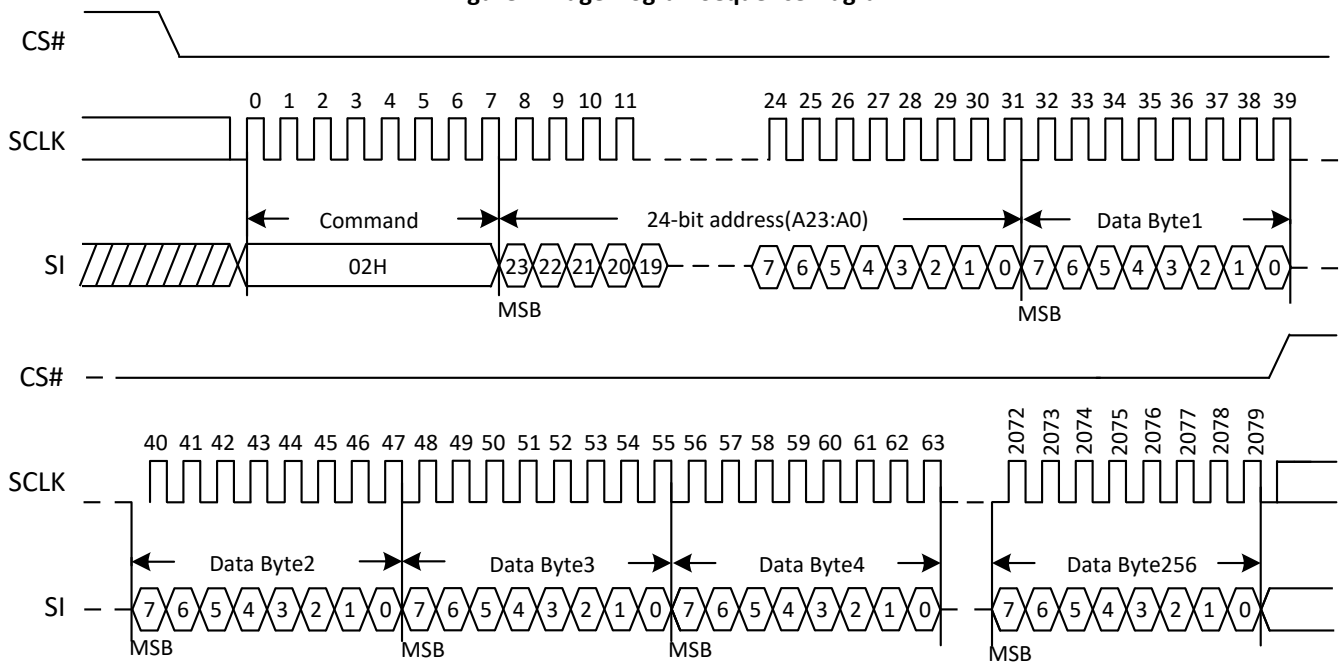
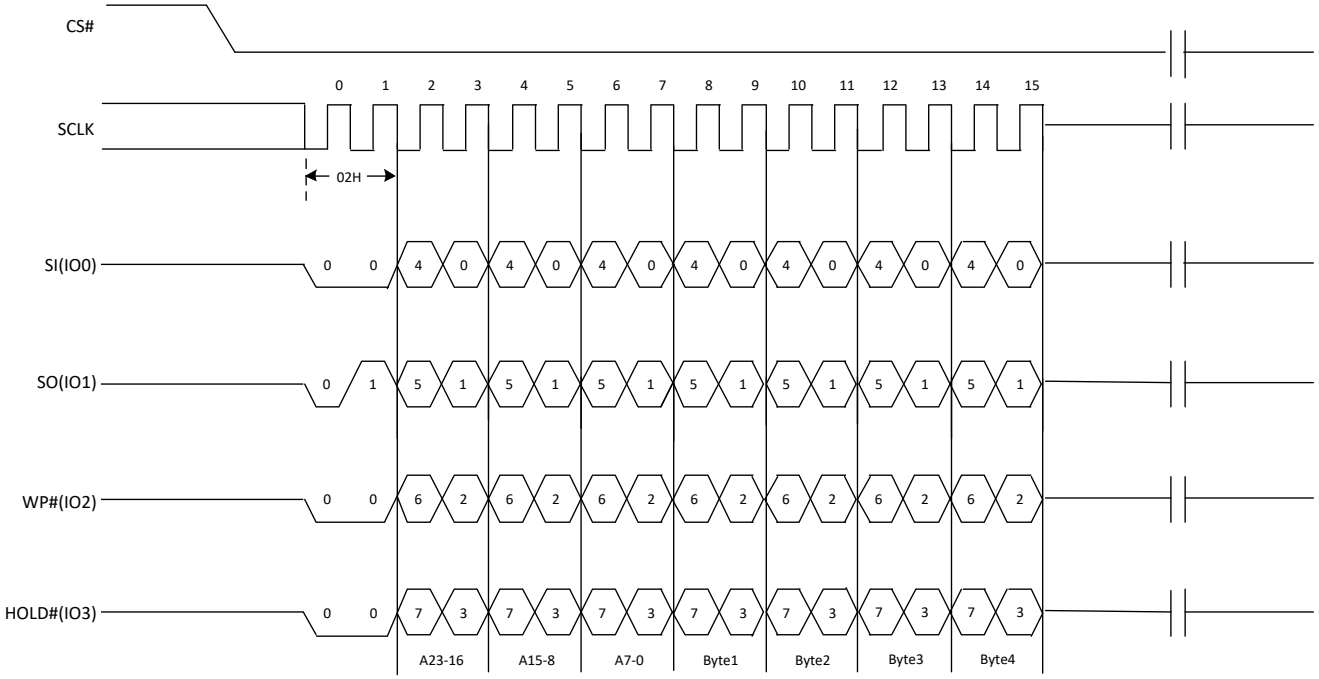


Figure17a. Page Program Sequence Diagram (QPI)



6.15. Quad Page Program (QPP) (32H)

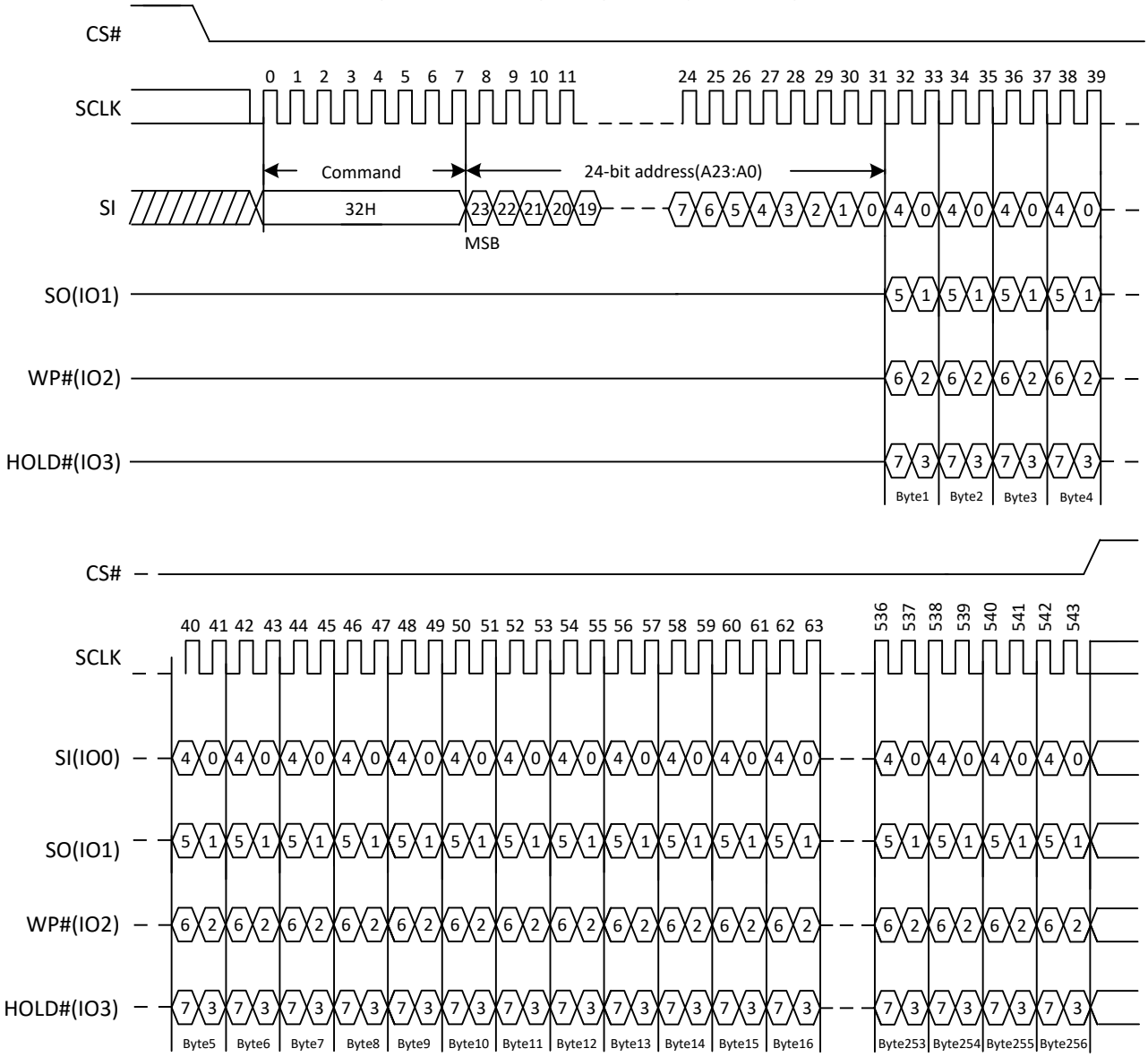
The Quad Page Program command is for programming the memory, while the data bytes are transfered via 4 pins: IO0, IO1, IO2, and IO3. To use Quad Page Program, the Quad enable in status register Bit9 must be set (QE=1). A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The Quad Page Program command is entered by driving CS# Low, followed by the command code (32H), three address bytes and at least one data byte on IO pins.

The command sequence is shown in Figure18. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program command will not be executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is tPP) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset

A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) will not be executed.

Figure18.Quad Page Program Sequence Diagram



6.16. Sector Erase (SE) (20H)

The Sector Erase (SE) command is for erasing all the data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit, before sending the Sector Erase command.. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command.

The Sector Erase command sequence: CS# goes low→sending Sector Erase command→3-byte address on SI→CS# goes high. The command sequence is shown in Figure20. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command will not be executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bit(see Table1.0&1.1) will not be executed.

Note: Power disruption during erase operation will cause incomplete erase, thus it is recommend to perform a re-erase once power resume.

Figure19. Sector Erase Sequence Diagram

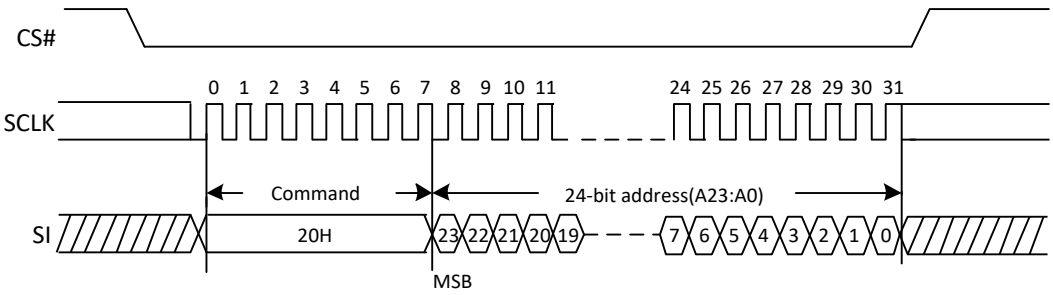
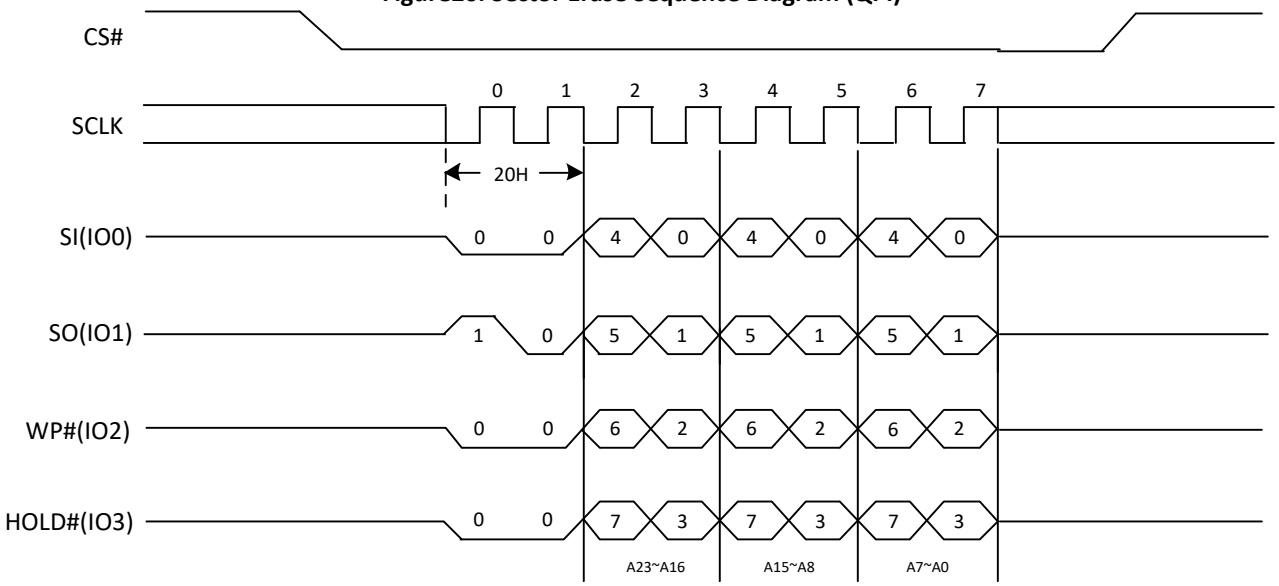


Figure20. Sector Erase Sequence Diagram (QPI)



6.17. 32KB Block Erase (BE) (52H)

The 32KB Block Erase (BE) command is for erasing all the data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit, before sending the 32KB Block Erase command. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI, driving CS# high.. Any address inside the block is a valid address for the 32KB Block Erase (BE) command.

The 32KB Block Erase command sequence: CS# goes low→sending 32KB Block Erase command→3-byte address on SI→CS# goes high. The command sequence is shown in Figure21. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command will not be executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table1.0&1.1) will not be executed.

Note: Power disruption during erase operation will cause incomplete erase, thus it is recommend to perform a re-erase once power resume.

Figure21. 32KB Block Erase Sequence Diagram

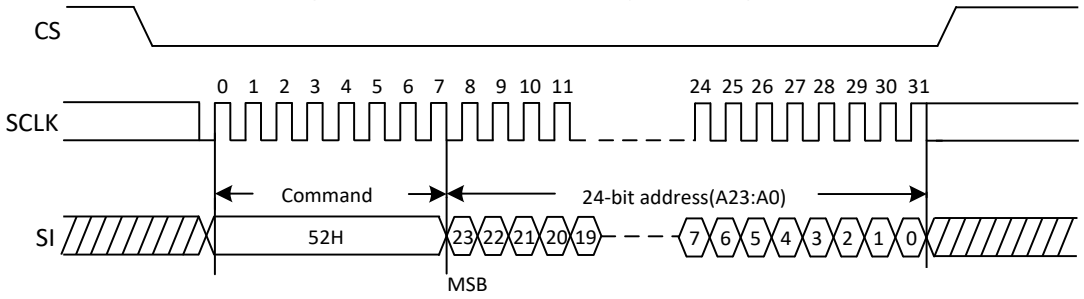
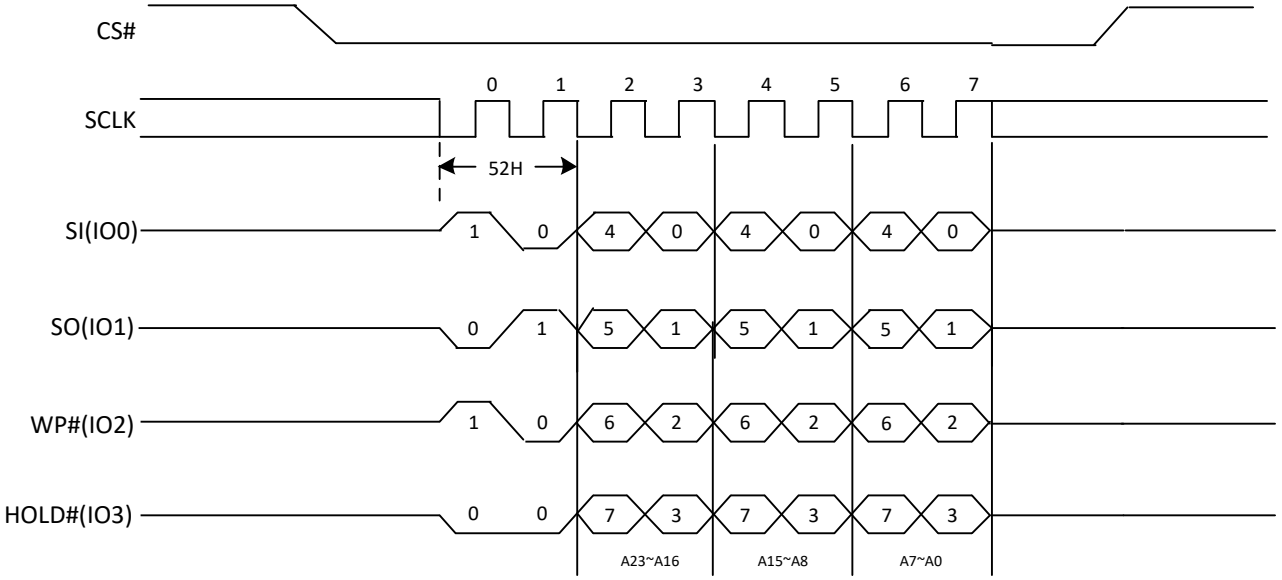


Figure21a. 32KB Block Erase Sequence Diagram (QPI)



6.18. 64KB Block Erase (BE) (D8H)

The 64KB Block Erase (BE) command is for erasing all the data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit, before sending the 64KB Block Erase command. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI, driving CS# high.. Any address inside the block is a valid address for the 64KB Block Erase (BE) command.

The 64KB Block Erase command sequence: CS# goes low→sending 64KB Block Erase command→3-byte address on SI→CS# goes high. The command sequence is shown in Figure22. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command will not be executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table1.0 & 1.1) will not be executed.

Note: Power disruption during erase operation will cause incomplete erase, thus it is recommend to perform a re-erase once power resume.

Figure22. 64KB Block Erase Sequence Diagram

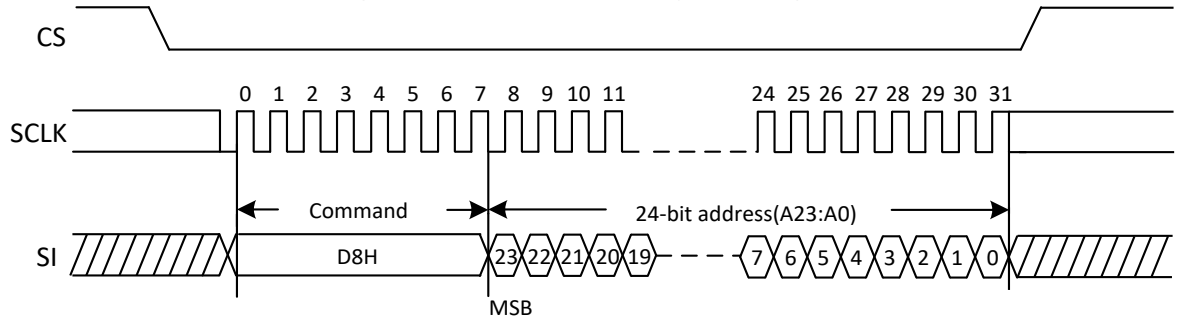
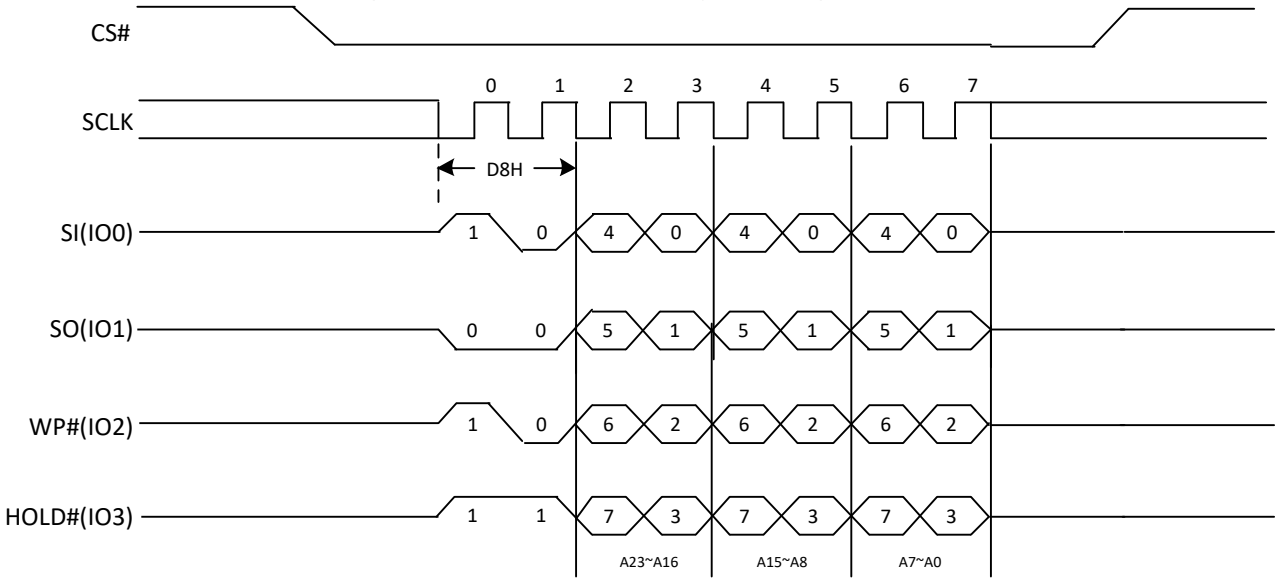


Figure22a. 64KB Block Erase Sequence Diagram (QPI)



6.19. Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is for erasing all the data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit, before sending the Chip Erase command .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI).

The Chip Erase command sequence: CS# goes low→sending Chip Erase command→CS# goes high. The command sequence is shown in Figure23. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Chip Erase command will not be executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed if the Block Protect (BP2, BP1, BP0) bits are 0 and CMP=0 or the Block Protect (BP2, BP1, and BP0)bits are 1 and CMP=1. The Chip Erase (CE) command is ignored if one or more sectors are protected.

Note: Power disruption during erase operation will cause incomplete erase, thus it is recommend to perform a re-erase once power resume.

Figure23. Chip Erase Sequence Diagram

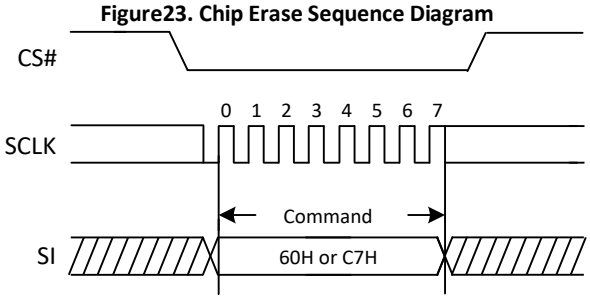
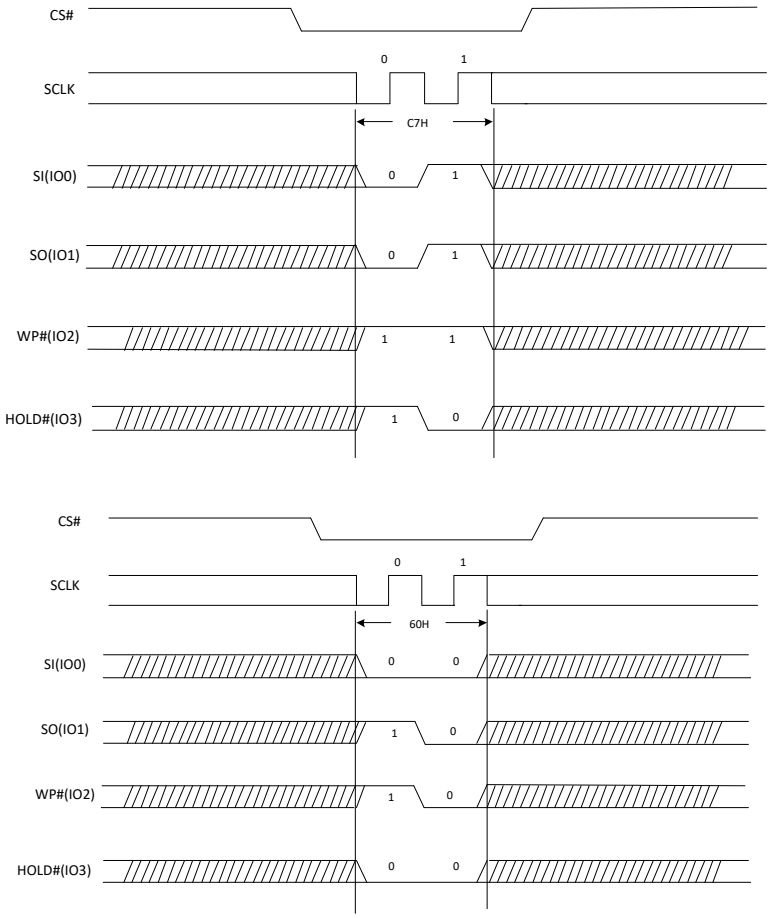


Figure23a. Chip Erase Sequence Diagram (QPI)



6.20. Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest power consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and that puts the flash memory in the Standby Mode (if there is no internal cycle currently in progress). But the Standby Mode is different from the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the flash memory has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command. This command release the flash memory from the Deep Power-Down Mode.

The Deep Power-Down Mode automatically stops at Power-Off, and the flash memory always Power-Up in the Standby Mode. The Deep Power-Down (DP) command is entered by driving CS# low, followed by the command code on SI, driving CS# high.

The Deep Power-Down command sequence: CS# goes low→sending Deep Power-Down command→CS# goes high. The command sequence is shown in Figure24. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command will not be executed. As soon as CS# is driven high, it requires a time duration of tDP before the supply current is reduced to ICC2 and the Deep Power-Down Mode is entered. Any input of Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, will be rejected without having any effects on the cycle that is in progress.

Figure24. Deep Power-Down Sequence Diagram

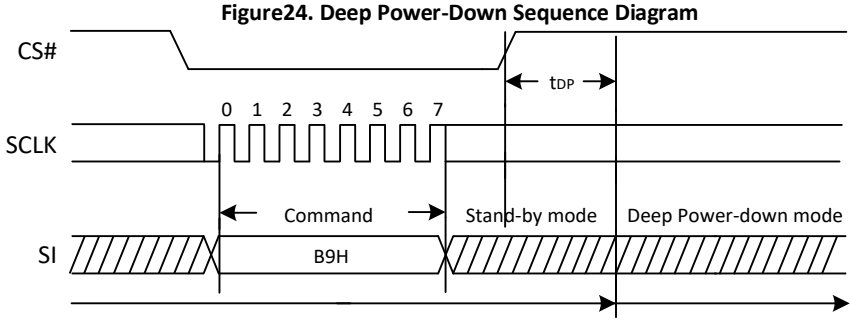
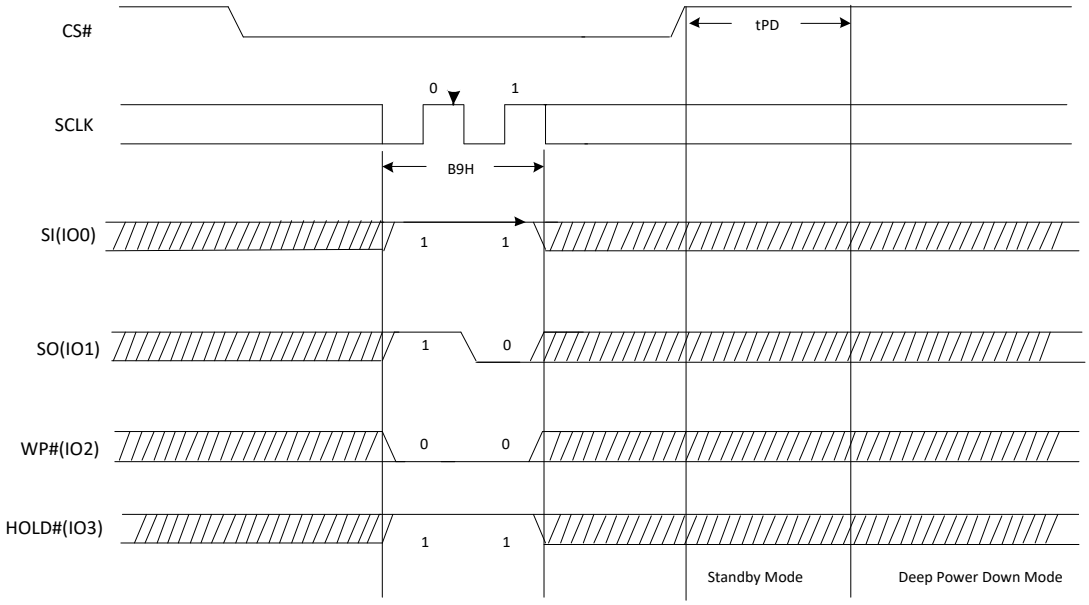


Figure24a. Deep Power-Down Sequence Diagram (QPI)



6.21. Release from Deep Power-Down And Read Device ID (RDI) (ABH)

Release from Power-Down and Read Device ID command is a multi-purpose command. It can be used to release the flash memory from the Power-Down state or obtain the flash memory electronic identification (ID) number.

To release the device from the Deep Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code “ABH” and driving CS# high as shown in Figure25. Release from Deep Power-Down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the tRES1 time duration.

When the command is used only to obtain the Device ID while the flash memory is not in the Deep Power-Down mode. The command is initiated by driving the CS# pin low and shifting the instruction code “ABH” followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure26. The Device ID value for the XT25F128B flash memory is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high. In QPI mode the dummy cycles can be configured by C0H command. When the dummy cycle is configured to 4, addr[0] input must be 0.

When the command is used to release the device from the Deep Power-Down state and obtain the Device ID, the command is the same as previously described, and shown in Figure26 and Figure26a, except that after CS# is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Deep Power-Down and Read Device ID command is issued while an Erasing, Programming or Writing cycle is in process (when WIP equal 1) the command will be ignored and will not have any effects on the current cycle.

Figure25. Release Power-Down Sequence Diagram

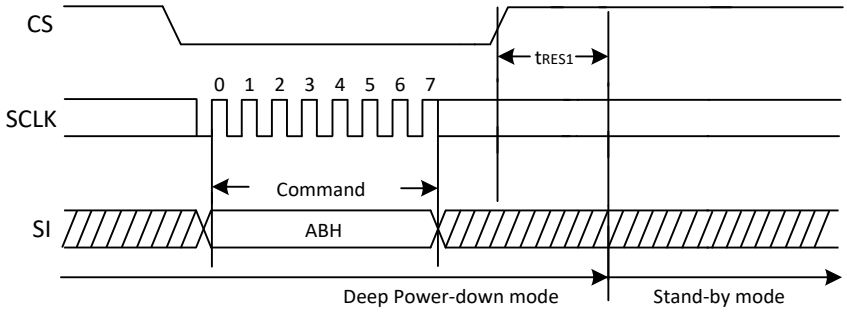


Figure25a. Release Power-Down Sequence Diagram (QPI)

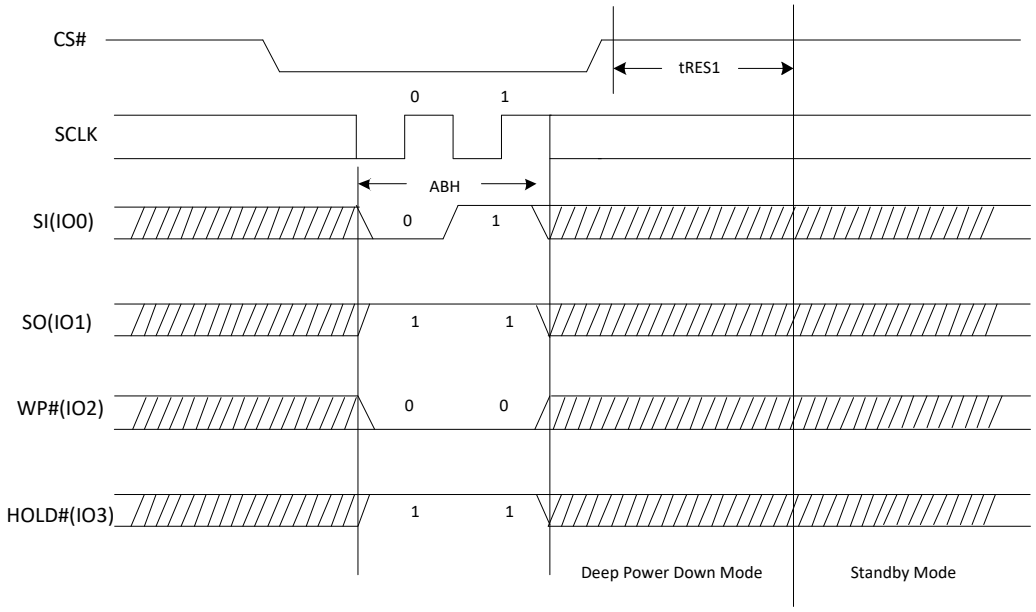


Figure26. Release Power-Down/Read Device ID Sequence Diagram

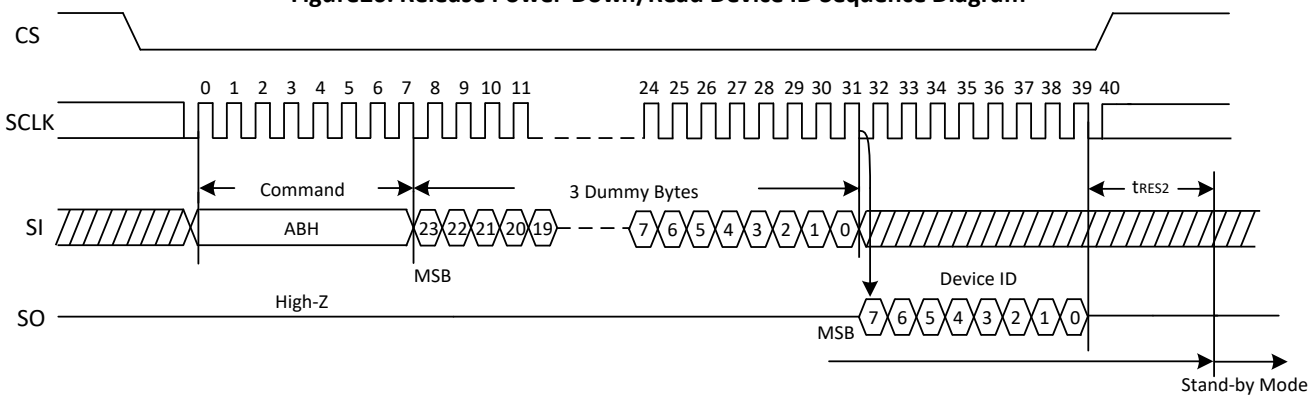
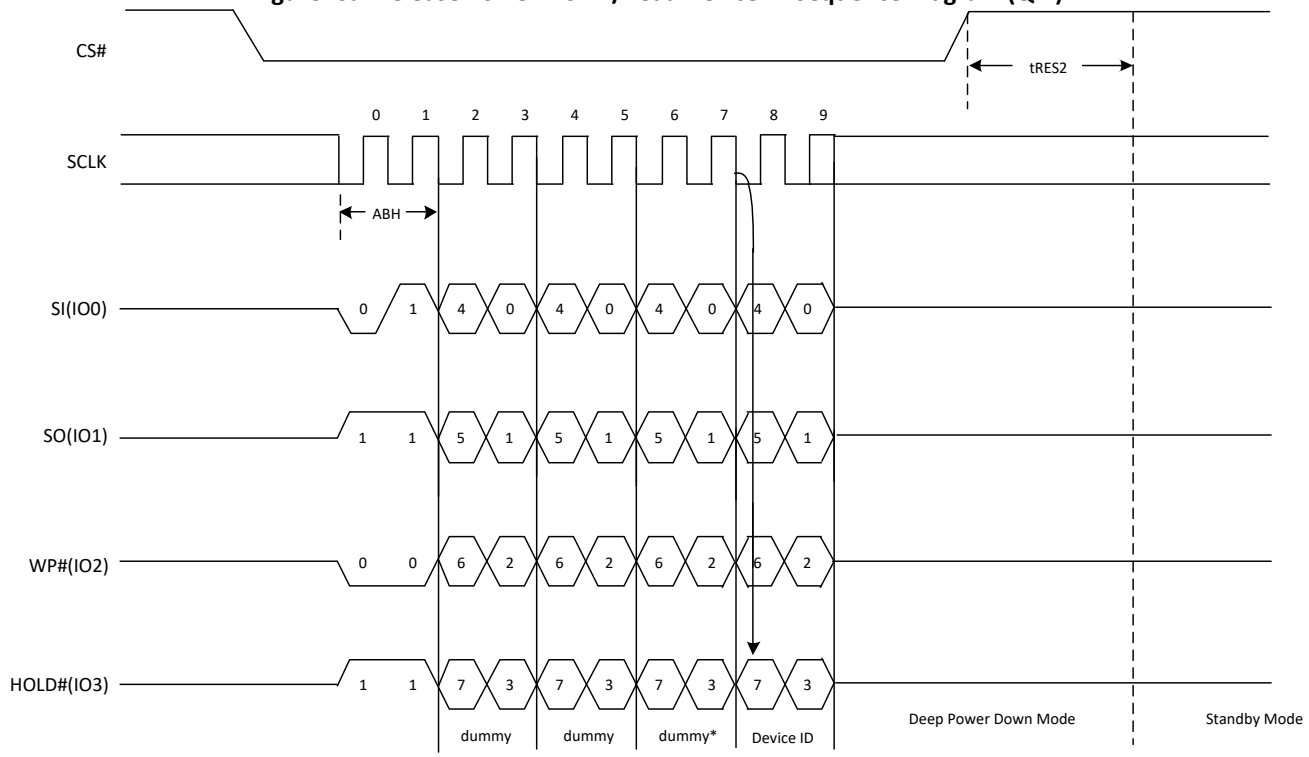


Figure26a. Release Power-Down/Read Device ID Sequence Diagram (QPI)



6.22. Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Deep Power-Down and Read Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code “90H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure27. If the 24-bit address is initially set to 000001H, the Device ID will be read first. In QPI mode the dummy cycles can be configured by C0H command. When the dummy cycle is configured to 4, addr [0] input must be 0.

Figure27. Read Manufacture ID/ Device ID Sequence Diagram

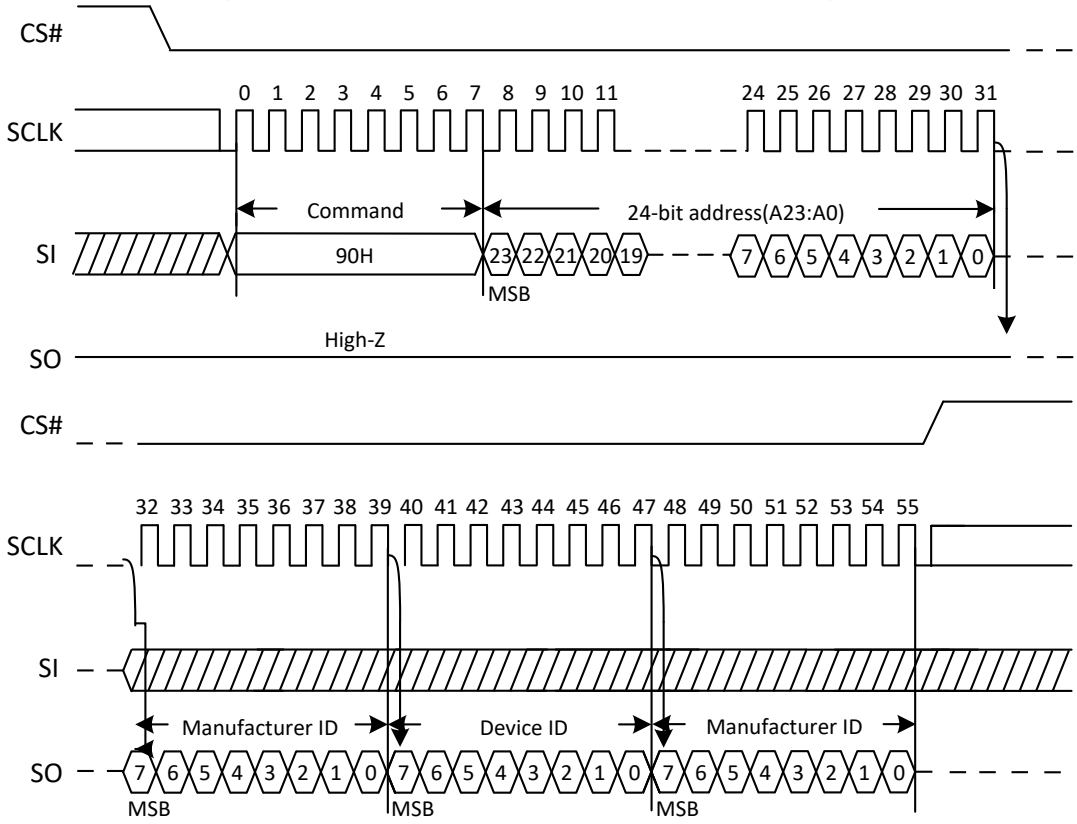
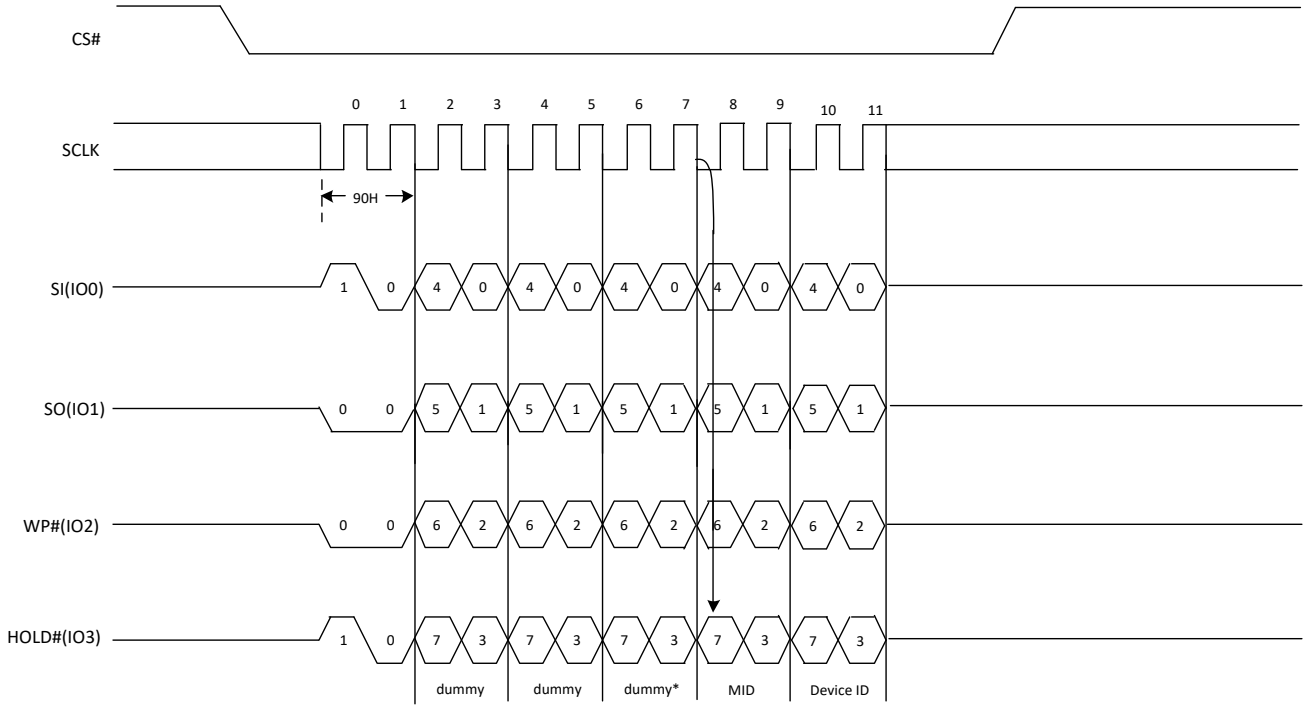


Figure27a. Read Manufacture ID/ Device ID Sequence Diagram (QPI)

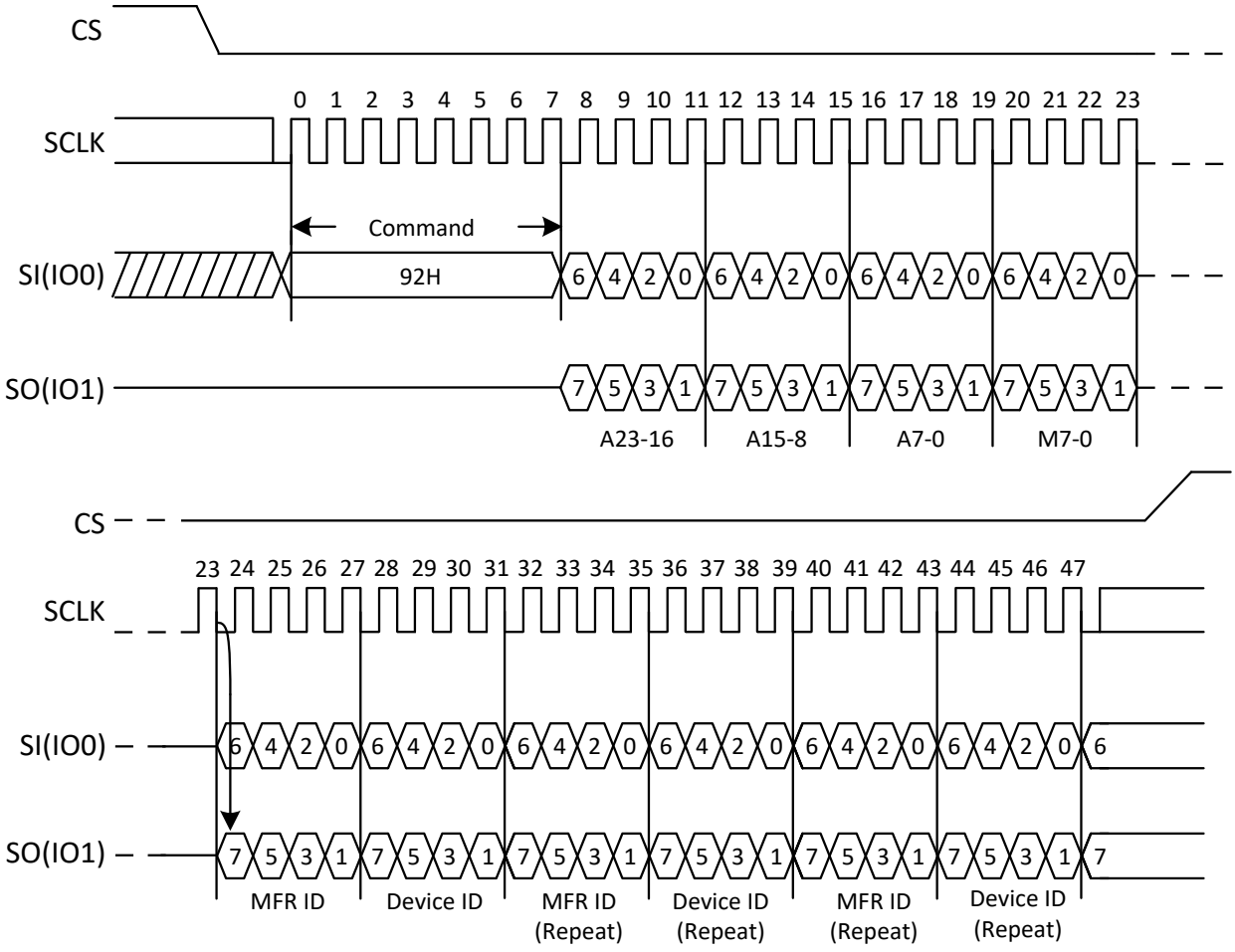


6.23. Read Manufacture ID/ Device ID Dual I/O (92H)

The Read Manufacturer/Device ID Dual I/O command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by dual I/O.

The command is initiated by driving the CS# pin low and shifting the command code “92H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure28. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure28. Read Manufacture ID/ Device ID Dual I/O Sequence Diagram

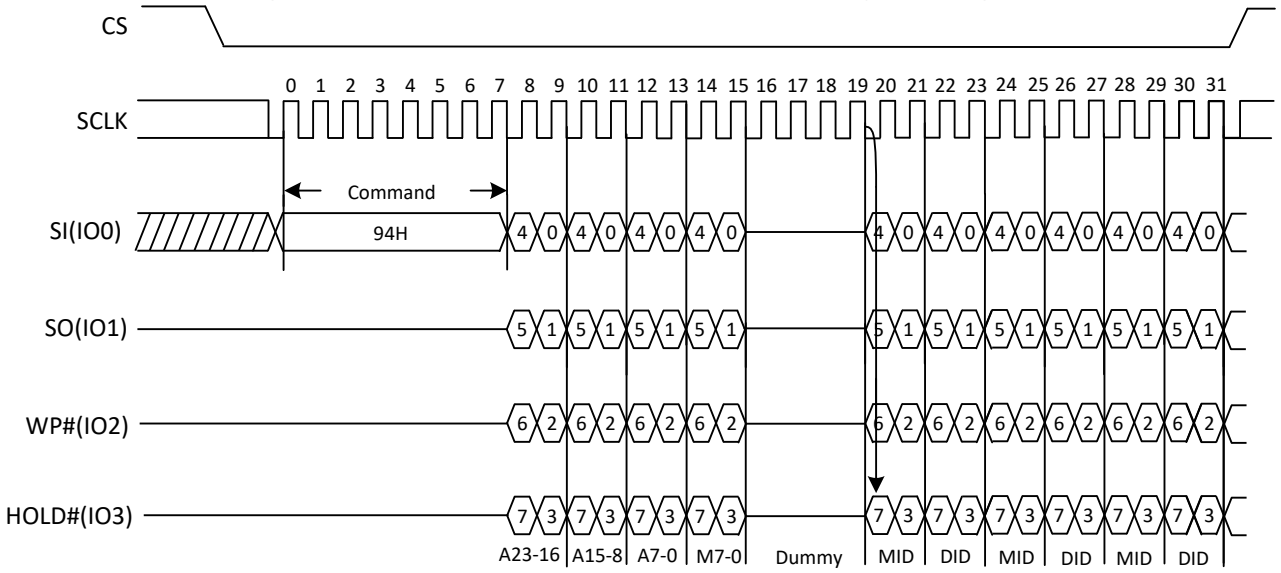


6.24. Read Manufacture ID/ Device ID Quad I/O (94H)

The Read Manufacturer/Device ID Quad I/O command is an alternative to the Release from Deep Power Down and Read Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O.

The command is initiated by driving the CS# pin low and shifting the command code "94H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 29. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure29. Read Manufacture ID/ Device ID Quad I/O Sequence Diagram

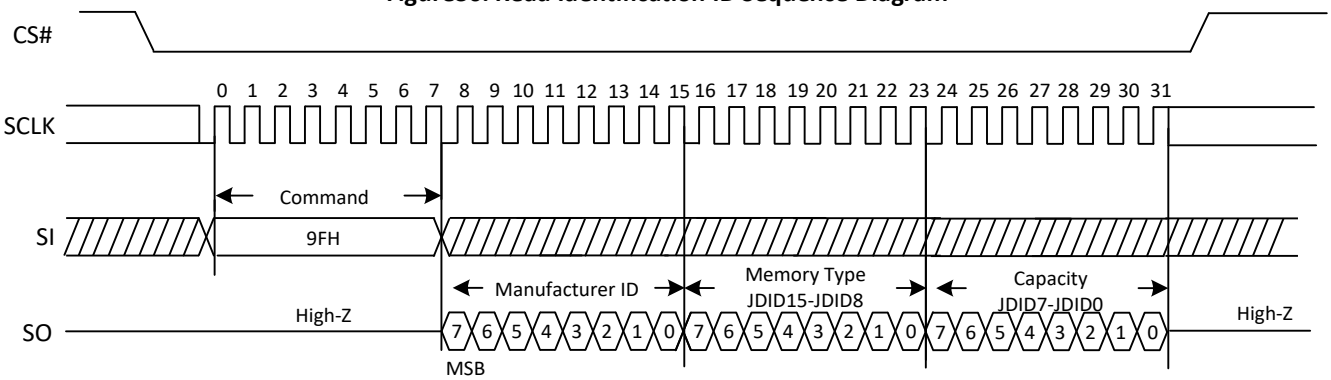


6.25. Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress, will not be decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit manufacture identification and device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in Figure30. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure30. Read Identification ID Sequence Diagram



6.26. Global Block/Sector Lock (7EH) or Unlock (98H)

All Block/Sector Lock bits can be set to 1 by the Global Block/Sector Lock command, or can set to 0 by the Global Block/Sector Unlock command.

The Global Block/Sector Lock command (7EH) sequence: CS# goes low –> SI: Sending Global Block/Sector Lock command –> CS# goes high. The command sequence is shown in Figure 31.

The Global Block/Sector Unlock command (98H) sequence: CS# goes low –> SI: Sending Global Block/Sector Unlock command –> CS# goes high. The command sequence is shown in Figure 32.

Figure 31. The Global Block/Sector Lock Sequence Diagram

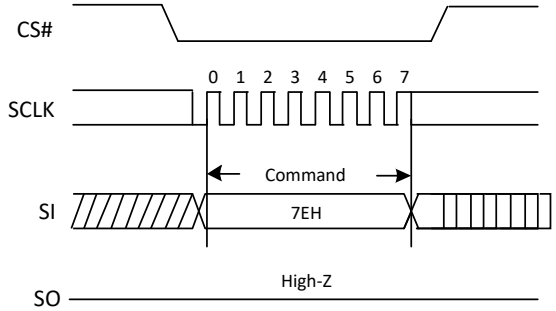


Figure31a. The Global Block/Sector Lock Sequence Diagram (QPI)

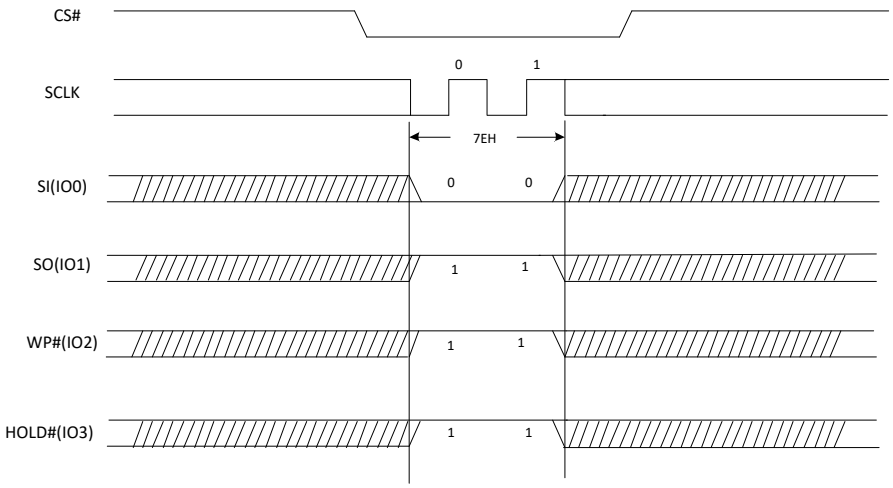


Figure 32. The Global Block/Sector Unlock Sequence Diagram

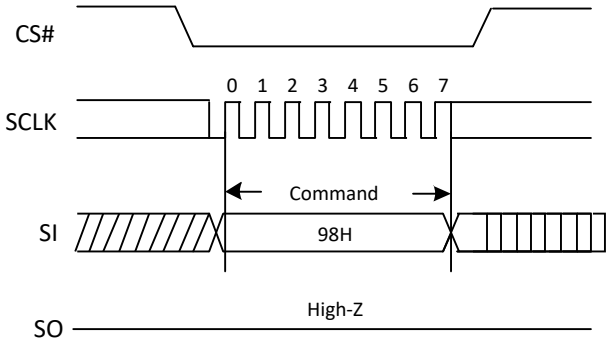
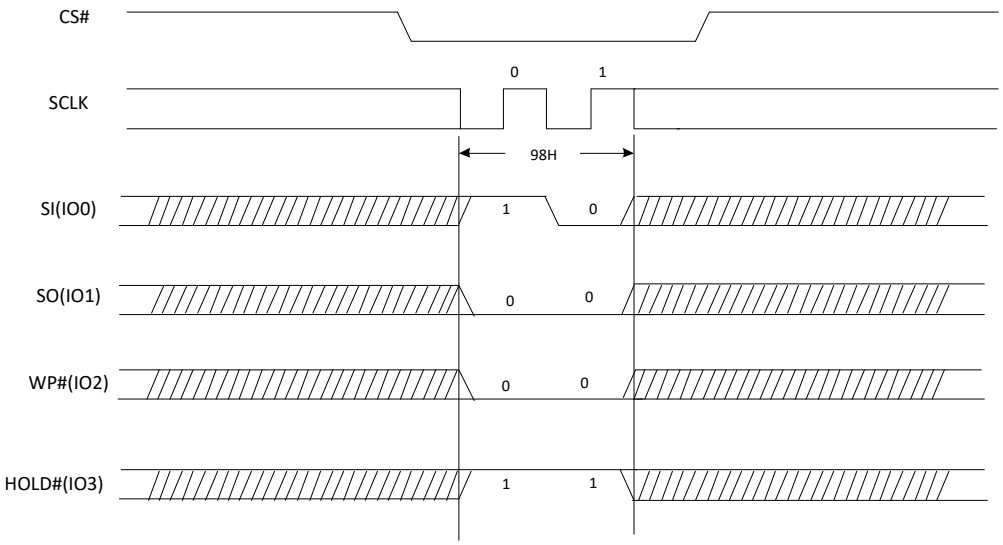


Figure 32a. The Global Block/Sector Unlock Sequence Diagram (QPI)



6.27. Individual Block/Sector Lock (36H)/Unlock (39H)/Read (3DH)

The individual block/sector lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register-3 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, BP (4:0) bits in the Status Register. The Individual Block/Sector Lock bits are volatile bits. The default values after device power up or after a Reset are 1, so the entire memory array is being protected.

The individual Block/Sector Lock command (36H) sequence: CS# goes low –> SI: Sending individual Block/Sector Lock command –> SI: Sending 24bits individual Block/Sector Lock Address –> CS# goes high. The command sequence is shown in Figure 33.

The individual Block/Sector Unlock command (39H) sequence: CS# goes low –> SI: Sending individual Block/Sector Unlock command –> SI: Sending 24bits individual Block/Sector Lock Address –> CS# goes high. The command sequence is shown in Figure 33a.

The Read individual Block/Sector lock command (3DH) sequence: CS# goes low –> SI: Sending Read individual Block/Sector Lock command –> SI: Sending 24bits individual Block/Sector Lock Address –> SO: The Block/Sector Lock Bit will out –> CS# goes high. If the least significant bit(LSB) is1, the corresponding block/sector is locked, if the LSB is 0, the corresponding block/sector is unlocked, Erase/Program operation can be performed. The command sequence is shown in Figure 33c.

Figure33. Individual Block/Sector Lock command Sequence Diagram

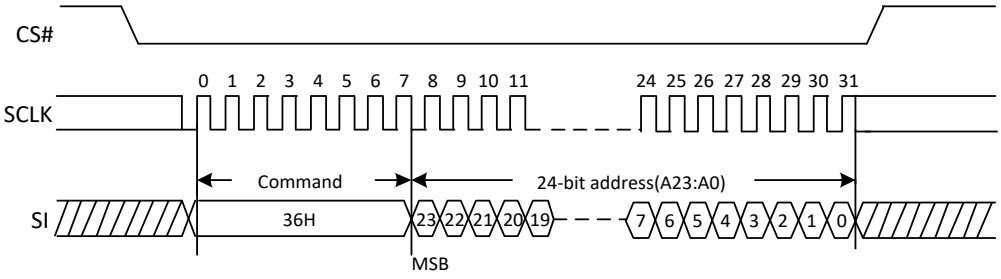


Figure33a. Individual Block/Sector Lock command Sequence Diagram (QPI)

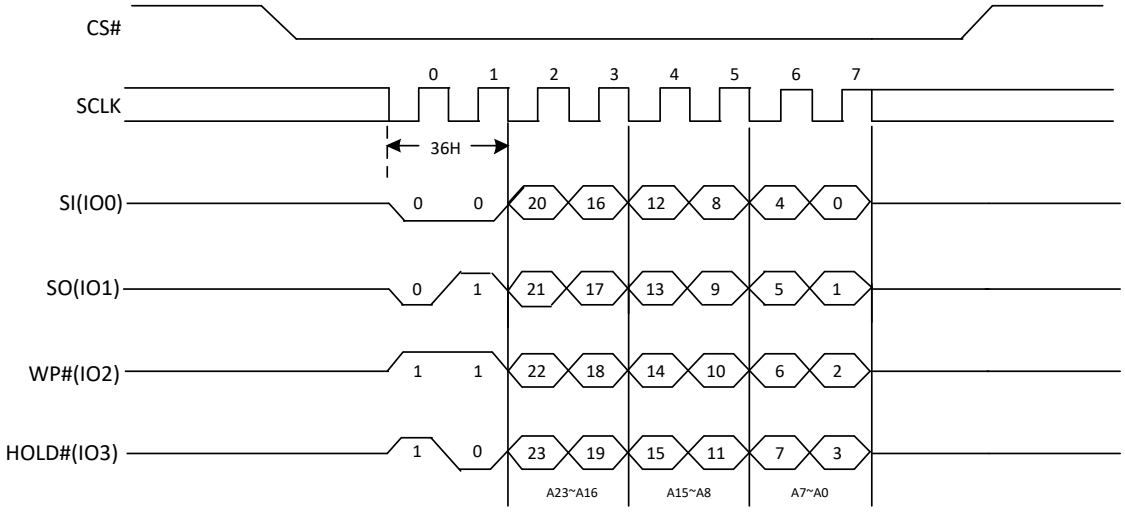


Figure33b. Individual Block/Sector Unlock command Sequence Diagram

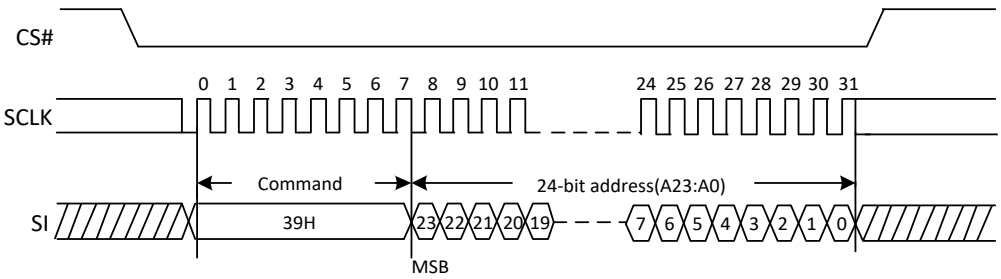


Figure 33c. Individual Block/Sector Unlock command Sequence Diagram (QPI)

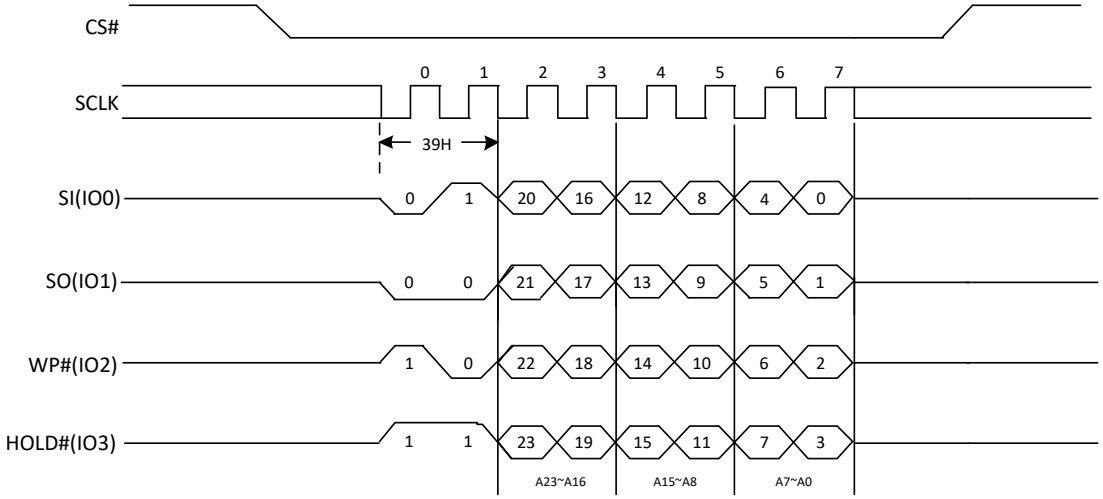


Figure 33d. Read Individual Block/Sector lock command Sequence Diagram

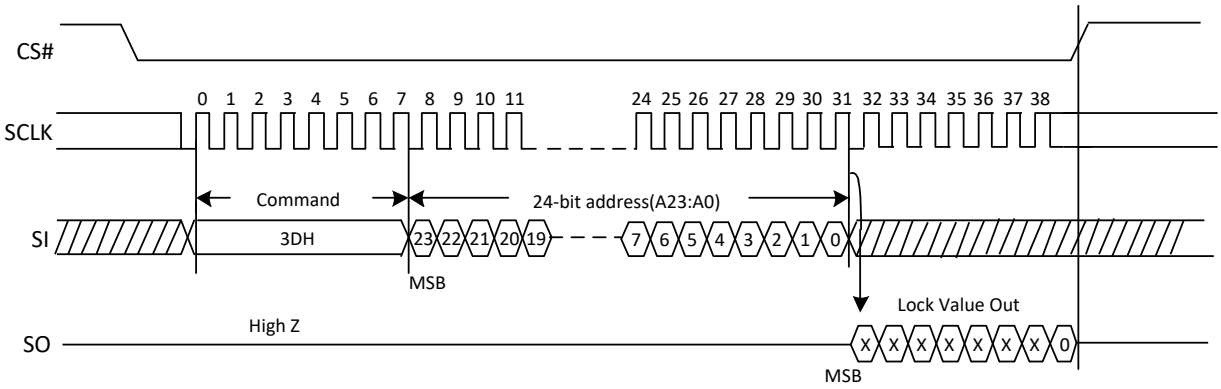
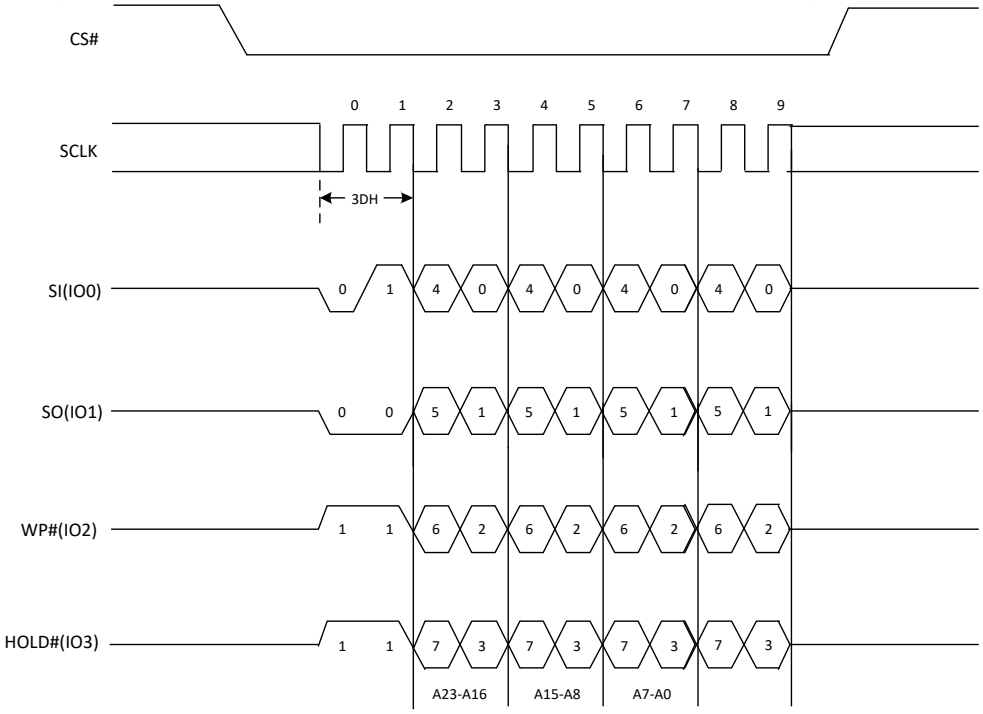


Figure 33e. Read Individual Block/Sector lock command Sequence Diagram (QPI)



6.28. Erase Security Registers (44H)

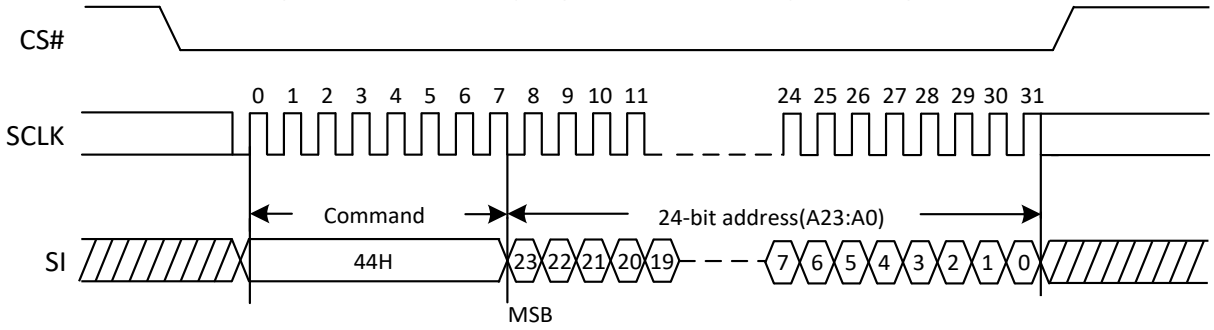
The XT25F128B flash memory provides four 256-byte Security Registers which can be erased all at once but can be programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low→sending Erase Security Registers command→CS# goes high. The command sequence is shown in Figure34. CS# must be driven high after the last address bit has been latched in, otherwise the Erase Security Registers command will not be executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB1, LB0) in the Status Register can be used as OTP to protect the security registers. Any of the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Address	A23-A16	A15-A10	A9-A0
Security Registers	00000000	000000	Don't Care

Figure34. Erase Security Registers command Sequence Diagram



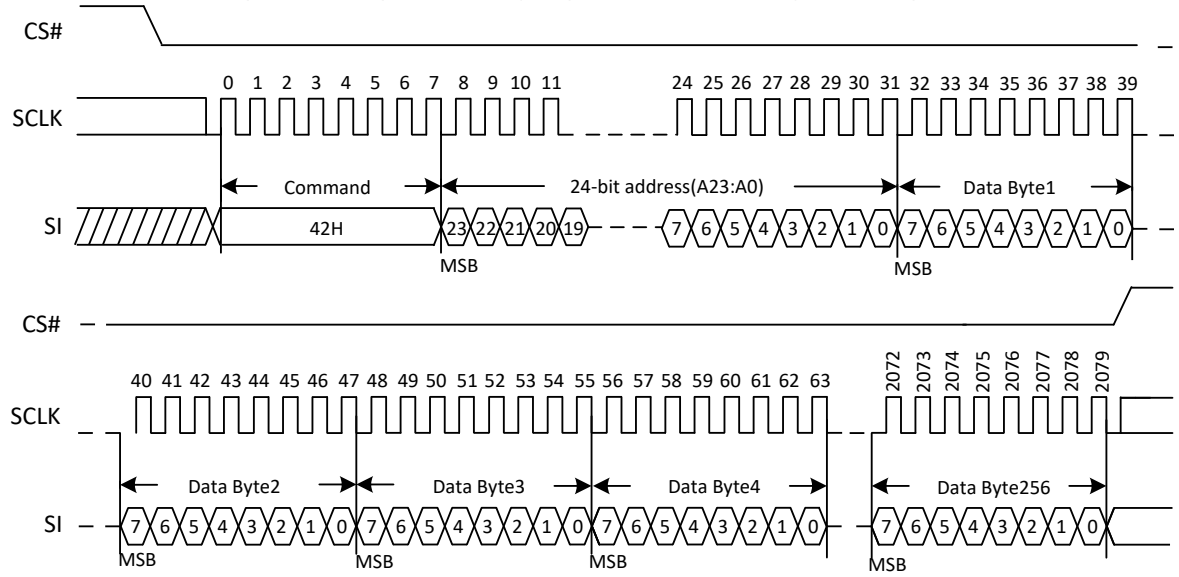
6.29. Program Security Registers (42H)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 256 byte of Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit 0 (LB0) is set to 1, the Security Registers 1 will be permanently locked. Program Security Registers 1command will be ignored.If the Security Registers Lock Bit 1 (LB1) is set to 1, the Security Registers 2 will be permanently locked. Program Security Registers 2command will be ignored.

Address	A23-A16	A15-A8	A7-A0
Security Registers 0	00H	00H	Byte Address
Security Registers 1	00H	01H	Byte Address
Security Registers 2	00H	02H	Byte Address
Security Registers 3	00H	03H	Byte Address

Figure 35. Program Security Registers command Sequence Diagram

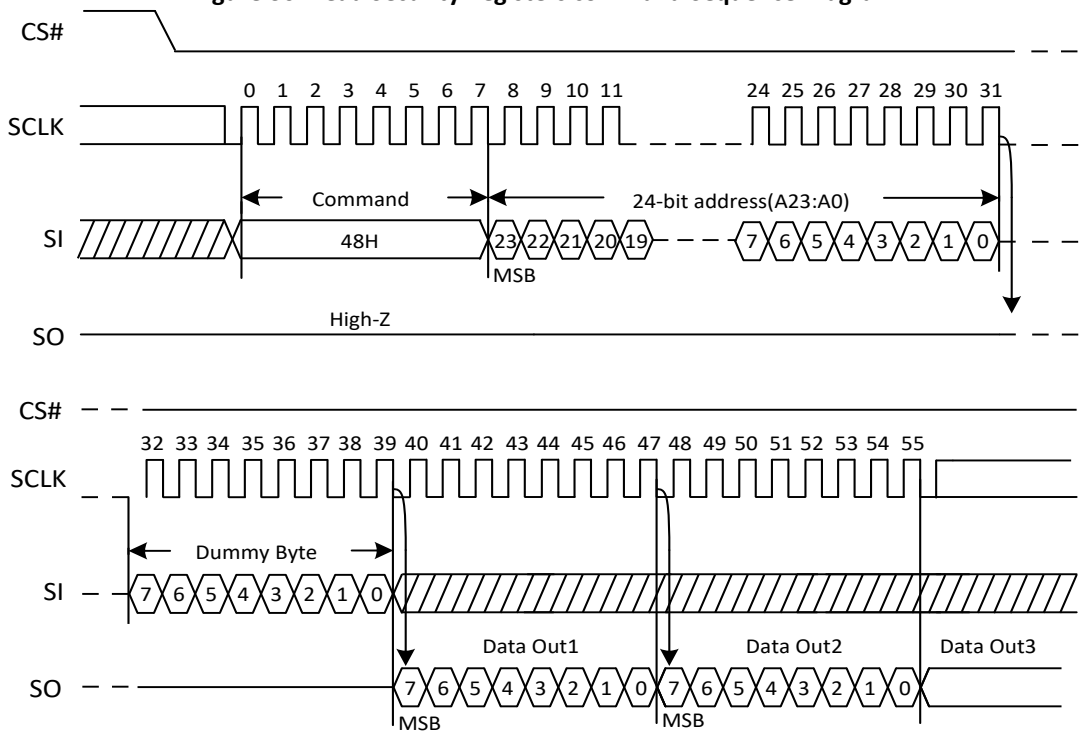


6.30. Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving CS# high.

Address	A23-A16	A15-A10	A9-A0
Security Registers	00000000	000000	Address

Figure 36. Read Security Registers command Sequence Diagram

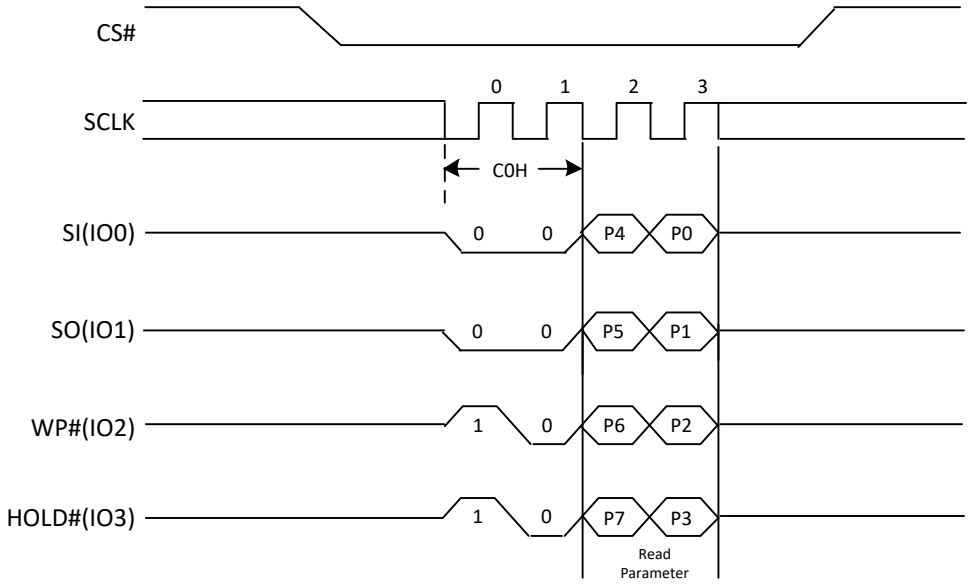


6.31. Set Read Parameters (C0H)

In QPI mode the “Set Read Parameters (C0H)” command can be used to configure the number of dummy clocks for “Fast Read (0BH)”, “Quad I/O Fast Read (EBH)” and “Burst Read with Wrap (0CH)” command, and to configure the number of bytes of “Wrap Length” for the “Burst Read with Wrap (0CH)” command. The “Wrap Length” is set by W5-6 bit in the “Set Burst with Wrap (77H)” command. This setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

P5-P4	Dummy Clocks	Maximum Read Freq.	P1-P0	Wrap Length
0 0	4	48MHz	0 0	8-byte
0 1	4	48MHz	0 1	16-byte
1 0	6	48MHz	1 0	32-byte
1 1	8	48MHz	1 1	64-byte

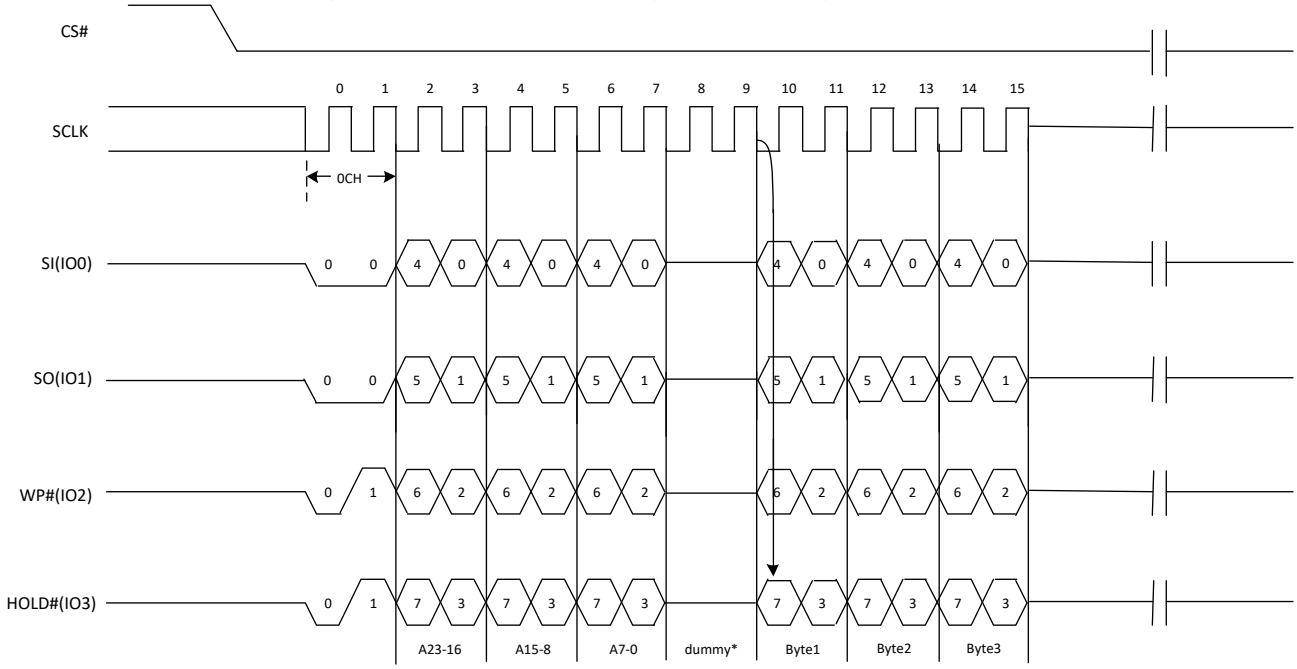
Figure 37. Set Read Parameters command Sequence Diagram



6.32. Burst Read with Wrap (0CH)

The “Burst Read with Wrap (0CH)” command provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. This command is similar to the “Fast Read (0BH)” command in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Around” once the ending boundary is reached. The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0H)” command. When the dummy cycle is configured to 4, addr[0] input must be 0.

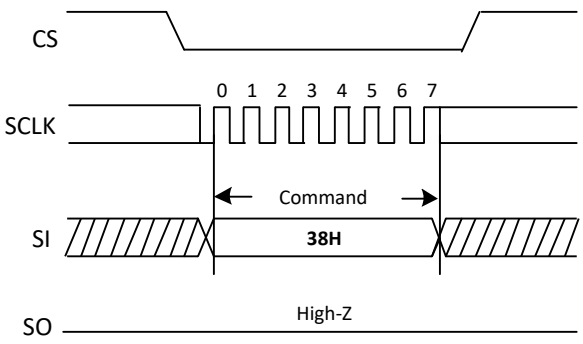
Figure 38. Burst Read with Wrap command Sequence Diagram



6.33. Enable QPI (38H)

The device support both Standard/Dual/Quad SPI and QPI mode. The “Enable QPI (38H)” command can switch the device from SPI mode to QPI mode. See the command Table 2a for all supported QPI commands. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register-1 must be set to 1 first, and “Enable QPI (38H)” command must be issued. If the QE bit is 0, the “Enable QPI (38H)” command will be ignored and the device will remain in SPI mode. When the device is switched from SPI mode to QPI mode, the existing Write Enable Latch and the Wrap Length setting will remain unchanged.

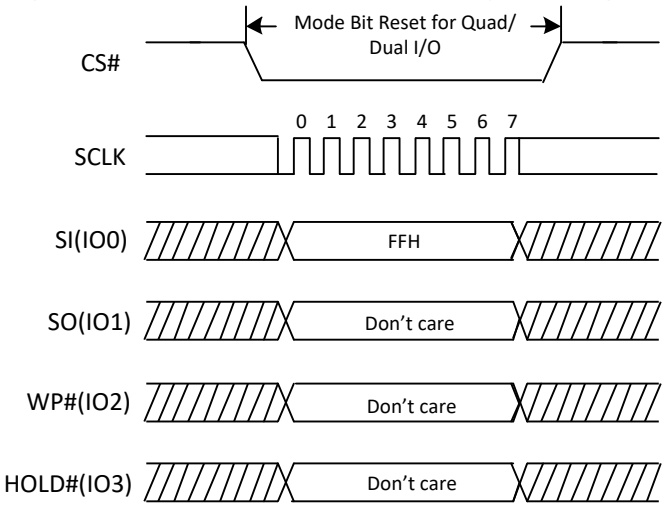
Figure 39. Enable QPI mode command Sequence Diagram



6.34. Continuous Read Mode Reset (CRMR) (FFH)/ Disable QPI (FFH)

In the Dual/Quad I/O Fast Read operations, “Continuous Read Mode” bits (M7-0) are implemented to further reduce command overhead. By setting the (M7-0) to AXH, the next Dual/Quad I/O Fast Read operations do not require the BBH/EBH/E7H command code. Because the XT25F128B flash memory has no hardware reset pin, so if Continuous Read Mode bits are set to “AXH”, the XT25F128B flash memory will not recognize any standard SPI commands. So Continuous Read Mode Reset command will release from the Continuous Read Mode and allow standard SPI command to be recognized. The command sequence is show in Figure 40.

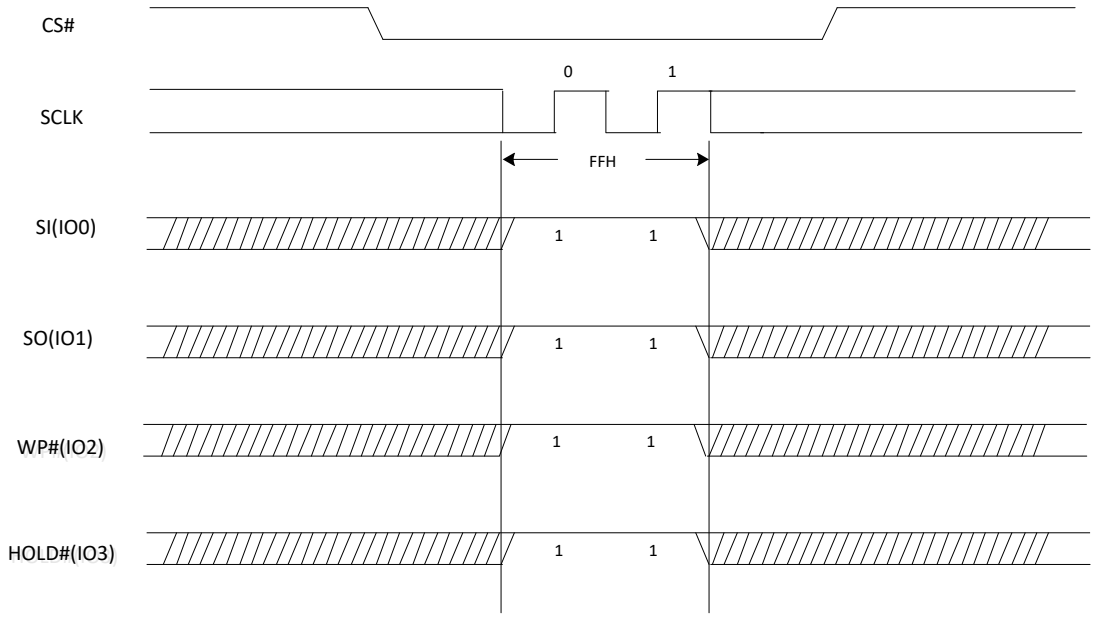
Figure40. Continuous Read Mode Reset Sequence Diagram



Disable QPI (FFH)

To exit the QPI mode and return to Standard/Dual/Quad SPI mode, the “Disable QPI (FFH)” command must be issued. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch and the Wrap Length setting will remain unchanged. When the device is in QPI Continuous Read Mode, the first FFH command will exit continuous read mode and the second FFH command will exit QPI mode.

Figure 40a. Disable QPI mode command Sequence Diagram



6.35. Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Read Parameter setting (P7-P0)and Wrap Bit Setting (W6-W4).

The “Reset (99H)” command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tRST_R to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit in Status Register before issuing the Reset command sequence.

Figure41a. Enable Reset and Reset command Sequence Diagram

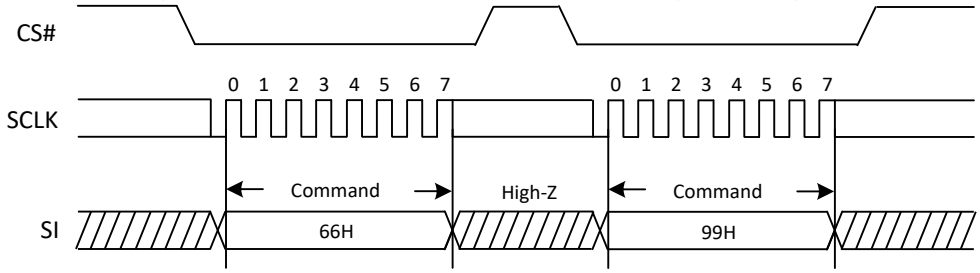
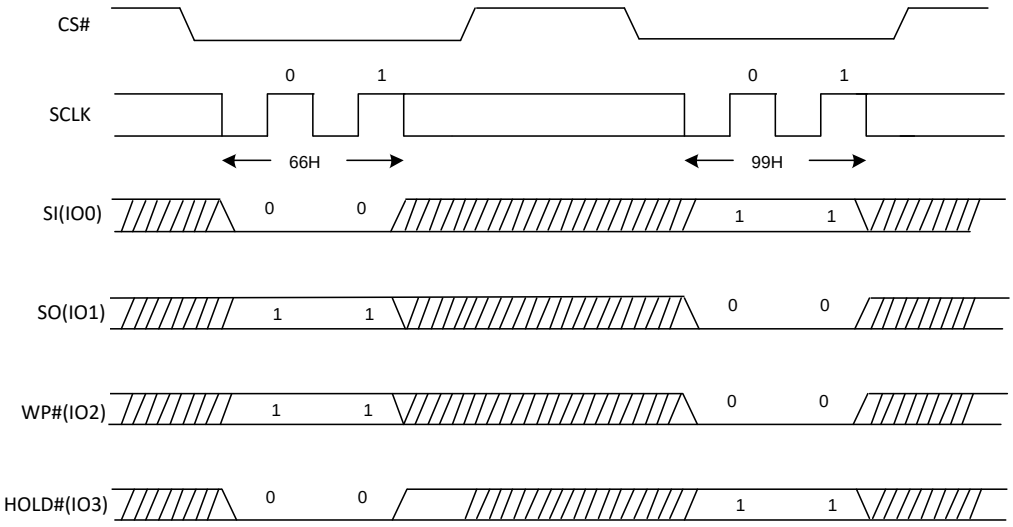


Figure41b. Enable Reset and Reset command Sequence Diagram (QPI)



6.36. Read Serial Flash Discoverable Parameter (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

Figure42a. Read Serial Flash Discoverable Parameter command Sequence Diagram

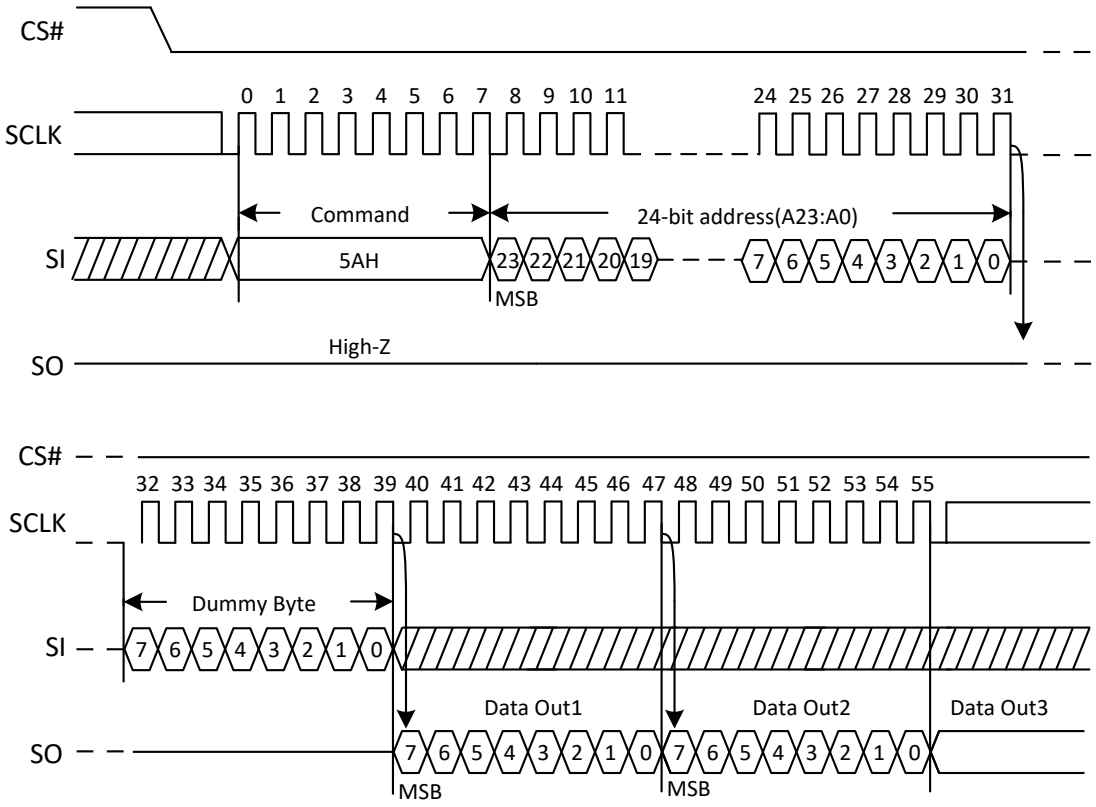
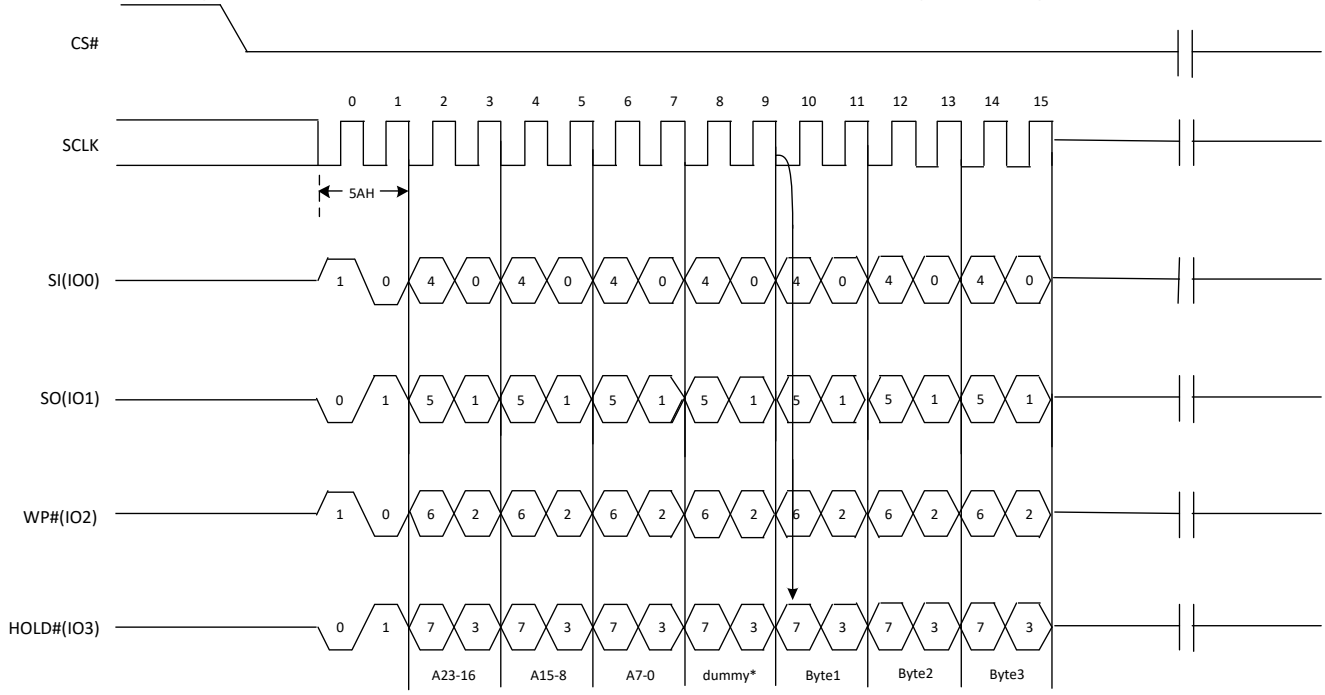


Figure42b. Read Serial Flash Discoverable Parameter command Sequence Diagram (QPI)



6.37. Read Unique ID (5AH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each XT25F128B device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → sending Read Unique ID command →00H →00H →94H → Dummy byte →128bit Unique ID Out → CS# goes high.

The command sequence is show below.

Figure 43 Read Unique ID (RUID) Sequence (Command 5AH)

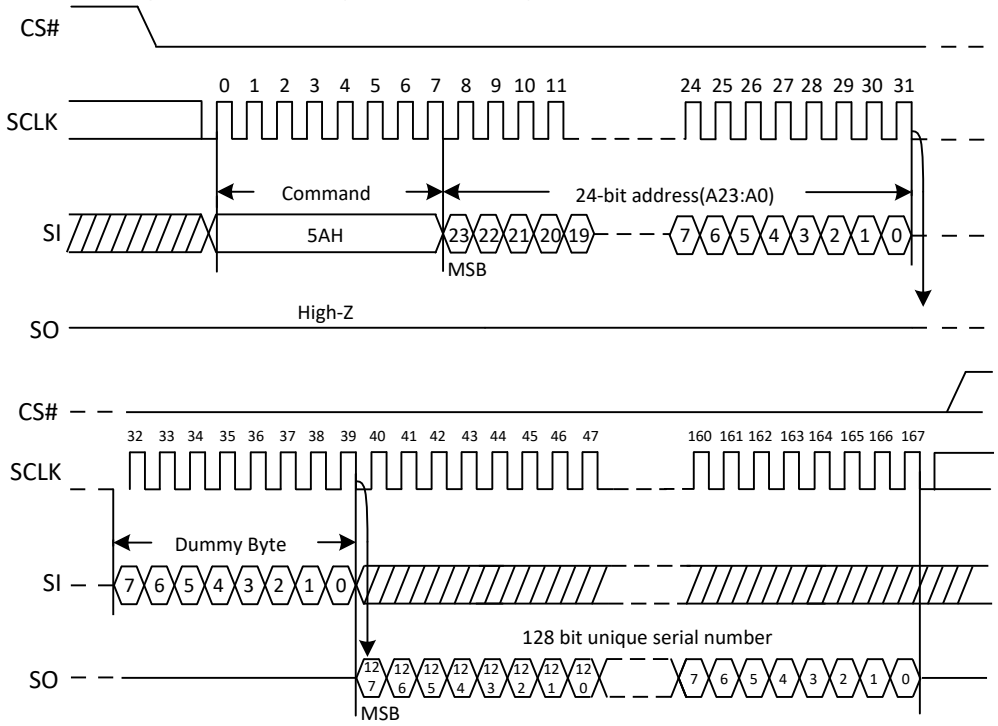


Figure 43b. Read Unique ID (RUID) Sequence (QPI)

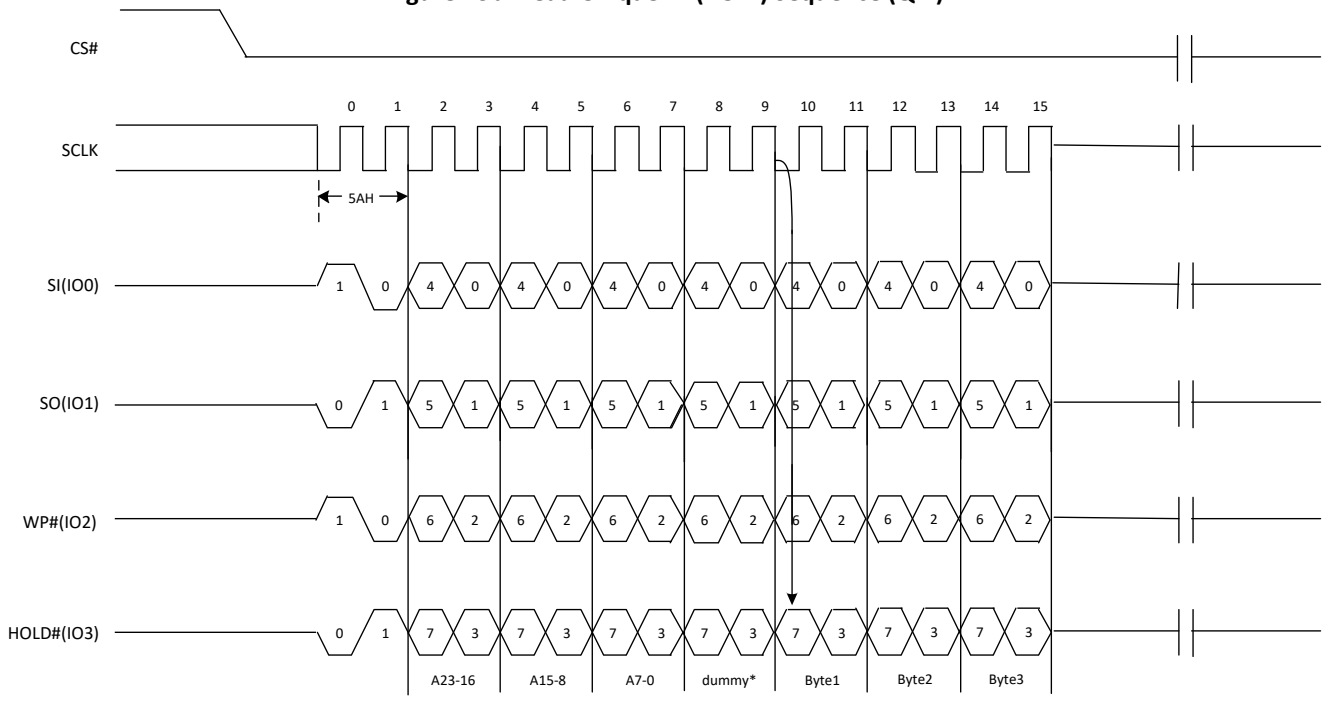


Table3. Signature and Parameter Identification Data Values

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
SFDP Signature	Fixed:50444653H	00H	07:00	53H	53H
		01H	15:08	46H	46H
		02H	23:16	44H	44H
		03H	31:24	50H	50H
SFDP Minor Revision Number	Start from 00H	04H	07:00	00H	00H
SFDP Major Revision Number	Start from 01H	05H	15:08	01H	01H
Number of Parameters Headers	Start from 00H	06H	23:16	01H	01H
Unused	Contains 0xFFH and can never be changed	07H	31:24	FFH	FFH
ID number (JEDEC)	00H: It indicates a JEDEC specified header	08H	07:00	00H	00H
Parameter Table Minor Revision Number	Start from 0x00H	09H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	0AH	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0BH	31:24	09H	09H
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0CH	07:00	30H	30H
		0DH	15:08	00H	00H
		0EH	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	0FH	31:24	FFH	FFH
ID Number(XTX Manufacturer ID)	It is indicates XTX manufacturer ID	10H	07:00	0BH	0BH
Parameter Table Minor Revision Number	Start from 0x00H	11H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	12H	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Param-eter table	13H	31:24	03H	03H
Parameter Table Pointer (PTP)	First address of XT-series Flash Parameter table	14H	07:00	60H	60H
		15H	15:08	00H	00H
		16H	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	17H	31:24	FFH	FFH

Table4. Parameter Table (0): JEDEC Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Block/Sector Erase Size	00: Reserved; 01: 4KB erase; 10: Reserved; 11: not support 4KB erase	30H	01:00	01b	E5H
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Requested for Writing to Volatile Status Registers	0: Nonvolatile status bit 1: Volatile status bit (BP status register bit)		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: Use 50H Opcode, 1: Use 06H Opcode, Note:If target flash status register is Nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31H	15:08	20H	20H
(1-1-2) Fast Read	0=Not support, 1=Support	32H	16	1b	F1H
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) clocking	0=Not support, 1=Support		19	0b	
(1-2-2) Fast Read	0=Not support, 1=Support		20	1b	
(1-4-4) Fast Read	0=Not support, 1=Support		21	1b	
(1-1-4) Fast Read	0=Not support, 1=Support		22	1b	
Unused			23	1b	
Unused		33H	31:24	FFH	FFH
Flash Memory Density		37H:34H	31:00	00FFFFFFH	
(1-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	38H	04:00	00100b	44H
(1-4-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		07:05	010b	
(1-4-4) Fast Read Opcode		39H	15:08	EBH	EBH
(1-1-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3AH	20:16	01000b	08H
(1-1-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		23:21	000b	
(1-1-4) Fast Read Opcode		3BH	31:24	6BH	6BH

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
(1-1-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3CH	04:00	01000b	08H
(1-1-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		07:05	000b	
(1-1-2) Fast Read Opcode		3DH	15:08	3BH	3BH
(1-2-2) Fast Read Number of Wait states		3EH	20:16	00010b	42H
(1-2-2) Fast Read Number of Mode Bits			23:21	010b	
(1-2-2) Fast Read Opcode		3FH	31:24	BBH	BBH
(2-2-2) Fast Read	0=not support 1=support	40H	00	0b	EEH
Unused			03:01	111b	
(4-4-4) Fast Read	0=not support 1=support		04	1b	
Unused			07:05	111b	
Unused		43H:41H	31:08	0xFFH	0xFFH
Unused		45H:44H	15:00	0xFFH	0xFFH
(2-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	46H	20:16	00000b	00H
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2-2) Fast Read Opcode		47H	31:24	FFH	FFH
Unused		49H:48H	15:00	0xFFH	0xFFH
(4-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	4AH	20:16	00000b	00H
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(4-4-4) Fast Read Opcode		4BH	31:24	FFH	FFH
Sector Type 1 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	4CH	07:00	0CH	0CH
Sector Type 1 erase Opcode		4DH	15:08	20H	20H
Sector Type 2 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	4EH	23:16	0FH	0FH
Sector Type 2 erase Opcode		4FH	31:24	52H	52H
Sector Type 3 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	50H	07:00	10H	10H
Sector Type 3 erase Opcode		51H	15:08	D8H	D8H
Sector Type 4 Size	Sector/block size=2^N bytes 0x00b: this sector type don't exist	52H	23:16	00H	00H
Sector Type 4 erase Opcode		53H	31:24	FFH	FFH

Table5. Parameter Table (1): XT-series Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Vcc Supply Maximum Voltage	2000H=2.000V 2700H=2.700V 3600H=3.600V	61H:60H	15:00	3600H	3600H
Vcc Supply Minimum Voltage	1650H=1.650V 2250H=2.250V 2300H=2.300V 2700H=2.700V	63H:62H	31:16	2700H	2700H
HW Reset# pin	0=not support 1=support	65H:64H	00	0b	F99FH
HW Hold# pin	0=not support 1=support		01	1b	
Deep Power Down Mode	0=not support 1=support		02	1b	
SW Reset	0=not support 1=support		03	1b	
SW Reset Opcode	Should be issue Reset Ena-ble(66H) before Reset cmd		11:04	99H	
Program Suspend/Resume	0=not support 1=support		12	0b	
Erase Suspend/Resume	0=not support 1=support		13	0b	
Unused			14	1b	
Wrap-Around Read mode	0=not support 1=support		15	1b	
Wrap-Around Read mode Opcode		66H	23:16	77H	77H
Wrap-Around Read data length	08H:support 8B wrap-around read 16H:8B&16B 32H:8B&16B&32B 64H:8B&16B&32B&64B	67H	31:24	64H	64H
Individual block lock	0=not support 1=support	6BH:68H	00	1b	E8D9H
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	36H	
Individual block lock Volatile protect bit default protect status	0=protect 1=unprotect		10	0b	
Secured OTP	0=not support 1=support		11	1b	
Read Lock	0=not support 1=support		12	0b	
Permanent Lock	0=not support 1=support		13	1b	
Unused			15:14	11b	
Unused			31:16	FFH	FFH

7. ELECTRICAL CHARACTERISTICS

7.1. Power-on Timing

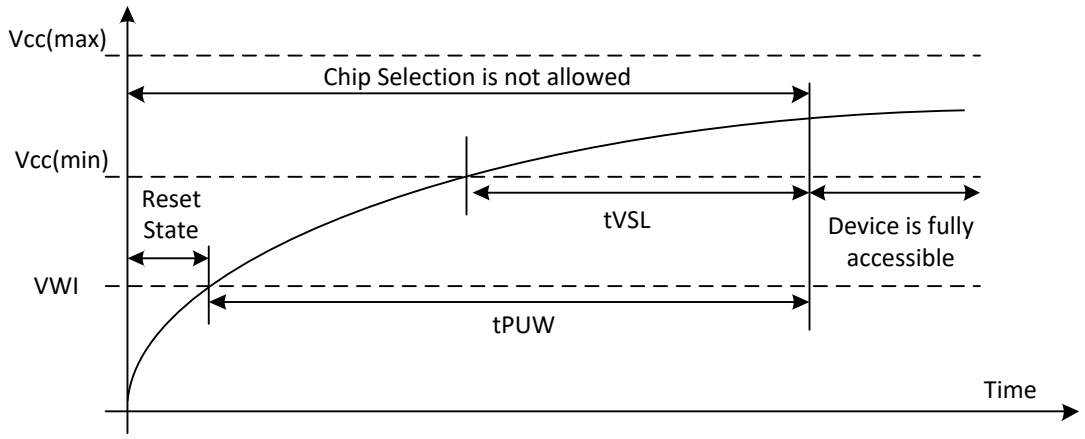


Table3. Power-Up Timing and Write Inhibit Threshold

Note: At power-down, need to ensure VCC drop to 0.5V before the next power-on in order for the device to have a proper power-on reset.

Symbol	Parameter	Min	Max	Unit
t_{VSL}	VCC(min) To CS# Low	10		us
t_{PUW}	Time Delay Before Write Instruction	1	-	ms
V_{WI}	Write Inhibit Voltage	1.5	2.5	V

7.2. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH).The Status Register contains 00H (all Status Register bits are 0).

7.3. Data Retention and Endurance

Parameter	Typical	Unit
Pattern Data Retention Time	20	Years
Erase/Program Endurance	100K	Cycles

7.4. Latch up Characteristics

Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

7.5. Absolute Maximum Ratings

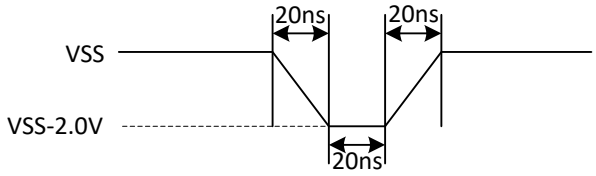
Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-65 to 150	℃
Output Short Circuit Current	200	mA
Applied Input/Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V

7.6. Capacitance Measurement Condition

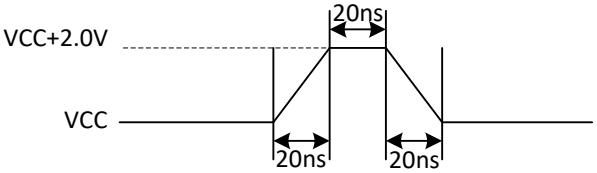
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
CL	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage		0.5VCC		V	

Input Test Waveform and Measurement Level

Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform



7.7. DC Characteristics

(T=-40℃~85℃,VCC=2.70~3.60V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit
I_{LI}	Input Leakage Current				±2	µA
I_{LO}	Output Leakage Current				±2	µA
I_{CC1}	Standby Current	CS#=VCC VIN=VCC or VSS		20	40	µA
I_{CC2}	Deep Power-Down Current	CS#=VCC VIN=VCC or VSS		0.1	4	µA
I_{CC3}	Operating Current(Read)	CLK=0.1VCC/0.9VCC at 108MHz, Q=Open(*1 I/O)		15	20	mA
		CLK=0.1VCC/0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O)		13	18	mA
		CLK=0.1VCC/0.9VCC at 50MHZ,Q=Open(*1 I/O)		7	10	mA
I_{CC4}	Operating Current(PP)	CS#=VCC			30	mA
I_{CC5}	Operating Current(WRSR)	CS#=VCC			30	mA
I_{CC6}	Operating Current(SE)	CS#=VCC			30	mA
I_{CC7}	Operating Current(BE)	CS#=VCC			30	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	IOL=1.6mA			0.4	V
V_{OH}	Output High Voltage	IOH=-100uA	VCC-0.2			V

Note: 1. Typical values given for TA=25°C.
2. Value guaranteed by design and/or characterization, are not 100% tested in production.

7.8. AC Characteristics

(T=-40℃~85℃,VCC=2.70~3.60V， C_L=30pF)

Symbol	Parameter	Min.	Typ	Max.	Unit
f_C	Serial Clock Frequency For:Fast Read (0BH), Dual Output(3BH)			108	MHz
f_{C1}	Serial Clock Frequency For:Dual I/O (BBH), Quad I/O(EBH),Quad Output(6BH)			108	MHz
f_{C2}	Serial Clock Frequency For QPI (0BH, EBH)			72	MHz
f_{R1}	Serial Clock Frequency For: Read (03H)			60	MHz
f_{R2}	Serial Clock Frequency For: Read Identification (9FH)			108	MHz
t_{CLH} (1)	Serial Clock High Time	45% PC			ns
t_{CLL} (1)	Serial Clock Low Time	45% PC			ns
t_{CLCH}	Serial Clock Rise Time(Slew Rate)	0.2			V/ns
t_{CHCL}	Serial Clock Fall Time(Slew Rate)	0.2			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (read/write)	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	1			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{HLCH}	Hold# Low Setup Time(relative to Clock)	5			ns
t_{HHCH}	Hold# High Setup Time(relative to Clock)	5			ns
t_{CHHL}	Hold# High Hold Time(relative to Clock)	5			ns
t_{CHHH}	Hold# Low Hold Time(relative to Clock)	5			ns
t_{CLQV}	Clock Low To Output Valid			6.5	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20			ns
t_{SHWL}	Write Protect Hold Time After CS# High	100			ns
t_{DP}	CS# High To Deep Power-Down Mode			0.1	µs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read			20	µs
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read			20	µs
t_{RST_R}	CS# High To Next Command After Reset (from read)			20	µs
t_{RST_P}	CS# High To Next Command After Reset (from program)			20	µs
t_{RST_E}	CS# High To Next Command After Reset (from erase)			12	ms
t_W	Write Status Register Cycle Time		80	800	ms
t_{PP}	Page Programming Time		0.3	0.75	ms
t_{SE}	Sector Erase Time		80	800	ms
t_{BE}	Block Erase Time(32K Bytes/64K Bytes)		0.15/0.2	1.2/1.6	s
t_{CE}	Chip Erase Time		35	120	s

Note: 1. Clock high or Clock low must be more than or equal to 45%Pc. Pc=1/fC(MAX)

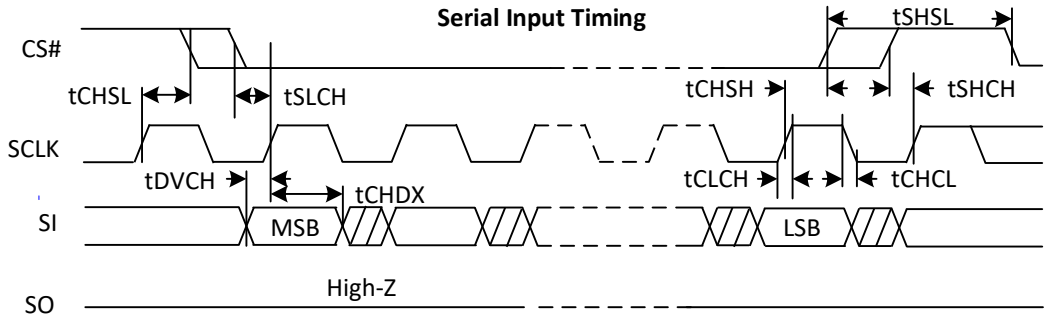
2. Value guaranteed by design and/or characterization, are not 100% tested in production.

3. Maximum Serial Clock Frequencies are measured results picked at the falling edge. For the result picked at the rising edge, please refer to the bellowing diagram.

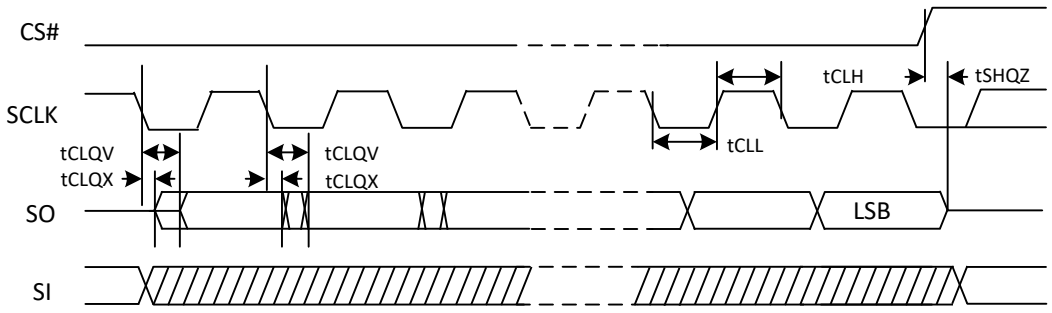
Serial Clock Frequency Result Picked At The Rising Edge

Symbol	Parameter	Min.	Typ	Max.	Unit
f_C	Serial Clock Frequency For:Fast Read (0BH), Dual Output(3BH)			96	MHz
f_{C1}	Serial Clock Frequency For:Dual I/O (BBH), Quad I/O(EBH),Quad Output(6BH)			72	MHz
f_{C2}	Serial Clock Frequency For QPI (0BH, EBH)			60	MHz
f_{R1}	Serial Clock Frequency For: Read (03H)			60	MHz
f_{R2}	Serial Clock Frequency For: Read Identification (9FH)			60	MHz

Serial Input Timing

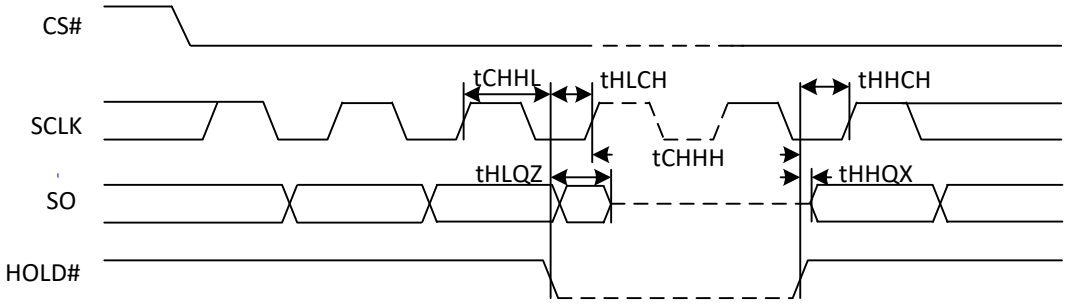


Output Timing



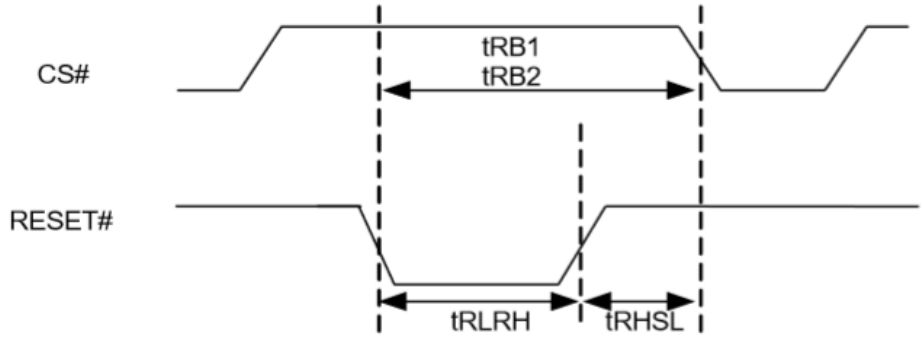
Least significant address bit (LSB) in

Hold Timing



SI do not care during HOLD operation

RESET Timing



Reset Timing

Symbol	Parameter	Setup	Speed	Unit.
tRLRH	Reset pulse width	MIN	1	us
tRHSL	Reset high time before read	MIN	50	ns
tRB1	Reset recovery time (For NOT busy mode)	MAX	5	us
tRB2	Reset recovery time (For busy mode)	MAX	60	us

8. ORDERING INFORMATION

The ordering part number is formed by a valid combination of the following:

XT 25F 128B SS I G U

Company Prefix

XT = XTX

Product Family

25F=2.70~3.60V Serial Flash Memory with 4KB Uniform-Sector

Product Density

128B = 128M bit

Product Package

SS = 8-pin SOP8(208mil)
SF = 16-pin SOP16(300mil)
DH = 8-pin DFN8(4x4x0.85mm)
WO = WSON 6x5
BG = BGA 8x6
WL = WLCSP

Temperature & Moisture Sensitivity Level

I = Industrial Level Temp. (-40℃ to +85℃), MSL3

Green Code

G = Green/Reach Package

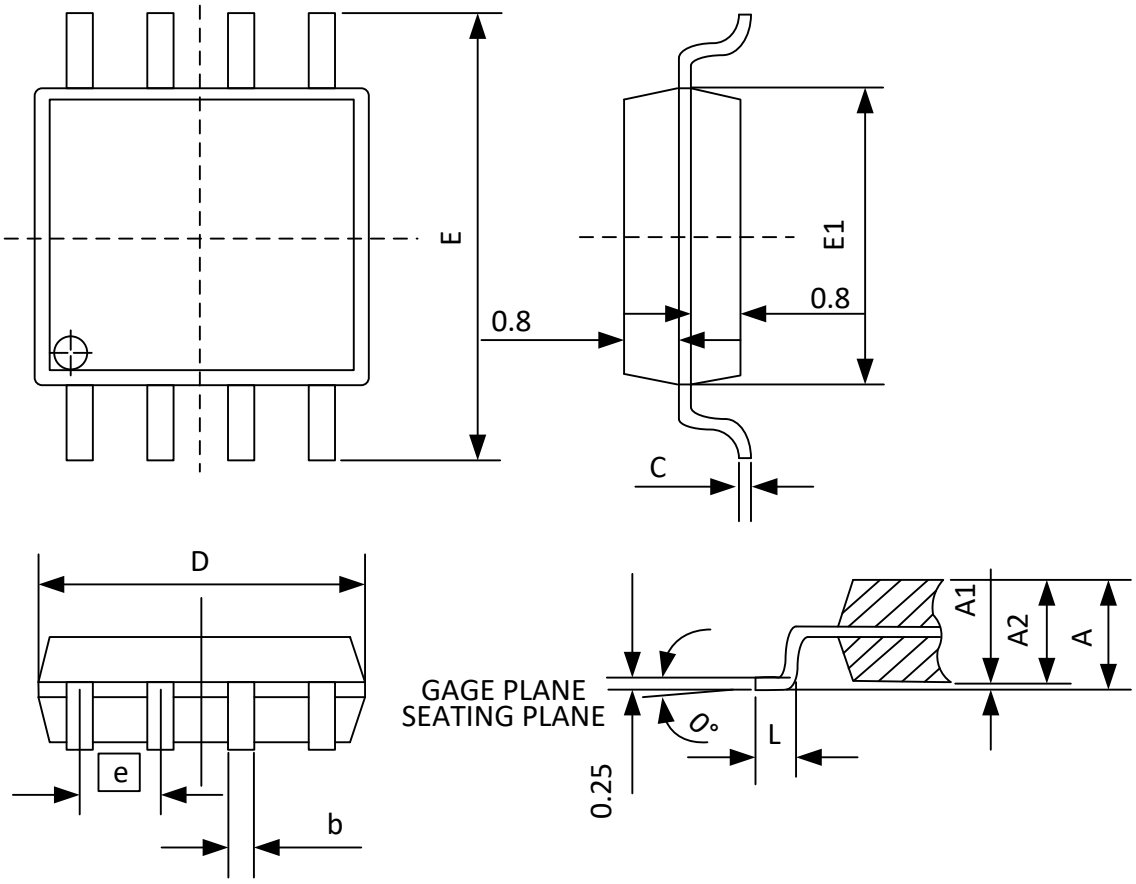
Product Carrier

U = Tube; **T** = Tape & Reel; **A** = Tray

NOTE:
Standard bulk shipment is in Tube. Any alternation of packing method (for Tape, Reel and Tray etc.), please advise in advance.

9. PACKAGE INFORMATION

9.1. Package SOP8 208MIL

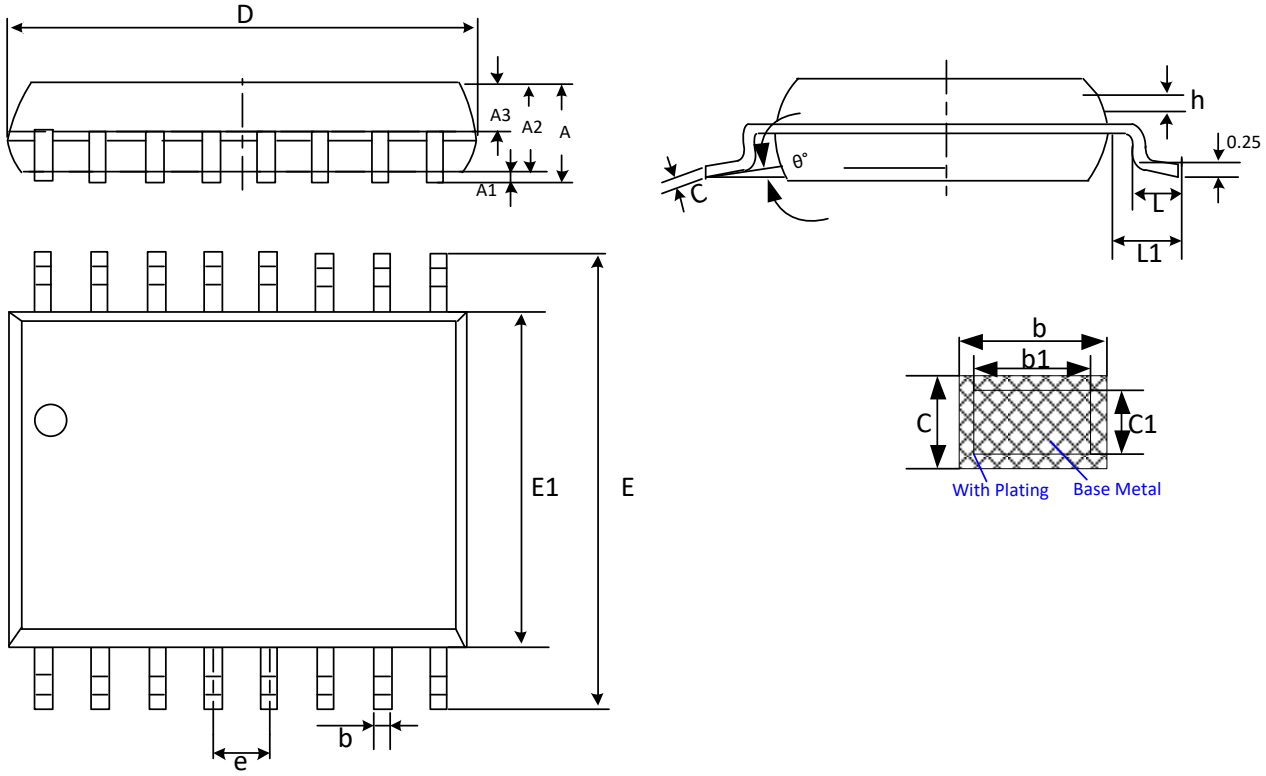


Symbol	Dimensions in Millimeters		
	Min	Norm	Max
A	1.750	1.950	2.160
A1	0.050	0.150	0.250
A2	1.700	1.800	1.910
b	0.350	0.420	0.480
c	0.190	0.20	0.250
D	5.130	5.230	5.330
E	7.700	7.900	8.100
E1	5.180	5.280	5.380
e	1.270 BSC		
L	0.500	0.650	0.800
θ	0°	----	8°

Note:

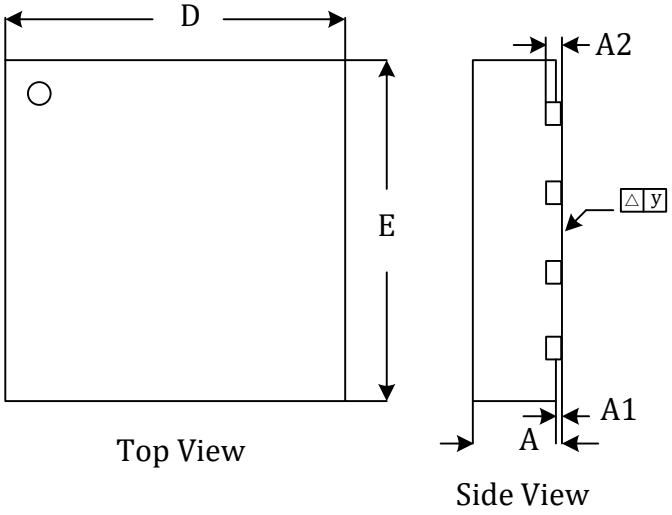
1. JEDEC Outline : N/A
2. Coplanarity: 0.1mm
3. Max allowable mold flash is 0.15mm at the package ends. 0.25mm between leads.

9.2. Package SOP16 300mil



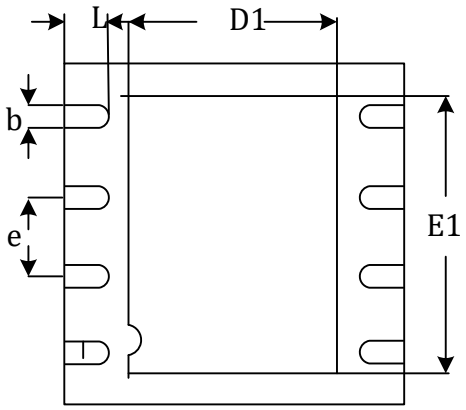
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	—	0.43
b1	0.34	0.37	0.40
C	0.25	—	0.29
C1	0.24	0.25	0.26
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 BSC		
L	0.55	—	0.85
L1	1.40 REF		
θ	0	—	8

9.3. Package DFN8 (4x4x0.85) mm



Top View

Side View

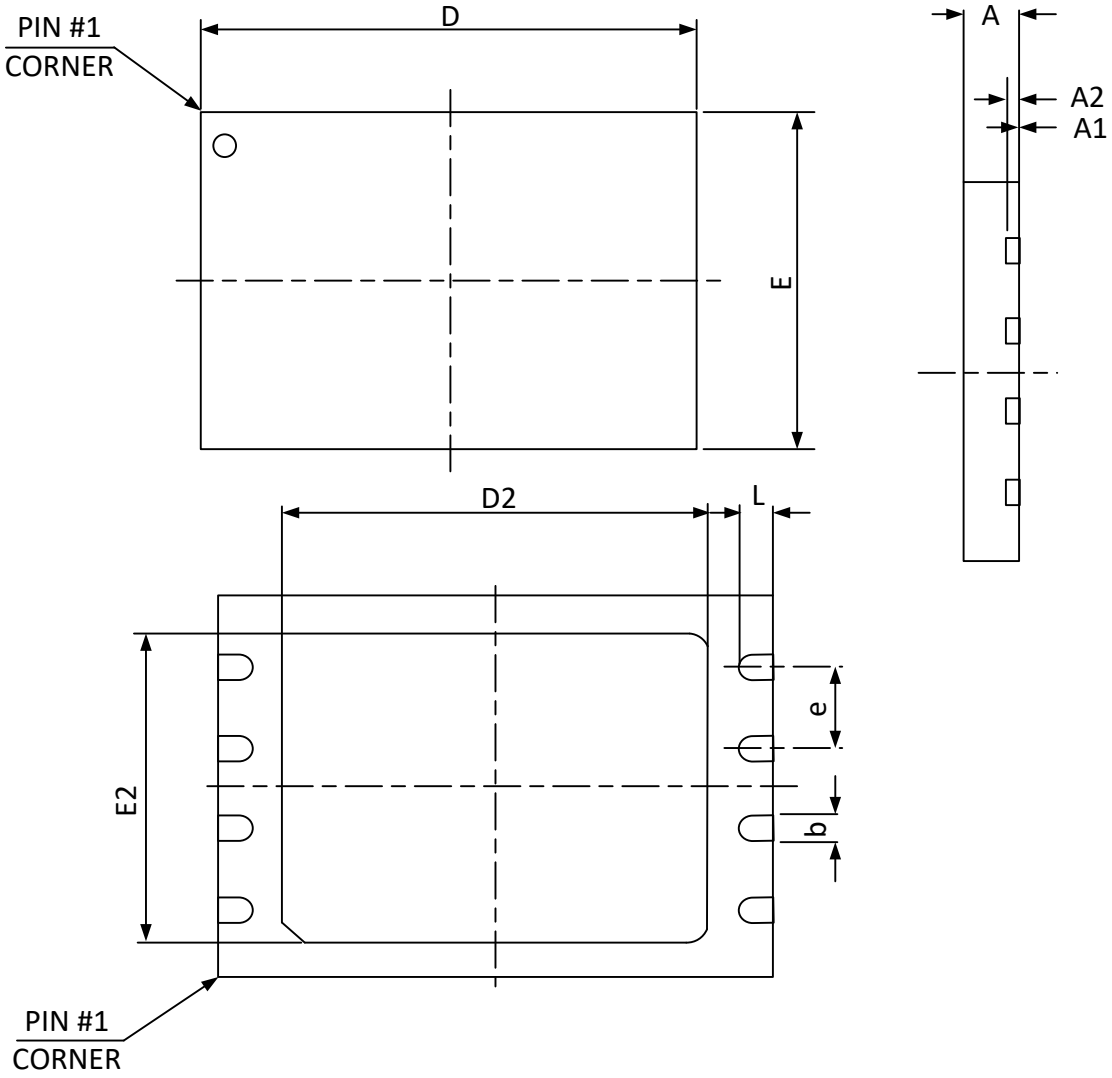


Bottom View

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	L
milli-mete	Min	0.80			0.25	3.90	2.20	3.90	2.60		0.35
	Norm	0.85		0.15	0.30	4.00	2.30	4.00	2.70	0.80	0.40
	Max	0.90	0.05		0.35	4.10	2.40	4.10	2.80		0.45

Note: Both package length and width do not include mold flash.

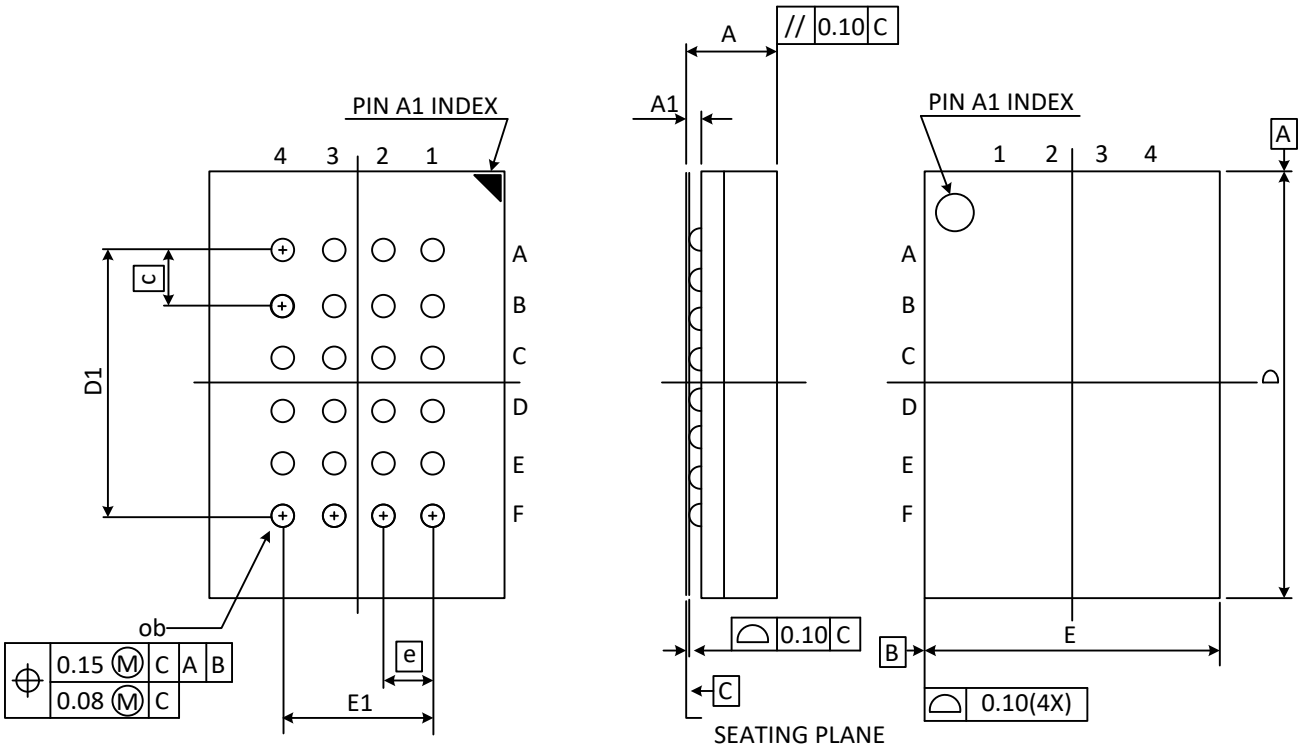
9.4. Package WSON (6x5) mm

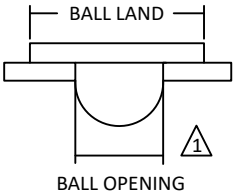


Symbol	Dimensions in Millimeters		
	Min	Norm	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.04
A2	---	0.20	---
D	5.90	6.00	6.10
E	4.90	5.00	5.10
D2	3.30	3.40	3.50
E2	3.90	4.00	4.10
e	---	1.27	---
b	0.35	0.40	0.45
L	0.55	0.60	0.65

Note: 1. Coplanarity: 0.1mm

9.5. Package BGA (8x6) mm





Note:

Ball land:0.45mm. Ball Opening:0.35mm.

PCB ball land suggested <=0.35mm

Symbol	Millimeters		
	Min	Norm	Max
A	---	---	1.20
A1	0.25	0.30	0.35
b	0.35	0.40	0.45
D	7.95	8.00	8.05
D1		5.00 BSC	
E	5.95	6.00	6.05
E1		3.00 BSC	
e		1.00 BSC	

10. REVISION HISTORY

Revision	Description	Date
0.0	Initial version	Oct 15, 2018
0.1	Revise to include UID command & description at page #15&55 and remove erase/program resume/suspend command at page #14-16&47-49.	Dec-07-2018
0.2	Revise to reset the QPI Frequency and add the note of erase process	Jan-24-2019
0.3	Revise the dimension DFN8 (4x4x0.85)	Mar-20-2019
0.4	Add the package VSOP / delete the package DFN2*3 and DFN4*3	May-10-2019
0.5	Add the package SOP16 300mil	May-13-2019
0.6	Revise the available OPN for package type and carrier ; 50H QPI diagram; value of I_{CC1} 、I_{CC2};Page48 description of 44H;Page22 description of 01H;Page14 description of LB1,LB0;	Aug-23-2019
0.7	Revise the access address of UID from 00-01-94 to00-00-94	Sep-04-2019
0.8	Updated 7.1 Power-on Timing description	Sep-19-2019
0.9	Corrected package information of SOP16 300mil	Sep-27-2019
1.0	Cancelled HW Reset under 8 pin package	Jan-20-2020
1.1	Replaced Read Speed based on results picked at the rising edge to which based on the falling edge and added note.	Mar-20-2020
1.2	Updated to deleted high temperature OPNs and command A3H DPD maximum change from 0.2uA to 4uA. Standby maximum changed from 20uA to 40uA. Deleted tHLQZ, tHHQX, and updated description of Hold in Device Operation.	Mar-30-2020