XTR20410

High Temperature 35V N-Channel Power MOSFET with Driver

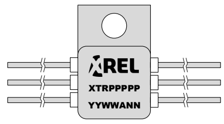
Rev 8 – November 2023 (DS-00025-11)

Data Sheet

PRODUCTION

DIP8
XTR20411A

CDFP8
XTR20411A



TO257-6
XTR20412B

FEATURES

- Operational beyond the -60°C to +230°C temperature range.
- Robust operation as low-side or high-side switch.
- Input-to-output level shifting from -30V to +35V.
- Standard Schmitt-trigger CMOS input.
- Exists in inverting and non-inverting versions
- Plug-and-play with any digital 5V output.
- Over current (desaturation) protection.
- Soft shut down
- Under voltage lockout UVLO protection on the output stage.
- Low on-resistance:
  - XTR20411: 1130 mΩ @ 230°C
  - XTR20412: 330 mΩ @ 230°C
- Large peak current capabilities:
  - XTR20411: 3.6A @ 230°C
  - XTR20412: 8.1A @ 230°C
- Low On- and Off-time (230nsec and 280nsec @ 230°C)
- Monolithic design.
- Latch-up free.
- Ruggedized SMT and thru-hole packages.
- Also available as bare die.

APPLICATIONS

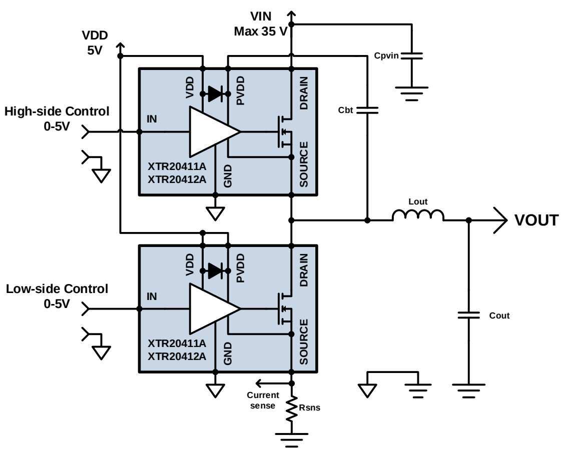
- Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
- DC/DC converters, motor drive, switching power supplies, switching control.

DESCRIPTION

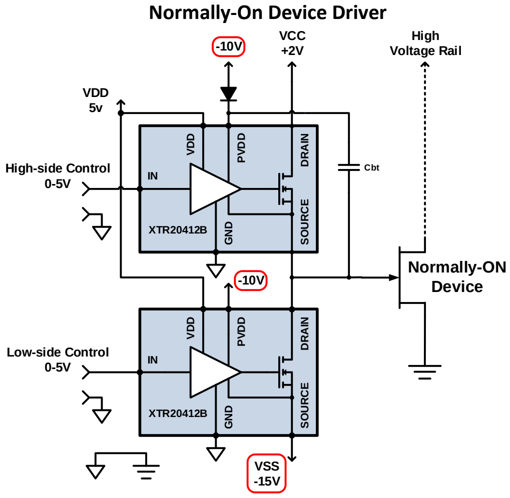
XTR20410 is a family of extremely flexible power N-channel MOSFETs with integrated driver designed for extreme reliability and high temperature applications such as DC/DC converters, motor control and power switching. XTR20410 parts can be used either as high-side (35V max), low-side, or low-side switch with negative offset (-30V max) on the output stage (SOURCE connected to a negative voltage), while receiving a control input signal referenced to GND. XTR20410 parts can be directly driven by any 5V digital output, making them fully plug-and-play devices, avoiding any time-consuming optimization of the matching network between driver and power transistor.
The XTR20410 family is composed of two different dies each with different maximum output current.
XTR20410 parts are robust to usual spikes associated with parasitic inductors and fast transients in switching applications.
Features of XTR20410 family parts include UVLO at the driver output, desaturation protection of the output transistor with soft shut-down functionality and possibility to select inversion of control signal.
Full functionality is guaranteed from -60°C to +230°C, though operation well beyond this temperature range is achieved. XTR20410 family parts have been designed to reduce system cost and ease adoption by reducing the learning curve and providing smart and easy to use features. The
Parts from the XTR20410 family are available in ruggedized SMD and through hole hermetic packages, as well as bare die.

PRODUCT HIGHLIGHT

DC-DC Power Stage



Normally-On Device Driver



ORDERING INFORMATION

X	TR	20	410
↓	↓	↓	↓
Source : X=X-REL Semi	Process: TR=HiTemp, HiRel	Part family	Part number

Product Reference	Temperature Range	Package	Pin Count	Marking
XTR20411-BD	-60°C to +230°C	Bare die		
XTR20411A-D	-60°C to +230°C	Ceramic side braze DIP	8	XTR20411A
XTR20411A-FE	-60°C to +230°C	Gull-wing flat pack with ePad	8	XTR20411A
XTR20412-BD	-60°C to +230°C	Bare die		
XTR20412A-T	-60°C to +230°C	TO257	6	XTR20412A
XTR20412B-T	-60°C to +230°C	TO257	6	XTR20412B

Other packages and packaging configurations possible upon request. For some packages or packaging configurations, MOQ may apply.

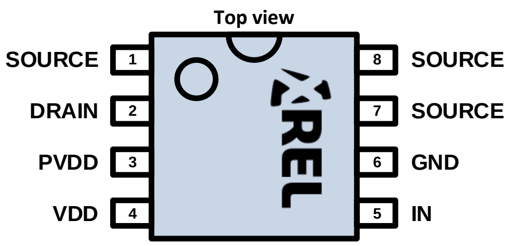
ABSOLUTE MAXIMUM RATINGS

Voltage on DRAIN to SOURCE	-1.5 to 45V
Voltage on IN and VDD to GND	-0.5 to 6.0V
Voltage on PVDD to SOURCE	-0.5 to 7.5V
Voltage on SOURCE to GND for XTR20411A and XTR20412A	-1 to 40V
Voltage on SOURCE to GND for XTR20411B and XTR20412B	-35V to 40V
Storage Temperature Range	-70°C to +230°C
Operating Junction Temperature Range	-70°C to +300°C
ESD Classification	1kV HBM MIL-STD-883

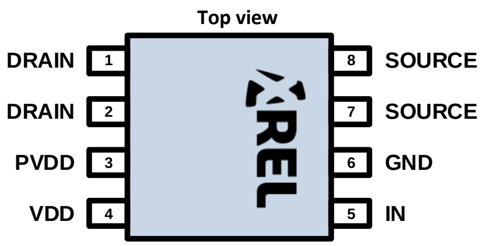
Caution: *Stresses beyond those listed in "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may permanently affect device reliability.*

PRODUCT VARIANTS

Side Brazed DIP8
XTR20411A-D

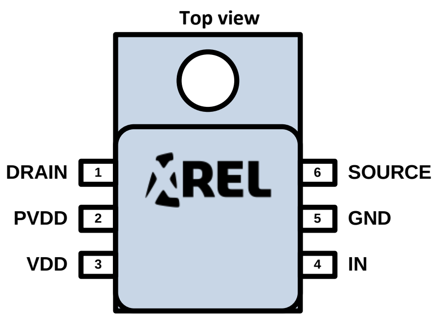


CDFP8 with ePad
XTR20411A-FE



ePAD (bottom of package) <u>must be</u> connected to SOURCE

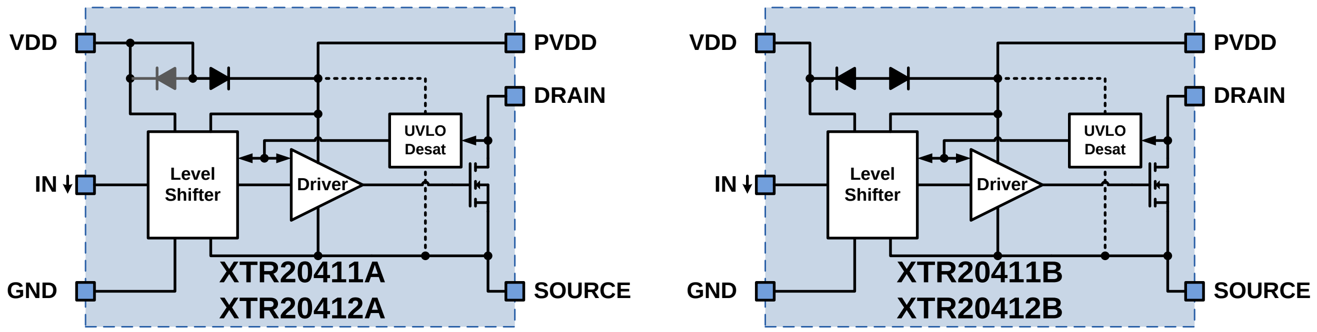
TO-257
XTR2041xA-T
XTR20412B-T



AVAILABLE FUNCTIONALITIES FOR EACH PRODUCT VERSION

Functionality	Product Version			
	XTR20411A-D	XTR20411A-FE	XTR20412A-T	XTR20412B-T
Inverting input				
Operation as low-side switch	✓	✓	✓	
Operation with negative offset				✓
Operation as high-side switch	✓	✓	✓	
Integrated bootstrap diode	✓	✓	✓	
Low power applications	✓	✓		
Mid power applications				
High power applications			✓	✓

BLOCK DIAGRAM



Arrows aside pin names indicate that pin is internally pulled down.
Different functionalities are available depending upon packaging configuration. Carefully read sections “Available Functionalities for Each Product Version” and “Theory of Operation” in order to select the packaging option that best fits your needs.

PIN DESCRIPTION

XTR20412A-T, XTR20412B-T		
Pin Number	Name	Description
1	DRAIN	Drain of the power NMOS transistor.
2	PVDD	Supply voltage of power section. Referenced to SOURCE.
3	VDD	Supply voltage of the input section. Referenced to GND.
4	IN	Input signal. Referenced to GND. Internally pulled down.
5	GND	Circuit ground.
6	SOURCE	Source of the power NMOS transistor.

XTR20411A-D		
Pin Number	Name	Description
1	SOURCE	Source of the power NMOS transistor.
2	DRAIN	Drain of the power NMOS transistor.
3	PVDD	Supply voltage of power section. Referenced to SOURCE.
4	VDD	Supply voltage of the input section. Referenced to GND.
5	IN	Input signal. Referenced to GND. Internally pulled down.
6	GND	Circuit ground.
7	SOURCE	Source of the power NMOS transistor.
8	SOURCE	Source of the power NMOS transistor.

XTR20411A-FE		
Pin Number	Name	Description
1	DRAIN	Drain of the power NMOS transistor.
2	DRAIN	Drain of the power NMOS transistor.
3	PVDD	Supply voltage of power section. Referenced to SOURCE.
4	VDD	Supply voltage of the input section. Referenced to GND.
5	IN	Input signal. Referenced to GND. Internally pulled down.
6	GND	Circuit ground.
7	SOURCE	Source of the power NMOS transistor.
8	SOURCE	Source of the power NMOS transistor.
ePAD	SOURCE	The ePAD must be connected to SOURCE.

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply voltage VDD to GND	4.5		5.5	V
Supply voltage PVDD to SOURCE	See UVLO threshold		5.5	V
SOURCE to GND voltage XTR20411A, XTR20412A	-1		35	V
SOURCE to GND voltage XTR20411B and XTR20412B	-30		35	V
Input voltage on IN to GND	-0.3		VDD	V
DRAIN-SOURCE voltage (V_{DS})	-1		+35	V
Junction Temperature[1] T_j	-60		230	°C

[1] *Operation beyond the specified temperature range is achieved with little degradation on electrical parameters.*

THERMAL CHARACTERISTICS

Parameter	Condition	Min	Typ	Max	Units
XTR20411A-D (Ceramic Side Brazed DIP8)					
Thermal Resistance: J-C R_{Th_J-C}			30		°C/W
Thermal Resistance: J-A R_{Th_J-A}			100		°C/W
XTR20411B-T (6-lead TO257)					
Thermal Resistance: J-C R_{Th_J-C}			10		°C/W
Thermal Resistance: J-A R_{Th_J-A}			50		°C/W
XTR20412A/B-T (6-lead TO257)					
Thermal Resistance: J-C R_{Th_J-C}			5		°C/W
Thermal Resistance: J-A R_{Th_J-A}			45		°C/W
XTR20411A-FE (DFP8 with exposed pad)					
Thermal Resistance: J-C R_{Th_J-C}	Measured on ePAD.		7		°C/W
Thermal Resistance: J-A R_{Th_J-A}	ePAD thermally connected to 3cm² PCB copper.		70		°C/W

ELECTRICAL SPECIFICATIONS XTR20411A

Static Characteristics

Unless otherwise stated, VDD=5V, PVDD=5V, GND=SOURCE, IN=0V, V_{DS}=20V, I_{DRAIN}=1A, -60°C<T_C<230°C.

Parameter	Condition	Min	Typ	Max	Units
Supply Current					
Static VDD Supply Current I_{VDD_Sta}	V_{IN}=GND or VDD T_C=-60°C T_C=85°C T_C=230°C		 11 17 22		µA
Static PVDD Supply Current I_{PVDD_Sta}	V_{IN}=GND or VDD Type A; T_C=-60°C Type A; T_C=230°C Type B; T_C=-60°C Type B; T_C=230°C		 95 175 115 200		µA
Control INPUT					
Low Level Input Voltage V_{IL}	T_C=85°C		1.7		V
High Level Input Voltage V_{IH}	T_C=85°C		3.3		V
Input Current I_{IN}	V_{IN}=GND or VDD T_C=-60°C T_C=85°C T_C=230°C		 2.3 3.4 4.5		µA
Under Voltage Lockout (UVLO)					
V_{PVDD} Start Voltage[1] V_{UVLOR}	Rising PVDD threshold XTR20411A	3.2	3.5 4.1	3.8 4.5	V
V_{PVDD} Start-stop Hysteresis V_{UVLOH}	XTR20411A		300 400		mV
Output Transistor					
Drain-Source Breakdown Voltage $V_{(BR)DSS}$	I_{DRAIN} = 100uA	55V			V
Off-State Drain Current I_{DSS}	Output transistor OFF and V_{DS}=35V T_C=85°C T_C=230°C		 0.01 6	 0.1 25	µA
Static ON Resistance R_{DSon}	I_{DRAIN}=1A, side brazed DIP8 package (XTR20411-D) T_C=-60°C T_C=85°C T_C=230°C		 485 755 1130		mΩ
Continuous Drain Current $I_{D(DC)}$	V_{IN}=VDD, side brazed DIP8 package (XTR20411-D) T_J=-60°C T_J=85°C T_J=230°C		 1.9 1.3 0.9		A
Source-Drain Body Diode					
Forward Voltage V_{BD}	I_{DS}=-0.5A T_C=-60°C T_C=85°C T_C=230°C		 1.13 1.01 0.89		V
Bootstrap Diode (XTR20411A)					
Continuous Forward Current I_{BSTD}	V_F=1.5V T_C=-60°C T_C=230°C		 0.48 0.44		A
Forward Voltage V_{BSTD}	I_{BSTD}=300mA T_C=-60°C T_C=230°C		 1.31 1.17		V

[1] *Below this threshold, the output nMOS is OFF, for PVDD rising.*

ELECTRICAL SPECIFICATIONS XTR20411A (CONTINUED)

Dynamic Characteristics

Unless otherwise stated, VDD=5V, PVDD=5V, GND=SOURCE, IN=0V, V_{DS}=20V, I_{DRAIN}=1A, -60°C<T_C<230°C.

Parameter	Condition	Min	Typ	Max	Units
Supply Current					
Dynamic VDD Supply Current I_{VDD_Dyn}	For input Freq = 1MHZ and duty cycle=50% T_C=-60°C T_C=230°C		 40 56		µA
Dynamic PVDD Supply Current I_{PVDD_Dyn}	Freq=200kHz and duty cycle=50% Freq=1MHz and duty cycle=50%		1.0 4.5		mA
Max drain current and DESAT protection					
Peak Drain Current during Blanking Time I_{Dpeak}	20us pulse with Duty Cycle = 0.2%; V_{DS}=20V T_C=-60°C T_C =85°C T_C=230°C		 7.6 5.2 3.9		A
Desaturation Drain Current after Blanking Time[1] I_{DESAT}	1us pulse with Duty Cycle = 0.2% T_C=-60°C T_C =85°C T_C=230°C		 6.5 4 3.6		A
Blanking Time[2] t_{Blank}	T_C=-60°C T_C =85°C T_C=230°C		560 460 450		ns
Soft Turn-off Time t_{SSD}[3]	T_C=-60°C T_C =85°C T_C=230°C		120 210 310		ns
Switching Time 20411A/B and 20414A [4]					
Delay ON Time [5] $t_{d(ON)}$	T_C=-60°C T_C =85°C T_C=230°C		110 155 210		ns
Delay OFF Time $t_{d(OFF)}$	T_C=-60°C T_C =85°C T_C=230°C		130 170 215		ns

[1] *Above this current threshold the desaturation protection is activated and turns off the driver till the next rising edge of the input signal.*

[2] *Once V_{GS} of the output transistor is high, a comparator checks if I_{DS}<I_{DESAT} after this blanking time.*

[3] *If desaturation arises (I_{DS}>I_{DESAT}) after the blanking time, the output transistor is softly turned OFF during the t_{SSD} time.*

[4] *Used as high side switch in a Buck converter configuration (35V supply, 300mA ON current)*

[5] *From 50% input signal to 10% V_{DS} on the output transistor.*

ELECTRICAL SPECIFICATIONS XTR20412

Static Characteristics

Unless otherwise stated, VDD=5V, PVDD=5V, GND=SOURCE, IN=0V, V_{DS}=20V, I_{DRAIN}=1A, -60°C<T_C<230°C.

Parameter	Condition	Min	Typ	Max	Units
Supply Current					
Static VDD Supply Current I_{VDD_Sta}	V_{IN}=GND or VDD T_C=-60°C T_C=85°C T_C=230°C		 12 17 22		µA
Static PVDD Supply Current I_{PVDD_Sta}	V_{IN}=GND or VDD Type A; T_C=-60°C Type A; T_C=230°C Type B; T_C=-60°C Type B; T_C=230°C		 90 170 125 210		µA
Control INPUT					
Low Level Input Voltage V_{IL}	T_C=85°C		1.7		V
High Level Input Voltage V_{IH}	T_C=85°C		3.3		V
Input Current I_{IN}	V_{IN}=GND or VDD T_C=-60°C T_C=85°C T_C=230°C		 2.3 3.4 4.5		µA
Under Voltage Lockout (UVLO)					
V_{PVDD} Start Voltage[1] V_{UVLOR}	Rising PVDD threshold XTR20412A XTR20412B	 3.2	 3.5 4.1	 3.8 4.5	V
V_{PVDD} Start-stop Hysteresis V_{UVLOH}	XTR20412A XTR20412B		300 400		mV
Output Transistor					
Drain-Source Breakdown Voltage $V_{(BR)DSS}$	I_{DRAIN} = 100uA	55V			V
Off-State Drain Current I_{DSS}	Output transistor OFF and V_{DS}=35V T_C=85°C T_C=230°C		 0.03 18	 0.2 75	µA
Static ON Resistance R_{DSon}	I_{DRAIN}=100mA, TO257 package (XTR20412-T) T_C=-60°C T_C=85°C T_C=230°C		 130 220 330		mΩ
Continuous Drain Current $I_{D(DC)}$	V_{IN}=VDD for TO-257 package (XTR20412-T) T_J=-60°C T_J=85°C T_J=230°C		 5.1 3.9 2.5		A
Source-Drain Body Diode					
Forward Voltage V_{BD}	I_{DS}=-1A T_C=-60°C T_C=85°C T_C=230°C		 1.03 0.88 0.73		V
Bootstrap Diode (XTR20412A only)					
Continuous Forward Current I_{BSTD}	V_F=1.5V T_C=85°C T_C=230°C		 0.52 0.50		A
Forward Voltage V_{BSTD}	I_{BSTD}=300mA T_C=85°C T_C=230°C		 1.22 1.15		V

[1] *Below this threshold, the output nMOS is OFF, for PVDD rising.*

ELECTRICAL SPECIFICATIONS XTR20412 (CONTINUED)

Dynamic Characteristics

Unless otherwise stated, VDD=5V, PVDD=5V, GND=SOURCE, IN=0V, V_{DS}=20V, I_{DRAIN}=1A, -60°C<T_C<230°C.

Parameter	Condition	Min	Typ	Max	Units
Supply Current					
Dynamic VDD Supply Current I_{VDD_Dyn}	For input Freq = 1MHZ and duty cycle=50% T_C=-60°C T_C=230°C		 44 60		µA
Dynamic PVDD Supply Current I_{PVDD_Dyn}	Freq=200kHz and duty cycle=50% Freq=1MHz and duty cycle=50%		2 10		mA
Max drain current and DESAT protection					
Peak Drain Current during Blanking Time I_{Dpeak}	20us pulse with Duty Cycle = 0.2%; V_{DS}=20V T_C=-60°C T_C =85°C T_C=230°C		 20.5 15.5 10.2		A
Desaturation Drain Current after Blanking Time[1] I_{DESAT}	1us pulse with Duty Cycle = 0.2% T_C=-60°C T_C =85°C T_C=230°C		 14.1 9.3 8.1		A
Blanking Time[2] t_{Blank}	T_C=-60°C T_C =85°C T_C=230°C		665 545 535		ns
Soft Turn-off Time t_{SSD}[3]	T_C=-60°C T_C =85°C T_C=230°C		220 240 340		ns
Switching Time 20412A/B[4]					
Delay ON Time [5] $t_{d(ON)}$	T_C=-60°C T_C =85°C T_C=230°C		115 160 215		ns
Delay OFF Time $t_{d(OFF)}$	T_C=-60°C T_C =85°C T_C=230°C		155 210 285		ns

[1] *Above this current threshold the desaturation protection is activated and turns off the driver till the next rising edge of the input signal.*
[2] *Once V_{GS} of the output transistor is high, a comparator checks if I_{DS}<I_{DESAT} after this blanking time.*
[3] *If desaturation arises (I_{DS}>I_{DESAT}) after the blanking time, the output transistor is softly turned OFF during the t_{SSD} time.*
[4] *Used as high side switch in a Buck converter configuration (35V supply, 300mA ON current).*
[5] *From 50% input signal to 10% V_{DS} on the output transistor.*

XTR20411 TYPICAL PERFORMANCE

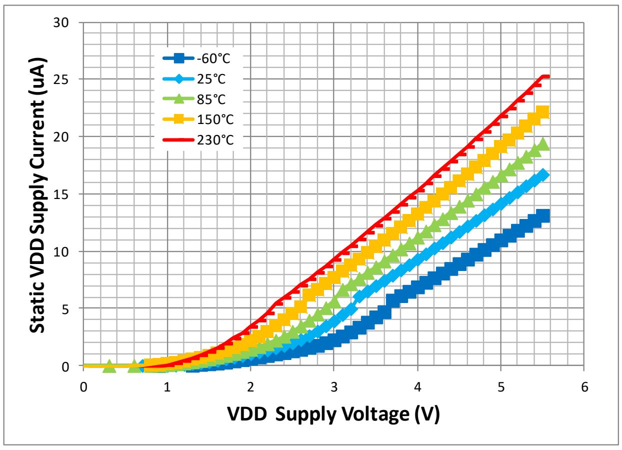


Figure 1. Static VDD supply current (I_{VDD}) vs V_{DD} supply voltage for several case temperatures.

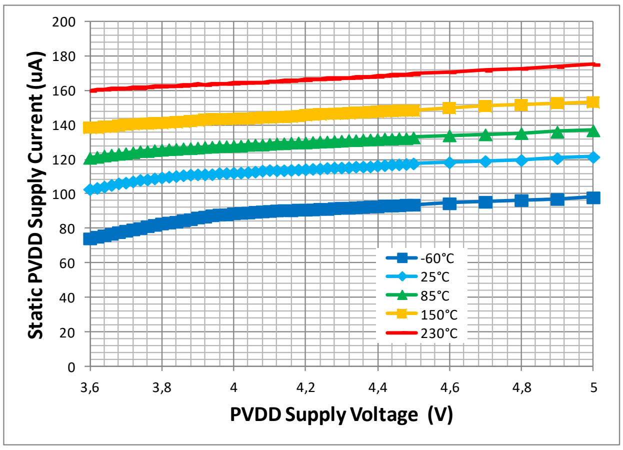


Figure 2. Static PVDD supply current (I_{PVDD}) vs P_{VDD} supply voltage for several case temperatures for Type A.

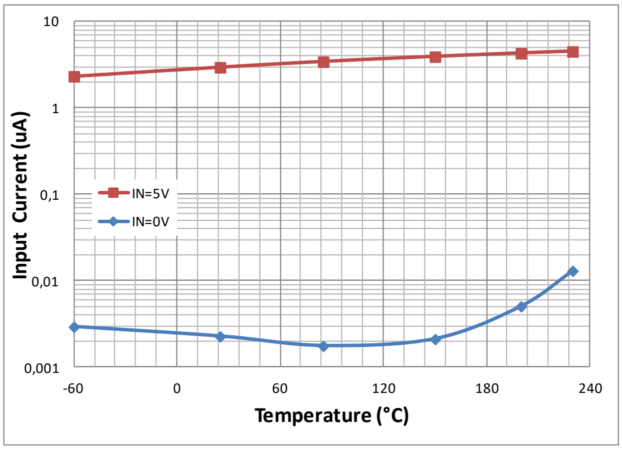


Figure 3. Input current (I_{IN}) vs case temperature. V_{DD}=5V.

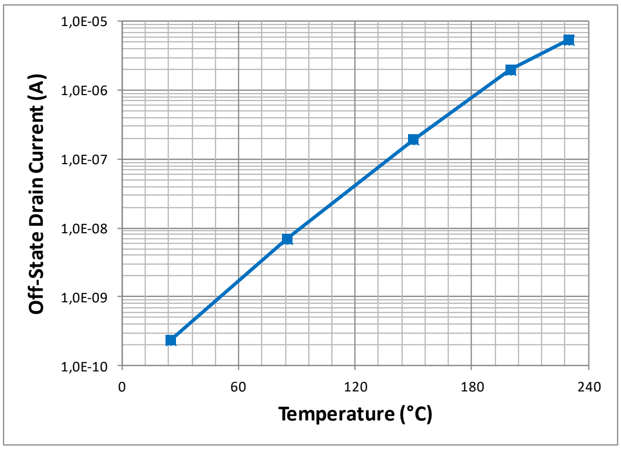


Figure 4. Off-state drain current (I_{DSS}) vs case temperature. Drain-Source=35V, IN=0V.

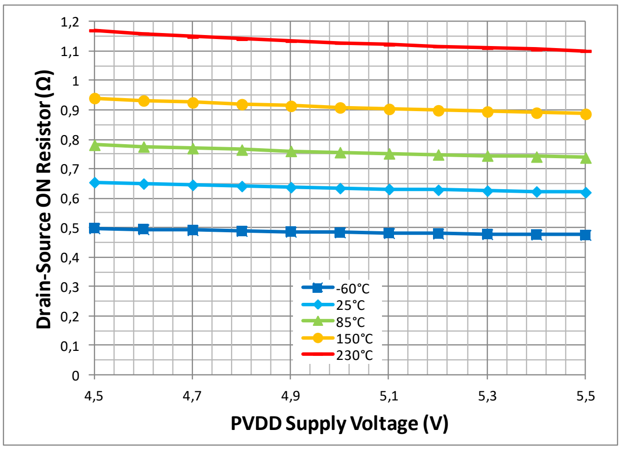


Figure 5. Drain-source ON resistance ($R_{DS(on)}$) vs P_{VDD} supply current for several case temperatures. Drain-Source=50mV and VIN=VDD=5V.

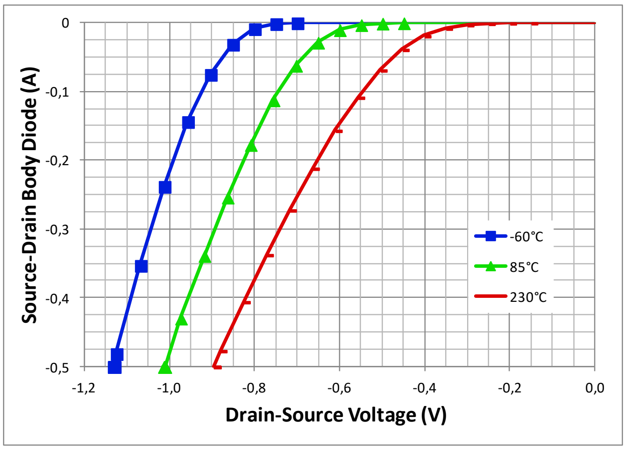


Figure 6. Source drain body diode current (I_{BD}) vs Drain-source voltage (V_{BD}) for several case temperatures. VIN=VDD=PVDD=5V.

XTR20411 TYPICAL PERFORMANCE (CONTINUED)

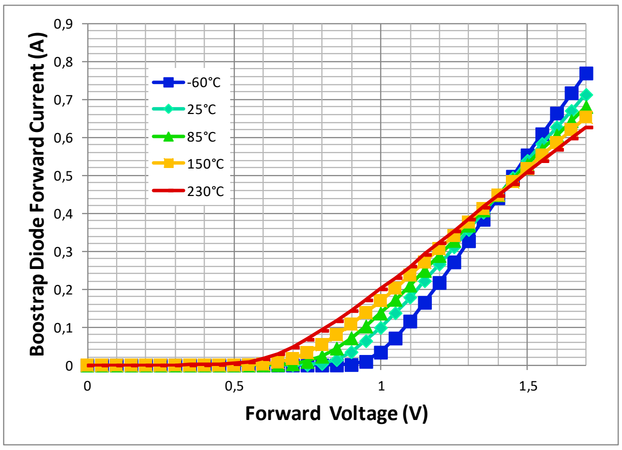


Figure 7. Boostrap diode forward current (I_{BSTD}) vs forward voltage (V_{BSTD}) for several case temperatures.

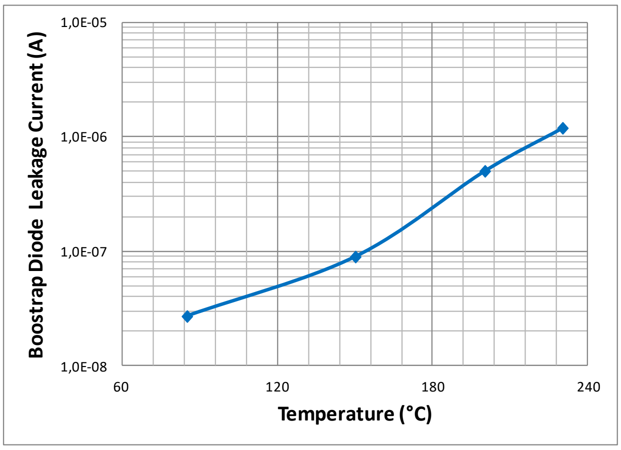


Figure 8. Boostrap diode leakage current (I_{BSTDSS}) vs case temperature. PVDD-VDD=35V.

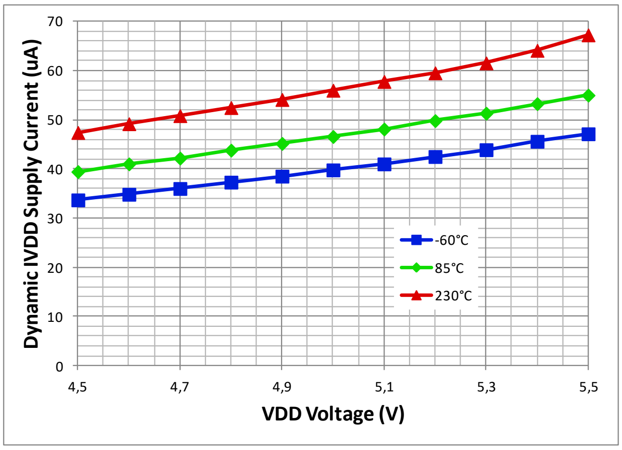


Figure 9. Dynamic VDD supply current (I_{VDD}) vs VDD supply voltage for several case temperatures. Input frequency 1MHZ and duty cycle 50%.

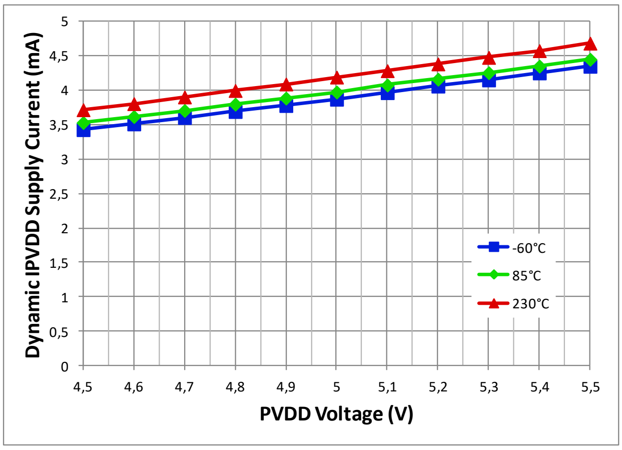


Figure 10. Dynamic PVDD supply current (I_{PVDD}) vs PVDD supply voltage for several case temperatures. Input frequency 1MHZ and duty cycle 50%.

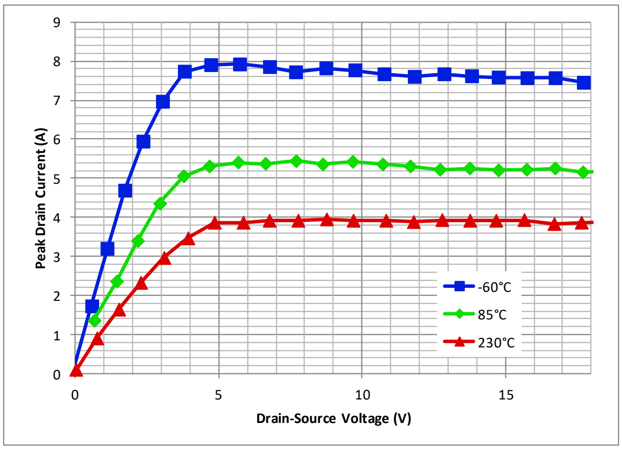


Figure 11. Peak drain current (I_{Dpeak}) vs drain-source voltage for several case temperatures. PVDD=5V.

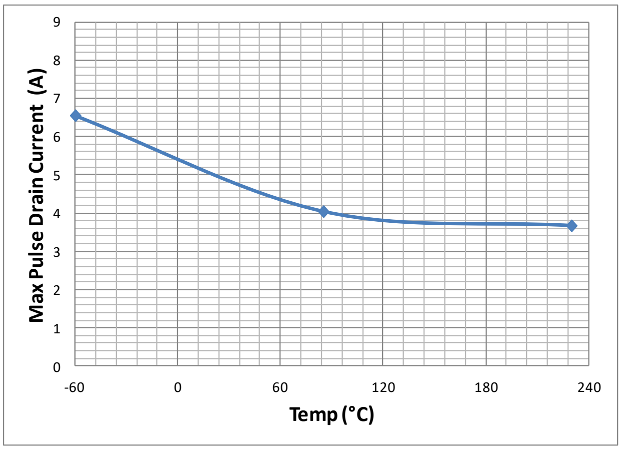


Figure 12. Pulsed drain current (I_{DESAT}) after the blanking time vs case temperature. PVDD=5V.

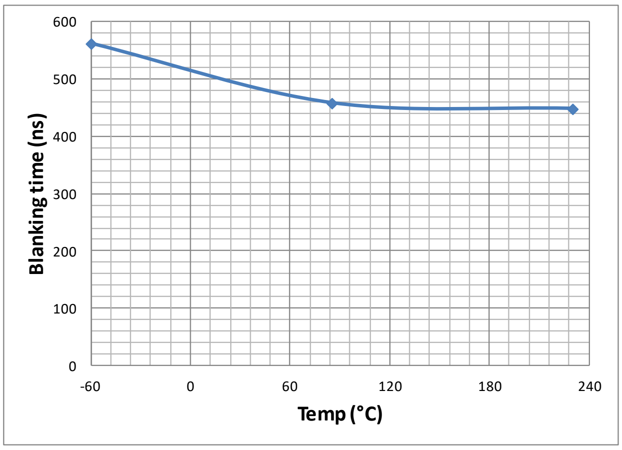


Figure 13. Blanking time (t_{Blank}) vs case temperature. IN=VDD=PVDD=5V.

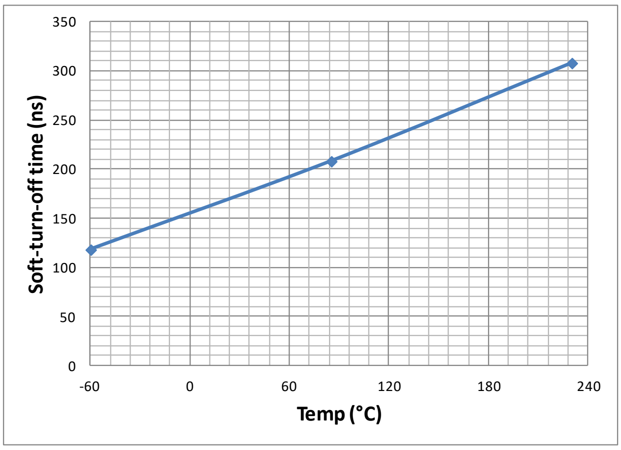


Figure 14. Soft turn off time (t_{SSD}) vs case temperature. IN=VDD=PVDD=5V.

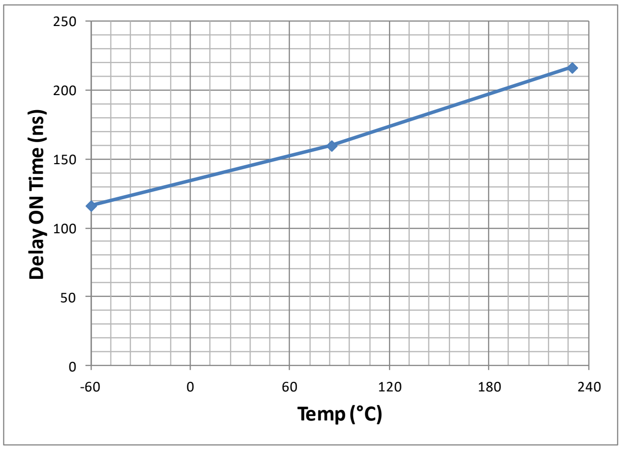


Figure 15. Delay ON time ($t_{d(ON)}$) vs case temperature. IN=VDD=PVDD=5V.

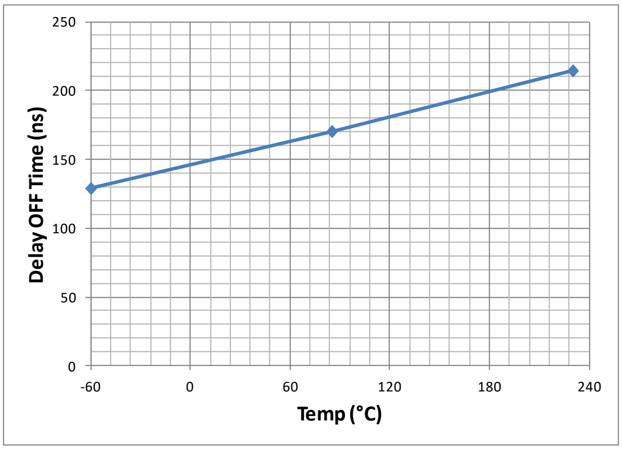


Figure 16. Delay OFF time ($t_{d(OFF)}$) vs case temperature. IN=VDD=PVDD=5V.

XTR20412 TYPICAL PERFORMANCE

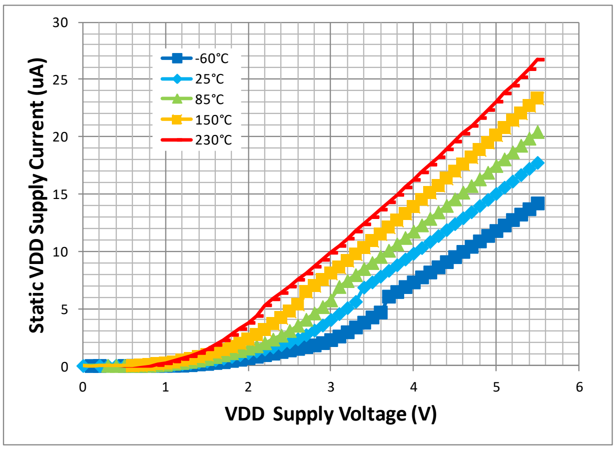


Figure 17. Static VDD supply current (I_{VDD}) vs V_{DD} supply voltage for several case temperatures.

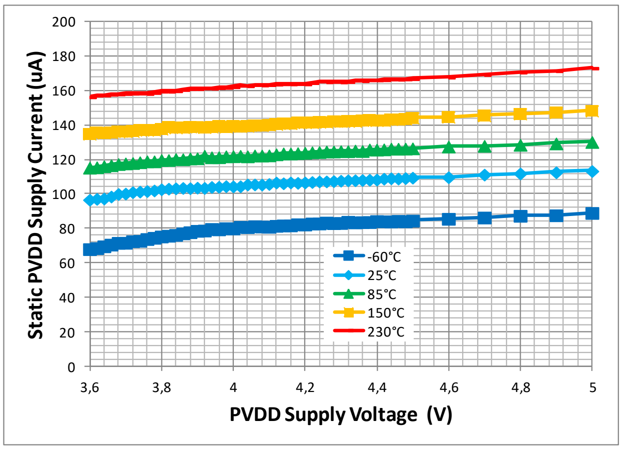


Figure 18. Static PVDD supply current (I_{PVDD}) vs P_{VDD} supply voltage for several case temperatures for Type A.

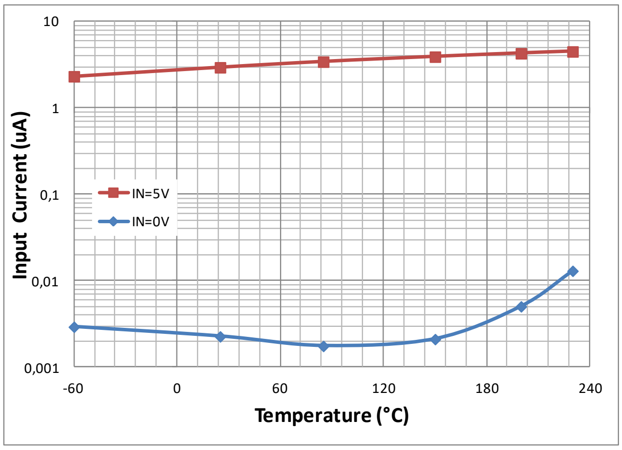


Figure 19. Input current (I_{IN}) vs case temperature. V_{DD}=5V.

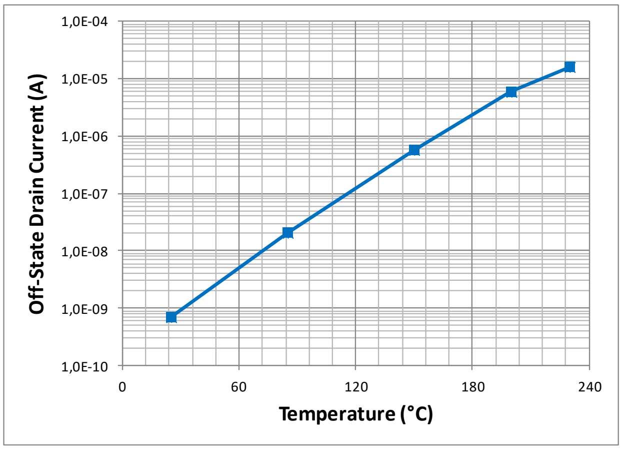


Figure 20. Off-state drain current (I_{DSS}) vs case temperature. Drain-Source=35V, IN=0V.

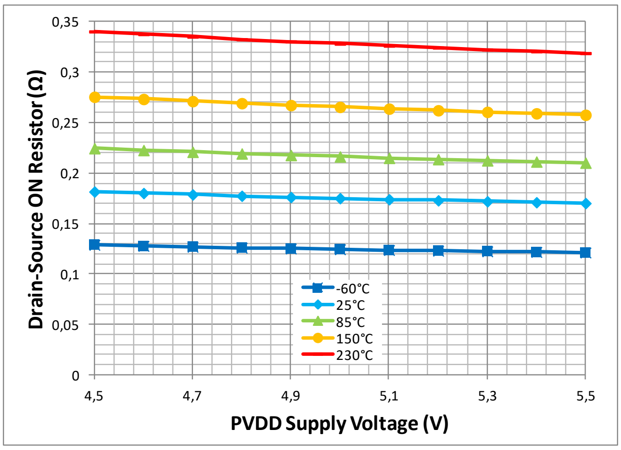


Figure 21. Drain-source ON resistance ($R_{DS(on)}$) vs P_{VDD} supply current for several case temperatures. Drain-Source=50mV and VIN=VDD=5V.

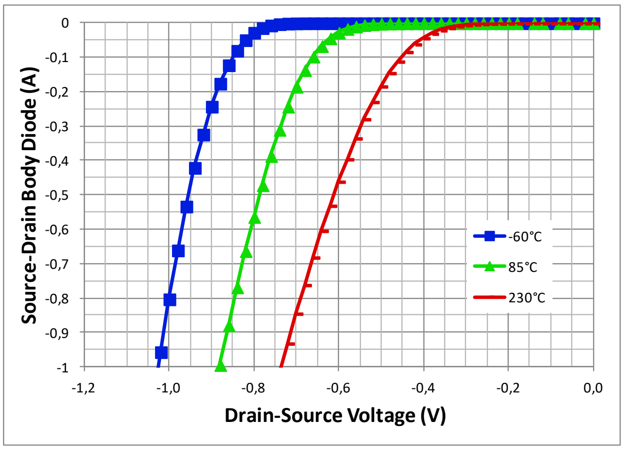


Figure 22. Source drain body diode current (I_{BD}) vs Drain-source voltage (V_{BD}) for several case temperatures. VIN=VDD=PVDD=5V.

XTR20412 TYPICAL PERFORMANCE (CONTINUED)

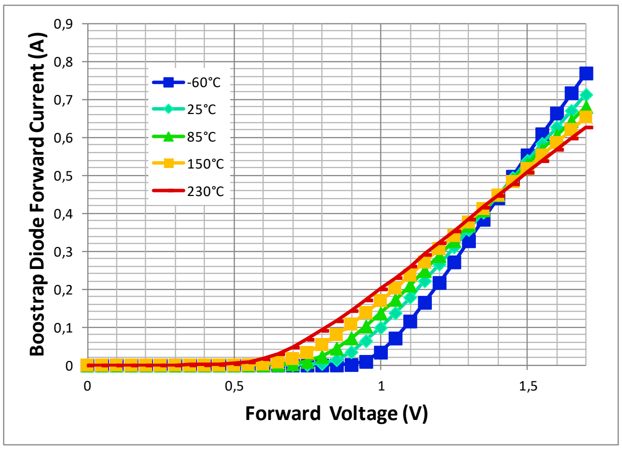


Figure 23. Boostrap diode forward current (I_{BSTD}) vs forward voltage (V_{BSTD}) for several case temperatures.

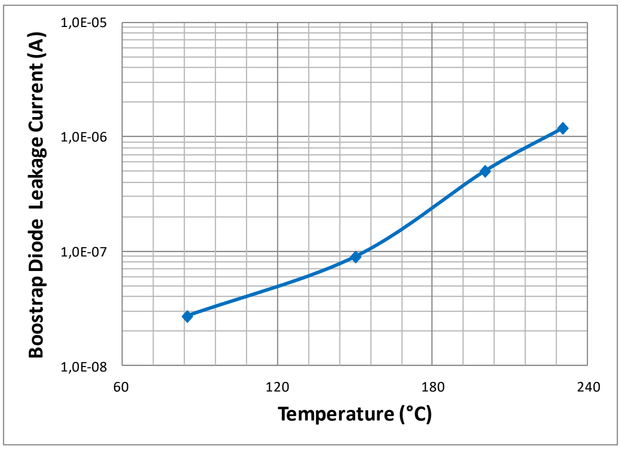


Figure 24. Boostrap diode leakage current (I_{BSTDSS}) vs case temperature. PVDD-VDD=35V.

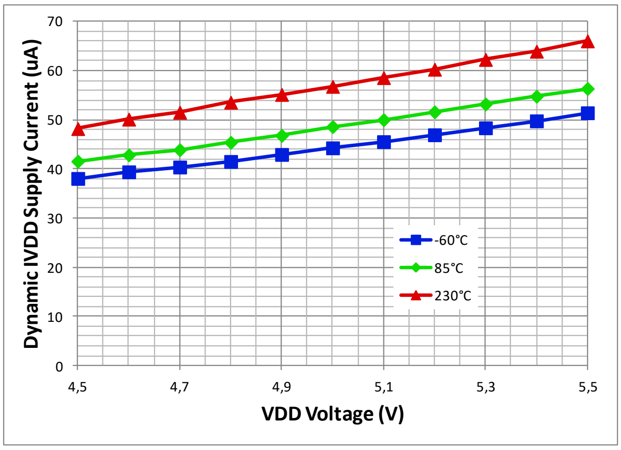


Figure 25. Dynamic VDD supply current (I_{VDD}) vs VDD supply voltage for several case temperatures. Input frequency 1MHZ and duty cycle 50%.

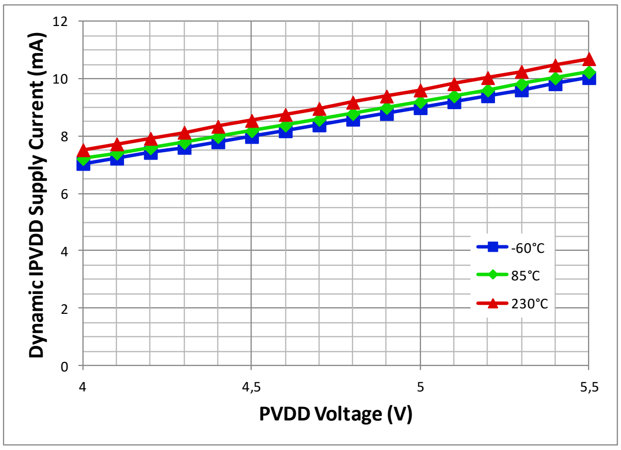


Figure 26. Dynamic PVDD supply current (I_{PVDD}) vs PVDD supply voltage for several case temperatures. Input frequency 1MHZ and duty cycle 50%.

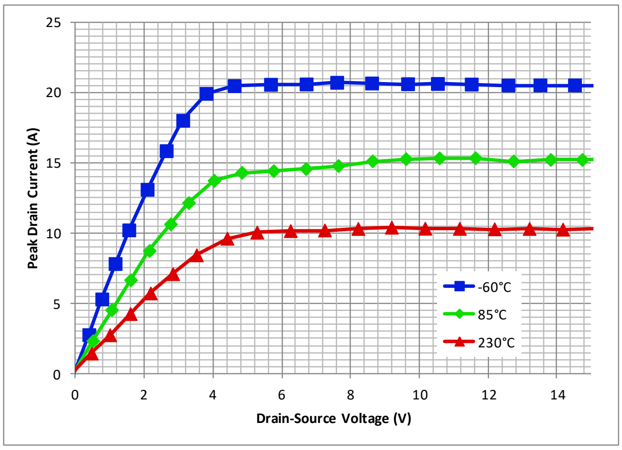


Figure 27. Peak drain current (I_{Dpeak}) vs drain-source voltage for several case temperatures. PVDD=5V.

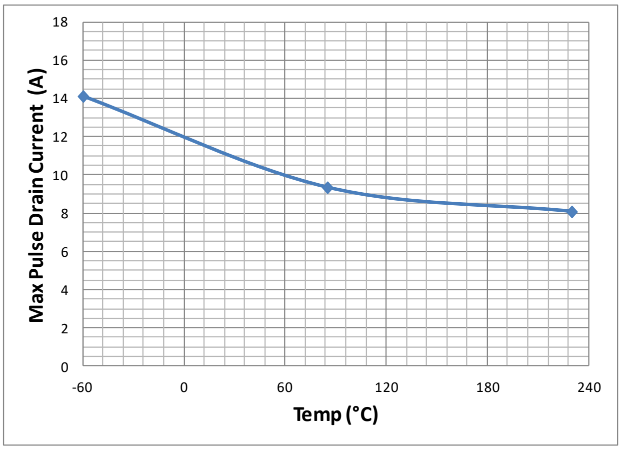


Figure 28. Pulsed drain current (I_{DESAT}) after the blanking time vs case temperature. PVDD=5V.

XTR20412 TYPICAL PERFORMANCE (CONTINUED)

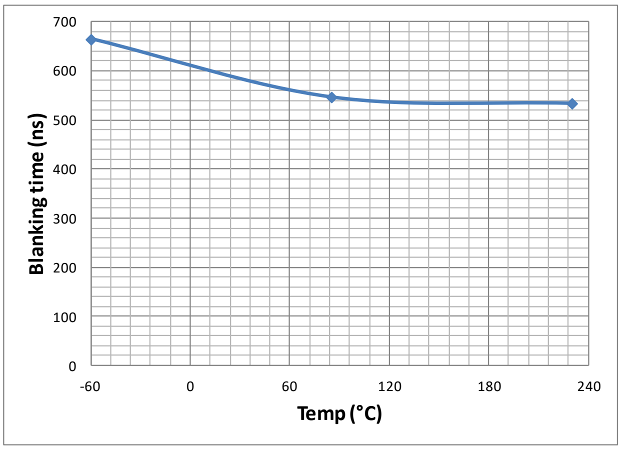


Figure 29. Blanking time (t_{Blank}) vs case temperature.
IN=VDD=PVDD=5V.

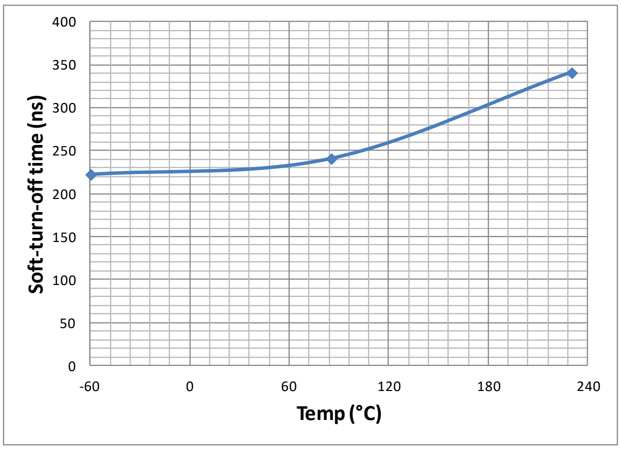


Figure 30. Soft turn off time (t_{SSD}) vs case temperature.
IN=VDD=PVDD=5V.

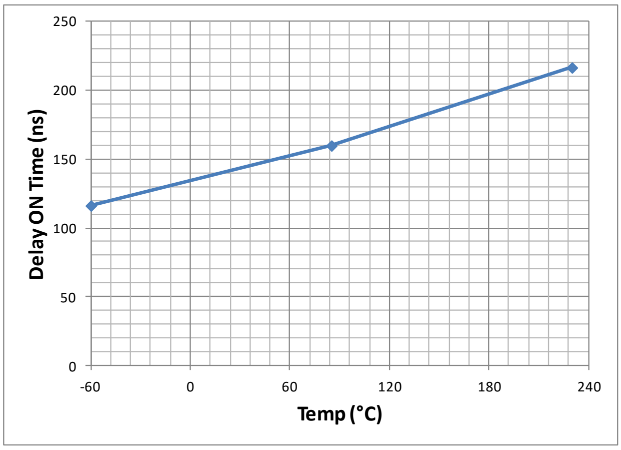


Figure 31. Delay ON time ($t_{d(ON)}$) vs case temperature.
IN=VDD=PVDD=5V.

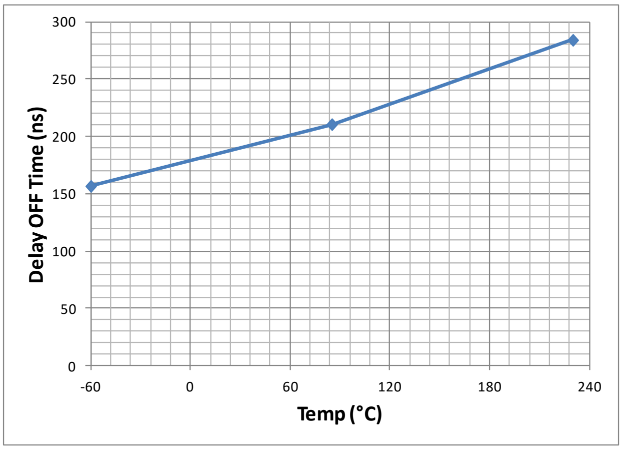


Figure 32. Delay OFF time ($t_{d(OFF)}$) vs case temperature.
IN=VDD=PVDD=5V.

THEORY OF OPERATION

Introduction

The XTR20410 is a family of 35V N-channel MOS transistors with integrated driver able to operate from -60°C to +230°C. Unique features of this product family make them an extremely flexible block when designing power switching applications.

Parts from the XTR20410 are divided into two variants depending upon the range of the common mode voltage of the output stage with respect to the input stage.

Devices with suffix “A” (XTR20411A and XTR20412A) accept output common modes from -1V up to 35V and include a high-current diode from VDD (input stage) to PVDD (output stage) which can be used as bootstrap diode when using these parts as high-side drivers.

On the other side, devices with suffix “B” (XTR20411B and XTR20412B) accept output common modes from -30V up to 35V. In this case the PVDD supply voltage must be provided by an independent supply.

Level shifting is performed inside the XTR20410 parts.

The XTR20410 family includes several protection features offering enhanced robustness for operation in switching applications.

- Despite the recommended upper DC limit voltage on VDD and PVDD, the circuit can tolerate repetitive transient spike voltages up to 3V above the operation limits.
- A desaturation protection is implemented which softly turns off the output transistor whenever its current level exceeds a defined current threshold when in ON state (after a defined blanking time).
- Soft shut-down is implemented to prevent high dV/dt and di/dt on the application when the desaturation protection is activated.
- An UVLO on the floating output supply (PVDD to SOURCE) guarantees that bellow a defined threshold the output MOSFET is off.
- The recommended V_{DD} range is between 4.5V and 5.5V. However, at lower V_{DD}, the circuit could be functional as expected (with longer propagation delay). For very low V_{DD} voltages (under 2-3V), it is guaranteed that the output MOSFET is off. Using this circuit bellow VDD=4.5V is however not recommended.

The XTR20410 family can also be packaged in such a way that the input signal logic is inverted (i.e. a low input level turns ON the output MOSFET)

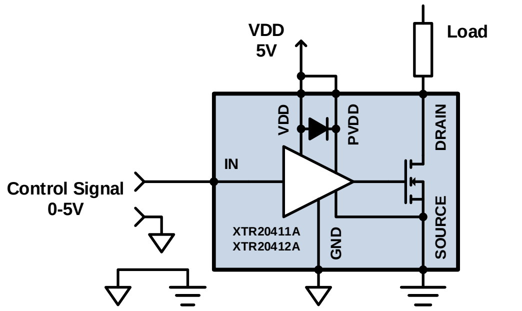
Operation Modes

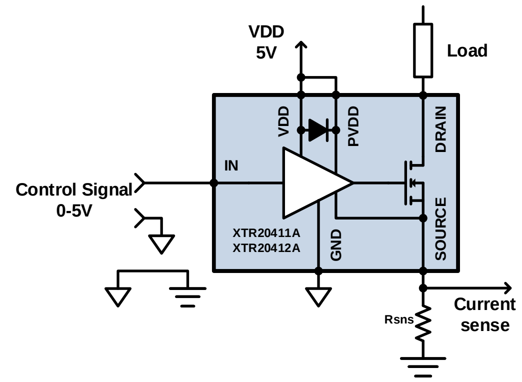
Low-side mode (V_{SOURCE}=0V)

In low-side mode operation, the SOURCE terminal is either directly tied to ground or through a small current sense resistor.

For this operation mode, variant A is recommended. In this case, VDD and PVDD must be shorted or connected through a low pass RC filter from VDD to PVDD in order to filter out transient current spikes in VDD supply. Use a resistor up to 100 ohms and a capacitor of at least 100nF. Variant B could also be used, though turn-off delays of variant B with SOURCE close to ground are about twice those of variant A at the same conditions.

The use of power and signal ground planes connected on a unique point as well as proper layout techniques is recommended.

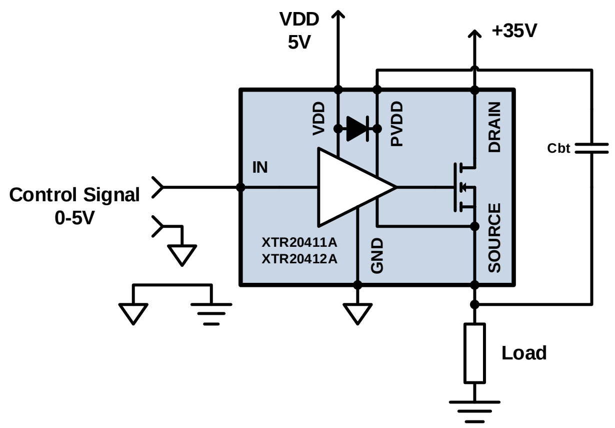


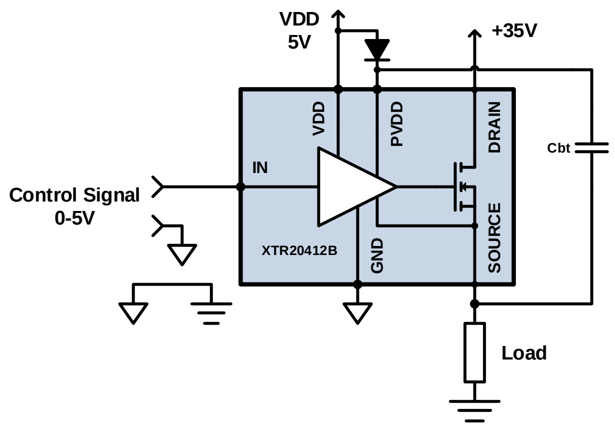


High-side mode

Operation in high-side mode can be obtained with both product variants (A and B). When using variant A, the bootstrap diode is already provided within the XTR20410 parts between VDD and PVDD terminals. For variant B, an external bootstrap diode must be used.

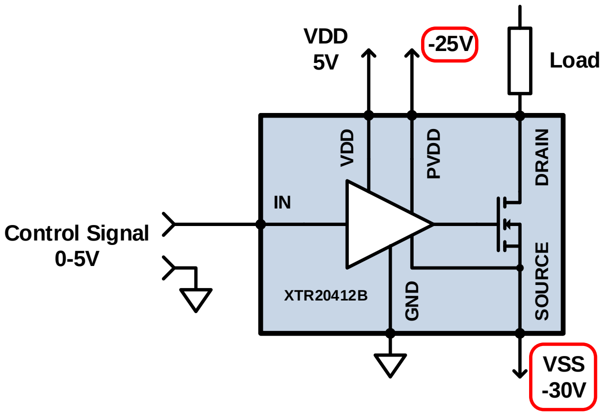
In high-side mode the drain of the power transistor is directly tied to the bus voltage while the load is seen on the source of the output transistor.





Floating mode

This operation mode can only be achieved with the B variant, allowing the output stage to be shifted to negative as well as to positive levels (from -30V to +35V) with respect to the input stage. In this case an external 5V floating source must be provided between PVDD and SOURCE.

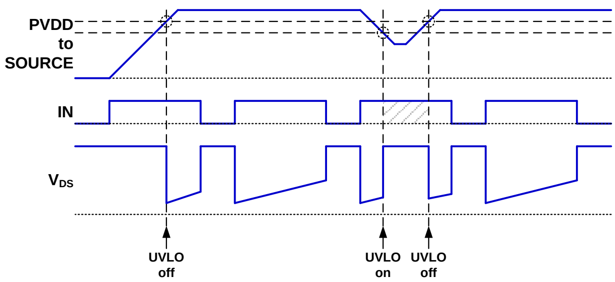


Protections

Under Voltage Lockout (UVLO)

An UVLO detector continuously monitors the output stage supply voltage (PVDD to SOURCE). During power-up, the UVLO protection guarantees that the output transistor is in off state for V_{PVDD}-V_{SOURCE} below the V_{UVLOR} threshold for whichever state of IN (or /IN). Above the V_{UVLOR} threshold, the output MOSFET is controlled by the IN (or /IN) terminal).

In case the UVLO protection is activated (UVLO on) while the output transistor is ON, this latter is immediately turned off. Once the UVLO event disappears (UVLO off), the output transistor state follows the input state.

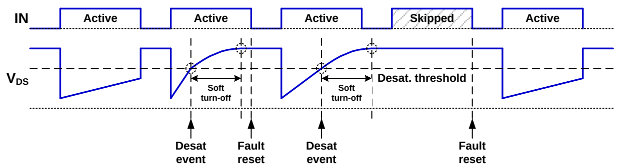


Note that due to internal ESD protections on the input pin (between GND and VDD), VDD could be self-supplied if a 5V signal is applied on the input while VDD pin is floating.

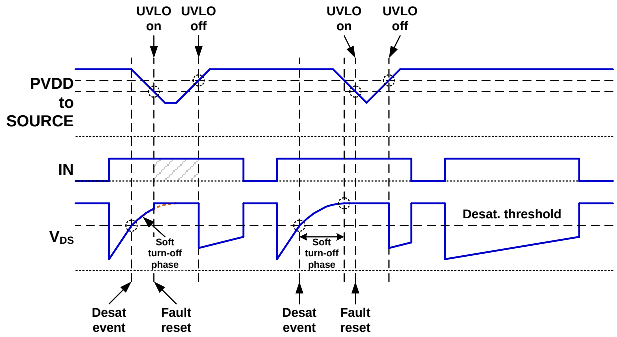
The recommended operation voltage for VDD is between 4.5V and 5.5V.

Desaturation (DESAT)

At each turn on of the output transistor, after a blanking time during which the desaturation protection is not allowed to react, the DRAIN to SOURCE voltage is continuously compared to an internal voltage threshold. For V_{DS} below this desaturation threshold, the output transistor still operates in its resistive regime (switch). If a desaturation event occurs after the blanking time, the output transistor is softly turned off and it remains off till the fault is cleared. If no UVLO event occurs during the soft shut down phase, the desaturation fault is cleared by the next falling edge of IN (rising edge for /IN) provided that the previous soft turn off is finished. If the soft shut down phase is not finished when the first falling edge arrives, the next input pulse is skipped and the output transistor remains off for one more period of the input signal.



If the UVLO is activated (V_{PVDD} too low) during a soft shut down phase, the UVLO protection takes over and immediately shuts down the output transistor. The activation of the UVLO protection also resets the desaturation fault, and the device can be turned on again as soon as the UVLO fault disappears.



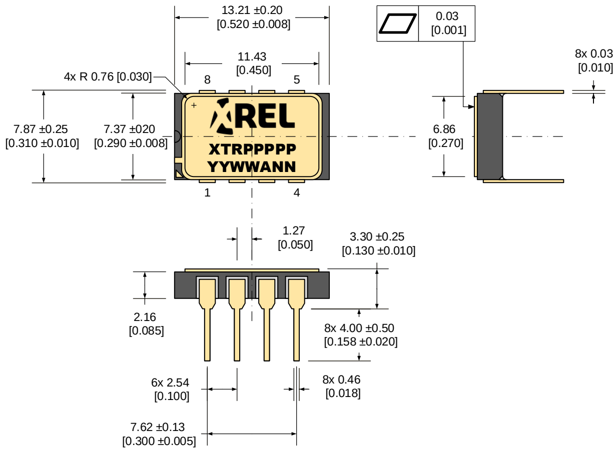
Robustness against over voltages

Though it is highly recommended to comply with the DC voltage limits of the part, in switching applications it is usually difficult to guarantee that aggressive spikes cannot occur in some cases due to fast dV/dt and di/dt. For these reasons, the XTR20410 products have been implemented in such a way that spikes of several volts over the recommended DC limits will not damage the device. For safe long-term reliability, these spikes should however be reduced by correct PCB layout, ground planes and clean decoupling.

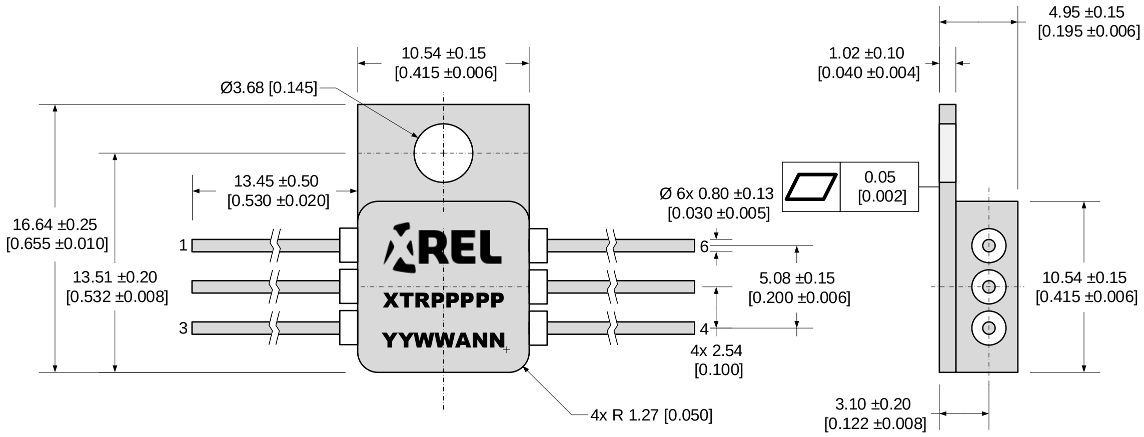
PACKAGE OUTLINES

Dimensions shown in mm [inches]. Tolerances ±0.13 mm [±0.005 in] unless otherwise specified.

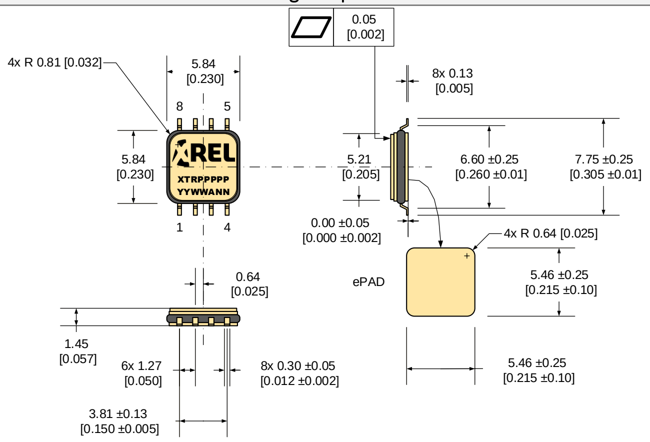
Ceramic Side Brazed Dual In-line DIP8



Ceramic Seal 6-lead TO-257



Ceramic Gull-wing Flat pack with ePad DFP8



Part Marking Convention	
Part Reference: XTRPPPPP	
XTR	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 15 = 2015).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

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