XTR20810

High Temperature 80V Low-Side N-Channel Power MOSFET with Driver

Rev 3 – August 2021 (DS-00558-14)

Data Sheet

PROTOTYPE

DIP8
XTR20811

FEATURES

- Operational beyond the -60°C to +230°C temperature range.
- Robust operation as low-side switch with drain spikes up to 90V.
- Standard Schmitt-trigger CMOS input
- Exists in inverting and non-inverting versions.
- Plug-and-play with any digital 5V output.
- Over current (desaturation) protection with soft turn-off.
- Under voltage lockout UVLO protection (MOSFET OFF).
- Low on-resistance:
  - XTR20811: 1700 mΩ @ 230°C
  - XTR20812: 780 mΩ @ 230°C
- Large peak current capabilities:
  - XTR20811: 1.6A @ 230°C
  - XTR20812: 3.8A @ 230°C
- Low On- and Off-time (<100 nsec @ 230°C).
- Monolithic design.
- Latch-up free.
- Ruggedized SMT and thru-hole packages.
- Also available as bare die.

APPLICATIONS

- Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
- DC/DC converters, motor drive, switching power supplies, switching control.

DESCRIPTION

XTR20810 is a family of extremely flexible power N-channel MOSFETs with integrated driver designed for extreme reliability and high temperature applications such as DC/DC converters, motor control and power switching. XTR20810 parts are intended to be used as low side switches. They can sustain drain spikes up to 100V. XTR20810 parts can be directly driven by any 5V digital output, making them fully plug-and-play devices, avoiding any time-consuming optimization of the matching network between driver and power transistor.

The XTR20810 family is composed of two different dies each with different output maximum current.

XTR20810 parts are robust to usual spikes associated with parasitic inductors and fast transients in switching applications.

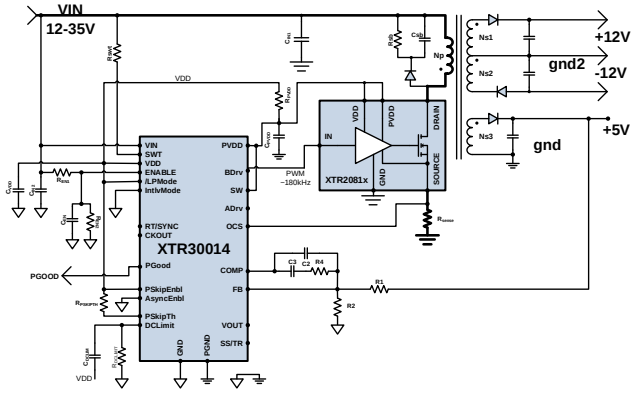
Features of XTR20810 family parts include UVLO (driver state is OFF whenever the supply is too low), desaturation protection of the output transistor with soft shut-down functionality and possibility to select inversion of control signal.

Full functionality is guaranteed from -60°C to +230°C, though operation well beyond this temperature range is achieved. XTR20810 family parts have been designed to reduce system cost and ease adoption by reducing the learning curve and providing smart and easy to use features. The

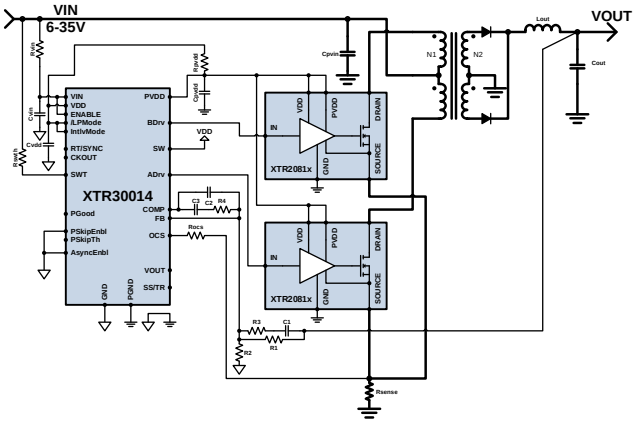
Parts from the XTR20810 family are available in ruggedized SMD and through hole hermetic packages, as well as bare die.

PRODUCT HIGHLIGHT

Isolated Flyback Converter



Push-pull DC-DC Converter



ORDERING INFORMATION

X	TR	20	810
Source : X=X-REL Semi	Process: TR=HiTemp, HiRel	Part family	Part number

Product Reference	Temperature Range	Package	Pin Count	Marking
XTR20811-BD	-60°C to +230°C	Bare die		
XTR20811-D	-60°C to +230°C	Ceramic side braze DIP	8	XTR20811
XTR20812-BD	-60°C to +230°C	Bare die		

Other packages and packaging configurations possible upon request. For some packages or packaging configurations, MOQ may apply.

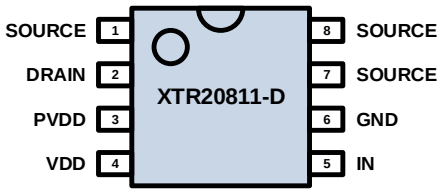
ABSOLUTE MAXIMUM RATINGS

Voltage on DRAIN to SOURCE	-1.5 to 90V
Voltage on IN and VDD to GND	-0.5 to 6.0V
Voltage on PVDD to SOURCE	-0.5 to 7.5V
Voltage on SOURCE to GND	-1 to 1V
Storage Temperature Range	-70°C to +230°C
Operating Junction Temperature Range	-70°C to +300°C
ESD Classification	1kV HBM MIL-STD-883

Caution: *Stresses beyond those listed in "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may permanently affect device reliability.*

PRODUCT VARIANTS

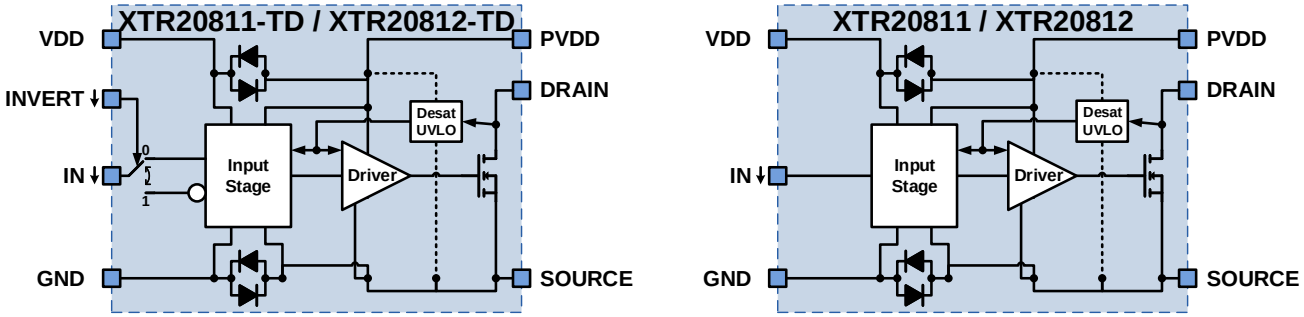
DIP8



AVAILABLE FUNCTIONALITIES FOR EACH PRODUCT VERSION

Functionality	Product Version
	XTR20811-D
Non-inverting input	✓
Inverting input	
Low power applications	✓
Mid power applications	
High power applications	

BLOCK DIAGRAM



Arrows aside pin names indicate that pin is internally pulled down.
Different functionalities are available depending upon packaging configuration. Carefully read sections "" and "Theory of Operation" in order to select the packaging option that best fits your needs.

PIN DESCRIPTION

XTR20811D		
Pin Number	Name	Description
1	SOURCE	Source of the power NMOS transistor.
2	DRAIN	Drain of the power NMOS transistor.
3	PVDD	Supply voltage of power section. Referenced to GND.
4	VDD	Supply voltage of the input section. Referenced to GND.
5	IN	Active HIGH input signal. Referenced to GND. Internally pulled down.
6	GND	Circuit ground.
7	SOURCE	Source of the power NMOS transistor.
8	SOURCE	Source of the power NMOS transistor.

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply voltage VDD to GND	4.5		5.5	V
Supply voltage PVDD to GND	4.5		5.5	V
SOURCE to GND voltage[1]	-0.3		0.3	V
Input voltage on IN (/IN) to GND	-0.3		VDD	V
DRAIN-SOURCE voltage (V_{DS})	-1		+80	V
Junction Temperature[2] T_j	-60		230	°C

[1] *This allows for a small drop on an optional external sense resistor to ground at the device's SOURCE.*
[2] *Operation beyond the specified temperature range is achieved with little degradation on electrical parameters.*

THERMAL CHARACTERISTICS

Parameter	Condition	Min	Typ	Max	Units
XTR20411A-D (Ceramic Side Brazed DIP8)					
Thermal Resistance: J-C $R_{Th\_J\text{-}C}$			30		°C/W
Thermal Resistance: J-A $R_{Th\_J\text{-}A}$			100		°C/W

ELECTRICAL SPECIFICATIONS XTR20811

Unless otherwise stated, VDD=PVDD=5V, GND=SOURCE, IN=0V, V_{DS}=20V, I_{DRAIN}=1A, -60°C<T_J<230°C.

Parameter	Condition	Min	Typ	Max	Units
Supply Current					
Static VDD+PVDD Supply Current I_{VDD_Sta}	IN=GND or VDD T_C=-60°C T_C=100°C T_C=230°C		 47 71 132		µA
Dynamic VDD+PVDD Supply Current I_{VDD_Dyn}	For Freq V_{IN}=1MHZ and duty cycle=50%		1.5		mA
Control INPUT					
Low Level Input Voltage V_{IL}			1.7		V
High Level Input Voltage V_{IH}			3.4		V
Input Current[1] I_{IN}	IN=VDD T_C=25°C T_C=230°C		 3 4		uA
Under Voltage Lockout (UVLO)					
V_{PVDD} Start Voltage[2] V_{UVLOR}	Rising PVDD threshold		4.2		V
V_{PVDD} Start-stop Hysteresis V_{UVLOH}			300		mV
Output Transistor					
Drain-Source Breakdown Voltage $V_{(BR)DSS}$	T_C=25°C	90	100		V
Off-State Drain Current I_{DSS}	For V_{IN}=GND and V_{DS}=80V. T_C=25°C T_C=230°C		 	 0.002 25	µA
Static ON Resistance R_{DSon}	I_{DRAIN}=1A T_C=25°C T_C=230°C		 840 1700		mΩ
Source-Drain Body Diode					
Continuous Forward Current I_{BD}		1			A
Forward Voltage V_{BD}	I_{DRAIN}=0.4A T_C=25°C T_C=230°C		 TBD TBD		V
Desaturation Protection (DESAT)					
Peak Drain Current I_{Dpeak}	300ns pulse, V_{DS}=40V T_C=-60°C T_C=230°C		 5.7 2.8		A
Desaturation Threshold V_{DESAT}			3.3		V
Blanking Time t_{BLANK}			400		ns
Soft Shut-down Time t_{SSD}	T_C=230°C		200		ns
Switching Time					
Delay ON Time [3] $t_{d(ON)}$	T_C=-60°C T_C=230°C		39 81		ns
Delay OFF Time[3] $t_{d(OFF)}$	T_C=-60°C T_C=230°C		46 100		ns

[1] *This current originates from an internal small pull-down source. Note that for the XTR20814, the /IN is also in pull down.*
[2] *Below this threshold, the output nMOS is OFF, for VDD rising.*
[3] *From 50% input signal to 50% VGS on the internal output transistor.*

ELECTRICAL SPECIFICATIONS XTR20812

Unless otherwise stated, VDD=5V, PVDD=5V, GND=SOURCE, IN=0V, VDS=40V, IDRAIN=1A, -60°C<Tj<230°C.

Parameter	Condition	Min	Typ	Max	Units
Supply Current					
Static VDD+PVDD Supply Current I_{VDD_Sta}	IN=GND or VDD T_C=-60°C T_C=100°C T_C=230°C		 47 71 132		µA
Dynamic VDD+PVDD Supply Current I_{VDD_Dyn}	For Freq V_{IN}=1MHZ and duty cycle=50%		3.5		mA
Control INPUT					
Low Level Input Voltage V_{IL}			1.7		V
High Level Input Voltage V_{IH}			3.4		V
Input current[1] I_{IN}	IN=VDD T_C=25°C T_C=230°C		 3 4		uA
Under Voltage Lockout (UVLO)					
V_{VDD} Start Voltage[2] V_{UVLOR}	Rising VDD threshold		4.2		V
V_{VDD} Start-stop Hysteresis V_{UVLOH}			300		mV
Output Transistor					
Drain-Source Breakdown Voltage $V_{(BR)DSS}$	T_C=25°C	90	100		V
Off-State Drain Current I_{DSS}	For V_{IN}=GND and V_{DS}=80V. T_C=25°C T_C=230°C			 0.005 60	µA
Static ON Resistance R_{DSon}	I_{DRAIN}=1A T_C=25°C T_C=230°C		 390 780		mΩ
Source-Drain Body Diode					
Continuous Forward Current I_{BD}		1			A
Forward Voltage V_{BD}	I_{DRAIN}=0.4A T_C=25°C T_C=230°C		 TBD TBD		V
Desaturation Protection (DESAT)					
Peak Drain Current I_{Dpeak}	300ns pulse, V_{DS}=40V T_C=-60°C T_C=230°C		 13.5 6.6		A
Desaturation Threshold V_{DESAT}			3.3		V
Blanking Time t_{BLANK}			400		ns
Soft Shut-down Time t_{SSD}	T_C=230°C		200		ns
Switching Time					
Delay ON Time [3] $t_{d(ON)}$	T_C=-60°C T_C=230°C		39 81		ns
Delay OFF Time[3] $t_{d(OFF)}$	T_C=-60°C T_C=230°C		46 100		ns

[1] *This current originates from an internal small pull-down source. Note that for the XTR20814, the /IN is also in pull down.*
[2] *Below this threshold, the output nMOS is OFF, for VDD rising.*
[3] *From 50% input signal to 50% VGS on the internal output transistor.*

THEORY OF OPERATION

Introduction

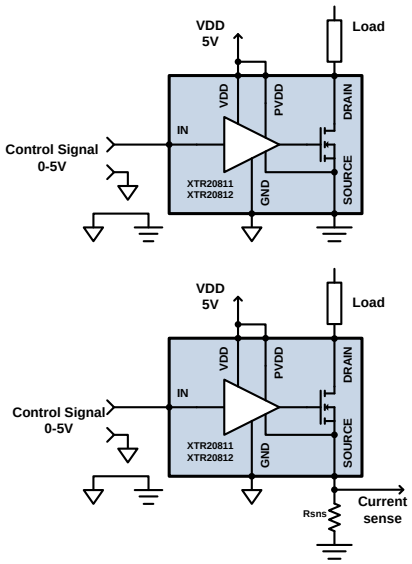
The XTR20810 is a family of 80V N-channel MOS transistors with integrated driver able to operate from -60°C to +230°C. Unique features of this product family make them an extremely flexible block when designing power switching applications using low-side switches.
The XTR20810 family includes several protection features for robust operation in switching applications.

- The circuit can tolerate transient spike voltages of up to 8V (3V above the operation limits) on VDD and PVDD.
- A desaturation protection is implemented in order to turn off the output nMOSFET whenever its Vds exceeds a defined threshold when the MOS is in on state.
- Soft shut-down is implemented to prevent high dV/dt and di/dt on the application when the desaturation protection is activated.
- An UVLO on VDD vs. GND guarantees that bellow a defined threshold, the output MOSFET is OFF.

Parts of the XTR20810 family are available with non-inverting and inverting (i.e. active low) inputs.

Low-side driver

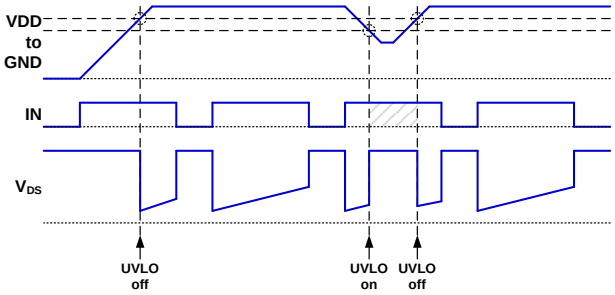
XTR20810 family is intended to be used as a low side driver in switching application. A small sense resistor with up to 300mV voltage drop can be added to its source if required. VDD and PVDD must be externally connected.
The use of power and signal ground planes connected on a unique point as well as proper layout techniques is highly recommended.
The drain current values mentioned in the electrical specification table are close to the saturation current of the driver's output nMOS. In practice, in switching application, it is not recommended to operate continuously close to this peak current level as the drain-source on-resistance is relatively high for such current levels. This would lead to a poor efficiency and an over-heat of the driver.



Protections

Under-voltage lockout (UVLO)

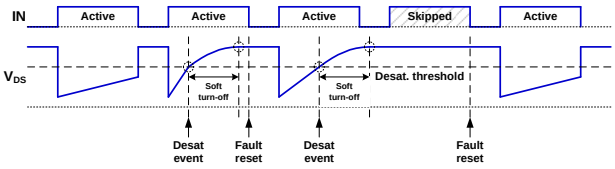
An UVLO detector continuously monitors the output stage supply voltage (PVDD to SOURCE). During power-up, the UVLO protection guarantees that the output transistor is in off state for V_{PVDD}-V_{SOURCE} below the V_{UVLOR} threshold for whichever state of IN (or /IN). Above the V_{UVLOR} threshold, the output MOSFET is controlled by the IN (or /IN) terminal).
In case the UVLO protection is activated (UVLO on) while the output transistor is ON, this latter is immediately turned off. Once the UVLO event disappears (UVLO off), the output transistor state follows the input state.



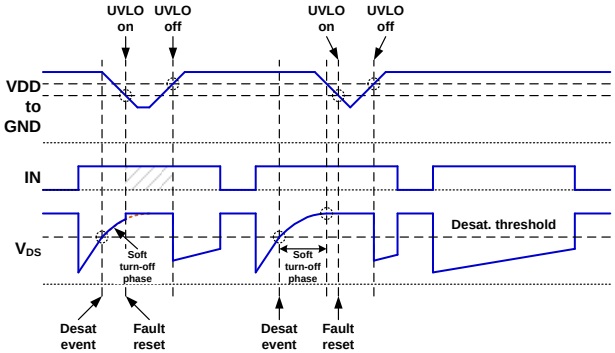
Note that due to internal ESD diode on the input pin (between GND and VDD), VDD could be self-supplied if a 5V signal is applied on the input while VDD pin is floating.
The recommended operation voltage for VDD is between 4.5V and 5.5V.

Desaturation (DESAT)

At each turn on of the output transistor, after a blanking time during which the desaturation protection is not allowed to react, the DRAIN to SOURCE voltage is continuously compared to an internal voltage threshold. For V_{DS} below this desaturation threshold, the output transistor still operates in its resistive regime (switch). If a desaturation event occurs after the blanking time, the output transistor is softly turned off and it remains off till the fault is cleared. If no UVLO event occurs during the soft shot down phase, the desaturation fault is cleared by the next falling edge of IN (rising edge for /IN) provided that the previous soft turn off is finished. If the soft shut down phase is not finished when the first falling edge arrives, the next input pulse is skipped and the output transistor remains off for one more period of the input signal.



If the UVLO is activated (V_{DD} too low) during a soft shut down phase, the UVLO protection takes over and immediately shuts down the output transistor. The activation of the UVLO protection also resets the desaturation fault, and the device can be turned on again as soon as the UVLO fault disappears.



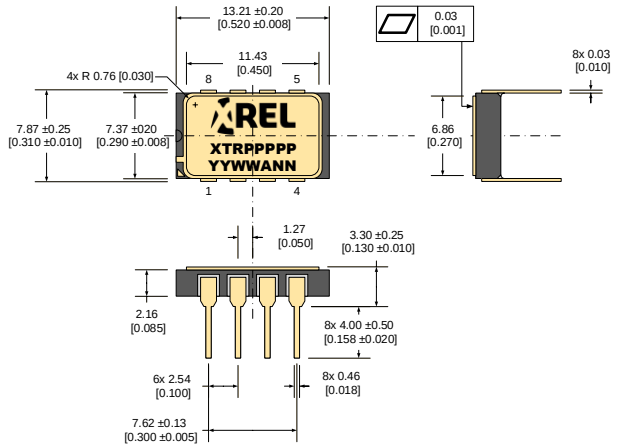
Robustness against over voltages

Though it is highly recommended to comply with the DC voltage limits of the part, in switching applications it is usually difficult to guarantee that aggressive spikes cannot occur in some cases due to fast dV/dt and di/dt. For these reasons, the XTR20810 products have been implemented in such a way that spikes of several volts over the recommended DC limits will not damage the device. For safe long-term reliability, these spikes should however be reduced by correct PCB layout, ground planes and clean decoupling.

PACKAGE OUTLINES

Dimensions shown in mm [inches]. Tolerances ±0.13 mm [±0.005 in] unless otherwise specified.

Ceramic Side Brazed Dual In-line DIP8



Part Marking Convention	
Part Reference: XTRPPPPPP	
XTR	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 15 = 2015).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

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90, Avenue Leon Blum 38100 Grenoble -– France
: +33 456 580 580
: support.XREL@easii-ic.com