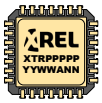
XTR25020

High Temperature Power Gate Driver

Rev 2 – August 2021 (DS-00662-14)

Data Sheet

PRODUCTION



LJCC28

XTR25021

FEATURES

- Operational beyond the -60°C to +230°C temperature range.
- Supply voltage from 4.5V to 35V.
- Integrated charge-pump inside pull-up driver allowing 100% duty-cycle PWM control signal.
- Internal 5V LDO regulator.
- Safe start-up of normally-on devices.
- Half bridge cross-conduction protection.
- Pull-up driver with 3A peak current and 1A continuous current capability.
- Pull-down driver with 3A peak current capability.
- On-chip active Miller clamp switch with 3A capability.
- Resistor-programmable Under voltage lockout (ULVO).
- Resistor-programmable over-current protection level (rail-to-rail, positive and negative current sense).
- Latch-up free.
- Ruggedized SMT packages. Also available as bare die.

APPLICATIONS

- Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole, Energy Conversion, Solar.
- Intelligent Power Modules (IPM).
- Power inverters and motor drives.
- Uninterruptible power supplies (UPS).
- Power conversion and power factor correction (PFC).
- DC/DC converters and switched mode power supplies (SMPS).

DESCRIPTION

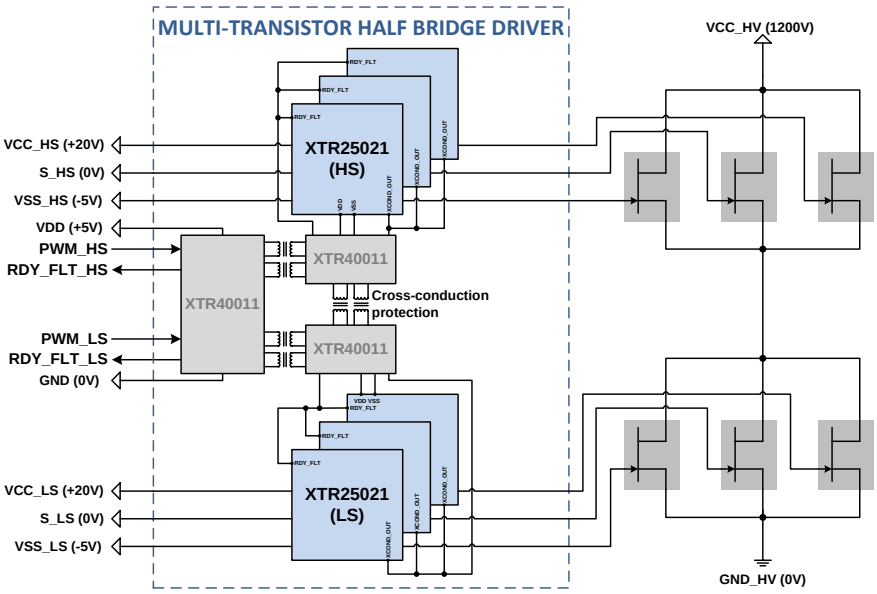
XTR25020 is a high-temperature, high reliability intelligent power transistor driver designed to provide a robust, reliable, compact and efficient solution for driving a large variety of high-temperature, high-voltage, and high-efficiency power transistors. XTR25020 is able to drive normally-On and normally-Off power transistors in Silicon Carbide (SiC), Gallium Nitride (GaN) and standard silicon, including JFETs, MOSFETs, BJTs, SJTs and MESFETs.

The XTR25020 includes one pull-up gate-drive-channel (PU_DR) capable of sourcing a typical 3A peak current and two pull-down gate-drive-channels capable of sinking a typical 3A peak current (PD_DR and PD_MC). The PD_DR channel is used for the effective turn-off of the power transistor, while PD_MC channel is used for Active Miller Clamping (AMC) function thanks to its internal gate level detection.

The circuit includes soft shut-down capability that slowly shuts down the power transistor in case of fault. The XTR25020 is able to detect failures due to over-current in the power switch or to UVLO detected on the power supply. In addition, safe start-up and cross-conduction protection are implemented to guarantee safe operation at system level.

The XTR25020 can be used to extend the drive capability of the XTR26020. It can also be used with the XTR40010 to drive multiple power transistors connected in parallel for very high-power applications.

PRODUCT HIGHLIGHT



ORDERING INFORMATION

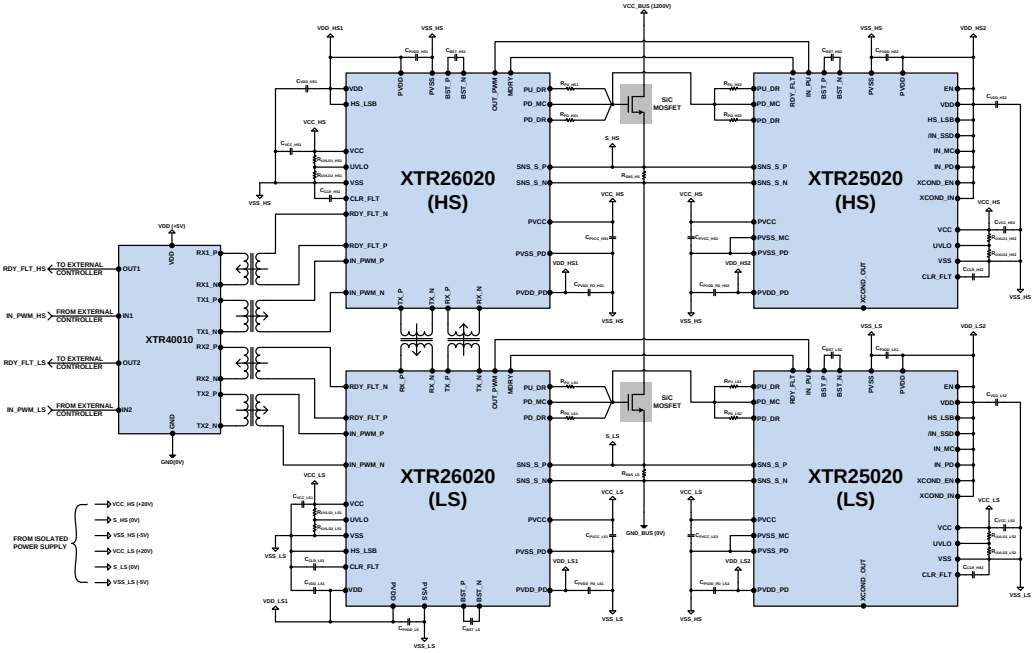
X	TR	25	020
Source: X = X-REL Semi	Process: TR = HiTemp, HiRel	Part family	Part number

Product Reference	Temperature Range	Package	Pin Count	Marking
XTR25020-BD	-60°C to +230°C	Bare die		
XTR25021-LJ	-60°C to +230°C	Ceramic LJCC28	28	XTR25021

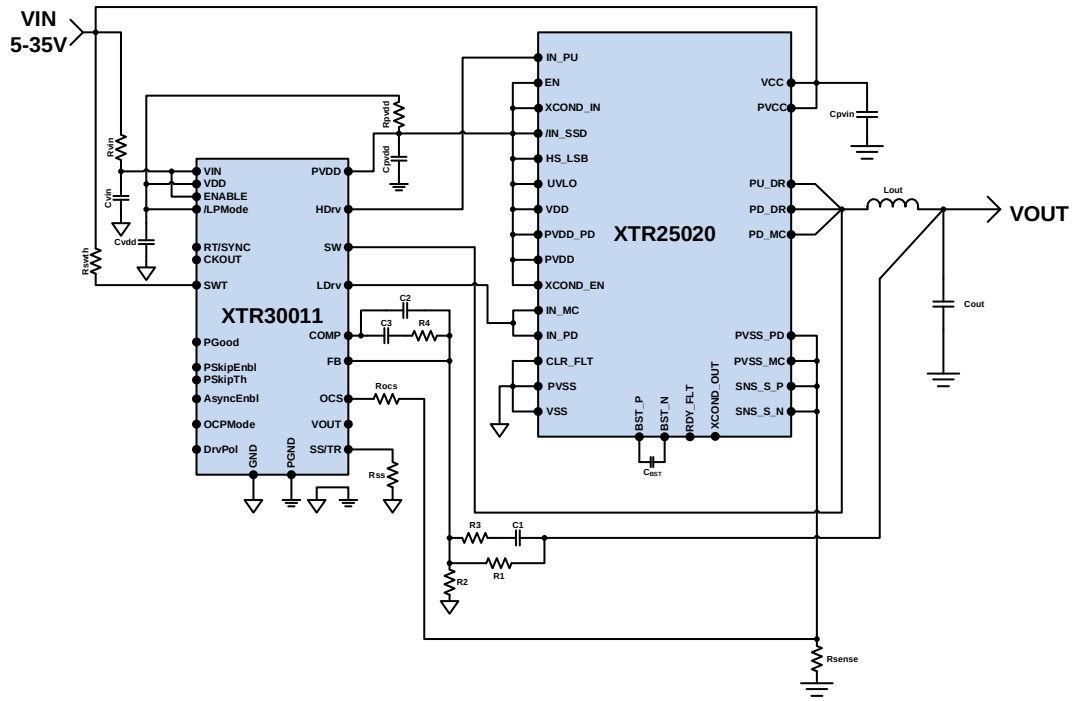
Other packages and packaging configurations possible upon request. For some packages or packaging configurations, MOQ may apply.

TYPICAL APPLICATIONS

SiC MOSFET Driving (6A peak current) to Reinforce XTR26020



Buck DC-DC Converter



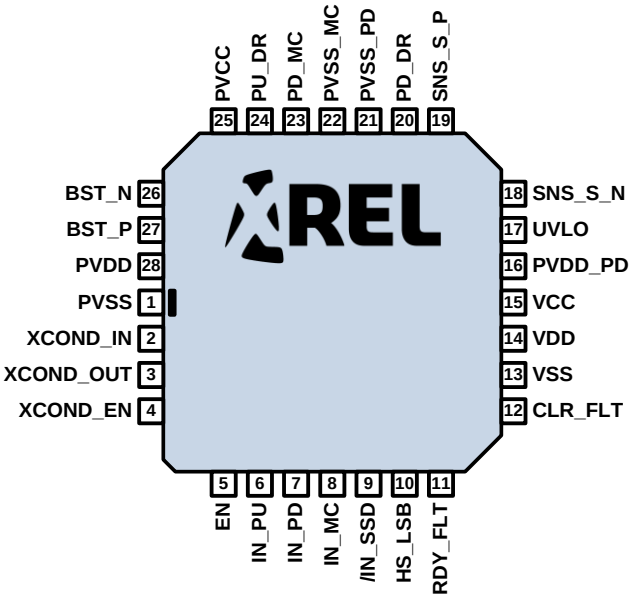
ABSOLUTE MAXIMUM RATINGS

Supply voltage	VCC_PVSS	-0.5V to 40V
	PVCC	PVSS-0.5V to VCC+0.5V
	PVDD-PVSS	-0.5V to 5.5V
	VDD, PVDD_PD	PVSS-0.5V to PVDD+0.5V
	VSS, PVSS_PD	PVSS-0.5V to PVSS+0.5V
Input pins	IN_PU, IN_PD, IN_MC, /IN_SSD, ULVO, HS_LSB, RDY_FLT, CLR_FLT, EN, XCOND_EN, XCOND_IN	PVSS-0.5V to PVDD+0.5V
	UVLO_SNS_S_P, SNS_S_N	PVSS-0.5V to VCC+0.5V
Outputs pins	PU_DR, PD_MC, PD_DR	PVSS-0.5V to VCC+0.5V
	RDY_FLT, XCOND_OUT	PVSS-0.5V to PVDD+0.5V
Sense pins	SNS_S_P or SNS_S_N	PVSS-0.5V to VCC+0.5V
	SNS_S_P versus SNS_S_N	-5V to +5V
Storage Temperature Range		-65°C to +230°C
Operating Junction Temperature Range		-65°C to +300°C
ESD Classification		1kV HBM MIL-STD-883

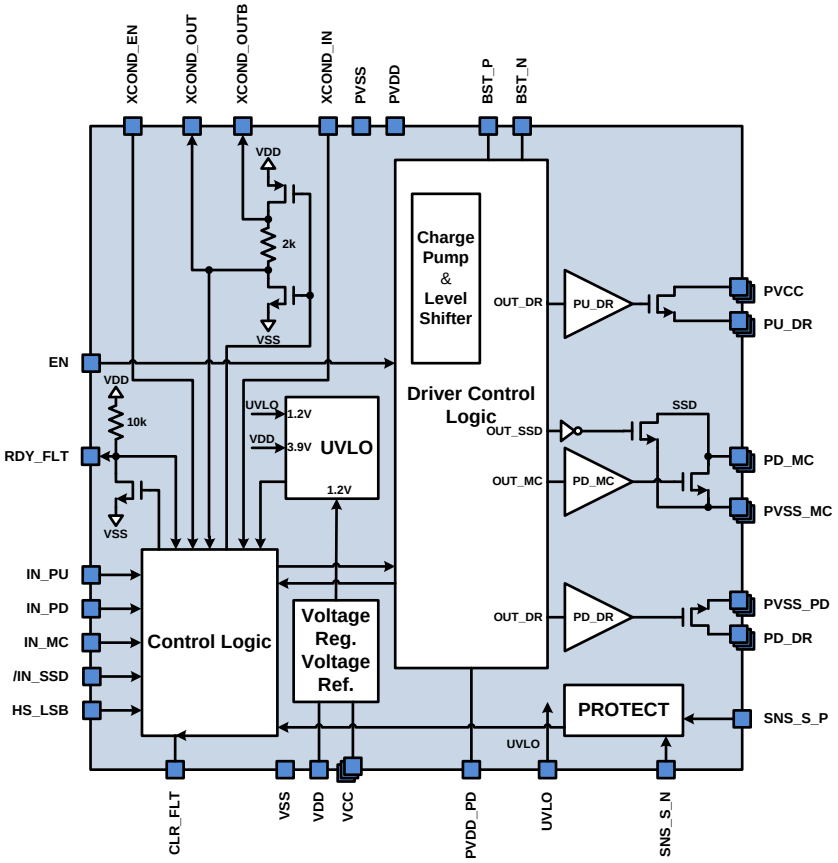
Caution: *Stresses beyond those listed in "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may permanently affect device reliability.*

PACKAGING

J-Formed Ceramic LJCC28
XTR25021-LJ



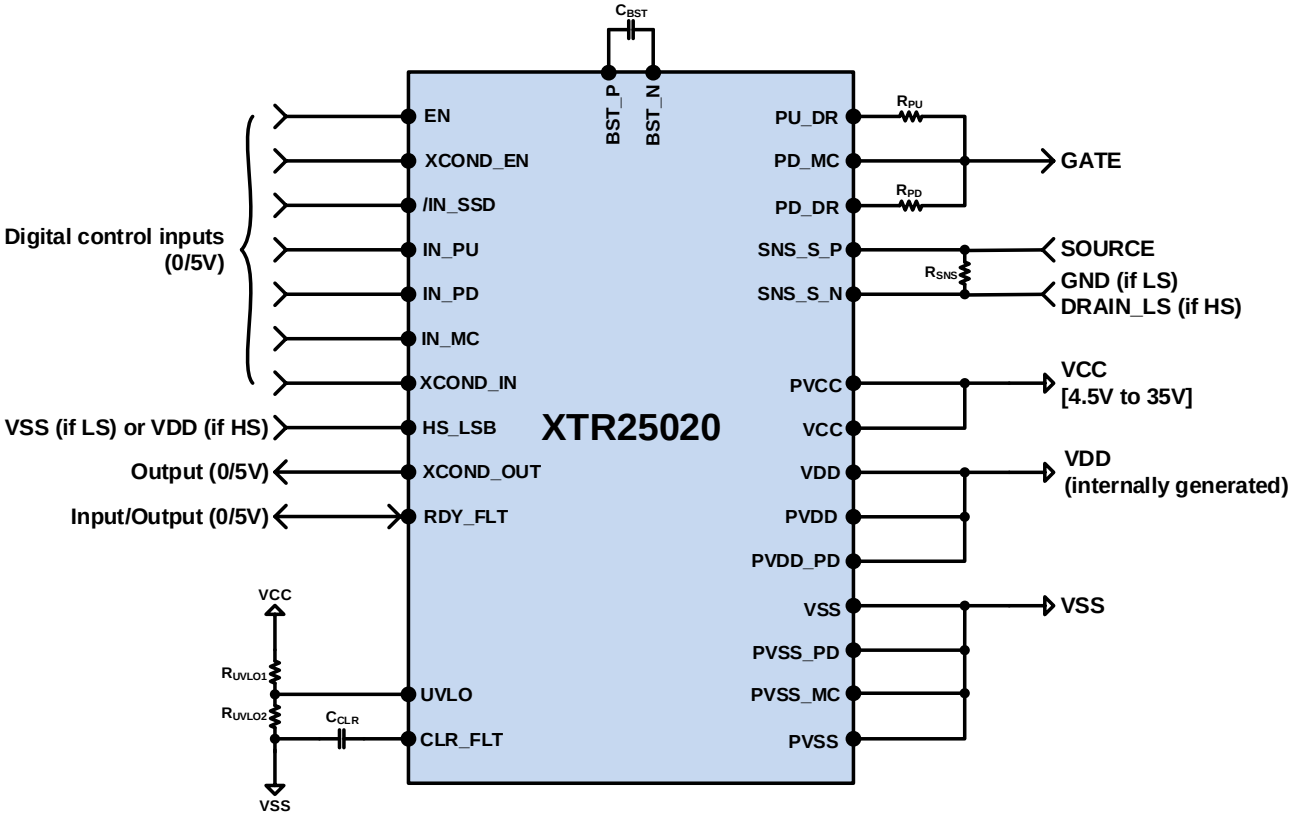
BLOCK DIAGRAM



PIN DESCRIPTION

Pin number	Name	Description
1	**PVSS**	Negative power supply. Connect to **VSS** through a local plane.
2	**XCOND_IN**	0/5V Schmitt triggered digital input versus **VSS** of the cross-conduction information between HS and LS. If this feature is not required, connect this pin to **VDD** (**HS_LSB** must be connected to **VDD** to be in slave mode).
3	**XCOND_OUT**	Open drain output versus **VSS** (for parallel connection of multiple XTR25020) of the cross-conduction information between HS and LS. If this feature is not required, leave this pin floating (**HS_LSB** must be connected to **VDD** to be in slave mode). If no parallel connection of multiple XTR25020 is needed, a second output **XCOND_OUTB** (only available in die form), can be shorted to **XCOND_OUT** to have a classical digital output instead of open drain.
4	**XCOND_EN**	0/5V Schmitt triggered digital input versus **VSS** to enable, when driven high, internal cross-conduction prevention between pull-up and pull-down drivers. When driven low, the outputs **PU_DR**, **PD_DR**, **PD_MC** are independently controlled by the inputs **IN_PU**, **IN_PD**, **IN_MC**, **/IN_SSD**, respectively.
5	**EN**	0/5V Schmitt triggered digital input versus **VSS** to enable, when driven high, the driver's outputs **PU_DR**, **PD_DR**, **PD_MC** are enabled. When driven low, the outputs **PU_DR** and **SSD** drivers are forced to high impedance mode and **PD_DR**, **PD_MC** are pulled-down to **PVSS_PD** and **PVSS_MC** respectively.
6	**IN_PU**	Active-high, Schmitt triggered digital input versus **VSS** for the pull-up driver PU_DR.
7	**IN_PD**	Active-high, Schmitt triggered digital input versus **VSS** for the pull-down driver PD_DR..
8	**IN_MC**	Active-high, Schmitt triggered digital input versus **VSS** for the Miller Clamp pull-down driver PD_MC.
9	**/IN_SSD**	Active-low, Schmitt triggered digital input versus **VSS** for Soft Shut-Down pull-down driver SSD.
10	**HS_LSB**	0/5V Schmitt triggered digital input versus **VSS** for driver operation selection as high-side (HS_LSB=1, slave mode) or low-side (HS_LSB=0, master mode).
11	**RDY_FLT**	Open drain input/output giving the "ready" (when it is high) or "fault" (when it is low) information of the circuit. When the XTR25020 is used together with the XTR26020 (or other XTR25020 circuits) this pin must be connected to **MRDY** pin of the XTR26020 (or to **RDY_FLT** pin of XTR25020). Indeed, this connection allows to synchronize "ready" or "fault" states between the two circuits to guarantee safe operation. If the XTR25020 is used alone this pin must be kept not connected.
12	**CLR_FLT**	Connect a capacitor between this pin and **VSS** to define the clear fault time-out. See section Theory of Operation for more details about the use of this pin.
13	**VSS**	Most negative supply voltage of the driver (its value depends on the power transistor to be driven). Connect to the reference **VSS** ground plane of the circuit.
14	**VDD**	5V supply voltage versus **VSS** generated by the internal LDO and supplying all logic except the output stage of the drivers and the transceiver. Connect to a local **VDD** plane.
15	**VCC**	Positive supply voltage of the driver. This voltage must be larger than or equal to the positive supply of the output pull up driver (PVCC). Connect to **VCC** plane.
16	**PVDD_PD**	Top plate of decoupling capacitor of the pull-down (PD_DR) pre-driver. Connect to **VDD** plane.
17	**UVLO**	Sense node through external resistor divider for the UVLO on **VCC** pin versus **VSS**. Voltage on this node is compared to an internal reference of 1.2V versus **VSS**. If this feature is not required, connect this pin to **VDD** via a pull-up resistor in the range of 100kΩ.
18	**SNS_S_N**	Negative sense pin of the **SOURCE** terminal of the power transistor (over-current detection). Connect it to the bottom of the source sense resistor using a Kelvin electrical connection. If the sense current feature is not required, this pin must be shorted with **SNS_S_P** and connected to **VDD** plane.
19	**SNS_S_P**	Positive sense pin of the **SOURCE** terminal of the power switch source (over-current detection). Connect it to the SOURCE of the switching device, on the top of the sense resistor, using a Kelvin electrical connection. If the sense current feature is not required, this pin must be shorted with **SNS_S_N** and connected to **VDD** plane.
20	**PD_DR**	Output of the pull-down driver PD_DR with a typical 3A peak drive current.
21	**PVSS_PD**	Power **VSS** of the PD_DR driver. Connect to **VSS** plane.
22	**PVSS_MC**	Power **VSS** of the PD_MC driver. Connect to **VSS** plane.
23	**PD_MC**	Output of the Miller Clamp pull-down driver with a typical 3A peak drive current.
24	**PU_DR**	Output of the pull-up driver PU_DR with typical 3A peak drive current.
25	**PVCC**	Positive supply voltage of PU_DR driver. Connect to local power **PVCC** plane if different than VCC. Otherwise, connect to VCC plane.
26	**BST_N**	Negative terminal of the bootstrap capacitor of the PU_DR driver.
27	**BST_P**	Positive terminal of the bootstrap capacitor of the PU_DR driver.
28	**PVDD**	5V supply voltage versus **PVSS** supplying the transceiver and the low voltage IO ring. Connect to a local power **VDD** plane.

RECOMMENDED OPERATING CONDITIONS

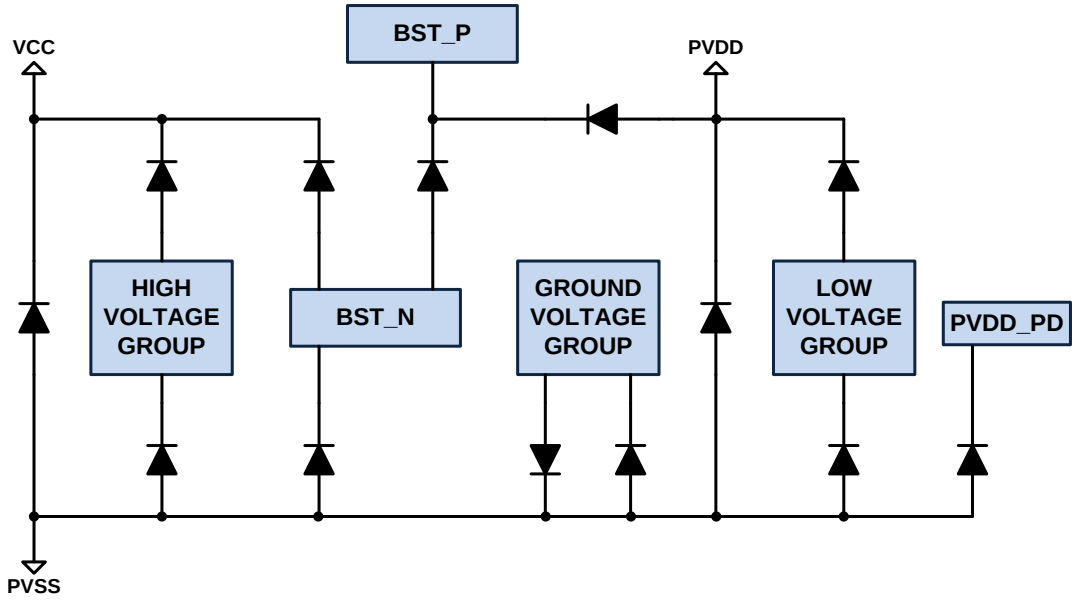


Parameter	Min	Typ	Max	Units
High voltage power supply VCC-VSS[1]	4.5		35	V
High voltage inputs: SNS_S_N, SNS_S_P	VSS		VCC	
High voltage outputs : PU_DR, PD_DR, PD_MC	VSS		VCC	
Low voltage power supply VDD-VSS (generated from internal voltage regulator)	4.5		5.5	V
Low voltage inputs: EN, XCOND_EN, /IN_SSD, IN_PU, IN_PD, IN_MC, HS_LSB, UVLO, RDY_FLT, XCOND_IN	VSS		VDD	
Low voltage outputs: XCOND_OUT, RDY_FLT	VSS		VDD	
Junction Temperature[2] T_j	-60		230	°C

[1]For VCC-VSS≤5.5V, VDD must be shorted to VCC.
[2] Operation beyond the specified temperature range is achieved.

ESD CLAMPING SCHEME

Pin Groups	Pins
High voltage power supply	VCC-PVSS
High voltage group	PD_DR, PU_DR, PVCC, SNS_S_N, SNS_S_P, PD_MC, UVLO
Low voltage power supply	PVDD-PVSS
Low voltage group	VDD, RDY_FLT, IN_PU, IN_PD, /IN_SSD, IN_MC, CLR_FLT, HS_LSB, XCOND_IN, XCOND_OUT, XCOND_EN, EN
Bootstrap voltages	BST_ N, BST _P
Power VDD voltage	PVDD_PD
Ground voltage group	VSS, PVSS_PD, PVSS_MC



ELECTRICAL SPECIFICATIONS

Unless otherwise stated, specification applies for VCC-VSS=25V and -60°C≤T_J≤230°C.

Parameter	Condition	Min	Typ	Max	Units
Supply Voltage					
VCC-VSS[1]		4.5		35	V
Source of power transistor		VSS		VCC	V
Quiescent current consumption	EN=0		1		mA
Fault mode current consumption	XCOND_EN=1 (IN_PU, IN_PD, IN_MC low, and /IN_SSD high)		3		mA
Ready mode current consumption	XCOND_EN=1 (IN_PU, IN_PD, IN_MC low, and /IN_SSD high)		5		mA
Functional mode current consumption	In ready mode with 200kHz, 50% duty cycle signal on IN_PU, XCOND_EN=1, (IN_PD, IN_MC and /IN_SSD high) 1nF output capacitor on driver output (PU_DR, PD_DR, PD_MC), and HS_LSB high (slave mode).		10		mA
Internal Linear Voltage Regulator (LDO)					
Total accuracy	7V≤VCC-VSS≤35V, 1mA≤I_{LOAD}≤50mA	-5		+5	%
	5.5V≤VCC-VSS≤7V, 1mA≤I_{LOAD}≤30mA	-10		+5	%
Load regulation	VCC-VSS=20V, 1mA≤I_{LOAD}≤50mA		-1		mV/mA
Line regulation	7V≤VCC-VSS≤35V, I_{LOAD}=25mA		±1		%
Output current	7V≤VCC-VSS≤35V	0		50	mA
	5.5V<VCC-VSS<7V	0		30	mA
Output load capacitance	0.01Ω≤ESR≤0.1Ω	0.33	1	3.3	µF
UVLO					
UVLO hysteresis			10		%
Internal comparator reference vs. VSS (for UVLO on VCC)		1.14	1.2	1.26	V
Internal comparator reference vs. VSS (for UVLO on VDD)			3.9		V
Allowed input current on UVLO pin	UVLO pin when clamping at about 5.7V versus VSS.			1	mA
Leakage current on UVLO pin	1.14V≤V_{UVLO}≤1.26V			1	µA
Over-current protection between SNS_S_P and SNS_S_N					
Sense threshold voltage			100		mV
Sense threshold voltage accuracy		-20		+20	%
Sense threshold voltage hysteresis			10		%
Driver					
Propagation delay/channel	from IN_PU, IN_PD, IN_MC to driver outputs (PU_DR, PD_DR, PD_MC)		200		ns
Rise time	1nF output capacitor per driver channel		15		ns
Fall time	1nF output capacitor per driver channel		15		ns
Minimum ON time t_{ON_min}	external cross-conduction protection active	1			µs
	without external cross-conduction protection	0.5			µs
Minimum OFF time t_{OFF_min}	external cross-conduction protection active	1			µs
	without external cross-conduction protection	0.5			µs
Peak output current of PU_DR driver			3		A
Continuous output current of PU_DR	VCC-VSS=7V[2]		1		
Peak output current of PD_DR driver			3		
Peak output current of PD_MC driver			3		
Soft-shutdown transistor R_{ON}		50	100	150	Ω
Control Logic					
High-Level Input Voltage **V_{IH}**	Schmitt triggered inputs (EN, XCOND_EN, /IN_SSD, IN_PU, IN_PD, IN_MC, HS_LSB, XCOND_IN)	4			V
Low-Level Input Voltage **V_{IL}**				1	
Schmitt triggered input hysteresis			2		
Blanking time **t_{BLANK}**	Internally fixed	0.2	0.4	0.8	µs
Clear fault time **t_{CLR_FLT}**	Externally set with C_{CLR}=1nF		30		µs
Miller Clamp activation threshold		0.7	1	1.45	V

[1] For VCC-VSS≤5.5V, pins VDD, PVDD, and PVDD_PD must be shorted to VCC.

[2] Care must be taken with the temperature increase due to the power dissipated in the circuit.

THEORY OF OPERATION

Introduction

XTR25020 is a high-temperature, high reliability intelligent power transistor driver integrated circuit specifically designed to drive normally-On as well as normally-Off Silicon Carbide (SiC), Gallium Nitride (GaN) and standard silicon power transistors, such as MOSFETs, JFETs, SJTs, BJTs, MESFETs and HEMTs. The XTR25020's main features are:

- Internal 5V linear regulator.
- Cross-conduction protection between high-side and low-side power drivers, which can be disabled for free-control of the three outputs PU_DR, PD_DR, PD_MC through their respective inputs IN_PU, IN_PD, IN_MC.
- Pull-up gate-drive-channel (PU_DR) capable of sourcing a peak current of 3A.
- Pull-down gate-drive-channel (PD_DR) capable of sinking 3A peak current.
- Active Miller clamp (AMC) on PD_MC channel with 3A current capability.
- On-chip soft-shut-down (SSD) capability that slowly shuts down on the PD_MC output the power transistor in case of fault.
- Rail-to-rail, positive and negative over-current detection on the source terminals of the power transistor.
- Safe start-up through UVLO (Under Voltage Lockout) function.

Truth Table

INPUTS						OUTPUTS			
EN	XCOND_EN	/IN_SSD	IN_PU	IN_PD	IN_MC	SSD[1]	PU_DR	PD_DR	PD_MC
0	X	X	X	X	X	HZ	HZ	PVSS	PVSS
1	0	0/1	0/1	0/1	0/1	PVSS/HZ	HZ/PVCC	HZ/PVSS	HZ/PVSS
1	1	0	X	X	0	PVSS	HZ	HZ	HZ
1	1	0	X	X	1	PVSS	HZ	HZ	PVSS[2]
1	1	1	1	X	X	HZ	PVCC	HZ	HZ
1	1	1	0	0	X	HZ	HZ	HZ	HZ
1	1	1	0	1	0	HZ	HZ	PVSS	HZ
1	1	1	0	1	1	HZ	HZ	PVSS	PVSS[2]

[1] The drain of the SDD transistor is connected on chip to PD_MC pin. For more clarity, it is added as an output in the truth table to show the state of the SSD transistor resulting from the state of the /IN_SSD input.

[2] The Miller clamp transistor is activated when node PD_MC goes under 1V. For PD_MC above 1V, the miller clamp transistor remains inactive. This ensures that the power transistor being driven is properly turned-off before gate clamping.

Operation Modes

XCOND_EN="0"

In this mode, as soon as the power supply is present in the circuit and the EN input is high, the outputs PU_DR, PD_DR, and PD_MC, follow with no condition ("0" corresponds to HZ, and "1" corresponds to PVCC for PU and to PVSS for PD) their respective inputs IN_PU, IN_PD, and IN_MC. For the soft-shut-down (SSD) driver, which has a common output PD_MC with the Miller Clamp driver, the output is inversed ("0" corresponds to PVSS, and "1" corresponds to HZ) versus its corresponding input /IN_SSD. If the circuit is in startup phase (not ready) or a "FAULT" state is detected, due to UVLO or over-current, the fault is reported via RDY_FLT output without any action on the outputs of the driver.

XCOND_EN="1"

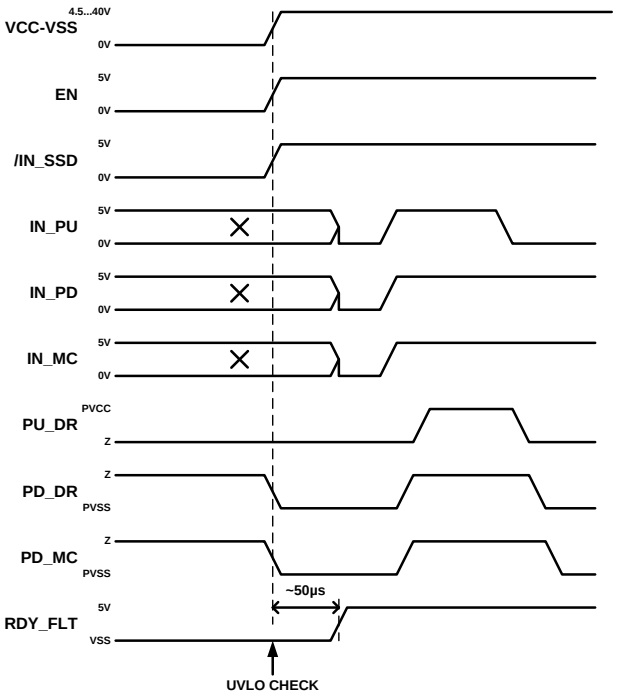
Startup phase

The startup phase is initialized by the turn on of the power supplies of the circuit VCC and VSS. After having enough voltage on the LDO output (around 3V for the logic to be operational), the PD_DR and PD_MC outputs are pulled-down to PVSS. This is mandatory to guarantee the charge of the bootstrap capacitor during the startup phase. The following checks are done during the startup phase:

- The UVLO on VCC checks if the power supply value is higher than the externally fixed threshold.
- An internal UVLO on VDD checks if VDD is higher than approximately 4V.
- The output gate is checked if it is close to VSS.

If all those checks are okay, an internal counter with a delay of 50µs is started. This delay secures the correct turn-on of the internal voltage reference. During the startup phase the PD_DR and PD_MC drivers outputs are activated for safe normally on start-up, and the input PWM is blanked (If a PWM signal is received, it is not transferred to the driver outputs). At the end of the counter, the signal RDY_FLT goes to "1" (through internal pull-down resistor of 10kΩ). The circuit enters into the functional phase: if a PWM signal is received, it is transferred to the driver outputs.

Hereafter is the timing diagram showing the operation of the circuit in startup phase (XCOND_EN="1").

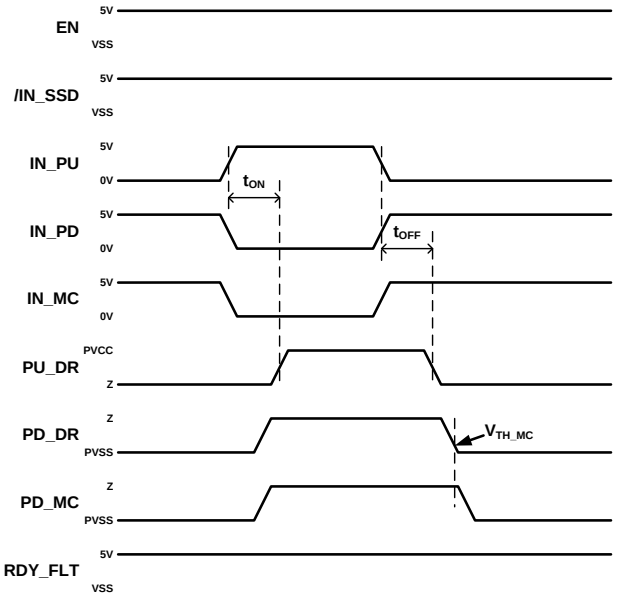


Functional phase

The functional phase starts when the RDY_FLT output flags a "1". In this phase, the circuit is ready to receive the input signals from the user (PWM controller, microcontroller…).

If the EN and SSD inputs are high, the input signals are transferred after the propagation delays (t_{ON} and t_{OFF}) from the inputs IN_PU, IN_PD, and IN_MC, to their respective outputs PU_DR, PD_DR, PD_MC. A minimum non-overlapping (of about 30ns) is guaranteed between PU and PD/MC drivers (PU is master). When the IN_PU signal turns-off, the PU_DR is

turned off after the propagation delay t_{OFF} and if the IN_PD is high, the PD_DR driver is turned-on after the non-overlapping delay. Then, the PD_MC driver is turned-on after checking the output gate to be close to VSS (V_{GATE}<V_{TH_MC}≈1V). Note that during this normal operation mode, the soft shut down pull down transistor is always OFF provided that the input /IN_SSD is high.



Fault phase

The fault phase is initialized if at least one of the following signals flags an error:

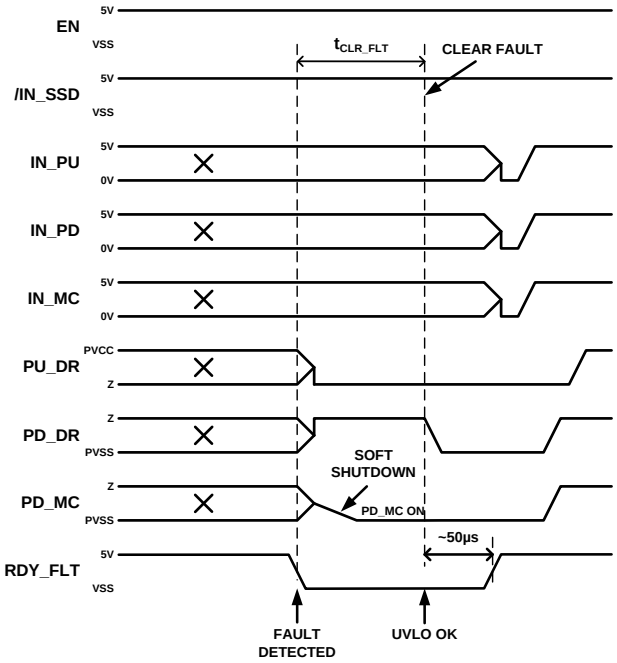
- UVLO on VCC supply versus VSS.
- UVLO on VDD versus VSS
- Over-current detection on the source or gate terminal of the power transistor that persists for a time longer than an internal blanking time of about 450ns.

Immediately after fault detection, RDY_FLT goes to "0". Then, regardless the states of the inputs, the PU_DR, PD_DR, and PD_MC drivers are turned-off and the Soft Shut-Down driver is turned-on. This slowly turns-off the power transistor via the PD_MC output, which should be directly connected to the gate or base terminal, to avoid high dV/dt and high turn-off current. After checking the output gate to be close to VSS (V_{GATE}<V_{TH_MC}≈1V), the PD_MC driver is turned-on to strongly maintain the off state.
To get out from this state, two alternatives are possible:

- If the CLR_FLT pin is shorted to VSS, a power supply reset is necessary to clear the FAULT and initialize a new startup phase.
- If a capacitor C_{CLR} is connected between CLR_FLT pin and VSS, a new startup phase starts after a time-out of t_{CLR_FLT} given by:

$$t_{CLR\_FLT}=30k\Omega*C_{CLR}$$

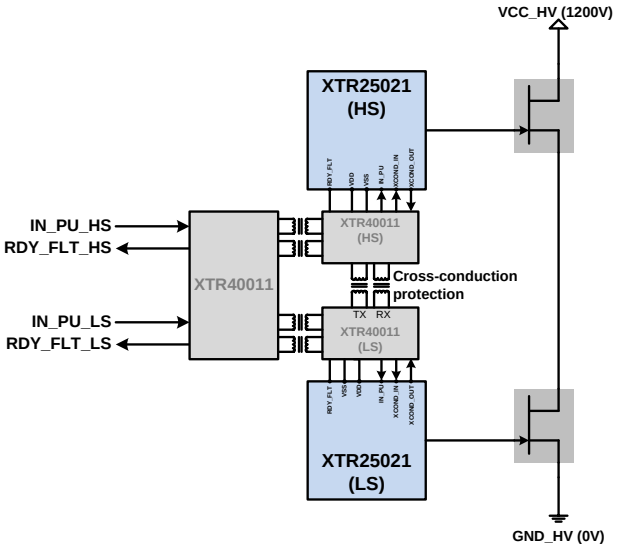
If no capacitor is connected the clear fault time out will be given by the parasitic capacitance on pin CLR_FLT (few pF) times 30kΩ.
Note that at the first startup of the circuit, when VCC is turning ON, the UVLOs faults are automatically cleared once all supplies are above the defined thresholds. No clear fault event is required in order to operate normally the circuit. However, during operation, if an UVLO event occurs, a clear fault event is required in order to reset the circuit.



Functional Features

Cross conduction protection

The cross-conduction protection has been implemented to prevent short-circuiting the high voltage power supply through the High Side (HS) and Low Side (LS) power transistors of a half bridge (see figure below).



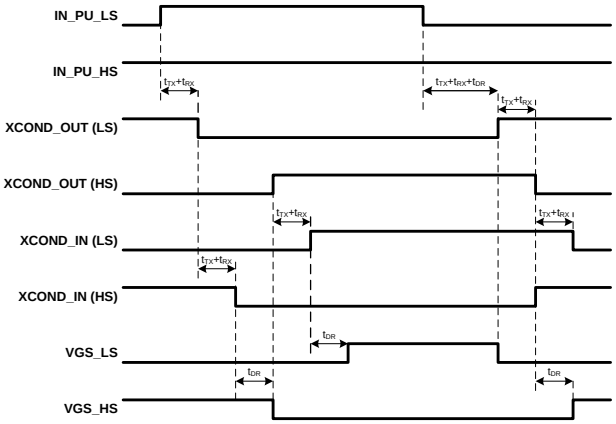
This is achieved through a bidirectional isolated data communication between the XTR25020 set as a HS driver and the XTR25020 set as a LS driver of the half bridge via 2 XTR40010 isolated transceivers. The XTR25020 LS is the master (HS_LSB input low) and the XTR25020 HS is the slave (HS_LSB input high). The operation of the cross-conduction protection is shown in the following timing diagrams for two states of the IN_PU_HS input:

- IN_PU_HS set to a permanent "1":
  When the IN_PU_LS signal turns-on, after t_{TX}+t_{RX} (t_{TX}≈20ns+50ns of Jitter and t_{RX}≈60ns) delay the XCOND_OUT (LS) sends a "0" to the XCOND_IN (HS) which receives it after t_{TX}+t_{RX} forcing the HS to turn-off its PU_DR and to turns-on its PD_DR and then its PD_MC. This takes t_{DR} delay (t_{DR} is composed of the propagation delay through the driver buffer and the rise or fall time). After checking that the gate of the HS power transistor is nearly discharged (V_{GATE}<1V) using the PD_MC pin, the XCOND_OUT (HS) sends a "1" to the XCOND_IN (LS) telling that the HS is off and that the LS can safely turn-on

after a delay of $t_{TX}+t_{RX}$. Then, the VGS_LS is turned-on after t_{DR} delay. Hence, the total turn-off/turn-on delays of the HS/LS are given by:

$$t_{OFF\_HS}=2*(t_{TX}+t_{RX})+t_{DR}$$
$$t_{ON\_LS}=3*(t_{TX}+t_{RX})+2*t_{DR}$$

These delays include a non-overlapping delay of $t_{TX}+t_{RX}+t_{DR}$.



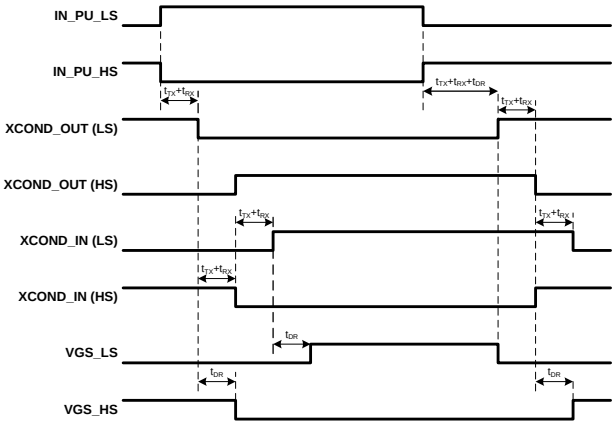
When the IN_PU_LS signal turns-off, the LS turns-off its PU_DR and turns-on its PD_DR and then its PD_MC after a delay of $t_{TX}+t_{RX}+t_{DR}$. After checking that the gate of the LS power transistor is nearly discharged (V_{GATE}<1V) using the PD_MC pin, the XCOND_OUT (LS) sends a "1" to the XCOND_IN (HS) telling that the HS can turn-on after $t_{TX}+t_{RX}$ delay. Finally, the high side turns-on its PU_DR after t_{DR} delay. Hence, the total turn-off/turn-on delays of the LS/HS are given by:

$$t_{OFF\_LS}=t_{TX}+t_{RX}+t_{DR}$$
$$t_{ON\_HS}=2*(t_{TX}+t_{RX})+2*t_{DR}$$

These delays include a non-overlapping delay of $t_{TX}+t_{RX}+t_{DR}$.

In this case, where IN_PU_HS is set to a permanent "1", the pulse transformer that transfers the PWM signal to the XTR25020 HS is not necessary.

- IN_PU_HS set to $\overline{\text{IN\_PU\_LS}}$ (this could be achieved easily by shorting PU_IN_HS to PU_IN_LS and setting POL_TX of the XTR40010_HS to "1"):

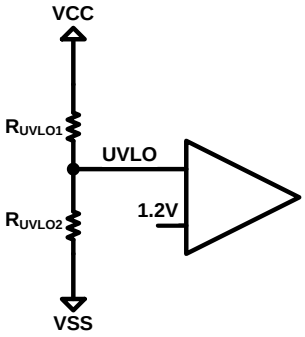


Using complementary signal on IN_PU_LS and IN_PU_HS, the same operation is obtained as with a permanent "1" on IN_PU_HS except that the propagation delay for turn-on from IN_PU_LS to VGS_LS can be reduced by $t_{TX}+t_{RX}$. This allows to have the same turn-on delay for HS and LS ($t_{ON\_HS}=t_{ON\_LS}$).

The cross-conduction protection can be disabled if the user wishes to manage it externally. To do this both the HS and LS drivers must be set as slave (HS_LSB pin connected to VDD) and the XCOND_IN must receive a "1" (XCOND_OUT must be kept floating).

Under Voltage Lockout (UVLO) operation

The UVLO block checks the value of the external power supply (VCC-VSS), and the internally generated VDD supply (5V versus VSS). A fraction of VDD value is compared to an internal reference of 1.2V versus VSS and an UVLO_VDD flag is set to "1" when the VDD reaches about 3.9V. For the external power supplies, the UVLO block compares an externally fixed threshold through a resistor divider to an internal reference of 1.2V versus VSS:



To simplify the equation for the computation of the UVLO threshold voltage V_{TH_UVLO}, we consider VSS=0V. The V_{TH_UVLO} is obtained in terms of R_{UVLO1} and R_{UVLO2} as follows:

$$V_{TH\_UVLO}=\frac{R_{UVLO1}+R_{UVLO2}}{R_{UVLO2}}\cdot 1.2V$$

The current that can be tolerated (100µA for example, it must be high enough compared to leakage current) in the resistor divider can give the value of R_{UVLO2} using:

$$R_{UVLO2}=\frac{1.2V}{100\mu A}=12k\Omega$$

Then, for V_{TH_UVLO}=15V, the R_{UVLO1} is obtained:

$$R_{UVLO1}=\left(\frac{V_{TH\_UVLO}}{1.2}-1\right)\cdot R_{UVLO2}=138k\Omega$$

The UVLO pin is internally clamped to VDD+0.7V with a maximum current sink of 1mA.
The UVLO thresholds on VDD and VCC have an internal hysteresis of about 10% when the power supply goes down after being up and higher than the UVLO thresholds defined above.
If this feature is not used, the UVLO pin must be pulled-up to VDD.

Over-current detection

The source or gate current is permanently measured using the differential voltage between SNS_S_P and SNS_S_N created by the sense resistor R_{SNS} and compared to an internal voltage reference of about 100mV. In the case of damage on the poser transistor or due to short-circuit in a half-bridge, the current should be higher than the fixed threshold indicating source failure for the circuit. The source or gate over-current threshold I_{TH} is given by:

$$I_{TH}=\frac{100mV}{R_{SNS}}$$

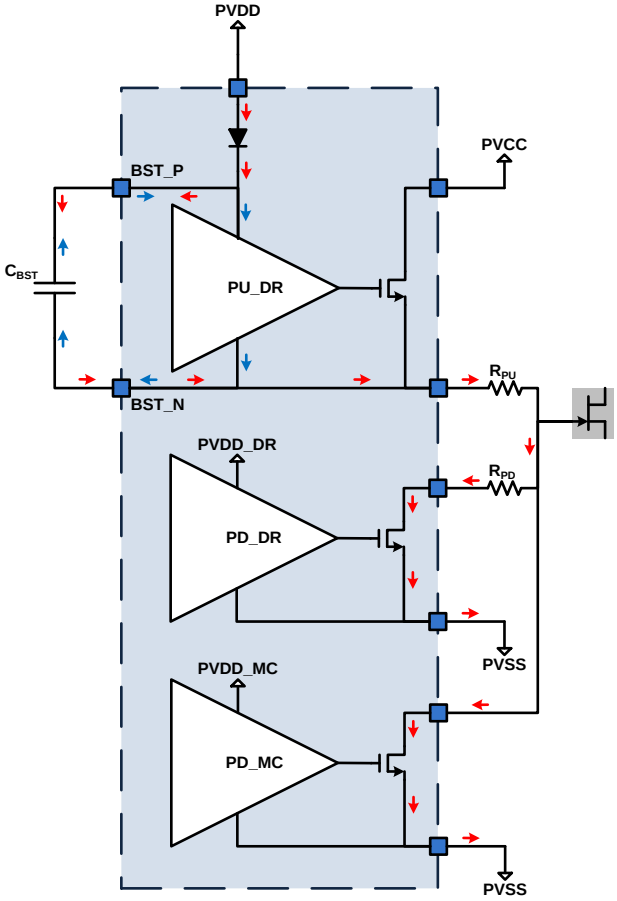
The current sense is functional at any common-mode voltage between VCC and VSS (rail-to-rail) and for both positive and negative current flowing to or from the source of the power transistor. In order to avoid false over-current detections due to spikes during the switching of the driver outputs, an internal blanking time of about 400ns is implemented.

The current sense comparator can also be used for any other protection purpose such as gate/base current sense for fatigue detection or to implement a thermal shut-down with external temperature sensor.

Bootstrap capacitors

The bootstrap capacitor value can be selected taking into account two conditions:

- The bootstrap capacitor C_{BST} is discharged in the PU_DR driver during the ON time t_{ON} as shown by the blue arrows in the figure below.



As shown in the graph above, in steady state, the voltage drop ΔV_{BST} on C_{BST} during discharge (red curve, ON time t_{ON}) is given by:

$$\Delta V_{BST} = (I_Q * t_{ON} + C_{eq} * V_{MAX}) / C_{BST}$$

Where I_Q=250µA is the quiescent current delivered from BST_P to the pull-up driver, C_{eq}≈500pF is the equivalent capacitor that must be charged by BST _P up to the voltage V_{MAX}, t_{ON}=1/fr-t_{OFF}, and f_R is the PWM frequency.

To have a first guess for C_{BST}, we consider the extreme values for V_{MAX} = VDD-V_{TD} (V_{TD} is the threshold voltage of the bootstrap diode), and ΔV_{BST}=300mV to ensure V_{MIN} > 4V, which is the threshold to turn-on the integrated charge pump. Indeed, the integrated charge pump has been designed to be able to maintain the on state permanently (PWM DTC 100%). It is not able to provide enough charge to the bootstrap capacitor when the PWM signal is switching. Therefore, the following condition on C_{BST} is obtained, which gives a lower limit:

$$C_{BST} > [I_Q * t_{ON} + C_{eq} * (VDD - V_{TD})] / \Delta V_{BST}$$

For VDD-V_{TD}=4.3V, fr=50kHz, and t_{ON}=19µs (t_{OFF}=1µs), C_{BST} must be higher than 23nF. As this is an extreme value, we recommend taking at least two times this value to reduce the voltage ripple ΔV_{BST}.

- The bootstrap capacitor C_{BST} is charged for the first time during the startup time given by the rise time of the power supply and the 50µs delay fixed by the startup counter. The charging path is, as described in the figure above with the red arrows, going from the 5V versus VSS power supply PVDD via the integrated bootstrap diode, then the external R_{PU}, and finally the PD_MC driver in parallel with the R_{PD} and the PD_DR driver. Hence, C_{BST} must fulfill the following condition to guarantee its total charge during the startup, which gives an upper limit:

$$C_{BST} < 50\mu s / (3 * R_{PU})$$

As the on resistances of the PU, PD, MC transistors are in the range of 1…2Ω, they are neglected compared to R_{PU} and R_{PD}. For R_{PU}=20Ω, C_{BST} must be smaller than 833nF.

In steady state, as shown in the graph above, the voltage drop ΔV_{BST} on C_{BST} during the charge (green curve, OFF time t_{OFF}) is given by:

$$\Delta V_{BST} = (VDD - V_{TD} - V_{MIN}) * (1 - \exp[-t_{OFF} / (R_{eq} * C_{BST})])$$

where R_{eq} is given by:

$$Req = (R_{PU} + R_{PD}) * t_{MC} / t_{OFF} + R_{PU} * (t_{OFF} - t_{MC}) / t_{OFF}$$

From the equation of ΔV_{BST} during the charge, the following condition on R_{eq} is obtained:

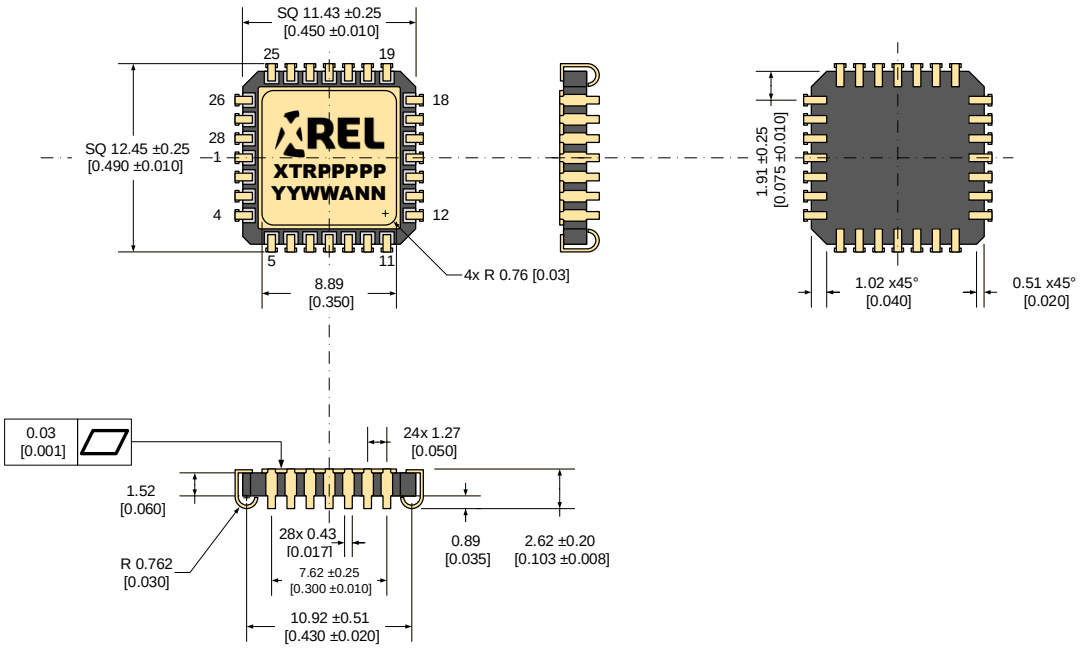
$$R_{eq} < -t_{OFF} / (C_{BST} * \ln[1 - \Delta V_{BST} / (VDD - V_{TD} - V_{MIN})])$$

For V_{MIN}=4V, t_{MC}=100ns, t_{OFF}=1µs, and C_{BST}=47nF, R_{eq} must be smaller than 32Ω. With R_{PU}=R_{PD}=20Ω (R_{eq}=22Ω), fr=50kHz, t_{OFF}=1µs, and C_{BST}=47nF, the following ripple characteristics are obtained:

ΔV_{BST} = 150mV
V_{MAX} = 4.21V
V_{MIN} = 4.06V

PACKAGE OUTLINES

J-Formed Leaded Chip Carrier LJCC28



Part Marking Convention	
Part Reference: XTRPPPPP	
XTR	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 11 = 2011).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

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