XTR54170

High Temperature Edge-Triggered D Flip-Flop

Rev 4 – August 2021 (DS-00550-13)

Data Sheet

PRODUCTION

DIP16
XTR54175

DIP8
XTR541G74

FEATURES

- Wide operating supply voltage from 2.8V to 5.5V.
- Operational beyond the -60°C to +230°C temperature range.
- Up to ±8mA output drive.
- Schmitt-Trigger Inputs allow better switching noise immunity.
- Ruggedized SMT packages.
- Also available as bare die.

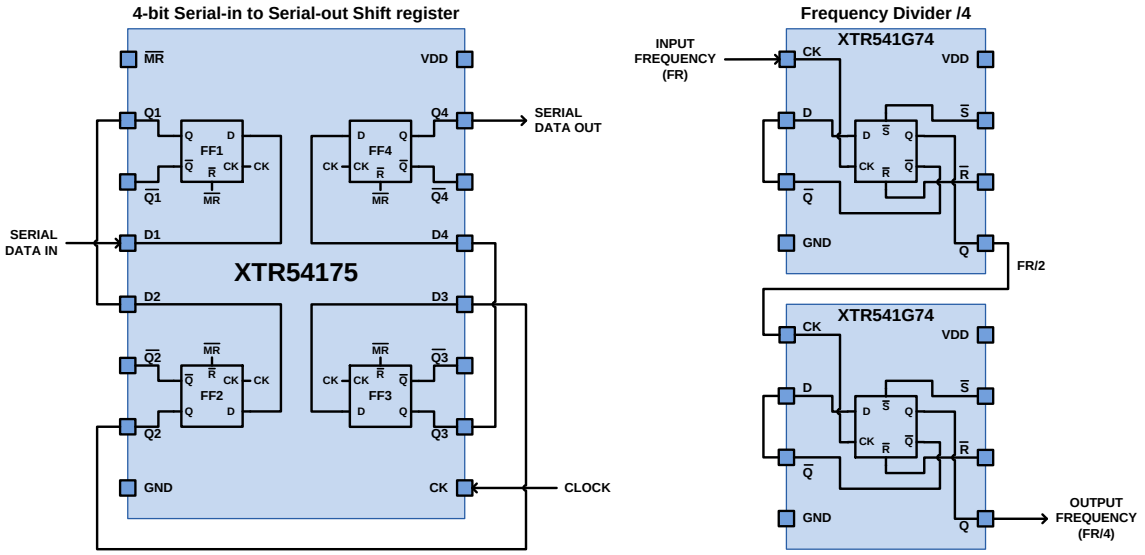
APPLICATIONS

- Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.

DESCRIPTION

The XTR54170 is a family of positive-edge-triggered D-type flip-flops. XTR54175 have four D-type flip-flops with individual data input D and both Q and $\overline{Q}$ outputs. The common clock CK and master reset $\overline{MR}$ inputs trigs and resets all flip-flops simultaneously.
XTR541G74 have a single D-type flip-flop with data D and clock CK inputs, Q and $\overline{Q}$ outputs, and set $\overline{S}$ and reset $\overline{R}$ inputs.
Parts from the XTR54170 family are available in ruggedized SMT and through-hole packages. Parts are also available as bare dies.

PRODUCT HIGHLIGHT



ORDERING INFORMATION

X	TR	54	170
Source : X = X-REL Semi	Process: TR = HiTemp, HiRel	Part family	Part number

Product Reference	Temperature Range	Package	Pin Count	Marking
XTR54170-TD	-60°C to +230°C	Tested Bare die		
XTR54175-D	-60°C to +230°C	Ceramic side braze DIP	16	XTR54175
XTR541G74-D	-60°C to +230°C	Ceramic side braze DIP	8	XTR541G74

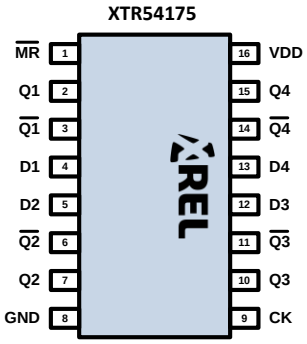
Other packages and packaging configurations possible upon request. For some packages or packaging configurations, MOQ may apply.

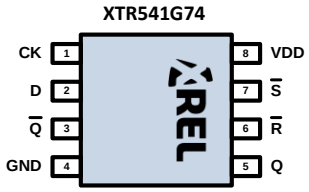
ABSOLUTE MAXIMUM RATINGS

Supply voltage VDD to GND (VDD)	-0.5 to 6.0V
Voltage on any pin, input or output, to GND	-0.5 to VDD+0.5V
Storage Temperature Range	-70°C to +230°C
Operating Junction Temperature Range	-70°C to +300°C
ESD Classification	1kV HBM MIL-STD-883

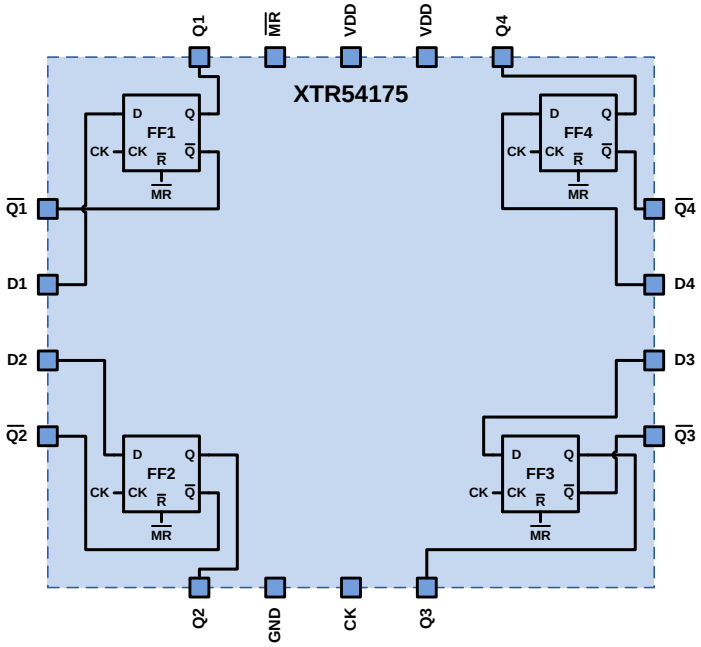
Caution: *Stresses beyond those listed in "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may permanently affect device reliability.*

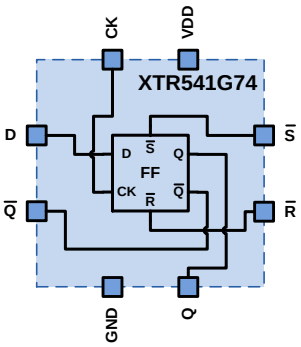
PRODUCT VARIANTS





BLOCK DIAGRAM





Please contact X-REL for XTR54170-BD block diagram and die information.

PIN DESCRIPTION

XTR54175		
Pin Number	**Name**	**Description**
1	$\overline{MR}$	Master reset, which resets all flip-flops simultaneously
2	Q1	Non-inverting output of FF1
3	$\overline{Q1}$	Inverting output of FF1
4	D1	Schmitt-Triggered input of FF1
5	D2	Schmitt-Triggered input of FF2
6	$\overline{Q2}$	Inverting output of FF2
7	Q2	Non-inverting output of FF2
8	GND	Negative supply voltage
9	CK	Positive edge trigger input of all flip-flops.
10	Q3	Non-inverting output of FF3
11	$\overline{Q3}$	Inverting output of FF2
12	D3	Schmitt-Triggered input of FF3
13	D4	Schmitt-Triggered input of FF4
14	$\overline{Q4}$	Inverting output of FF4
15	Q4	Non-inverting output of FF4
16	VDD	Positive supply voltage

XTR541G74		
Pin Number	**Name**	**Description**
1	CK	Positive edge trigger input
2	D	Schmitt-Triggered input of FF
3	$\overline{Q}$	Inverting output of FF
4	GND	Negative supply voltage
5	Q	Non-inverting output of FF
6	$\overline{R}$	Schmitt-Triggered reset input of FF
7	$\overline{S}$	Schmitt-Triggered set input of FF
8	VDD	Positive supply voltage

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply voltage **VDD-GND**	2.8		5.5	V
Voltage on D1, D2, D3, D4, D, $\overline{MR}$, $\overline{R}$, $\overline{S}$, CK	0[1]		VDD[1]	V
Junction Temperature[2] T_j	-60		230	°C

[1] During transient operation, these pins can reach values under 0V and above VDD. Extreme values are limited by internal clamping diodes to GND and to VDD.

[2] Operation beyond the specified temperature range is achieved.

XTR54175 ELECTRICAL SPECIFICATIONS

Unless otherwise stated, specification applies for -60°C<T_J<230°C and C_{OUT}=50pF.

Parameter	Condition	Min	Typ	Max	Units
Quiescent current					
Supply quiescent current I_{DD}	All inputs at Low state and VDD=5.5V @230°C (worst case)		5	20	uA
Input voltage					
High-level Input Voltage V_{IH}	VDD=2.8V VDD=3.3V VDD=5V VDD=5.5V	2.3 2.6 3.7 4.0	1.9 2.3 3.3 3.6		V
Low-level Input Voltage V_{IL}	VDD=2.8V VDD=3.3V VDD=5V VDD=5.5V		0.9 1.1 1.6 1.8	0.6 0.8 1.2 1.4	V
Output voltage					
High-level Output Voltage V_{OH}	VDD=2.8V, I_{OUT}=-4mA (device sourcing) VDD=3.3V, I_{OUT}=-6mA (device sourcing) VDD=5V, I_{OUT}=-8mA (device sourcing)	2.50 2.95 4.65	2.60 3.05 4.76		V
Low-level Output Voltage V_{OL}	VDD=2.8V, I_{OUT}=4mA (device sinking) VDD=3.3V, I_{OUT}=6mA (device sinking) VDD=5V, I_{OUT}=8mA (device sinking)		200 250 220	300 350 320	mV
Timing Requirements					
Maximum Clock Frequency f_{MAX}	VDD=2.8V VDD=3.3V VDD=5V	10 15 20			MHz
Clock Pulse-width t_W	VDD=2.8V VDD=3.3V VDD=5V	15 10 5			ns
Setup Time t_{SU}	VDD=2.8V VDD=3.3V VDD=5V	11 9 7	3.6 3.0 2.5		ns
Hold Time t_{HD}	VDD=2.8V VDD=3.3V VDD=5V	8 6 4	2.6 2.0 1.4		ns
Master Reset Pulse-width t_{W_MR}	VDD=2.8V VDD=3.3V VDD=5V	25 20 12			ns
Removal Time t_{REM}	$\overline{MR}$ going inactive to rising edge of CK VDD=2.8V VDD=3.3V VDD=5V	20 15 10	6 5 3.5		ns
Switching Characteristics					
Propagation Delay from CK to Q or $\overline{Q}$ t_{PD_CK}	VDD=2.8V VDD=3.3V VDD=5V		35 26 15	70 50 26	ns
Rise Time Q or $\overline{Q}$ t_{RISE}	VDD=2.8V VDD=3.3V VDD=5V		5.0 3.7 2.0	15 11 7	ns
Fall Time Q or $\overline{Q}$ t_{FALL}	VDD=2.8V VDD=3.3V VDD=5V		6.0 4.5 2.5	18 15 8	ns
Propagation Delay from $\overline{MR}$ to Q or $\overline{Q}$ $t_{PD\_\overline{MR}}$	VDD=2.8V VDD=3.3V VDD=5V		31 24 14	66 47 24	ns

XTR541G74 ELECTRICAL SPECIFICATIONS

Unless otherwise stated, specification applies for -60°C<T_J<230°C and C_{OUT}=50pF.

Parameter	Condition	Min	Typ	Max	Units
Quiescent current					
Supply quiescent current I_{DD}	All inputs at Low state and VDD=5.5V @230°C (worst case)		3.5	15	uA
Input voltage					
High-level Input Voltage V_{IH}	VDD=2.8V VDD=3.3V VDD=5V VDD=5.5V	2.3 2.6 3.7 4.0	1.9 2.3 3.3 3.6		V
Low-level Input Voltage V_{IL}	VDD=2.8V VDD=3.3V VDD=5V VDD=5.5V		0.9 1.1 1.6 1.8	0.6 0.8 1.2 1.4	V
Output voltage					
High-level Output Voltage V_{OH}	VDD=2.8V, I_{OUT}=-4mA (device sourcing) VDD=3.3V, I_{OUT}=-6mA (device sourcing) VDD=5V, I_{OUT}=-8mA (device sourcing)	2.50 2.95 4.65	2.60 3.05 4.76		V
Low-level Output Voltage V_{OL}	VDD=2.8V, I_{OUT}=4mA (device sinking) VDD=3.3V, I_{OUT}=6mA (device sinking) VDD=5V, I_{OUT}=8mA (device sinking)		200 250 220	300 350 320	mV
Timing Requirements					
Maximum Clock Frequency f_{MAX}	VDD=2.8V VDD =3.3V VDD=5V	10 15 20			MHz
Clock Pulse-width t_W	VDD=2.8V VDD=3.3V VDD=5V	15 10 5			ns
Setup Time t_{SU}	VDD=2.8V VDD =3.3V VDD=5V	11 9 7	3.6 3.0 2.5		ns
Hold Time t_{HD}	VDD=2.8V VDD=3.3V VDD=5V	8 6 4	2.6 2.0 1.4		ns
Set or Reset Pulse-width t_{W_SR}	VDD=2.8V VDD=3.3V VDD=5V	25 20 12			ns
Removal Time t_{REM}	$\overline{R}$ or $\overline{S}$ going inactive to rising edge of CK VDD=2.8V VDD=3.3V VDD=5V	20 15 10	6 5 3.5		ns
Switching Characteristics					
Propagation Delay from CK to Q or $\overline{Q}$ t_{PD_CK}	VDD=2.8V VDD=3.3V VDD=5V		35 26 15	70 50 26	ns
Rise Time Q or $\overline{Q}$ t_{RISE}	VDD=2.8V VDD=3.3V VDD=5V		5.0 3.7 2.0	15 11 7	ns
Fall Time Q or $\overline{Q}$ t_{FALL}	VDD=2.8V VDD=3.3V VDD=5V		6.0 4.5 2.5	18 15 8	ns
Propagation Delay from $\overline{S}$ or $\overline{R}$ to Q or $\overline{Q}$ t_{PD_SR}	VDD=2.8V VDD=3.3V VDD=5V		29 21 13	60 45 35	ns

XTR54175 TYPICAL PERFORMANCE

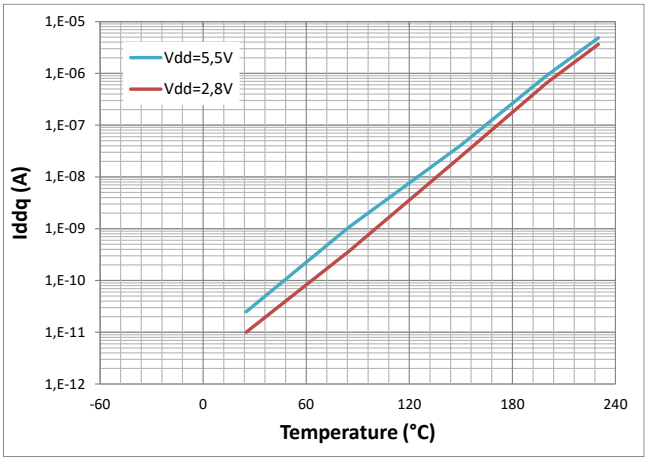


Figure 1. Total Quiescent Current (I_{DD}) vs. Temperature for different Supply Voltages.All inputs at Low state.

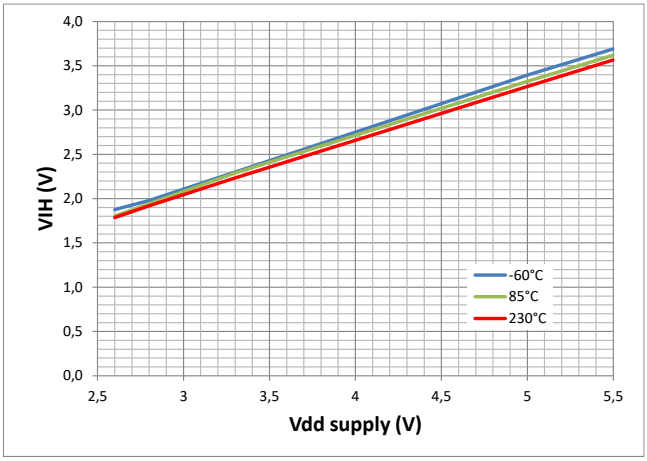


Figure 2. HIGH-level Input Voltage (V_{IH}) vs. Supply Voltage for different Case Temperatures.

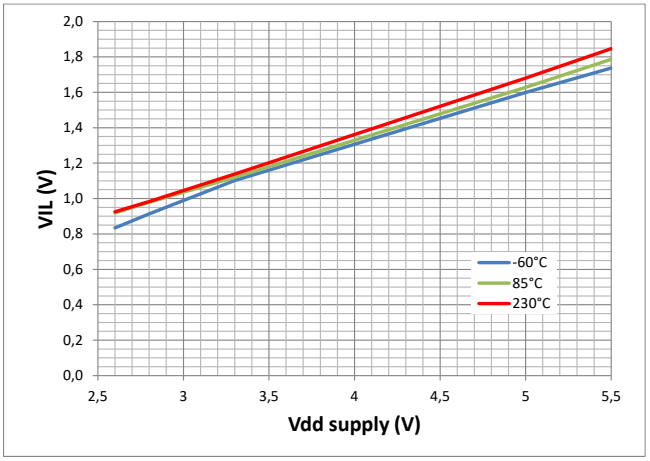


Figure 3. LOW-level Input Voltage (V_{IL}) vs. Supply Voltage for different Case Temperatures.

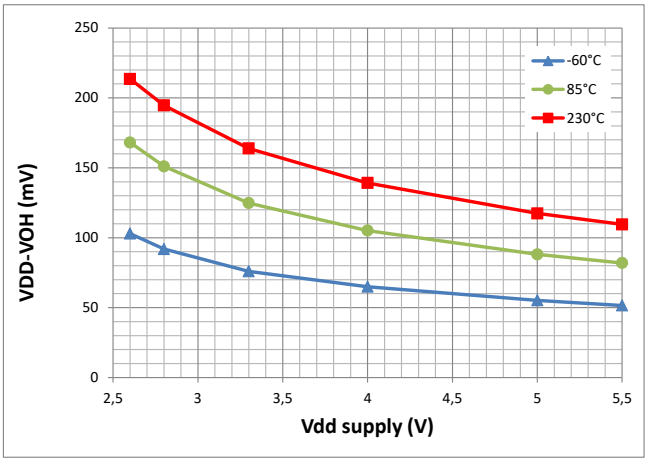


Figure 4. HIGH-level Output Voltage (V_{OH}) vs. Supply Voltage for different Case Temperatures and Iout=4mA sinking.

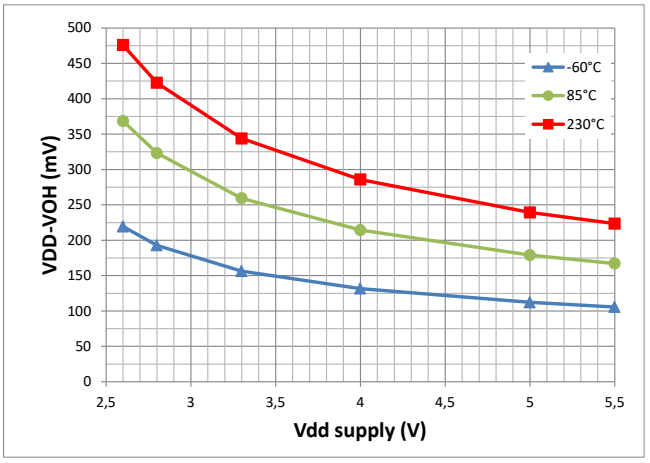


Figure 5. HIGH-level Output Voltage (V_{OH}) vs. Supply Voltage for different Case Temperatures and Iout=8mA sinking

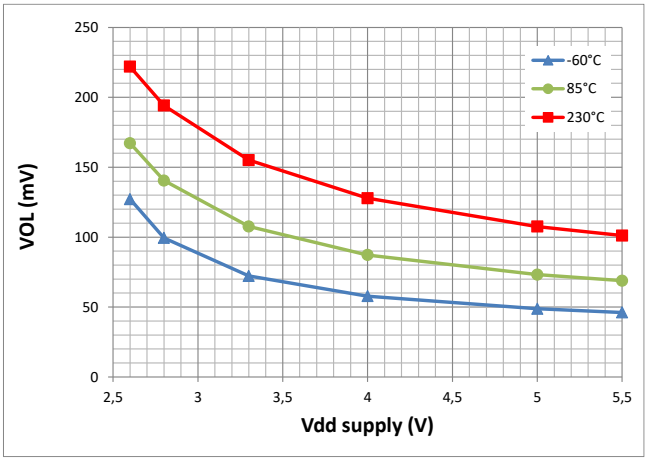


Figure 6. LOW-level Output Voltage (V_{OL}) vs. Supply Voltage for different Case Temperatures and Iout=4mA sourcing.

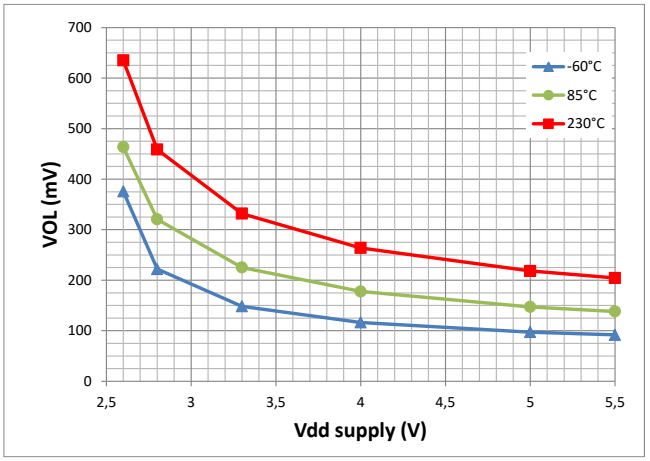


Figure 7. LOW-level Output Voltage (V_{OL}) vs. Supply Voltage for different Case Temperatures and Iout=8mA sourcing.

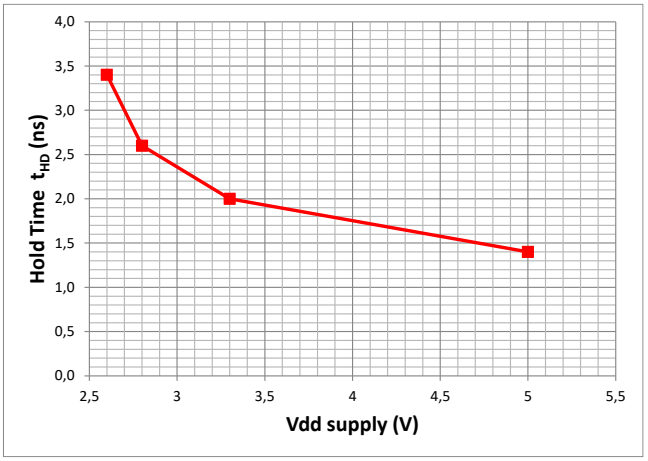


Figure 8. Hold Time (t_{HD}) vs. Supply Voltage at 230°C (worst case).

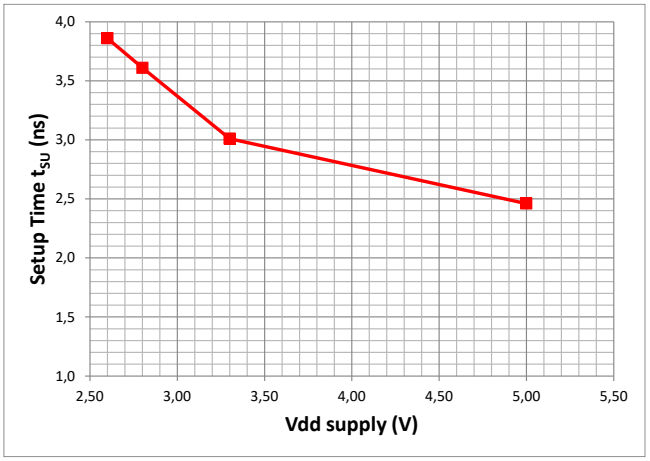


Figure 9. Setup Time (t_{SU}) vs. Supply Voltage at 230°C (worst case).

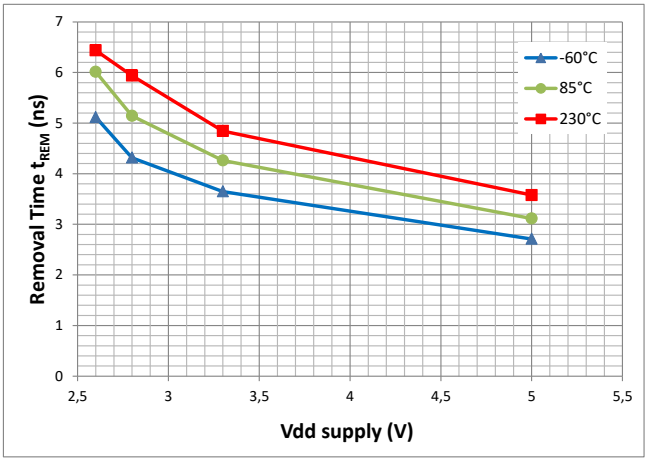


Figure 10.Removal Time (t_{rem}) vs. Supply Voltage for different Case Temperatures.

XTR54175 TYPICAL PERFORMANCE (CONTINUED)

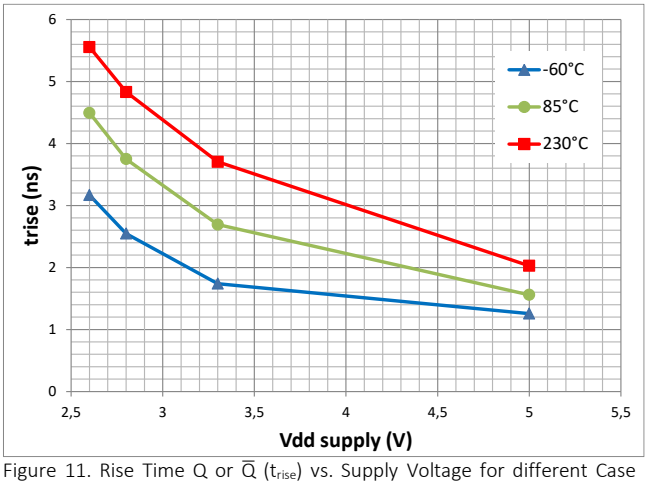


Figure 11. Rise Time Q or $\overline{Q}$ (t_{rise}) vs. Supply Voltage for different Case Temperatures.
C_{OUT} = 50pF.

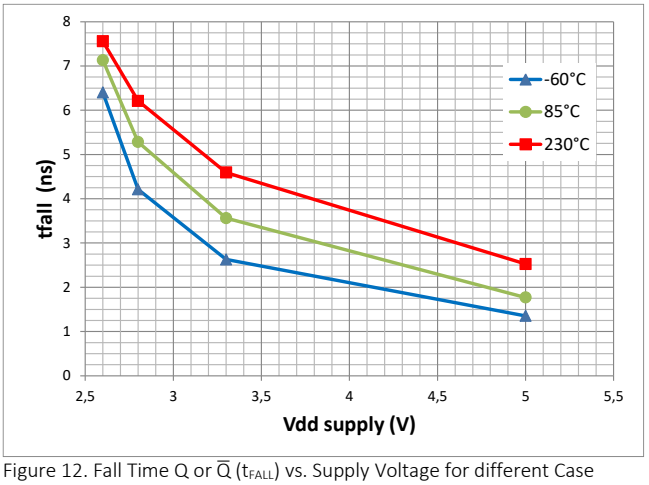


Figure 12. Fall Time Q or $\overline{Q}$ (t_{FALL}) vs. Supply Voltage for different Case Temperatures.
C_{OUT} = 50pF.

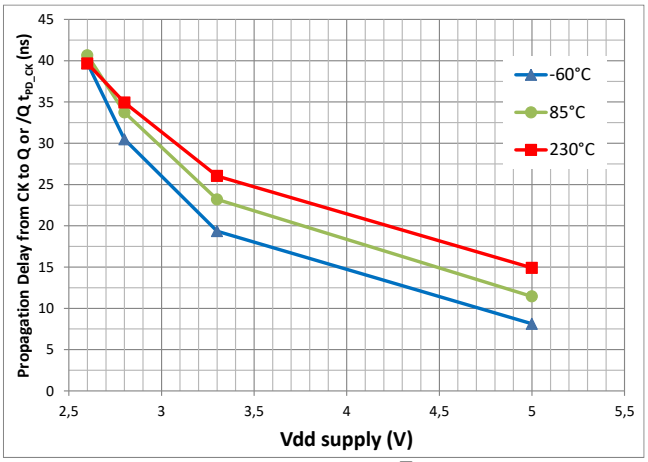


Figure 13. Propagation Delay from CK to Q or $\overline{Q}$ (t_{PD_CK}) vs. Supply Voltage for different Case Temperatures.
C_{OUT} = 50pF.

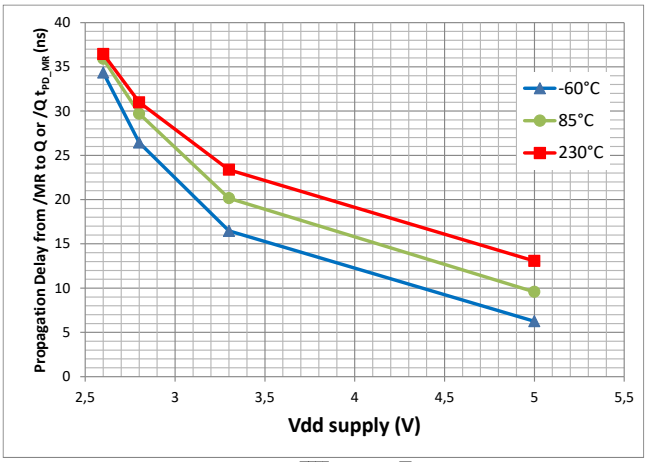


Figure 14. Propagation Delay from $\overline{MR}$ to Q or $\overline{Q}$ ($t_{PD\_\overline{MR}}$) vs. Supply Voltage for different Case Temperatures.
C_{OUT} = 50pF.

XTR541G74 TYPICAL PERFORMANCE

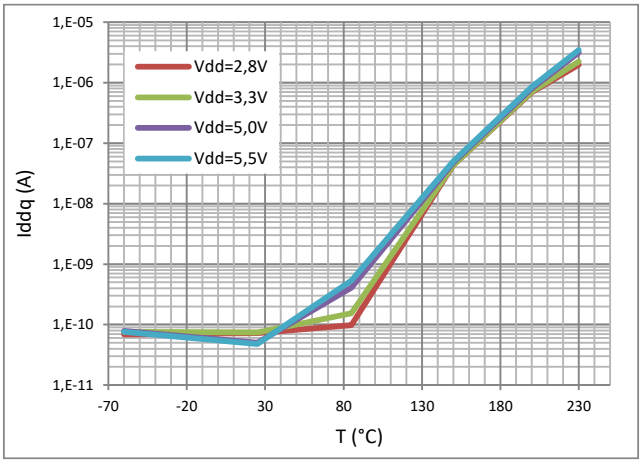


Figure 15. Total Quiescent Current (I_{DD}) vs. Temperature for different Supply Voltages. All inputs at Low state.

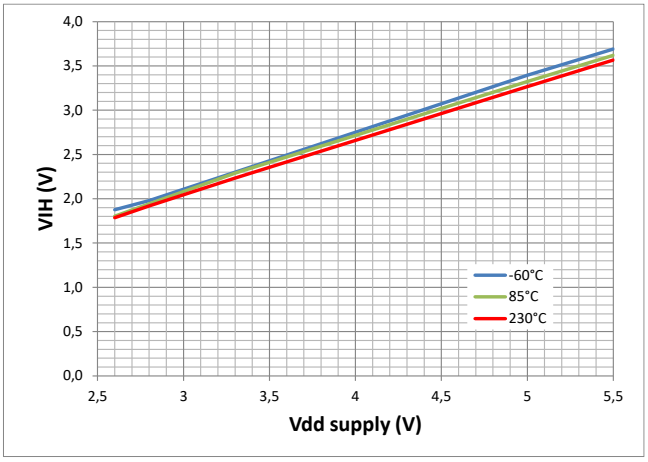


Figure 16. HIGH-level Input Voltage (V_{IH}) vs. Supply Voltage for different Case Temperatures.

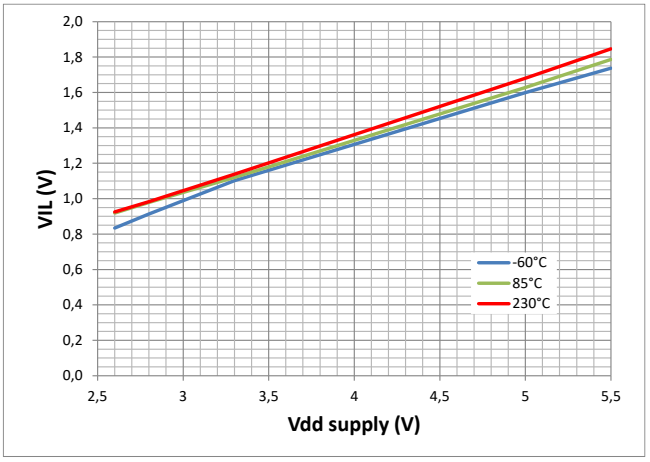


Figure 17. LOW-level Input Voltage (V_{IL}) vs. Supply Voltage for different Case Temperatures.

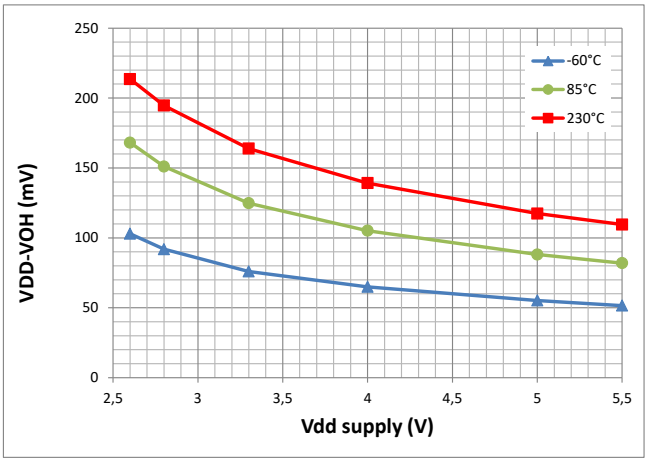


Figure 18. HIGH-level Output Voltage (V_{OH}) vs. Supply Voltage for different Case Temperatures and Iout=4mA sinking.

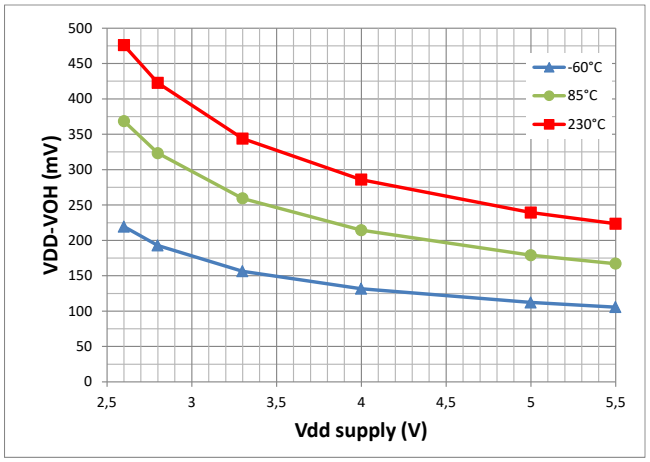


Figure 19. HIGH-level Output Voltage (V_{OH}) vs. Supply Voltage for different Case Temperatures and Iout=8mA sinking

XTR541G74 TYPICAL PERFORMANCE (CONTINUED)

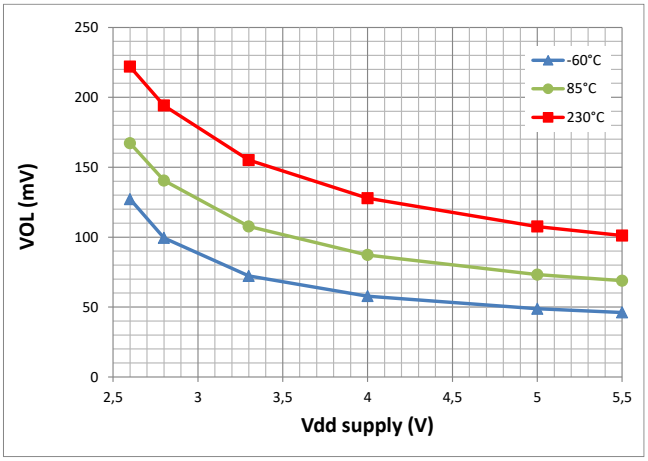


Figure 20. LOW-level Output Voltage (V_{OL}) vs. Supply Voltage for different Case Temperatures and Iout=4mA sourcing.

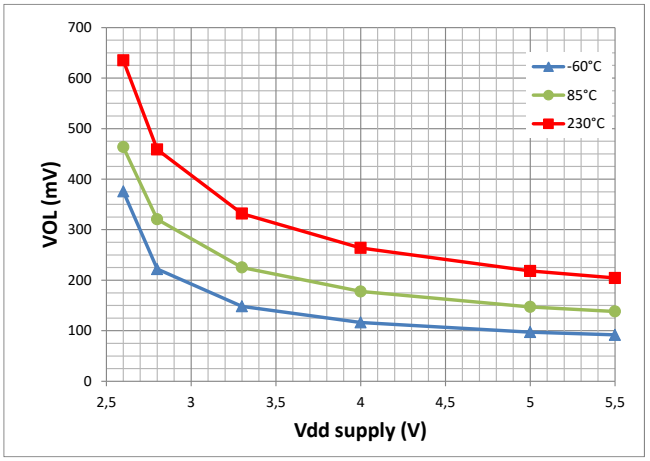


Figure 21. LOW-level Output Voltage (V_{OL}) vs. Supply Voltage for different Case Temperatures and Iout=8mA sourcing.

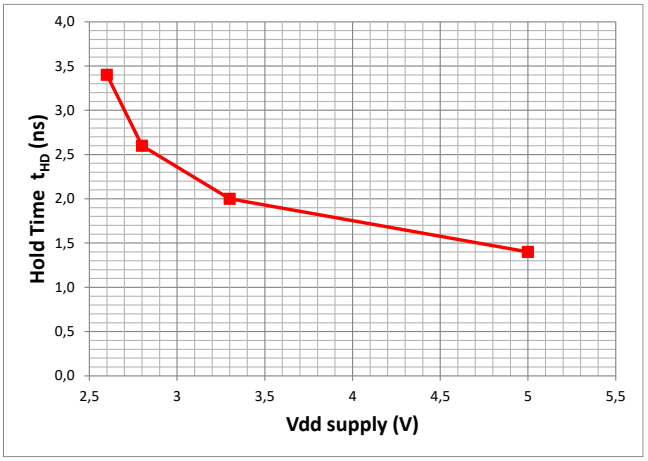


Figure 22. Hold Time (t_{HD}) vs. Supply Voltage at 230°C (worst case).

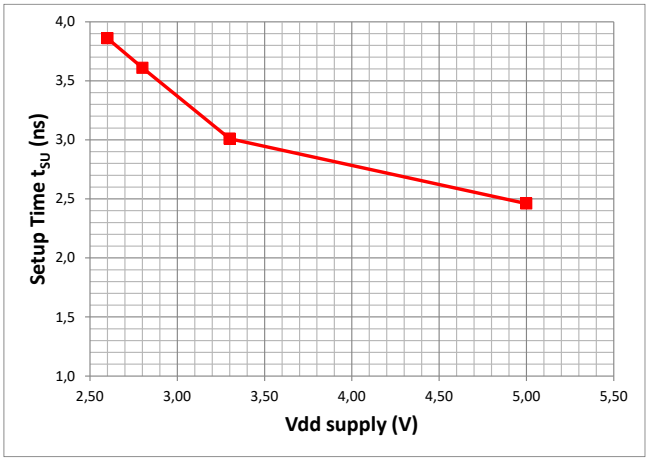


Figure 23. Setup Time (t_{SU}) vs. Supply Voltage at 230°C (worst case).

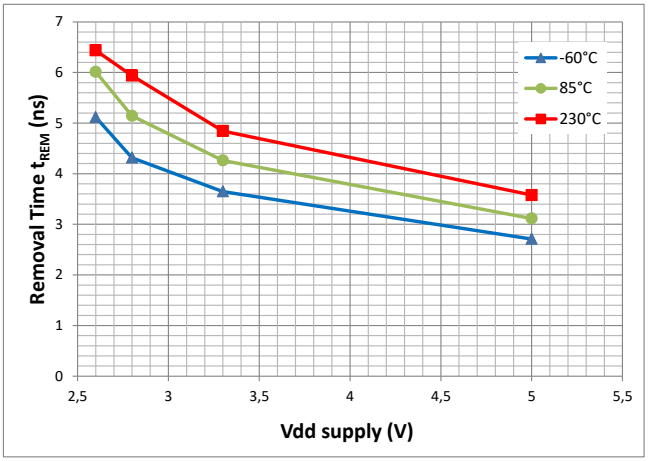


Figure 24.Removal Time (t_{rem}) vs. Supply Voltage for different Case Temperatures.

XTR541G74 TYPICAL PERFORMANCE (CONTINUED)

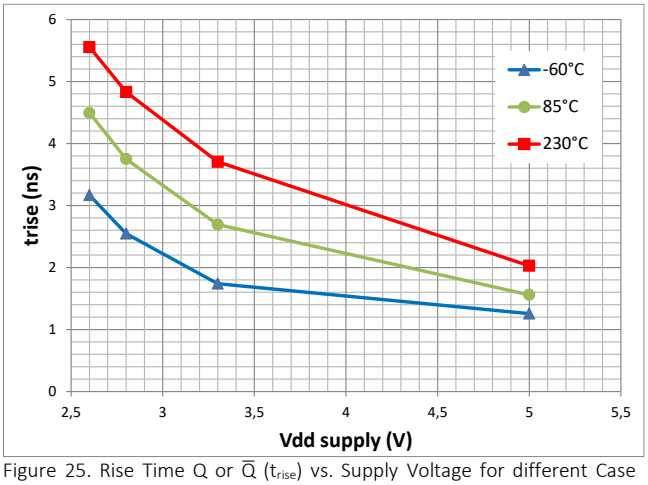


Figure 25. Rise Time Q or $\overline{Q}$ (t_{rise}) vs. Supply Voltage for different Case Temperatures.
C_{OUT} = 50pF.

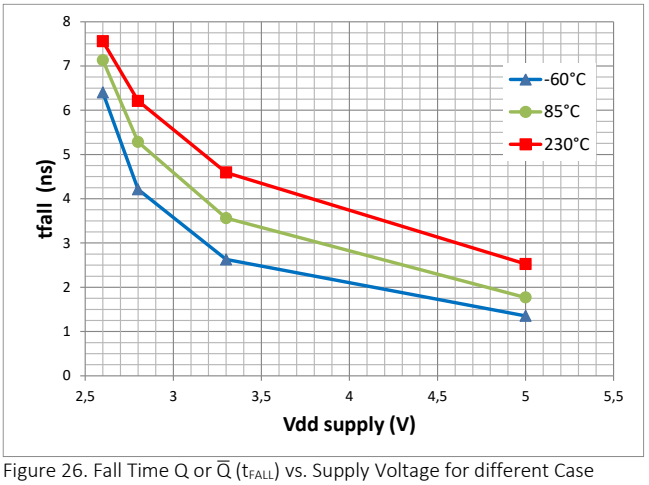


Figure 26. Fall Time Q or $\overline{Q}$ (t_{FALL}) vs. Supply Voltage for different Case Temperatures.
C_{OUT} = 50pF.

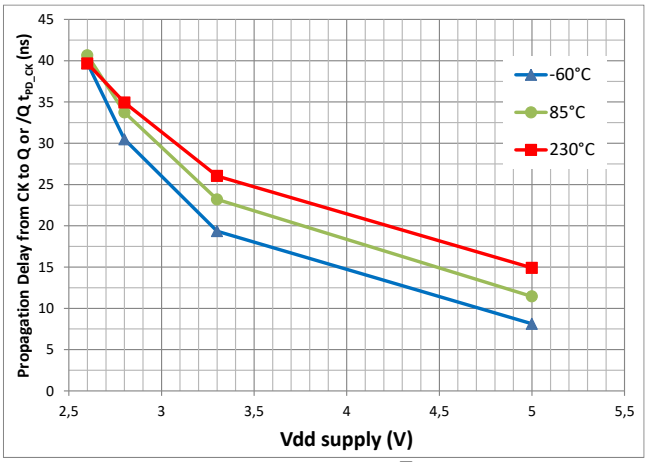


Figure 27. Propagation Delay from CK to Q or $\overline{Q}$ (t_{PD_CK}) vs. Supply Voltage for different Case Temperatures.
C_{OUT} = 50pF.

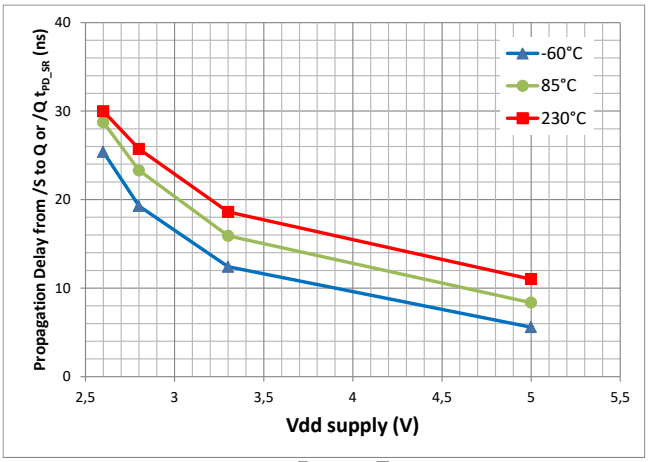


Figure 28. Propagation Delay from $\overline{S}$ to Q or $\overline{Q}$ (t_{PD_SR}) vs. Supply Voltage for different Case Temperatures.
C_{OUT} = 50pF.

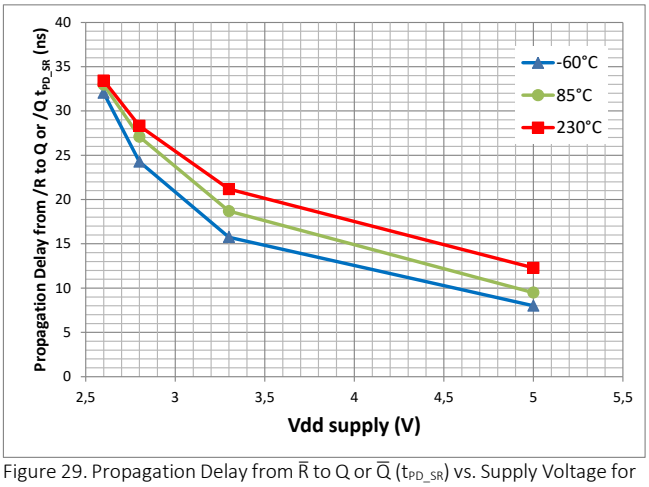


Figure 29. Propagation Delay from $\overline{R}$ to Q or $\overline{Q}$ (t_{PD_SR}) vs. Supply Voltage for different Case Temperatures.
C_{OUT} = 50pF.

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THEORY OF OPERATION

Introduction

The XTR54170 is a family of positive-edge-triggered D-type flip-flops.
XTR54175 have four D-type flip-flops with individual data input D and both Q and $\overline{Q}$ outputs. The common clock CK and master reset $\overline{MR}$ inputs trigs and resets all flip-flops simultaneously.
XTR541G74 have a single D-type flip-flop with data D and clock CK inputs, Q and $\overline{Q}$ outputs, and set $\overline{S}$ and reset $\overline{R}$ inputs.

XTR54175 operation

The XTR54175 architecture (for one flip-flop) is shown in the figure below.
A low level at the master reset ($\overline{MR}$) input reset the outputs, regardless of the levels of the other inputs. When $\overline{MR}$ is inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

Truth Table

INPUTS			OUTPUTS	
$\overline{MR}$	CK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q_0}$

XTR541G74 operation

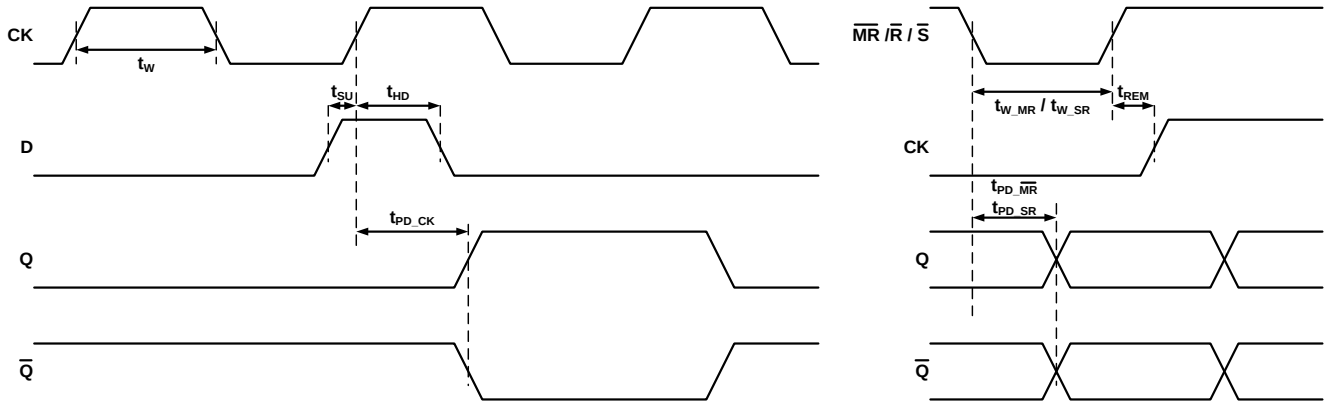
The XTR541G74 architecture is shown in the figure below.
A low level at the set ($\overline{S}$) or reset ($\overline{R}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{S}$ and reset $\overline{R}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

Truth Table

INPUTS				OUTPUTS	
$\overline{S}$	$\overline{R}$	CK	D	Q	$\overline{Q}$
L	L	X	X	L[1]	L[1]
L	H	X	X	H	L
H	L	X	X	L	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

[1] Outputs in this configuration will not persist when $\overline{S}$ or $\overline{R}$ returns to its inactive (HIGH) level. To guarantee known outputs when removing this state, make sure one of $\overline{S}$ or $\overline{R}$ remains in LOW state for at least a removal time.

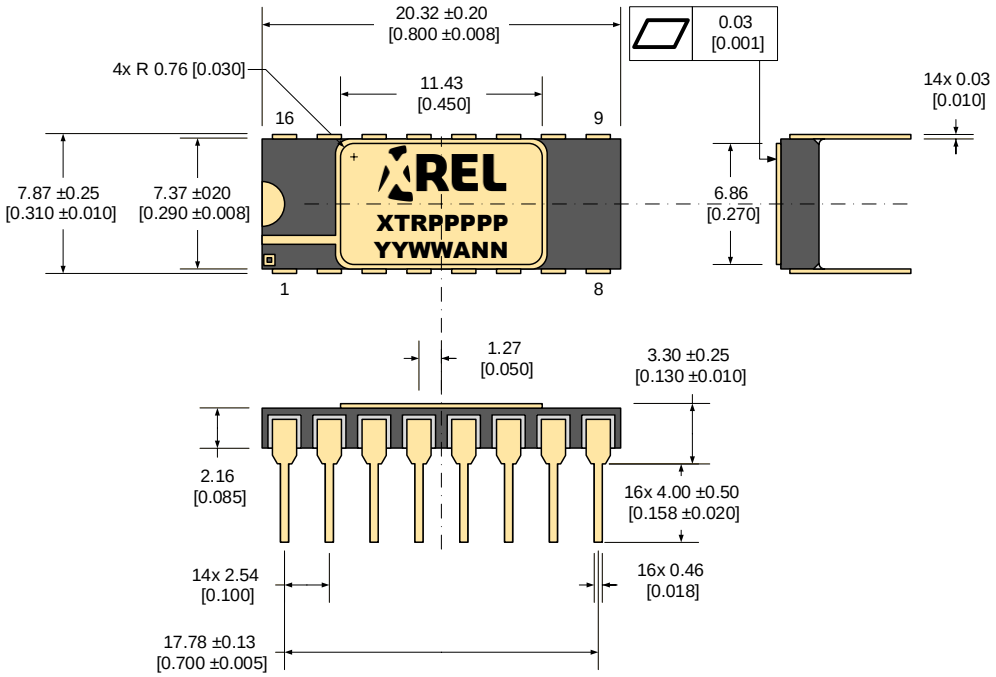
Timing definition



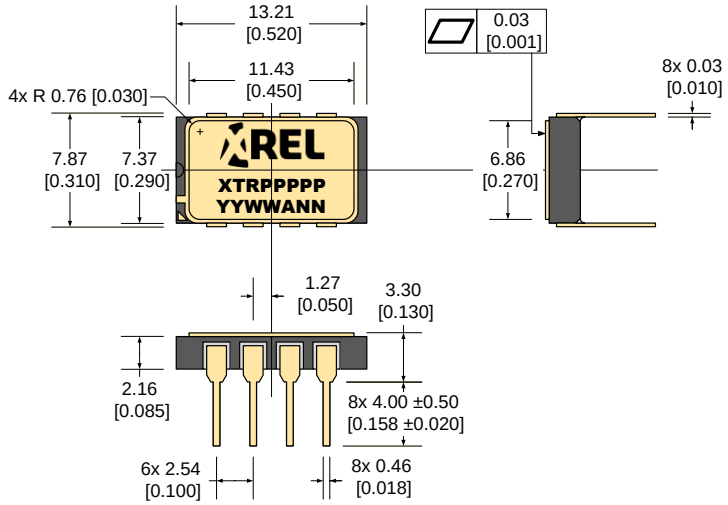
PACKAGE OUTLINES

Dimensions shown in mm [inches].

Ceramic Side Brazed Dual In-line DIP16



Ceramic Side Brazed Dual In-Line DIP8



Part Marking Convention	
Part Reference: XTRPPPPPP	
XTR	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 11 = 2011).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

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