HIGH-TEMPERATURE VERSATILE TIMER

FEATURES

- ▲ Supply voltage from 2.8V to 5.5V.
- ▲ Operational beyond the -60°C to +230°C temperature range.
- ▲ Monostable, Astable, PWM and PPM modes of operation.
- ▲ Complementary, non-overlapping outputs.
- ▲ Outputs can source or sink 50mA @ 230°C.
- ▲ Complementary high-voltage open-drain outputs.
- ▲ XTR655: drop-in replacement of 555.
- ▲ DISABLE mode.
- ▲ Integrated timing capacitor of 200pF for reduced BoM.
- ▲ Integrated coarse temperature sensor.
- ▲ Several packaging options including drop-in replacement of 555.
- ▲ Latch-up free.
- ▲ Ruggedized SMT and thru-hole packages.

APPLICATIONS

- ▲ Reliability-critical, Automotive, Aeronautics & Aerospace, Down-hole.
- ▲ Timing and pulse generation, frequency generation, pulse width modulation (PWM), pulse position modulation (PPM), linear ramp generator.

DESCRIPTION

XTR650 is a family of highly stable, small footprint and versatile timers designed for extreme reliability and temperature applications such as accurate time delays or frequency generators. Being able to operate from supply voltages from 2.8V to 5.5V, the XTR650 timers can generate timing periods from some hundreds of nanoseconds and oscillations with duty-cycles from virtually zero to 100%, overcoming the limitations of existing 555.

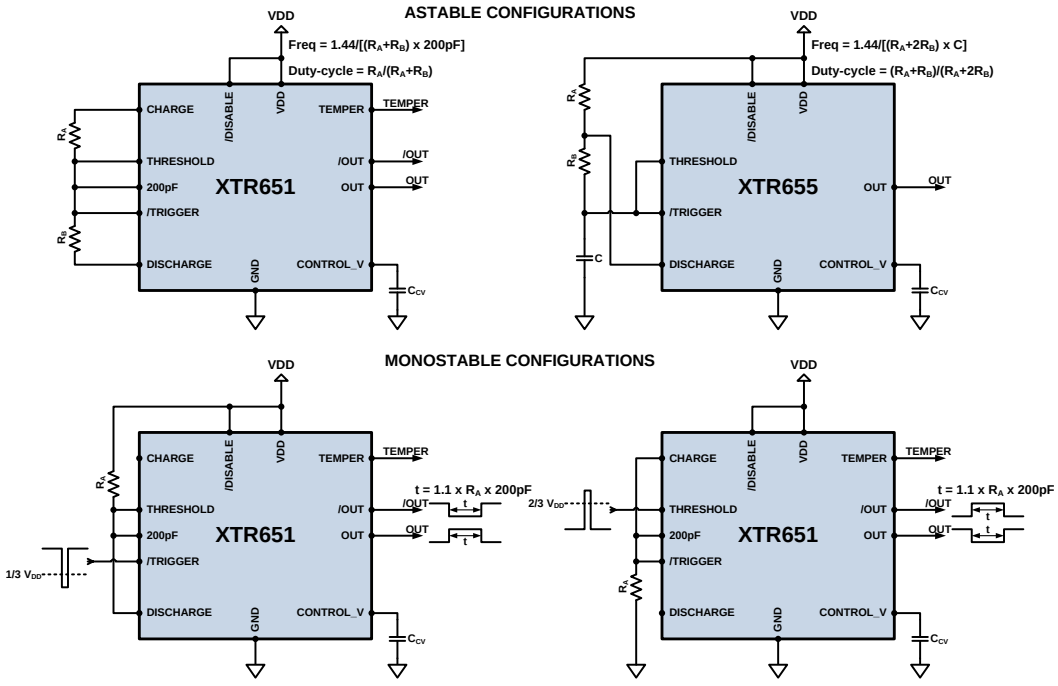
Other features include the availability of high current complementary and non-overlapping outputs, complementary high-voltage open-drain outputs, integrated timing capacitor of 200pF for reduced bill-of-material (BoM), and integrated coarse temperature sensor.

Especial design techniques were used allowing the XTR650 parts to offer a precise, robust and reliable operation in critical applications. Full functionality is guaranteed from -60°C to +230°C, though operation well below and above this temperature range is achieved.

XTR650 has been designed to reduce system cost and ease adoption by reducing the learning curve and providing smart and easy to use features.

Parts from the XTR650 family are available in ruggedized SMT and thru-hole packages.

PRODUCT HIGHLIGHT



ORDERING INFORMATION

X	TR	650
Source: X = X-REL Semi	Process: TR = HiTemp, HiRel	Part number

Product Reference	Temperature Range	Package	Pin Count	Marking
XTR650-TD	-60°C to +230°C	Tested bare die		
XTR651-D	-60°C to +230°C	Ceramic side braze DIP	14	XTR651
XTR655-D	-60°C to +230°C	Ceramic side braze DIP	8	XTR655

Other packages and packaging configurations possible upon request. For some packages or packaging configurations, MOQ may apply.

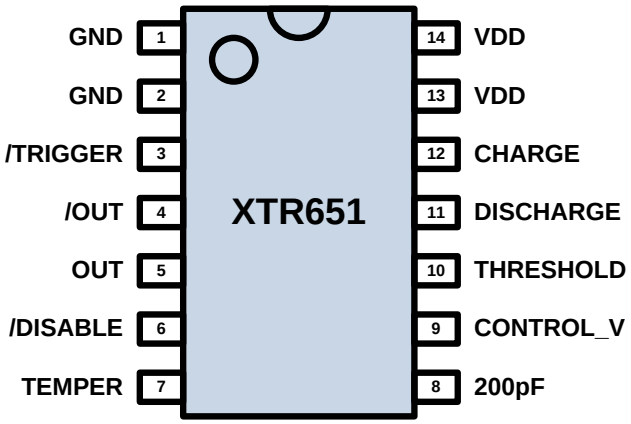
ABSOLUTE MAXIMUM RATINGS

Voltage to GND	
CHARGE	-35V to VDD+0.5V
DISCHARGE	-0.5V to 50V
All other pins	-0.5V to 6.0V
Storage Temperature Range	-70°C to +230°C
Operating Junction Temperature Range	-70°C to +300°C
ESD Classification	
CHARGE	250V HBM MIL-STD-883
DISCHARGE	500V HBM MIL-STD-883
All other pins	2kV HBM MIL-STD-883

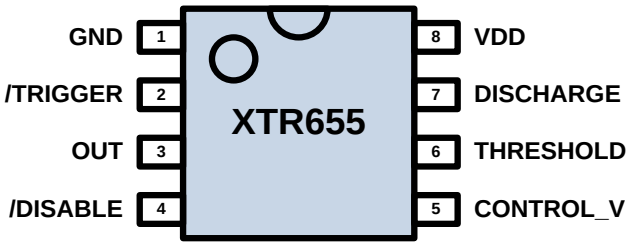
Caution: *Stresses beyond those listed in "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only and functionality of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to "ABSOLUTE MAXIMUM RATINGS" conditions for extended periods may permanently affect device reliability.*

PRODUCT VARIANTS

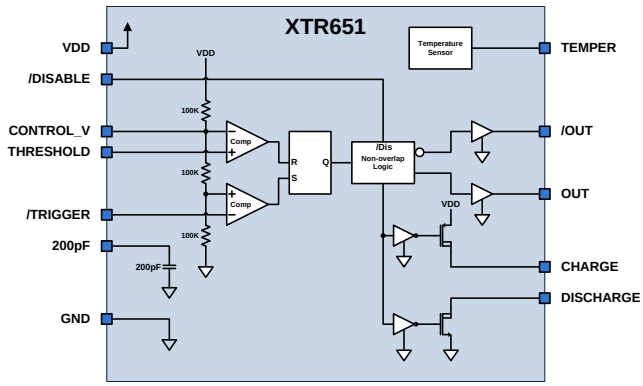
Ceramic side-brazed DIP14

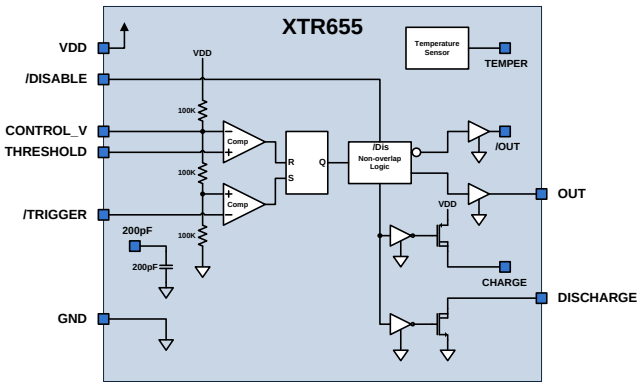


Ceramic side-brazed DIP8



BLOCK DIAGRAM





PIN DESCRIPTION

Pin Number		Name	Description
XTR651	XTR655		
1	1	GND	Circuit ground.
2	—	GND	Circuit ground.
3	2	/TRIGGER	Sets the internal flip-flop when going under 1/3VDD.
4	—	/OUT	Complementary output.
5	3	OUT	Main output.
6	4	/DISABLE[1]	Active LOW disable. Sets the device in the disable state.
7	—	TEMPER	Coarse temperature sensor. Output voltage decreases as temperature increases.
8	—	200pF	Internal timing capacitor. Second terminal is internally grounded.
9	5	CONTROL_V	Tap from internal resistor divider. It can be externally forced to change the triggering thresholds.
10	6	THRESHOLD	Resets the internal flip-flop when going above 2/3VDD.
11	7	DISCHARGE	N-type, open-drain output with respect to GND.
12	—	CHARGE	P-type, open-drain output with respect to VDD.
13	—	VDD	Supply voltage.
14	8	VDD	Supply voltage.

Table 1. Function Table

/DISABLE	THRESHOLD	/TRIGGER	OUT	/OUT	DISCHARGE	CHARGE
L[1]	Don't care	Don't care	L	L	ON	OFF
H	>2/3V_{DD}	Don't care	L	H	ON	OFF
H	<2/3V_{DD}	<1/3V_{DD}	H	L	OFF	ON
H	<2/3V_{DD}	>1/3V_{DD}	Previous state	Previous state	Previous state	Previous state

[1] This state does not reset the timer. When recovering from the disable state, outputs will return to their state previous to asserting /DISABLE=LOW.

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply voltage **V_{DD}**	2.8		5.5	V
Voltage on **/TRIGGER, THRESHOLD, CONTROL_V, 200PF**	-0.3		V_{DD}+0.3	V
Voltage on **DISCHARGE** (with respect to GND)			40	V
Voltage on **CHARGE** (with respect to VDD)	-30			V
Maximum operating frequency **F_O**		4		MHz
Junction Temperature[1] **T_j**	-60		230	°C

[1] Operation beyond the specified temperature range is achieved.

ELECTRICAL SPECIFICATIONS

Unless otherwise stated, specification applies for V_{DD}=5V, -60°C<T_j<230°C.

Parameter	Condition	Min	Typ	Max	Units
Supply					
Supply voltage **V_{DD}**		2.8		5.5	V
Supply current **I_{DD}**	R_A=R_B=∞		170	250	µA
Complementary Output Stage (OUT, /OUT)					
Peak output current (source or sink) **I_{Opk}**	T_j=230°C	±50			mA
Pull-up output resistance **R_{OH}**	Output sourcing 10mA. T_j=230°C			40	Ω
Pull-down output resistance **R_{OL}**	Output sinking 10mA. T_j=230°C			35	Ω
Open Drain Outputs (CHARGE, DISCHARGE)					
Maximum DISCHARGE voltage **$V_{DISCHMax}$**	With respect to GND			40	V
DISCHARGE switch on-state resistance **$R_{DISCHON}$**	V_{DISCH}=500mV T_j=150°C T_j=230°C		17 20		Ω
DISCHARGE switch off-state leakage current **$I_{DISCHOFF}$**	V_{DISCH}=V_{DD} T_j=150°C T_j=230°C		0.02 1		µA
Minimum CHARGE voltage **V_{CHMax}**	With respect to VDD	-30			V
CHARGE switch on-state resistance **R_{CHON}**	VDD-V_{CH}=500mV T_j=150°C T_j=230°C		28 35		Ω
CHARGE switch off-state leakage current **I_{CHOFF}**	V_{CH}=0V (GND) T_j=150°C T_j=230°C		0.150 7		µA
Tripping Voltages					
Control voltage (open circuit) **V_{CV}**	2.8V<V_{DD}<5.5V		66.7		%V_{DD}
Control voltage operating range **$V_{CONTROL\_V}$**	2.8V<V_{DD}<5.5V	1.7		VDD	V
Threshold voltage[1] **V_{TH}**	2.8V<V_{DD}<5.5V		66.7		%V_{DD}
Trigger voltage[2] **V_{TR}**	2.8V<V_{DD}<5.5V		33.3		%V_{DD}

[1] The tripping voltage of the THRESHOLD input is equal to the voltage applied on the CONTROL_V pin.
[2] The tripping voltage of the /TRIGGER input is equal to half the voltage applied on the CONTROL_V pin.

ELECTRICAL SPECIFICATIONS (CONTINUED)

Unless otherwise stated, specification applies for V_{DD}=5V, -60°C<T_j<230°C.

Parameter	Condition	Min	Typ	Max	Units
Internal Timing Capacitor (200pF)					
Capacitor value **C_{INT}**		170	200	230	pF
Leakage current **I_{CINT}**	V_{DD}=5V T_j=230°C		50		nA
Temperature Sensor (TEMPER)					
Output voltage **V_{TEMP}**	T_j=-60°C T_j=25°C T_j=150°C T_j=230°C		1.75 1.50 1.11 0.85		V
Dynamic Timing Characteristics					
Non-overlap time **t_{no}**	Time from OUT (/OUT) going down to /OUT (OUT) going up. OUT and /OUT loaded with 100pF	20	45	80	nsec
THRESHOLD to OUT propagation delay **t_{PDTh}**	OUT and /OUT loaded with 100pF		250	290	nsec
/TRIGGER to /OUT propagation delay **t_{PDTr}**	OUT and /OUT loaded with 100pF		105	150	nsec
Astable Configuration					
Initial accuracy	R_A=R_B=1kΩ to 1MΩ, C=10nF, T_j=85°C		-2.5		%
Drift with temperature	R_A=R_B=1kΩ to 1MΩ, C=10nF		-130		ppm/°C
Drift with supply voltage	R_A=R_B=1kΩ to 1MΩ, C=10nF 2.8V<V_{DD}<5.5V 4.5V<V_{DD}<5.5V		1 0.3		%/V
Monostable Configuration					
Initial accuracy	R_A=1kΩ to 1MΩ, C=10nF		-2		%
Drift with temperature	R_A=1kΩ to 1MΩ, C=10nF		-150		ppm/°C
Drift with supply voltage	R_A=1kΩ to 1MΩ, C=10nF 2.8V<V_{DD}<5.5V		1		%/V

TYPICAL PERFORMANCE

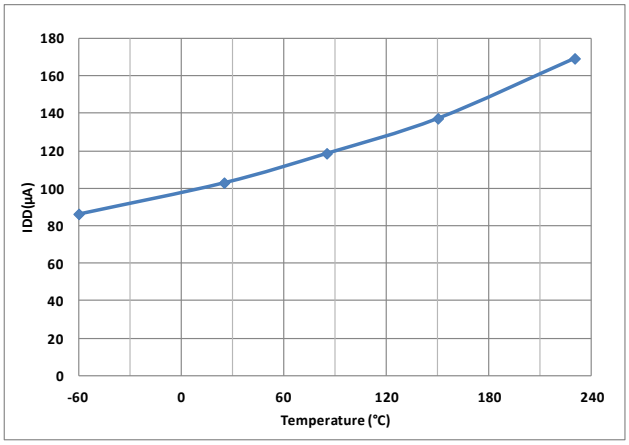


Figure 1. Quiescent Supply Current vs. Temperature for V_{DD}=5.5V.

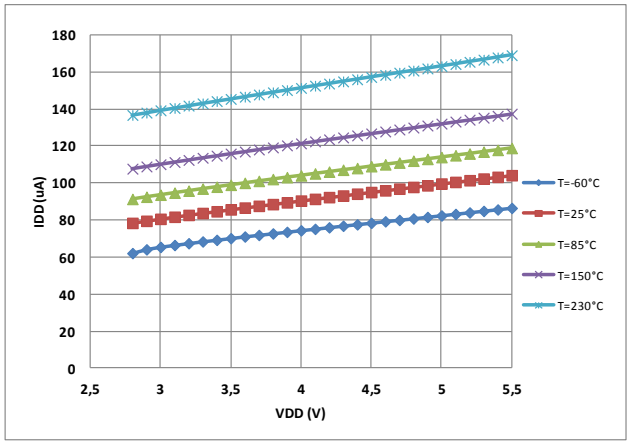


Figure 2. Quiescent Supply Current vs. Supply Voltage (V_{DD}) for different temperatures.

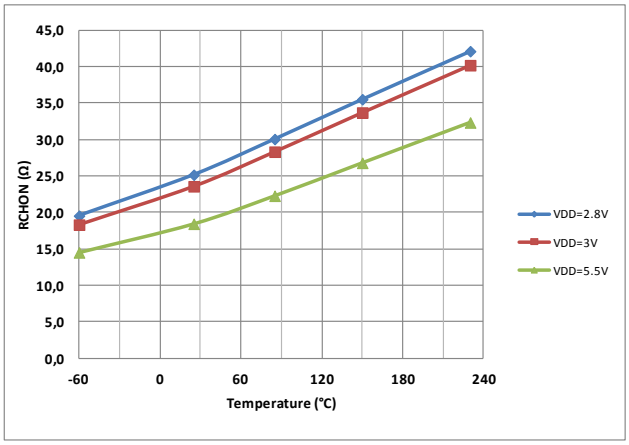


Figure 3. Charge Transistor On-resistance vs. Temperature for different supply voltages. V_{DD}-V_{CH}=0.5V.

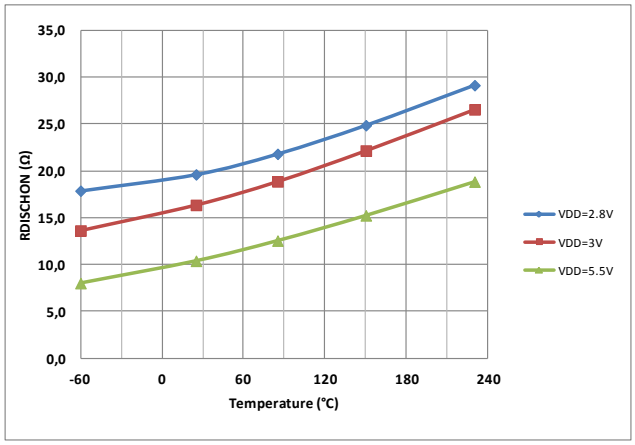


Figure 4. Discharge Transistor On-resistance vs. Temperature for different supply voltages. V_{DISCH}=0.5V.

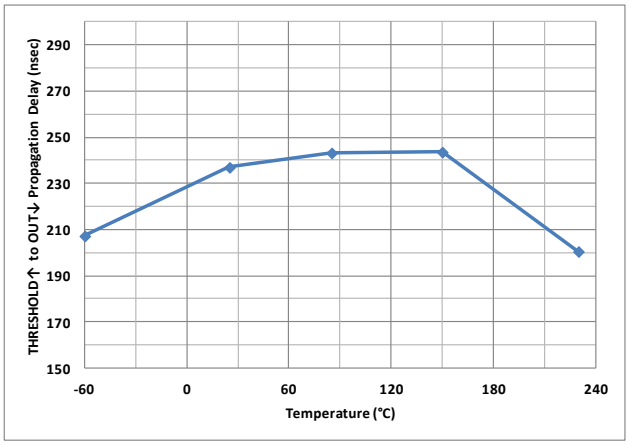
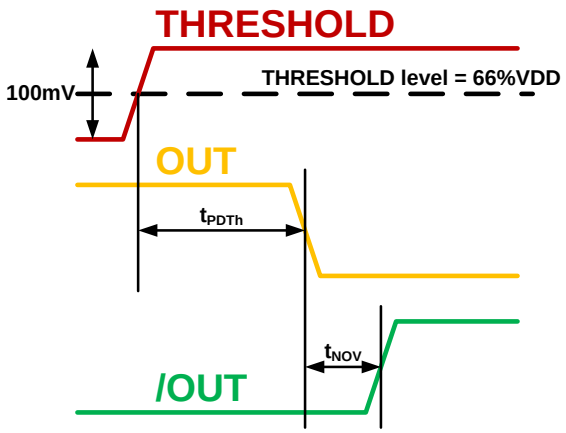


Figure 5. THRESHOLD↑ to OUT↓ propagation delay vs. Temperature: t_{PDTh} (50%-50%). OUT and /OUT loaded with 100pF. V_{DD}=5.0V. See .



TYPICAL PERFORMANCE (CONTINUED)

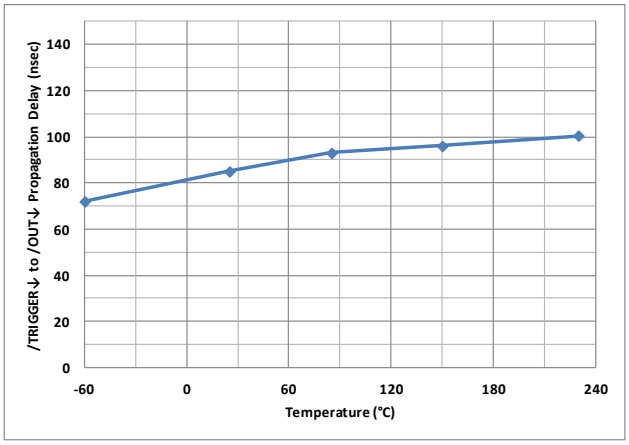
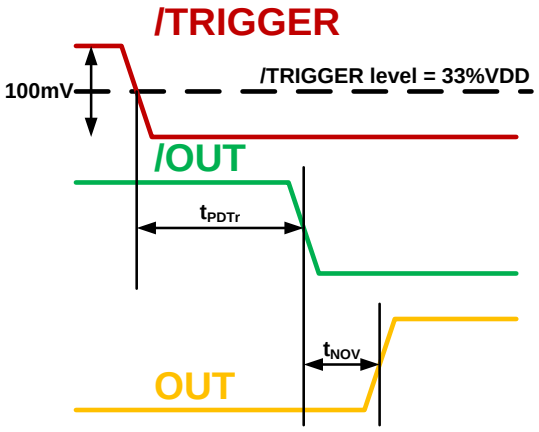


Figure 6. /TRIGGER↓ to /OUT↓ propagation delays vs. Temperature: t_{PDTr} (50%-50%). OUT and /OUT loaded with 100pF. V_{DD}=5.0V. See .



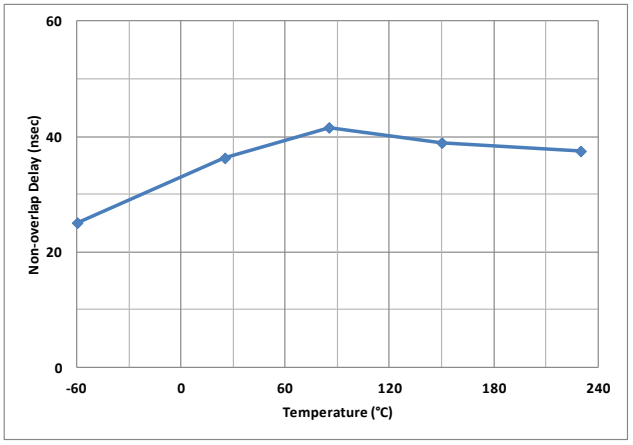


Figure 7. Non-overlap delay vs. Temperature: t_{no} (OUT to /OUT and /OUT to OUT, 50%-50%). OUT and /OUT loaded with 100pF. V_{DD}=5.0V. See .

TYPICAL PERFORMANCE (CONTINUED)

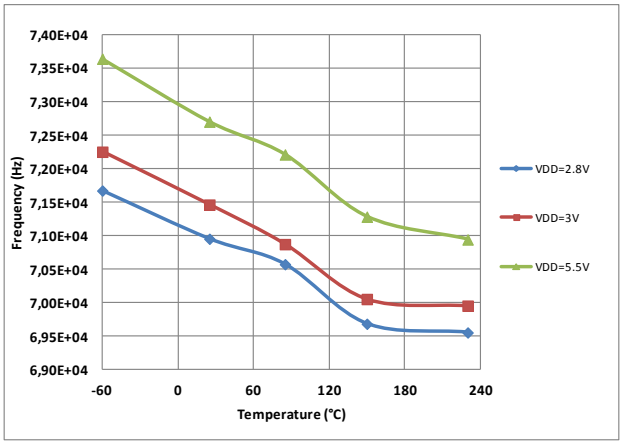


Figure 8. Oscillation frequency in astable mode vs. Temperature (see). R_A=1k, R_B=1k, C=9.7nF.

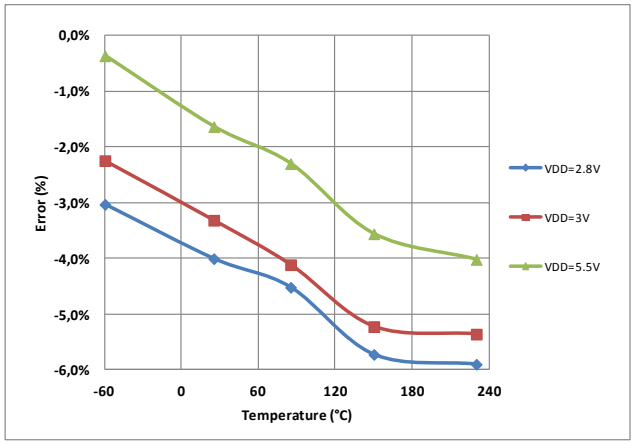


Figure 9. Error of oscillation frequency in astable mode vs. Temperature with respect to the theoretical value (see). R_A=1k, R_B=1k, C=9.7nF.

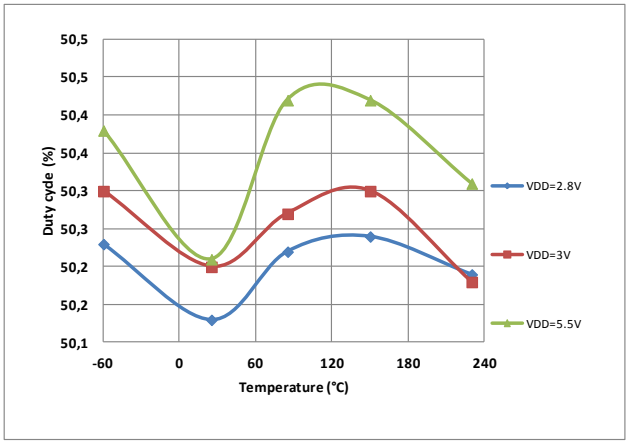


Figure 10. Duty-ratio in astable mode vs. Temperature (see). R_A=1k, R_B=1k, C=9.7nF.

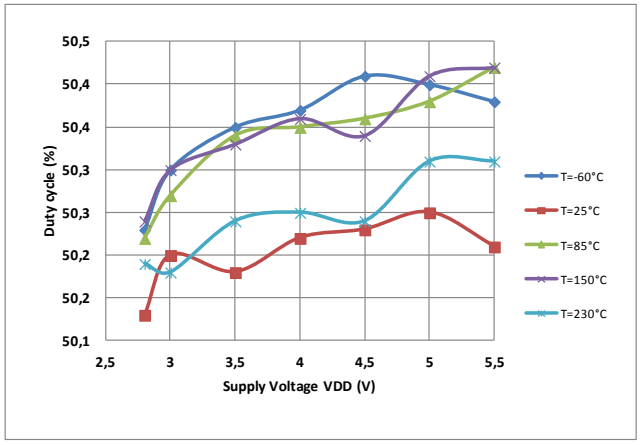


Figure 11. Duty-ratio in astable mode vs. Supply Voltage (see). R_A=1k, R_B=1k, C=9.7nF.

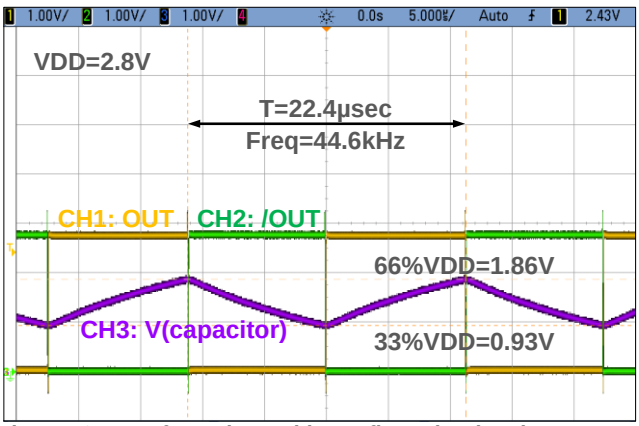


Figure 12. Waveforms in astable configuration (see). V_{DD}=2.8V, Ra=15k, Rb=15k, C=1.06nF.

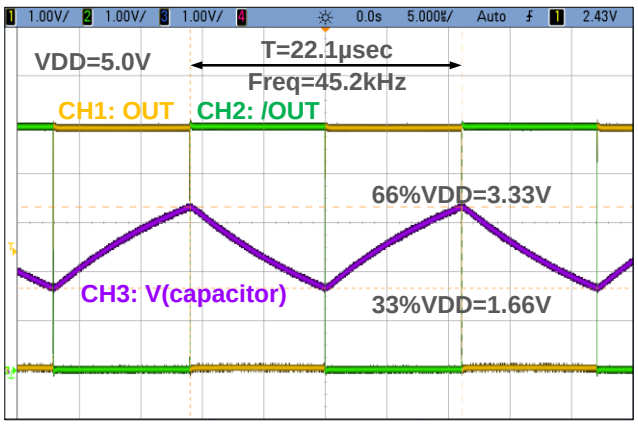


Figure 13. Waveforms in astable configuration (see). V_{DD}=5.0V, Ra=15k, Rb=15k, C=1.06nF.

TYPICAL PERFORMANCE (CONTINUED)

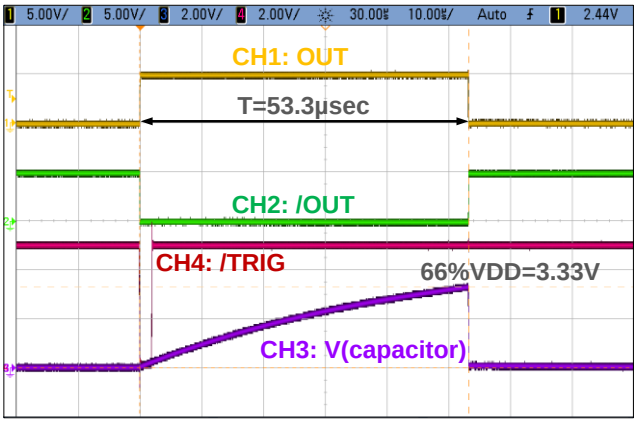


Figure 14. Waveforms in monostable configuration. Triggered by a negative going trigger signal applied on /TRIGGER (see Figure 20). V_{DD}=5.0V, R_A=15k, C=1.06nF.

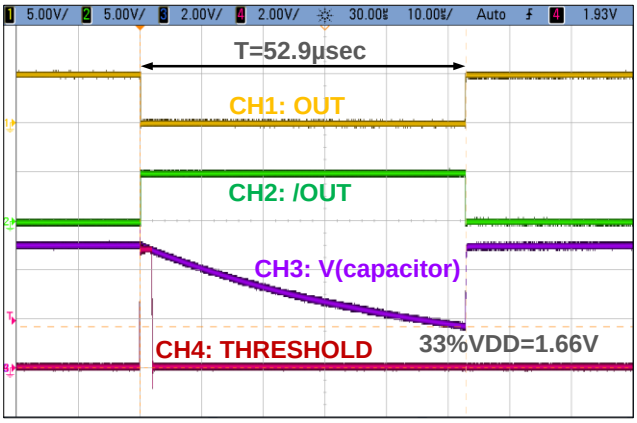


Figure 15. Waveforms in monostable configuration. Triggered by a positive going trigger signal applied on THRESHOLD (see Figure 21). V_{DD}=5.0V, R_A=15k, C=1.06nF.

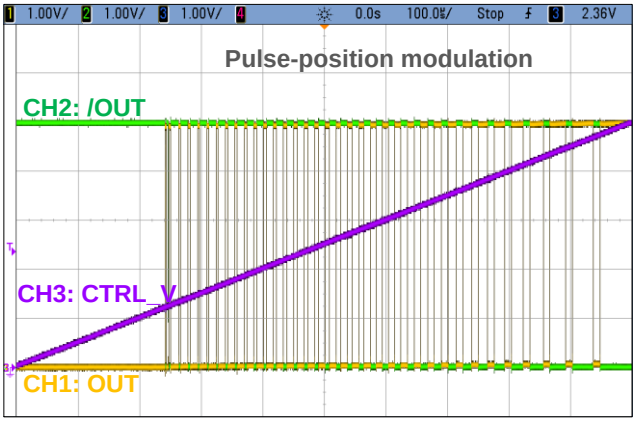


Figure 16. Waveforms in Pulse Position Modulation (PPM): astable configuration with modulating signal on CONTROL_V (see Figure 22). V_{DD}=5.0V, R_A=R_B=15k, C=1.06nF.

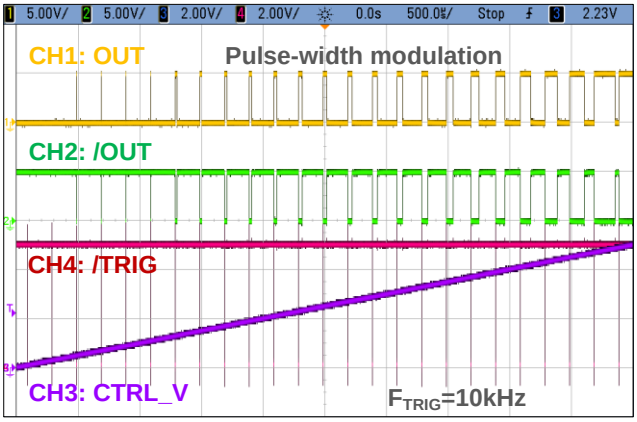


Figure 17. Waveforms in Pulse Width Modulation (PWM): externally retriggered monostable configuration with modulating signal on CONTROL_V (see Figure 23). V_{DD}=5.0V, F_{TRIG}=10kHz, R_A=R_B=15k, C=1.06nF.

TEST CIRCUIT CONFIGURATION

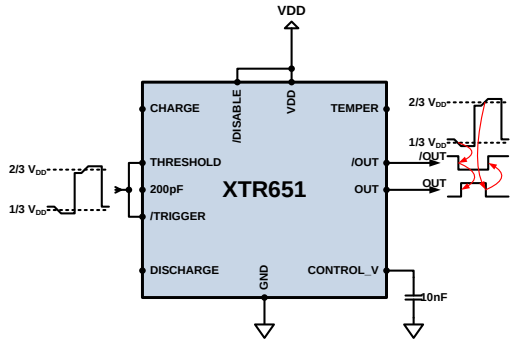


Figure 18. Test circuit used for propagation delay and non-overlap time measurements.

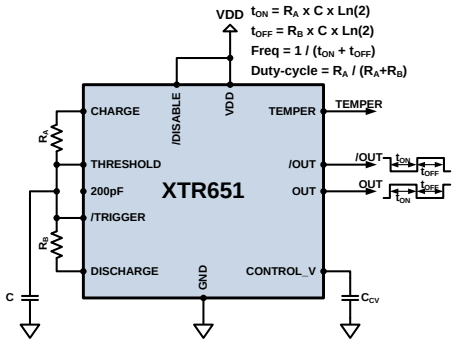


Figure 19. Test circuit used for astable oscillation.

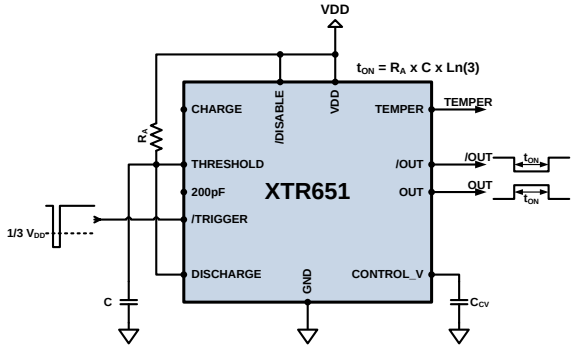


Figure 20. Test circuit for monostable configuration with negative going trigger signal applied on /TRIGGER.

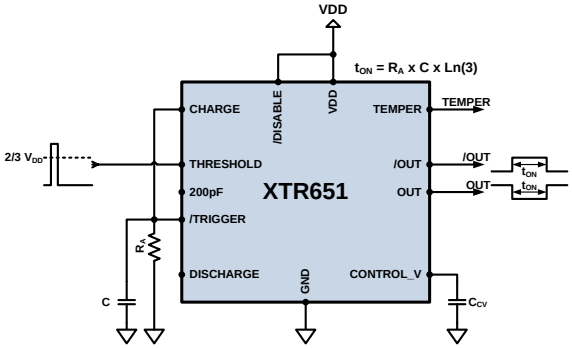


Figure 21. Test circuit for monostable configuration with positive going trigger signal applied on THRESHOLD.

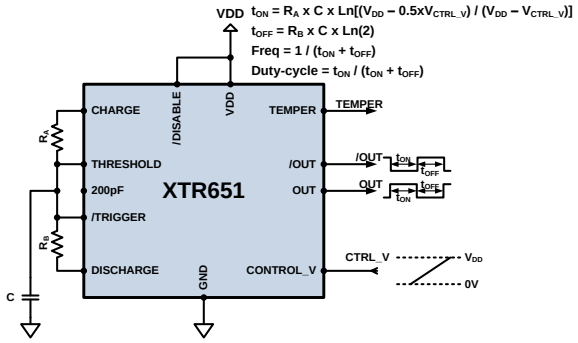


Figure 22. Test circuit for Pulse Position Modulation (PPM): astable configuration with modulating signal on CONTROL_V.

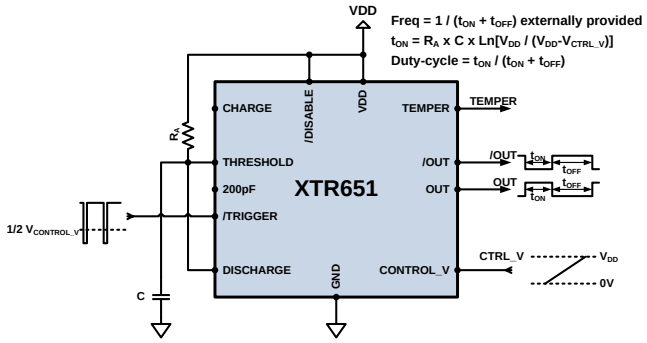


Figure 23. Test circuit for Pulse Width Modulation (PWM): externally retriggered monostable configuration with modulating signal on CONTROL_V.

THEORY OF OPERATION

Introduction

The XTR650 is a family of versatile timers able to operate from -60°C to +230°C, with supply voltages from 2.8V to 5.5V. It can operate as astable, monostable, pulse-width modulator and pulse-position modulator.

Packaging configuration XTR655 can be used as a drop-in replacement of the well known 555. The only difference in the functionality of XTR655 and another commercial 555 concerns the behavior when /DISABLE of the XTR655 is pulled LOW. In the XTR655, the disabled state does not reset the timer. When recovering from the disabled state, outputs will return to their state previous to asserting /DISABLE=LOW or to those determined by the state of THRESHOLD and /TRIGGER.

The XTR650 offers several other packaging configurations allowing the use of the XTR650 specific features.

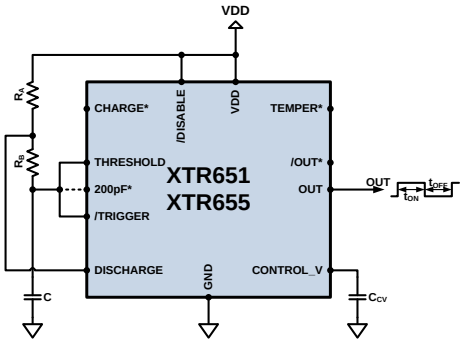
XTR650 design presents a symmetry with respect to VDD/GND. This feature is implemented by the inclusion of complementary outputs (OUT and /OUT) as well as complementary high-voltage open-drain switches (CHARGE and DISCHARGE). This symmetry allows the XTR650 to implement monostable configurations which can be triggered with either falling or rising edges, circumventing the limitation of the standard 555. Additionally, as only one resistor is used as charge or discharge path of the timing capacitor when operating in astable mode, the output duty cycle can be selected from virtually zero to 100%, which also circumvents a limitation of the standard 555.

Operation Modes

Astable Modes

Astable configurations can be implemented in several ways. The principle of the astable configuration is to periodically charge and discharge a capacitor (internal or external) between two fixed levels. In XTR650 parts, as well as in any “555” part, the timing capacitor charges and discharges between the threshold (≈2/3V_{DD}) and trigger (≈1/3V_{DD}) levels. As the timing capacitor charges, the output remains at the HIGH state for a period equal to t_{ON}. When the voltage on the capacitor reaches 2/3V_{DD}, the output pin goes down and remains LOW for t_{OFF} seconds. During this period, the capacitor is discharged until its voltage reaches 1/3V_{DD}. At this moment, the output goes up to V_{DD} and the capacitor starts charging again starting a new oscillation cycle.

The most known astable, though not the most flexible, is the standard one used with the “555” where a capacitor is charged and discharged through two distinct current paths. The “charge” path uses R_A in series with R_B, whereas the “discharge” path uses only R_B. This configuration can be implemented with both XTR651 and XTR655 parts as shown in the figure below. Pins marked with asterisk (*) are only present in the XTR651 and can be left floating in this configuration, though it is recommended to connect CHARGE and 200pF pins to V_{DD}. Notice that the internal 200pF capacitor can be used as timing capacitor.



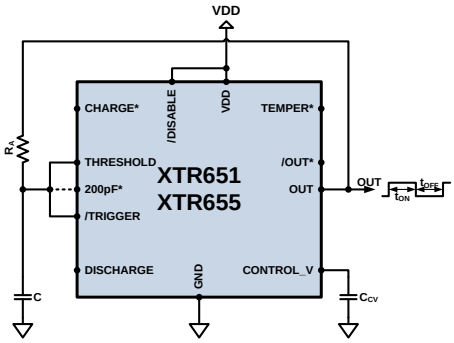
The timing equations are the following:

$$t_{ON} = Ln2 \cdot (R_A + R_B) \cdot C$$
$$t_{OFF} = Ln2 \cdot R_B \cdot C$$
$$t = t_{ON} + t_{OFF}$$

$$Freq = \frac{1}{t} = \frac{1}{Ln2 \cdot (R_A + 2R_B) \cdot C} \approx \frac{1.44}{(R_A + 2R_B) \cdot C}$$

$$Duty - cycle = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{R_A + R_B}{R_A + 2R_B} > 50\%$$

Another possibility is to implement a single resistor configuration as shown in the image below, where the same resistor is used in the “charge” and “discharge” paths. As in the previous case, the internal 200pF capacitor can be used as timing capacitor and CHARGE and DISCHARGE can be left floating if not used. However, it is recommended to connect CHARGE to VDD and DISCHARGE to GND in order to reduce noise.



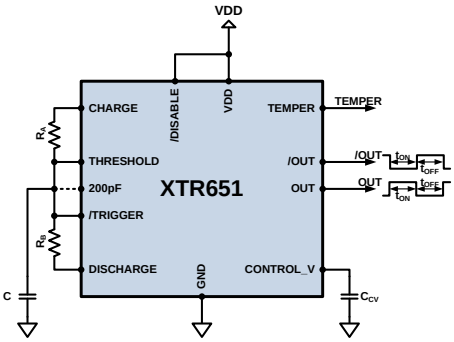
The timing equations in this configuration are:

$$t_{ON} = Ln2 \cdot R_A \cdot C$$
$$t_{OFF} = Ln2 \cdot R_A \cdot C$$
$$t = t_{ON} + t_{OFF}$$

$$Freq = \frac{1}{t} = \frac{1}{Ln2 \cdot 2R_A \cdot C} \approx \frac{0.72}{R_A \cdot C}$$

$$Duty - cycle = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{R_A}{2R_A} = 50\%$$

A more flexible astable configuration can be implemented with the XTR651 versions. This configuration uses two resistors, each used only in either the charge or discharge path of the timing capacitor. The timing capacitor can be internal (200pF), external or a combination of the internal and external one.



The timing equations in this configuration are:

$$t_{ON} = Ln2 \cdot R_A \cdot C$$
$$t_{OFF} = Ln2 \cdot R_B \cdot C$$
$$t = t_{ON} + t_{OFF}$$

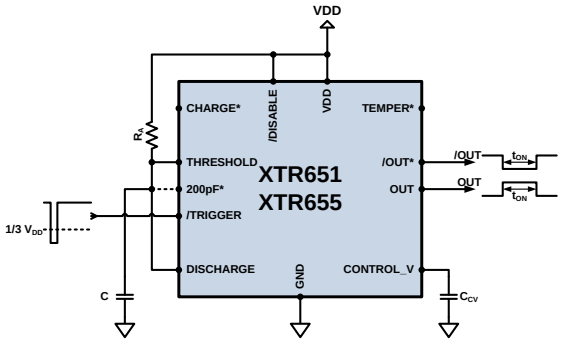
$$Freq = \frac{1}{t} = \frac{1}{Ln2 \cdot (R_A + R_B) \cdot C} \approx \frac{1.44}{(R_A + R_B) \cdot C}$$

$$Duty - cycle = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{R_A}{R_A + R_B}$$

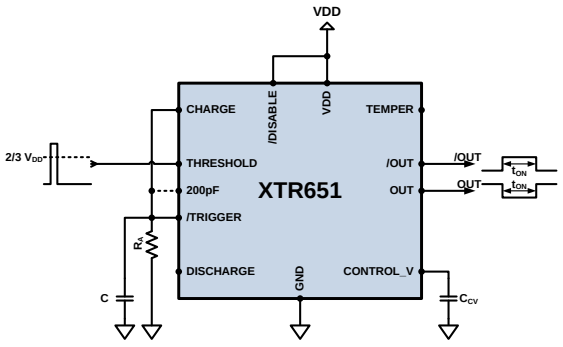
Notice that in the last astable configuration the oscillation frequency depends only on (R_A+R_B) and C whereas the duty-cycle can be chosen to be any value, from virtually 0% to 100%, by

selecting the appropriate R_A, provided that R_A+R_B remains constant.
In all astable configurations the duty-cycle is independent of the value of the timing capacitor.

Monostable Modes
Two simple monostable configurations can be implemented with the XTR651. One of these configurations is identical to that implemented with any 555. A second monostable configuration is derived from the previous one, and makes use of the symmetry of the XTR651 structure. These two configurations can be seen as the complementary from each other. In both cases, the timing capacitor charges and discharges through a single resistor R_A.
In the first configuration, initially output OUT is LOW (/OUT is HIGH) and the timing capacitor is discharged. When /TRIGGER is shortly pulled under $1/3V_{DD}$, OUT goes HIGH (/OUT goes LOW) and the timing capacitor starts charging to V_{DD} through R_A. When the voltage on the timing capacitor reaches $2/3V_{DD}$, the internal flip-flop is reset and the DISCHARGE switch shorts the capacitor to GND. In this case OUT presents a positive pulse and /OUT presents a negative pulse. This configuration can also be implemented with an XTR655. In the figure below, pins marked with an asterisk (*) are available only in the XTR651 version.



In the second configuration, initially output OUT is HIGH (/OUT is LOW) and the timing capacitor is fully charged to V_{DD}. When THRESHOLD is shortly pulled above $2/3V_{DD}$, OUT goes to LOW (/OUT goes HIGH) and the timing capacitor starts discharging to GND through R_A. When the voltage on the timing capacitor reaches $1/3V_{DD}$, the internal flip-flop is set and the CHARGE switch shorts the capacitor to V_{DD}. In this case OUT presents a negative pulse and /OUT presents a positive pulse.

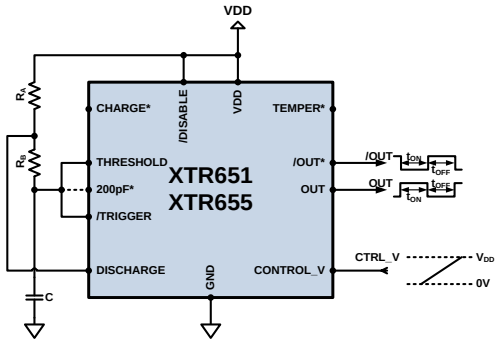


In both monostable configurations the timing period lasts

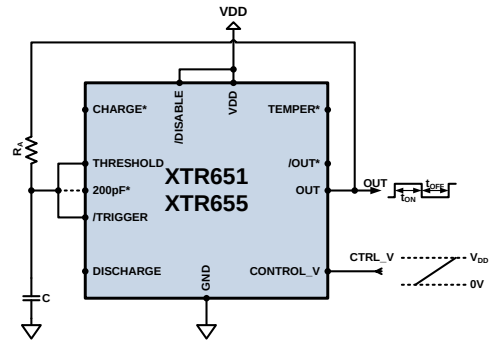
$$t_{ON} = Ln3 \cdot R_A \cdot C \approx 1.1 \cdot R_A \cdot C$$

Applications

Pulse Position Modulation (PPM) Generator
A pulse position modulator is a system that generates a fixed width pulse (positive or negative) with a varying total period (frequency) which depends upon the value of a modulating signal.
This modulator can be derived from the astable configuration, where the modulating signal is provided through the CONTROL_V pin. Any of the three astable configurations presented above can be used. What changes among these configurations is the dependence of the ON-time upon the control voltage.
Below are shown the different astable configurations and the associated timing equations. In the figures below, pins marked with an asterisk (*) are only available in the XTR651 version.

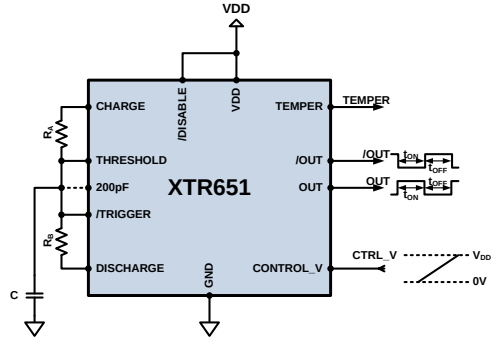


$$t_{ON} = (R_A + R_B) \cdot C \cdot Ln\left(\frac{V_{DD} - 0.5 \cdot V_{CONTROL\_V}}{V_{DD} - V_{CONTROL\_V}}\right)$$
$$t_{OFF} = Ln2 \cdot R_B \cdot C$$
$$t = t_{ON} + t_{OFF}$$
$$Freq = \frac{1}{t}$$
$$Duty - cycle = \frac{t_{ON}}{t_{ON} + t_{OFF}}$$



$$t_{ON} = R_A \cdot C \cdot Ln\left(\frac{V_{DD} - 0.5 \cdot V_{CONTROL\_V}}{V_{DD} - V_{CONTROL\_V}}\right)$$
$$t_{OFF} = Ln2 \cdot R_A \cdot C$$
$$t = t_{ON} + t_{OFF}$$
$$Freq = \frac{1}{t}$$
$$Duty - cycle = \frac{t_{ON}}{t_{ON} + t_{OFF}}$$

Notice that in this configuration the duty-cycle is independent of the timing resistor and capacitor.



$$t_{ON} = R_A \cdot C \cdot Ln\left(\frac{V_{DD} - 0.5 \cdot V_{CONTROL\_V}}{V_{DD} - V_{CONTROL\_V}}\right)$$
$$t_{OFF} = Ln2 \cdot R_B \cdot C$$
$$t = t_{ON} + t_{OFF}$$

$$Freq = \frac{1}{t}$$

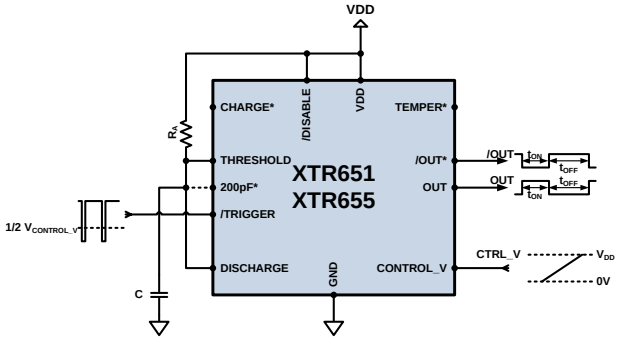
$$Duty - cycle = \frac{t_{ON}}{t_{ON} + t_{OFF}}$$

In all PPM generators presented the OFF-time does not depend on the modulation voltage.

Pulse Width Modulation (PWM) Generator

A pulse width modulator is a system that generates a fixed frequency signal with duty-cycle depending upon a modulating signal.

This modulator can be implemented based on the standard monostable configuration triggered in a periodic manner by an external fixed frequency source, where the modulating signal is provided through the CONTROL_V pin.



$$Freq = \frac{1}{t}$$

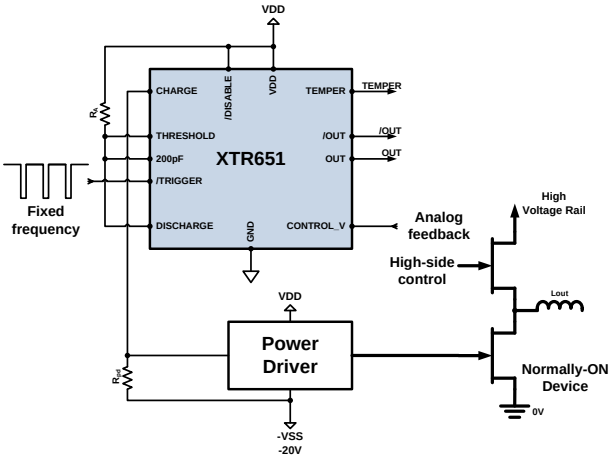
$$t_{ON} = R_A \cdot C \cdot Ln\left(\frac{V_{DD}}{V_{DD} - V_{CONTROL\_V}}\right)$$

$$Duty - cycle = t_{ON} \cdot Freq$$

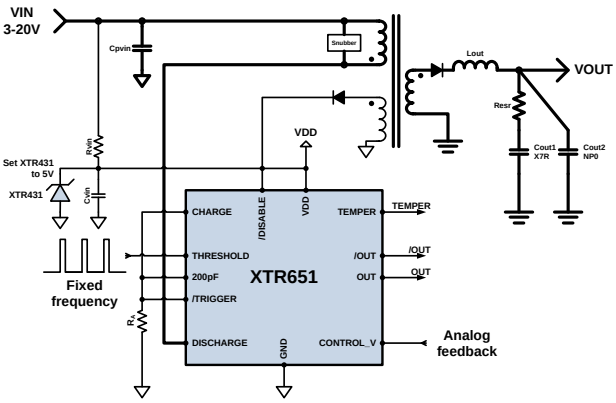
High-voltage Open-drain Outputs (CHARGE / DISCHARGE)

The high-voltage capability of CHARGE and DISCHARGE open-drain outputs widely opens the field of possible applications.

The following figure shows an application where the XTR651 is used to send a PWM signal to a driver with a negative VSS supply voltage. This is typically the case where a power driver is used to control a normally-on jFET transistor. In this case, the CHARGE output (open drain of a PMOS transistor) is used to provide a signal referenced to a negative voltage, used as the control input of a power driver. The power driver is then able to provide a gate signal to the jFET transistor slewing from –VSS to +VDD. A fixed frequency input signal must be provided to the XTR651 in order to periodically trigger the turn-on of the CHARGE output. Input CONTROL_V is used as the analog feedback in order to set the PWM duty-cycle.



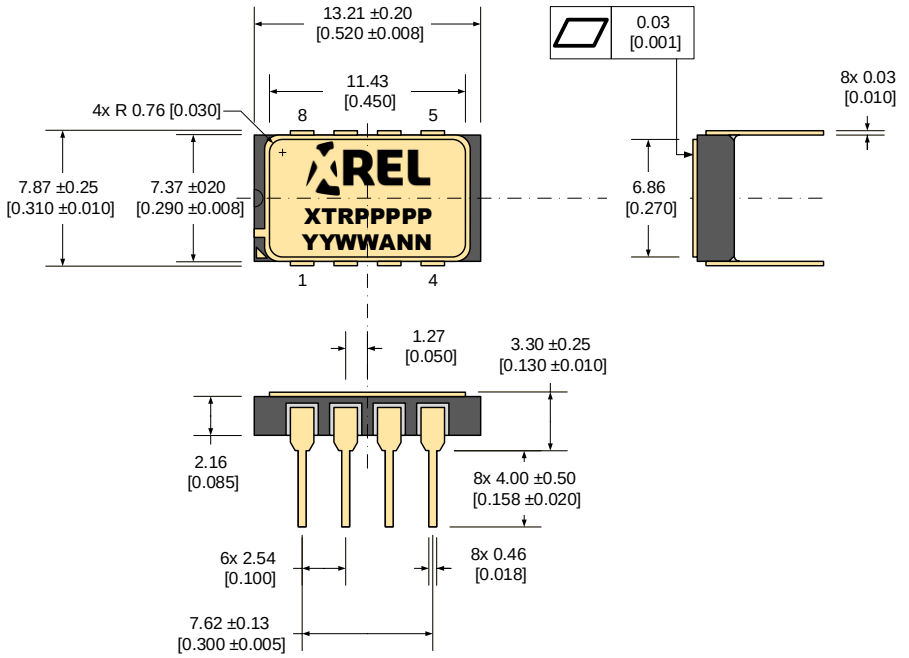
In the following figure, the XTR651 is used to implement a low-power flyback converter. The DISCHARGE output (open drain of an NMOS transistor) is used to drive the primary winding of the flyback transformer. Input CONTROL_V is used as the analog feedback in order to set the PWM duty-cycle to control the output voltage VOUT.



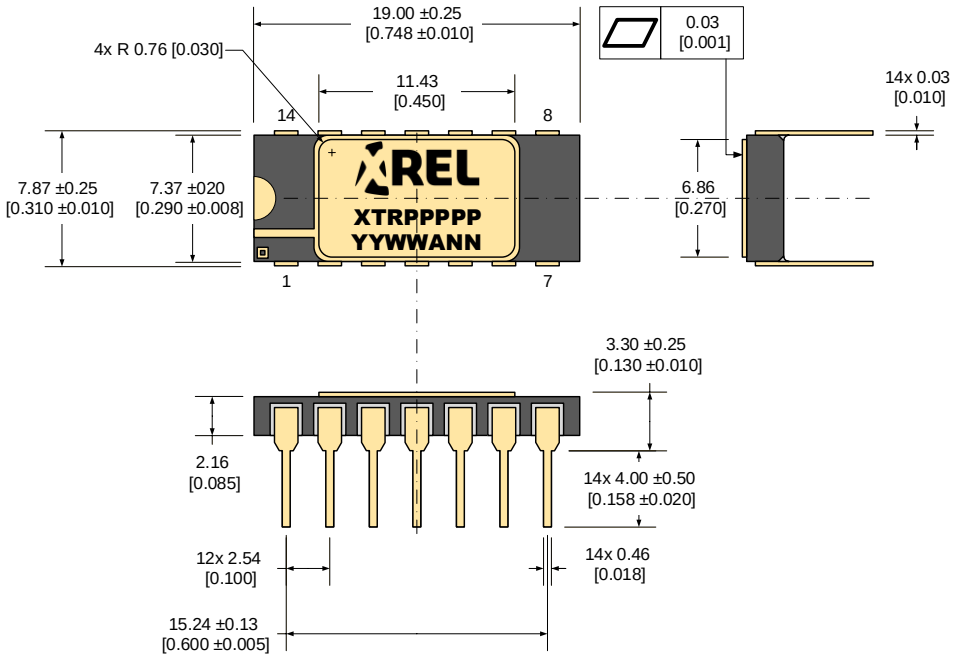
PACKAGE OUTLINES

Dimensions are shown in mm [inches].

SIDE BRAZE CDIP8



SIDE BRAZE CDIP14



Part Marking Convention	
Part Reference: XTRPPPPPP	
XTR	X-REL Semiconductor, high-temperature, high-reliability product (XTRM Series).
PPPPP	Part number (0-9, A-Z).
Unique Lot Assembly Code: YYWWANN	
YY	Two last digits of assembly year (e.g. 11 = 2011).
WW	Assembly week (01 to 52).
A	Assembly location code.
NN	Assembly lot code (01 to 99).

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- ✓ Information: info@x-relsemi.com
- ✓ Support: support@x-relsemi.com

X-REL Semiconductor
90, Avenue Léon Blum
38100 Grenoble
France