

# Dual N-Channel JFET Switch

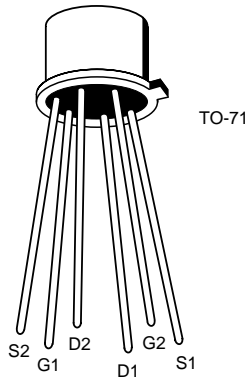


## U401 – U406

### FEATURES

- Minimum System Error and Calibration
- Low Drift With Temperature
- Operates From Low Power Supply Voltages
- High Output Impedance

### PIN CONFIGURATION



CJ2

### ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Gate-Drain or Gate-Source Voltage	50V
Gate Current (Note 1)	10mA
Storage Temperature Range	$-65^\circ\text{C}$ to $+200^\circ\text{C}$
Operating Temperature Range	$-55^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10sec)	$+300^\circ\text{C}$

	One Side	Both Sides
Power Dissipation ( $T_A = 85^\circ\text{C}$ )	300mW	500mW
Derate above $25^\circ\text{C}$	2.6mW/ $^\circ\text{C}$	5mW/ $^\circ\text{C}$

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ORDERING INFORMATION

Part	Package	Temperature Range
U401-6	Hermetic TO-71	$-55^\circ\text{C}$ to $+150^\circ\text{C}$
XU401-6	Sorted Chips in Carriers	$-55^\circ\text{C}$ to $+150^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

SYMBOL	PARAMETER	U401		U402		U403		U404		U405		U406		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$BV_{GSS}$	Gate-Source Breakdown Voltage	-50		-50		-50		-50		-50		-50		V	$V_{DS} = 0, I_G = -1\mu\text{A}$
$I_{GSS}$	Gate Reverse Current (Note 2)		-25		-25		-25		-25		-25		-25	pA	$V_{DS} = 0, V_{GS} = -30\text{V}$
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-5	-2.5	-5	-2.5	-5	-2.5	-5	-2.5	-5	-2.5	-5	-2.5	V	$V_{DS} = 15\text{V}, I_D = 1\text{nA}$
$V_{GS(on)}$	Gate-Source Voltage (on)		-2.3		-2.3		-2.3		-2.3		-2.3		-2.3		$V_{DG} = 15\text{V}, I_D = 200\mu\text{A}$
$I_{DSS}$	Saturation Drain Current (Note 3)	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA	$V_{DS} = 10\text{V}, V_{GS} = 0$
$I_G$	Operating Gate Current (Note 2)		-15		-15		-15		-15		-15		-15	pA	$V_{DG} = 15\text{V}, I_D = 200\mu\text{A}$ $T_A = 125^\circ\text{C}$
			-10		-10		-10		-10		-10		-10	nA	
$BV_{G1-G2}$	Gate-Gate Breakdown Voltage	$\pm 50$		$\pm 50$		$\pm 50$		$\pm 50$		$\pm 50$		$\pm 50$		V	$V_{DS} = 0, V_{GS} = 0,$ $I_G = \pm 1\mu\text{A}$
$g_{fs}$	Common-Source Forward Transconductance (Note 3)	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	$\mu\text{S}$	$V_{DS} = 10\text{V},$ $V_{GS} = 0$ $f = 1\text{kHz}$
$g_{os}$	Common-Source Output Conductance		20		20		20		20		20		20		
$g_{fs}$	Common-Source Forward Transconductance	1000	2000	1000	2000	1000	2000	1000	2000	1000	2000	1000	2000		$V_{DG} = 15\text{V},$ $I_D = 200\mu\text{A}$ $f = 1\text{kHz}$
$g_{os}$	Common-Source Output Conductance		2.0		2.0		2.0		2.0		2.0		2.0		
$C_{iss}$	Common-Source Input Capacitance (Note 6)		8.0		8.0		8.0		8.0		8.0		8.0	pF	$f = 1\text{MHz}$
$C_{rss}$	Common-Source Reverse Transfer Capacitance (Note 6)		3.0		3.0		3.0		3.0		3.0		3.0		
$e_n$	Equivalent Short-Circuit Input Noise Voltage		20		20		20		20		20		20	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	$V_{DS} = 15\text{V},$ $V_{GS} = 0$ $f = 10\text{Hz}$ (Note 6)
CMRR	Common-Mode Rejection Ratio	95		95		95		95		90				dB	$V_{DG} = 10$ to $20\text{V},$ $I_D = 200\mu\text{A}$ (Note 5, 6)
$ V_{GS1} - V_{GS2} $	Differential Gate-Source Voltage		5		10		10		15		20		40	mV	$V_{DG} = 10\text{V}, I_D = 200\mu\text{A}$
$\frac{ \Delta V_{GS1} - V_{GS2} }{\Delta T}$	Gate-Source Voltage Differential Drift (Note 4)		10		10		25		25		40		80	$\mu\text{V}/^\circ\text{C}$	$V_{DG} = 10\text{V},$ $I_D = 200\mu\text{A}$ $T_A = -55^\circ\text{C}$ $T_B = +25^\circ\text{C}$ $T_C = +125^\circ\text{C}$

- NOTES:**
- Per transistor.
  - Approximately doubles for every  $10^\circ\text{C}$  increase in  $T_A$ .
  - Pulse test duration =  $300\mu\text{s}$ ; duty cycle  $\leq 3\%$ .
  - Measured at end points  $T_A, T_B, T_C$ .
  - $\text{CMRR} = 20 \log_{10} \left[ \frac{\Delta V_{DD}}{\Delta |V_{GS1} - V_{GS2}|} \right], \Delta V_{DD} = 10\text{V}.$
  - For design reference only, not 100% tested.