# N-Channel JFET Monolithic Dual

calogic CORPORATION

## U443 / U444

### FEATURES

- **High Gain . . . . . $g_{fs}$ > 6 mS typical**
- **Low Leakage . . . . . $I_G$ < 1pA typical**
- **Low Noise**

### APPLICATIONS

- **Differential Wideband Amplifiers**
- **VHF/UHF Amplifiers**
- **Test and Measurement**
- **Multi-Chip/Hybrids**

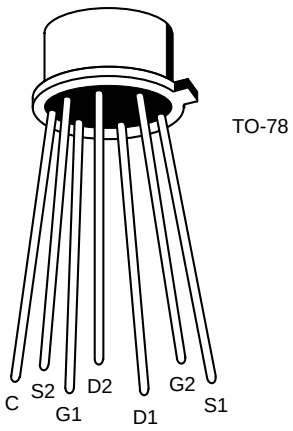
### DESCRIPTION

The U443 Series is an N-Channel Monolithic Dual JFET designed for high speed amplifier circuits. Featuring high gain ( > 6 mS typical), low leakage (< 1pA typical) and low noise this device is an excellent choice for high performance test and measurement, wideband amplifiers and VHF/UHF circuits.

### ORDERING INFORMATION

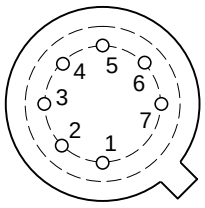
| Part | Package | Temperature Range |
|---|---|---|
| U443-4 | Hermetic M0-002AG (TO-78) | -55°C to +150°C |
| XU443-4 | Sorted Chips in Carriers | -55°C to +150°C |

### PIN CONFIGURATION




TO-78

1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 CASE/BODY
5 SOURCE 2
6 DRAIN 2
7 GATE 2




BOTTOM VIEW

**CJ1**

**ABSOLUTE MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Parameter/Test Condition | Symbol | Limit | Unit |
|---|---|---|---|
| Gate-Drain Voltage | $V_{GD}$ | -25 | V |
| Gate-Source Voltage | $V_{GS}$ | -25 | V |
| Gate-Gate Voltage | $V_{GG}$ | ±50 | V |
| Forward Gate Current | $I_G$ | 50 | mA |
| Power Dissipation (per side) | $P_D$ | 367 | mW |
| (total) | | 500 | mW |
| Power Derating (per side) | | 3 | mW/ °C |
| (total) | | 4 | mW/ °C |
| Operating Junction Temperature | $T_J$ | -55 to 150 | °C |
| Storage Temperature | $T_{stg}$ | -65 to 200 | °C |
| Lead Temperature (1/16" from case for 10 seconds) | $T_L$ | 300 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| SYMBOL | CHARACTERISTCS | TYP[1] | U443 | | U444 | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | | |
| **STATIC** | | | | | | | | |
| $V_{(BR)GSS}$ | Gate-Source Breakdown Voltage | -35 | -25 | | -25 | | V | $I_G$ = -1µA, $V_{DS}$ = 0V |
| $V_{GS(OFF)}$ | Gate-Source Cut off Voltage | -3.5 | -1 | -6 | -1 | -6 | | $V_{DS}$ = 10V, $I_D$ = 1nA |
| $I_{DSS}$ | Saturation Drain Current [2] | 15 | 6 | 30 | 6 | 30 | mA | $V_{DS}$ = 10V, $V_{GS}$ = 0V |
| $I_{GSS}$ | Gate Reverse Current | -1 | | -500 | | -500 | pA | $V_{GS}$ = -15V, $V_{DS}$ = 0V |
| | | -2 | | | | | nA | $T_A$ = 150°C |
| $I_G$ | Gate Operating Current | -1 | | -500 | | -500 | pA | $V_{DG}$ = 10V, $I_D$ = 5mA |
| | | -0.3 | | | | | nA | $T_A$ = 125°C |
| $V_{GS(F)}$ | Gate-Source Forward Voltage | 0.7 | | | | | V | $I_G$ = 1mA, $V_{DS}$ = 0V |
| **DYNAMIC** | | | | | | | | |
| $g_{fs}$ | Common-Source Forward Transconductance | 6 | 4.5 | 9 | 4.5 | 9 | mS | $V_{DG}$ = 10V, $I_D$ = 5mA f = 1kHz |
| $g_{os}$ | Common-Source Output Conductance | 70 | | 200 | | 200 | µS | |
| $C_{iss}$ | Common-Source Input Capacitance | 3 | | | | | pF | $V_{DG}$ = 10V, $I_D$ = 5mA f = 1MHz |
| $C_{rss}$ | Common-Source Reverse Transfer Capacitance | 1 | | | | | | |
| $\bar{e}_n$ | Equivalent Input Noise Voltage | 4 | | | | | nV/$\sqrt{Hz}$ | $V_{DG}$ = 10V, $I_D$ = 5mA f = 10kHz |
| **MATCHING** | | | | | | | | |
| $\lvert V_{GS1}-V_{GS2}\rvert$ | Differential Gate-Source Voltage | 6 | | 10 | | 20 | mV | $V_{DG}$ = 10V, $I_D$ = 5mA |
| $\frac{\Delta \lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$ | Gate-Source Voltage Differential Change with Temperature | 20 | | | | | µV/ °C | T = -55 to 25°C; $V_{DG}$ =10V, $I_D$ = 5mA |
| | | 20 | | | | | | T = 25 to 125°C; $V_{DG}$ =10V, $I_D$ = 5mA |
| $\frac{I_{DSS1}}{I_{DSS2}}$ | Saturation Drain Current Ratio | 0.97 | | | | | | $V_{DS}$ = 10V, $V_{GS}$ = 0V |
| $\frac{g_{fs1}}{g_{fs2}}$ | Transconductance Ratio | 0.97 | | | | | | $V_{DG}$ = 10V, $I_D$ = 5mA f= 1 kHz |
| CMRR | Common Mode Rejection Ratio | 85 | | | | | dB | $V_{DD}$ = 5 to 10V, $I_D$ = 5mA |

NOTES: 1. For design aid only, not subject to production testing.
2. Pulse test; PW = 300µs, duty cycle ≤ 3%.