VocalFusion® XVF3610 Voice Processor

DATASHEET

XM-014380-PC - Issue 7

XMOS

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PRODUCT FEATURES

The VocalFusion® XVF3610 is a high-performance voice processor, derived from XMOS xcore.ai, that is optimised for integrated applications. This document should be read in conjunction with the XU316-1024-QF60(A/B) datasheets (See section 8.1) which contains electrical, design and integration data. The XVF3610 has the following key features:

VOICE PROCESSING

- Two PDM microphone interfaces
- Digital signal processing pipeline
  - Full duplex, stereo, Acoustic Echo Cancellation (AEC)
  - Reference audio via I2S with automatic bulk delay insertion
  - Point noise suppression via interference canceller
  - Switchable stationary noise suppressor
- Programmable Automatic Gain Control (AGC)
- Independent audio paths for communications and Automatic Speech Recognition (ASR)

DEVICE INTERFACES

- Full speed USB2.0 compliant device supporting USB Audio Class (UAC) 1.0
- USB HID and Endpoint 0 control interfaces
- Flexible Peripheral Interfaces
  - Programmable digital general-purpose inputs and outputs
  - I2C interface for system control and local peripheral control
  - I2S slave interface input & output of audio data
  - SPI master interface for control and interrogation of a local SPI slave devices

FIRMWARE MANAGEMENT

- Boot from QSPI Flash
  - Default firmware image for power-on operation
  - Update image delivered via USB
  - Persistent user data maintained across firmware upgrade cycles
  - User-programmable setup for SPI peripherals
- Option to boot from a local host processor via SPI
- Device Firmware Update (DFU) via I2C or USB

PACKAGE

- 7mm x 7mm 60pin QFN package

POWER CONSUMPTION

- Typical power consumption 300-350mW

CONTENTS

1. VOCALFUSION XVF3610 VOICE PROCESSOR

1.1. XVF3610 OVERVIEW

The XMOS VocalFusion® XVF3610 voice processor uses microphone array processing to capture clear, high-quality audio from anywhere in the room. XVF3610 processors use highly optimised digital signal processing algorithms to implement 'barge-in', suppress point noise sources and reduce ambient noise levels increasing the effective Signal to Noise Ratio (SNR) to achieve a reliable voice interface whatever the environment.

The processor is designed for seamless integration into consumer electronic products requiring voice interfaces for Automatic Speech Recognition (ASR), or communication and conferencing. In addition to the class-leading voice processing, XVF3610 processor implements specific features and interfaces required for use in closely integrated applications such and incorporated into a TV or set-top box.

Two modes of operation are supported by the XVF3610

- 3610-UA - Audio and control via a USB2.0 interface
- 3610-INT – Audio via I2S and control over I2C interfaces

The functional block diagram of the XVF3610 is shown in the figures below.

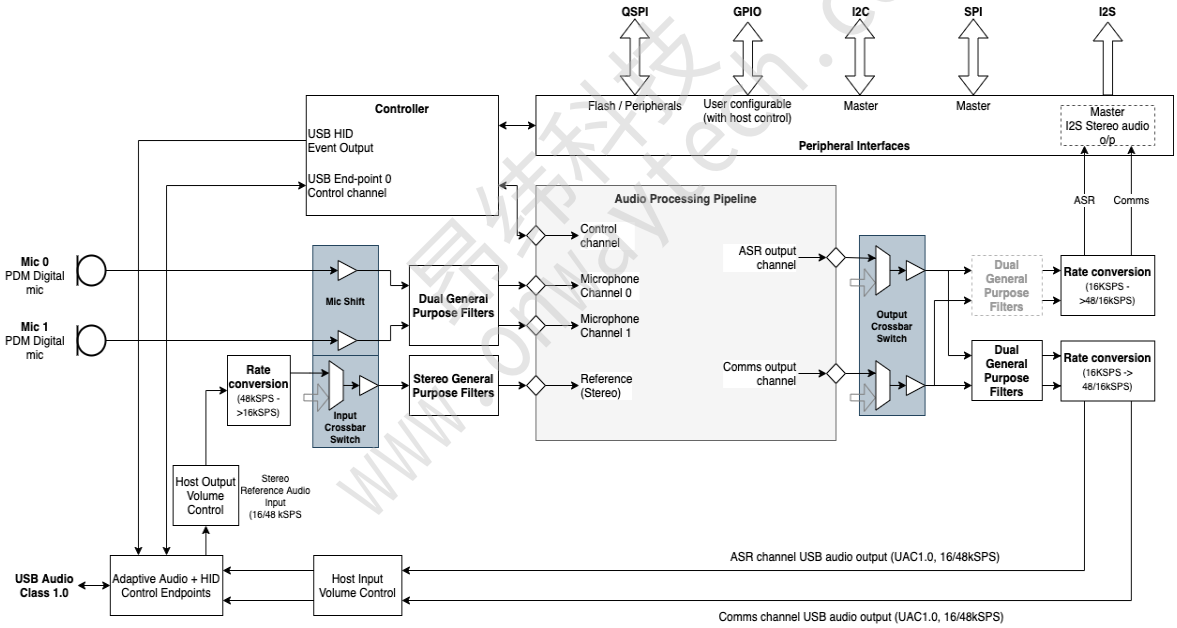

Figure 1-1 Functional block diagram of XVF3610 in UA configuration

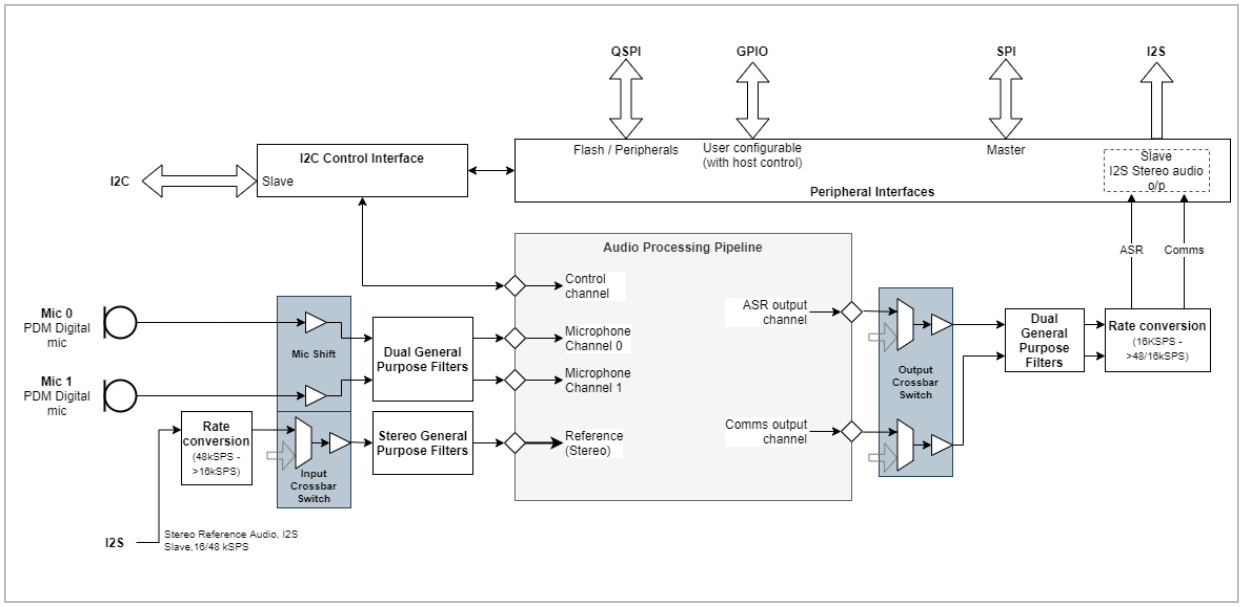

Figure 1-2 Functional block diagram of XVF3610 in INT configuration

The VocalFusion XVF3610 voice processor converts and enhances audio captured using a pair of low-cost digital microphones. Processed audio streams are suitable for use in Automatic Speech Recognition (ASR) or voice communications applications and benefit from a range of configurable audio processing techniques to allow customisation to the use case. The embedded audio processing provides the following features:

- 2 microphone far-field operation.
- Full 360-degree operation in “coffee table” applications or 180 degree for operation in edge-of-room products such as smart TVs.
- 16kHz voice processing, with optional 16kHz and 48kHz interface sample rates.
- Full duplex, Stereo, Acoustic Echo cancellation with a maximum tail length of 225ms accommodating highly reverberant environments. (Reference audio for cancellation provided via I2S Slave interface).
- Automatic bulk delay insertion, of up to 150ms, to account for positive or negative reference audio delays ensuring optimal echo cancellation with all audio output paths.
- Cancellation of point noise sources via a 256-frequency band Interference Canceller.
- Switchable stationary noise suppressor.
- Adjustable gain over a 60dB range with automatic gain control.
- Audio output filtering and range limiter.
- Independent audio processing paths and control of parameters for communications and ASR audio.

The VocalFusion XVF3610 voice processor provides the following additional interfaces to increase usability and reduce total system cost:

- 4 General Purpose Output pins. These can be configured as simple digital I/O pins, Pulse Width Modulated (PWM) outputs and rate adjustable LED flashers.
- 4 General Purpose Input pins. These can be used as simple logic inputs or event capture (edge detection).

- SPI master interface to control and interrogate an SPI slave device, such as ADCs, DACs or external keyword detection devices.

The VocalFusion XVF3610 voice processor can be booted over SPI by a local host processor or from a separate, user-supplied, QSPI Flash memory. When operating with flash, the memory can be used for the following functions:

- A default firmware image for power-on operation.
- An upgrade image. Upgrades are provided via I2C or USB providing a host-controlled upgrade process for over-the-air device management.
- A persistent user information space to allow user-configured data such as board identifiers and serial numbers to be maintained across multiple firmware upgrade cycles.
- An upgradable user command space. Commands stored in this space are executed at boot time allowing the definition of start-up behaviour, VocalFusion XVF3610 configuration and setup of SPI peripheral devices connected to it.

With the exception of the persistent user information the contents of the flash, and therefore the configuration of the system can be upgraded and configured using the Device Firmware Upgrade (DFU) mechanism from the host processor.

Note: The two XVF3610 configurations; one providing I2S/I2C interface (XVF3610-INT) and one providing a USB interface (XVF3610-UA) are delivered as separate sets of firmware.

1.2. XVF3610 AUDIO PROCESSING PIPELINE

The XVF3610 audio processing pipeline takes inputs from a pair of MEMS Pulse Density Modulation (PDM) microphones and uses advanced signal processing to create audio streams suitable for use in Automatic Speech Recognition (ASR) and voice communication applications. The block diagram of this audio processing pipeline is shown in the figure below.

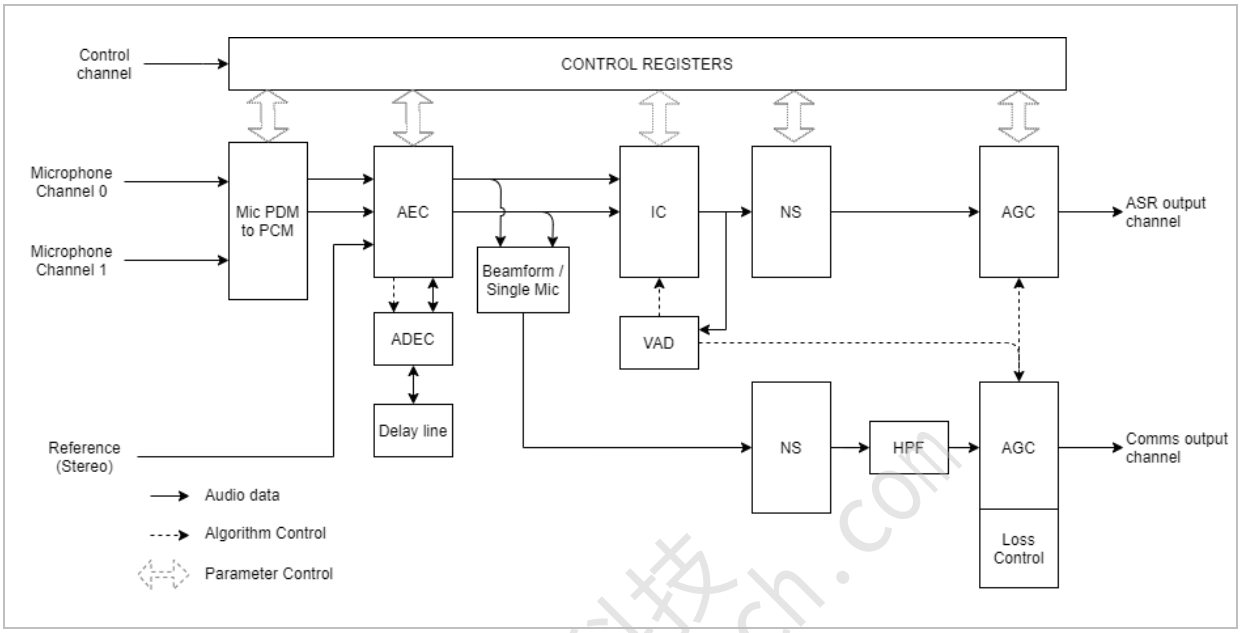

Figure 1-3 XVF3610 audio processing pipeline

The pipeline enhances the captured audio stream using a set of complementary signal enhancement and noise reduction processes:

- **Microphone Pulse Density Modulation (PDM) to Pulse Code Modulation (PCM) conversion:** Converts the PDM audio input from the microphones into PCM format allowing further processing.
- **Acoustic Echo Cancellation (AEC):** enables the XVF3610 to detect voice signals in the presence of high volume, stereo audio from the product into which it is integrated. This process takes the stereo audio from the product as a reference signal and models the echo characteristics between each speaker and microphone caused by the acoustic environment of the device and room. These four models are used to continuously remove the echoes from out the audio outputs from the microphone audio input. The models are continuously adapted to the acoustic environment to accommodate changes in the room created by events such as doors opening or closing and people moving in the room.
- **The Automatic Delay Estimation Control (ADEC):** automatically monitors and manages the delay between the reference audio and the echo received by the microphone to ensure optimal AEC cancellation when the audio output latency is variable or non-zero.
- **Interference Cancellation (IC):** suppresses static noise from point sources such as cooker hoods, washing machines, or radios for which there is no reference audio signal available. When an internal Voice Activity Detector (VAD) indicates the absence of voice, the IC adapts to suppress point noise sources in the environment. When voice is detected adaption is suspended maintaining suppression of the interfering noise source.

- **Noise Suppression (NS):** suppresses diffuse noise from sources whose frequency characteristics do not change rapidly over time such as air conditioning or city background noise.
- **Automatic Gain Control (AGC):** tunes separate AGC channels for Automatic Speech Recognition (ASR) and communications output. The internal VAD is used to prevent gain changes in the ASR output channel during speech to improve speech recognition performance.

1.3. REFERENCE SIGNAL DELAY

As shown above, the XVF3610 includes an Automatic Delay Estimator Control (ADEC) which is used to time-align the reference and microphone signals, allowing the AEC to work effectively. This is an essential aspect of device operation for situations where the audio output path is unknown, such as in TVs and set-top box architectures.

The ADEC applies a time shift to one of the signals based on an automatic estimate between them or a user-defined delay, to deliver a synchronised input to the AEC.

A delay of between 0-150ms can be applied to either the reference signal or microphone input, equivalent to 0-2400 samples at 16kHz sample frequency.

The ADEC runs in one of three modes:

- Automatic - the ADEC runs immediately the device starts. It constantly monitors the reference signal and microphone input for changes of time alignment and automatically adjusts its delay as necessary.
- Manual – in this mode, the ADEC waits in a disabled state until the device is manually triggered by the host. The delay is estimated at the trigger point, or a selected fixed delay applied. The delay set will be used until it is changed by:
  - manually applying a different fixed delay.
  - manually triggering a new delay estimate.
  - switching to automatic mode.
- Estimate on Start-up (default) - The ADEC runs immediately the device starts, calculates the delay between the two signals and applies that delay to all subsequent signals. After making the initial delay estimate and delay setting, no further changes will be made unless manually triggered or automatic mode is selected.

For further information on the usage of ADEC please refer to the XVF3610 User Guide.

1.4. EXAMPLE APPLICATION

The essential components and signals for a XVF3610-INT application using QSPI flash memory with 1V8 I/0 is shown in the figure below.

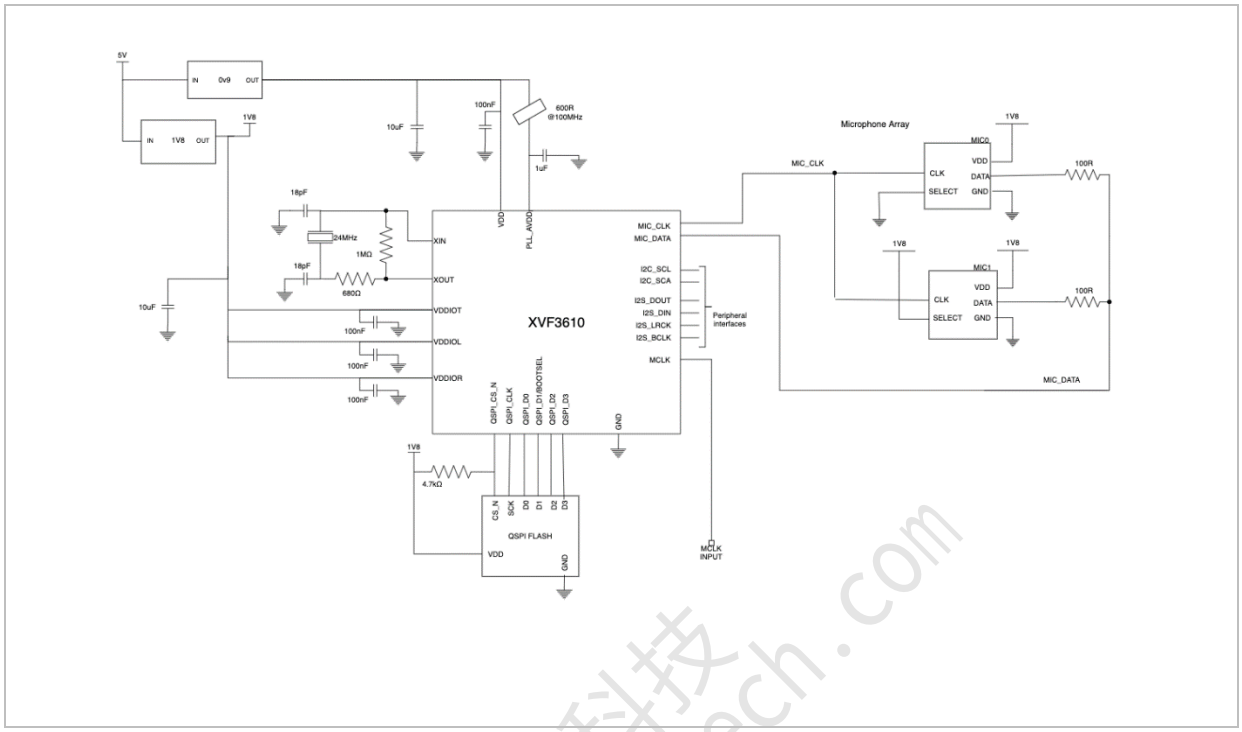

Figure 1-4 Essential components of an XVF3610-INT application with VDDIO = 1V8

The essential components and signals for a XVF3610-UA application 3V3 I/0 is shown in the figure below.

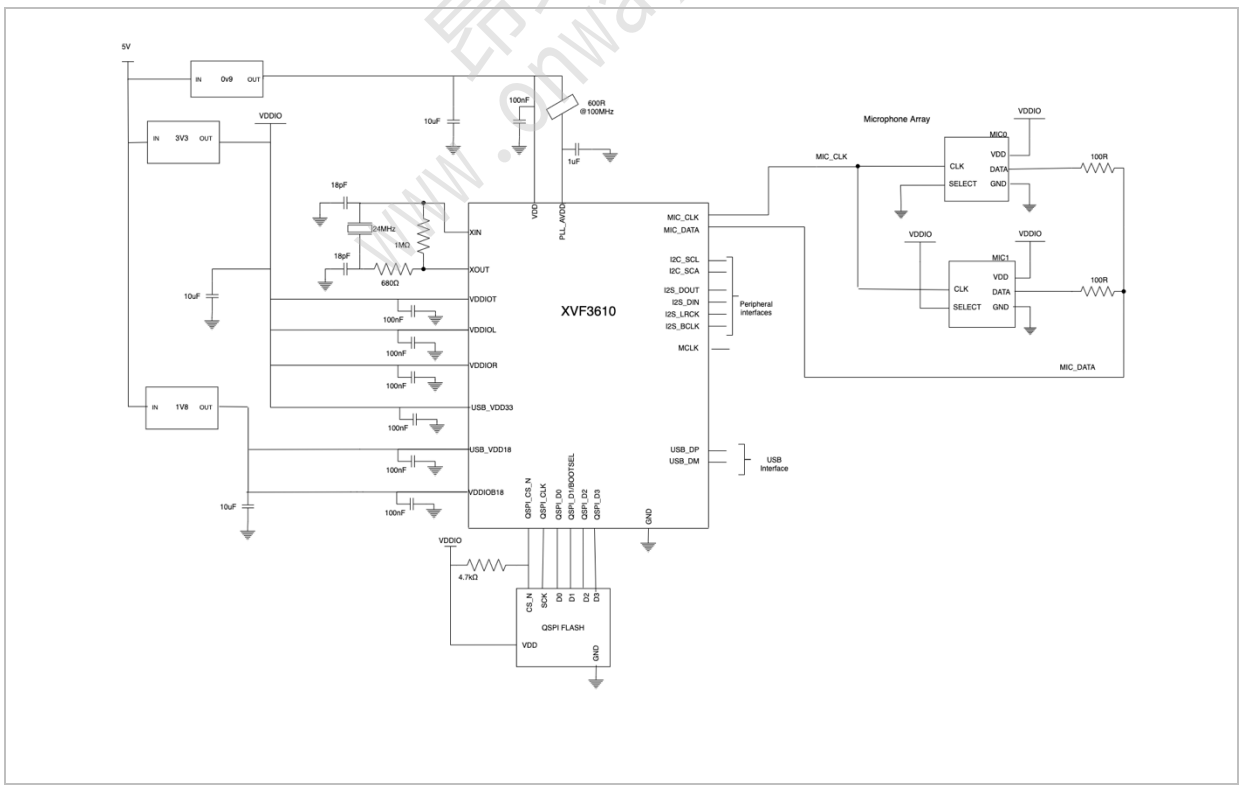

Figure 1-5 Essential components of an XVF3610-UA application with 3V3 IO

2. PIN DIAGRAM

2.1. PIN CONFIGURATION

The pinout of the XVF3610, including all optional interfaces, is shown in the figure below.

Pins marked RESVD are internally connected and should remain unconnected.

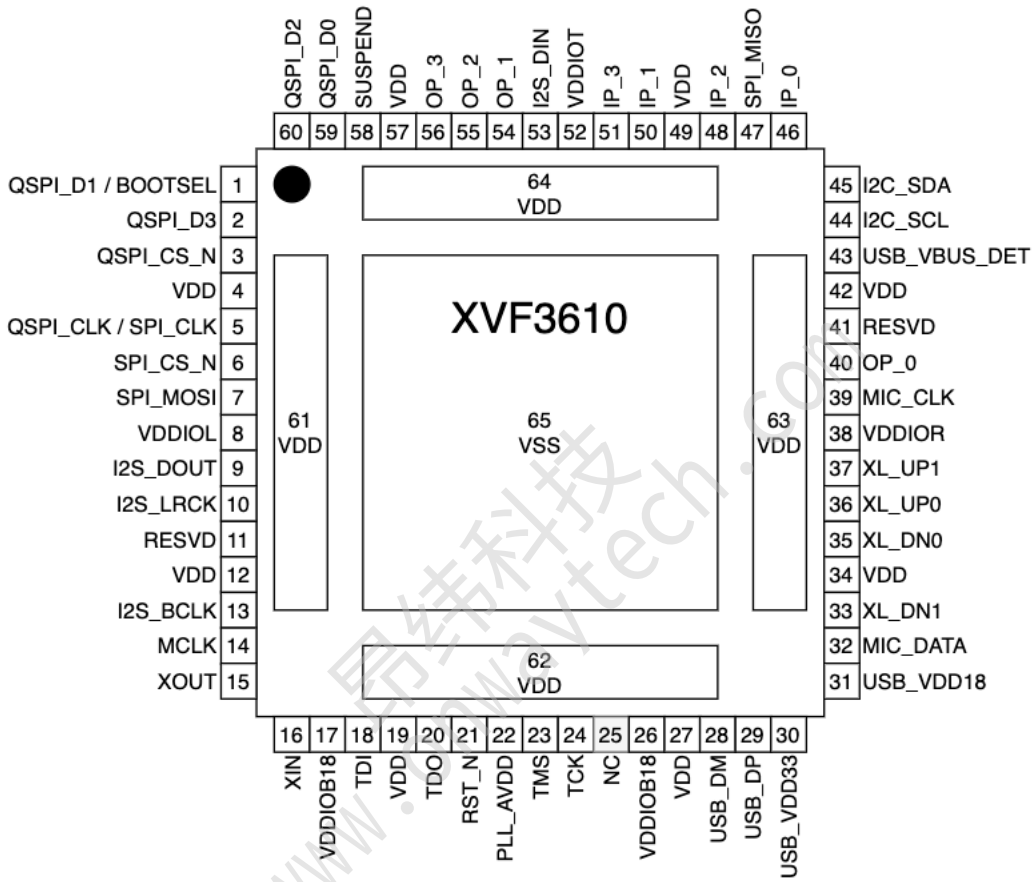

Figure 2-1 VocalFusion XVF3610 Pin configuration

Note: Two package variants are available:

QF60A – (1V8 I/0) – VDDIOT, VDDIOL and VDDIOR should be connected a 1V8 supply

QF60B – (3V3 I/0) – VDDIOT, VDDIOL and VDDIOR should be connected a 3V3 supply

In both variants, VDDIO18 must be connected to a 1V8 supply and all VDD pins must be connected to a 0V9 supply. All package paddles (pins 61 to 65) must be connected. It is advised that vias be placed under paddles to connect directly to PCB supply planes

2.2. SIGNAL DESCRIPTION

The table below lists the functions of all the pins shown in Figure 2-1 above in the order they appear around the package.

> Note: The function of some pins changes depending on the firmware configuration loaded during boot (-INT/-UA).

Table 2-1 XVF3610 pin functions

NAME	PIN	TYPE	DESCRIPTION	INTERFACE MASTER/SLAVE OPERATION			NOTE
				DURING BOOT	-INT CONFIG	-UA CONFIG	
QSPI_D1 / BOOTSEL	1	I/O	QSPI Boot Flash - QSPI Data Line 1 and Boot selection This pin is sampled during power-on-reset to determine boot mode. (High = SPI slave boot mode, Floating/Low = QSPI Flash boot mode)				
QSPI_D3	2	I/O	QSPI Boot Flash - QSPI Data Line 3				
QSPI_CS_N	3	I	QSPI Boot Flash - Chip Select This pin should be pulled high externally to the device using a 4.7k ohm resistor				
QSPI_CLK / SPI_CLK	5	I (when SPI Boot) O (otherwise)	QSPI Boot Flash - QSPI Clock and SPI Clock	Flash clock O/P; or SPI boot clock I/P depending on the state of BOOT_SEL	SPI master clock O/P	SPI master clock O/P	
SPI_CS_N	6	I (when SPI Boot) O (otherwise)	Slave SPI boot / Peripheral SPI Master Chip Select This pin should be pulled high externally to the device using a 4.7k ohm resistor	Slave (I/P) if SPI boot mode	SPI master Chip Select O/P	SPI master Chip Select O/P	

NAME	PIN	TYPE	DESCRIPTION	INTERFACE MASTER/SLAVE OPERATION			NOTE
				DURING BOOT	-INT CONFIG	-UA CONFIG	
SPI_MOSI	7	I (when SPI Boot) O (otherwise)	SPI Master Out Slave In	SPI Slave Data I/P if SPI boot mode	SPI Master Data O/P	SPI Master Data O/P	
VDDIOL	8	PWR	I/O Power Supply				A, B
I2S_DOUT	9	O	Peripheral I2S interface - I2S data output		Slave	Master	
I2S_LRCK	10	I (INT) or O (UA)	Peripheral I2S interface - I2S left-right clock		Slave (Clock I/P)	Master (Clock O/P)	
RESVD	11		Reserved - Do not connect				
I2S_BCLK	13	I (INT) or O (UA)	Peripheral I2S interface - I2S bit clock		Slave (Clock I/P)	Master (Clock O/P)	
MCLK	14	I (INT) or O (UA)	Audio master clock		Slave (Clock I/P)	Master (Clock O/P)	
XOUT	15	O	Crystal oscillator output Note that this pin should be left floating when using the CMOS clock input				
XIN	16	I	Crystal oscillator input or CMOS clock input				
VDDIOB18	17, 26	PWR	I/O Power Supply				A,C
TDI	18	I	JTAG test data input This pin has a weak internal pull-up				

NAME	PIN	TYPE	DESCRIPTION	INTERFACE MASTER/SLAVE OPERATION			NOTE
				DURING BOOT	-INT CONFIG	-UA CONFIG	
TDO	20	O	JTAG test data output				
RST_N	21	I	Device reset - active low. This pin has a Schmitt trigger input and an internal weak pull up				
PLL_AVDD	22	PWR	Analogue Phase Locked-Loop power supply				
TMS	23	I	JTAG test mode select This pin has a weak internal pull-up				
TCK	24	I	JTAG test clock input This pin has a Schmitt trigger input and an internal weak pull-down				
NC	25		Not connected. This pin should NOT be connected to any net				
USB_DM	28	I/O	USB D- line May be left floating if USB is not required				
USB_DP	29	I/O	USB D+ line May be left floating if USB is not required				
USB_VDD33	30	PWR	USB 3.3V power for the USB transceiver May be left floating if USB is not required				A
USB_VDD18	31	PWR	USB 1.8V power for the USB transceiver May be left floating if USB is not required				A

NAME	PIN	TYPE	DESCRIPTION	INTERFACE MASTER/SLAVE OPERATION			NOTE
				DURING BOOT	-INT CONFIG	-UA CONFIG	
MIC_DATA	32	I	Mic data Note that this is a DDR input, permitting a pair of digital DDR microphones to share this input				
XL_DN1	33	I/O	XMOS high-speed debug link (downlink bit 1) Required for debug only, optional - may be left floating				
XL_DN0	35	I/O	XMOS high-speed debug link (downlink bit 0) Required for debug only, optional - may be left floating				
XL_UP0	36	I/O	XMOS high-speed debug link (uplink bit 0) Required for debug only, optional - may be left floating				
XL_UP1	37	I/O	XMOS high-speed debug link (uplink bit 1) Required for debug only, optional - may be left floating				
VDDIOR	38	PWR	I/O Power Supply				A ,B
MIC_CLK	39	O	Microphone clock output (3.072MHz)				
OP_0	40	O	General purpose output 0				
RESVD	41		Reserved Do not connect				

NAME	PIN	TYPE	DESCRIPTION	INTERFACE MASTER/SLAVE OPERATION			NOTE
				DURING BOOT	-INT CONFIG	-UA CONFIG	
USB_VBUS_DET	43	I	USB VBUS detect for self-powered systems May be left floating if USB is not required or in bus-powered systems. Requires voltage divider				
I2C_SCL	44	I (INT) or O (UA)	I2C serial clock line		Slave (Clock I/P)	Master (Clock O/P)	
I2C_SDA	45	I/O	I2C serial data line		Slave	Master	
IP_0	46	I	General purpose input 0 May be left floating if not required				
SPI_MISO	47	O (INT) or I (UA)	SPI Master - SPI Master In Slave Out May be left floating if not required	Not Used	Slave (Data O/P)	Master (Data I/P)	
IP_2	48	I	General purpose input 2 May be left floating if not required				
IP_1	50	I	General purpose input 1 May be left floating if not required				
IP_3	51	I	General purpose input 3 May be left floating if not required				
VDDIOT	52	PWR	I/O Power Supply				A, B
I2S_DIN	53	I	Peripheral I2S interface - I2S data input		Slave	Master	

NAME	PIN	TYPE	DESCRIPTION	INTERFACE MASTER/SLAVE OPERATION			NOTE
				DURING BOOT	-INT CONFIG	-UA CONFIG	
OP_1	54	O	General purpose output 1				
OP_2	55	O	General purpose output 2				
OP_3	56	O	General purpose output 3				
SUSPEND	58	O	Reserved for future. Do not connect.				
QSPI_D0	59	I/O	QSPI Boot Flash QSPI Data Line 0				
QSPI_D2	60	I/O	QSPI Boot Flash QSPI Data Line 2				
VDD	4, 12, 19, 27, 34, 42, 49, 57, 61-64	PWR	Core power supply				A, D
VSS	65	PWR	Device ground (Must be connected)				D

A. All VDD pins must be connected, excluding the USB_VDD supplies which can be left floating if USB is not required.

B. Two package variants are available:
QF60A – (1V8 I/0) – VDDIOT, VDDIOL and VDDIOR must be connected a 1V8 supply
QF60B – (3V3 I/0) – VDDIOT, VDDIOL and VDDIOR must be connected a 3V3 supply

C. In both variants, VDDIO18 must be connected to a 1V8 supply must be connected.

D. All package paddles must be connected. It is advised that vias be placed under paddles to connect directly to PCB supply planes

3. DEVICE INTERFACES

3.1. PDM MICROPHONE INPUTS

Two standard PDM MEMS microphones should be connected to the MIC_DATA pin. The data input makes use of the left and right channel output capability of standard MEMS microphones and the microphone data is read on alternative edges of the MIC_CLK signal. The XVF3610 reads one microphone on the positive edge of the microphone clock and the other microphone on the negative edge of the clock.

The XVF3610 outputs a microphone clock at 3.072MHz on the MIC_CLK output, which must be fed directly to both microphones. This signal must be used to clock the microphone PDM output to avoid undefined artifacts in the processed audio stream. One microphone should be set to be left (output on rising edge of clock) and the other right (output on the falling edge of clock).

An example microphone circuit is shown in the figure below:

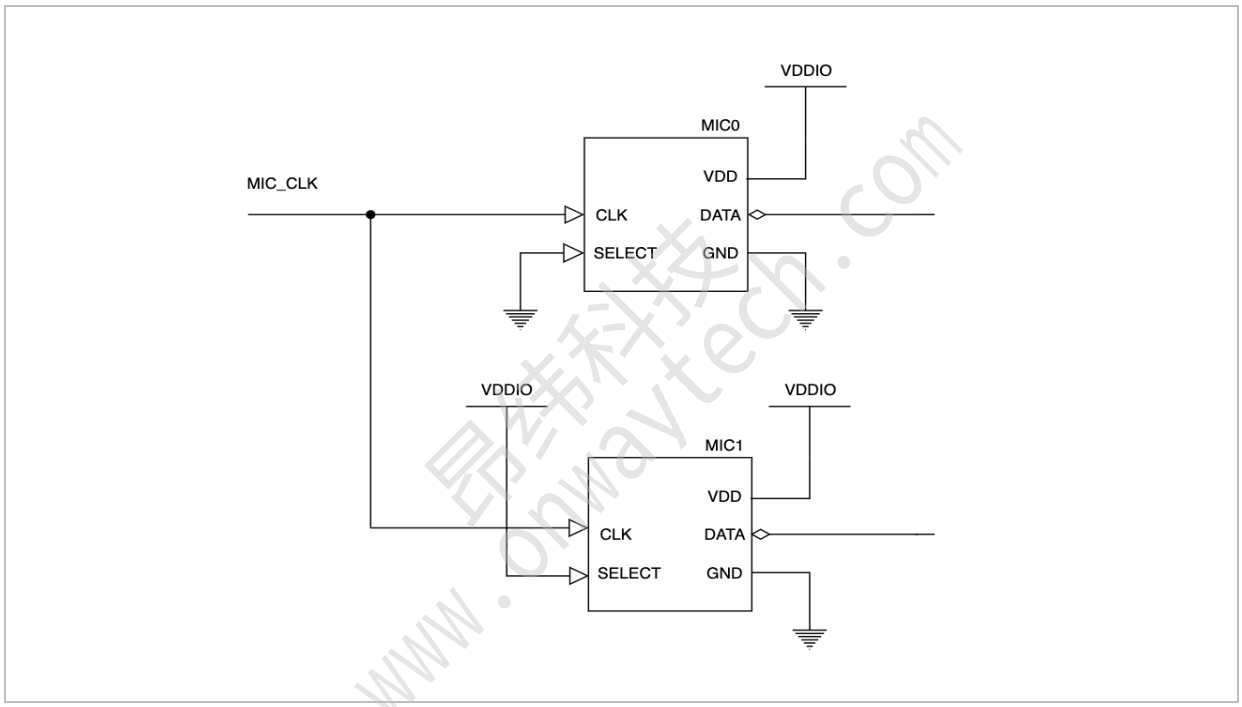

Figure 3-1 PDM microphone schematic

The voice processor has been tested and characterised with microphones placed with a 71mm separation and connected to the product enclosure in such a way that the acoustic path to each microphone from outside the product is independent. The XVF3610 algorithms automatically adapt to alternative spacing, but differences in audio performance may occur and should be thoroughly characterised.

3.2. QSPI

When QSPI boot mode is enabled (default), the XVF3610 enables the six QSPI pins, see table below, and drives the QSPI clock as a QSPI Master. A READ command is issued with a 24-bit address 0x000000.

Table 3-1 QSPI signals

SIGNAL	DESCRIPTION	COMMENT	PIN	I/O
QSPI_CS_N	QSPI Chip Select	Pull high externally to the device using a 4.7k ohm resistor	3	O
QSPI_CLK/SPI_CLK	QSPI Clock		5	O
QSPI_D0	QSPI Data Line 0		59	I/O
QSPI_D1/BOOTSEL	QSPI Data Line 1 and boot selection.	If pin is tied high via a 4.7k ohm resistor on startup, the device will start in SPI slave boot mode. If the pin is left floating, pulled low or connected to a quad SPI D1 pin on a memory device, the device will start in QSPI master mode and attempt to boot from a local QSPI flash memory.	1	I/O
QSPI_D2	QSPI Data Line 2		60	I/O
QSPI_D3	QSPI Data Line 3		2	I/O

The XVF3610 expects each byte to be transferred with the least-significant nibble first. Programmers that write bytes into a QSPI interface using the most significant nibble first may have to reverse the nibbles in each byte of the image stored in the QSPI device. When bulk programming flash devices the Quad Enable bit in the flash setting register should be set.

For further information about the boot sequence refer to the XU316-1024-QF60(A/B) datasheet.

3.3. SPI

The SPI interface can be utilised in both Master and Slave configurations for peripheral control of components like DACs and ADCs (Master), and SPI boot from host a host processor (Slave).

3.3.1. PERIPHERAL COMPONENT CONTROL

Once the XVF3610 has successfully booted, the SPI interface can be used to configure peripheral components such as DACs, ADCs and keyword detection devices. In this mode the SPI interface operates as a master, and transfers data held in flash, or received from the host over the control interface. The interface operates with the following specifications:

- 1MHz SPI clock
- Up to 128 bytes SPI write
- Up to 56 bytes SPI read

For further information on this configuration consult the User Guide.

3.3.2. SPI SLAVE BOOT

To enable the SPI boot from an external host processor, the QSPI_D1/BOOTSEL should be pulled to VDDIO on power-up. This activates the SPI interface, which operates as a slave to the host processor for the transfer of the boot image, which is clocked in with the least significant bit first in each transferred byte.

This is an alternative to using an attached QSPI flash to automatically transfer boot data on start-up.

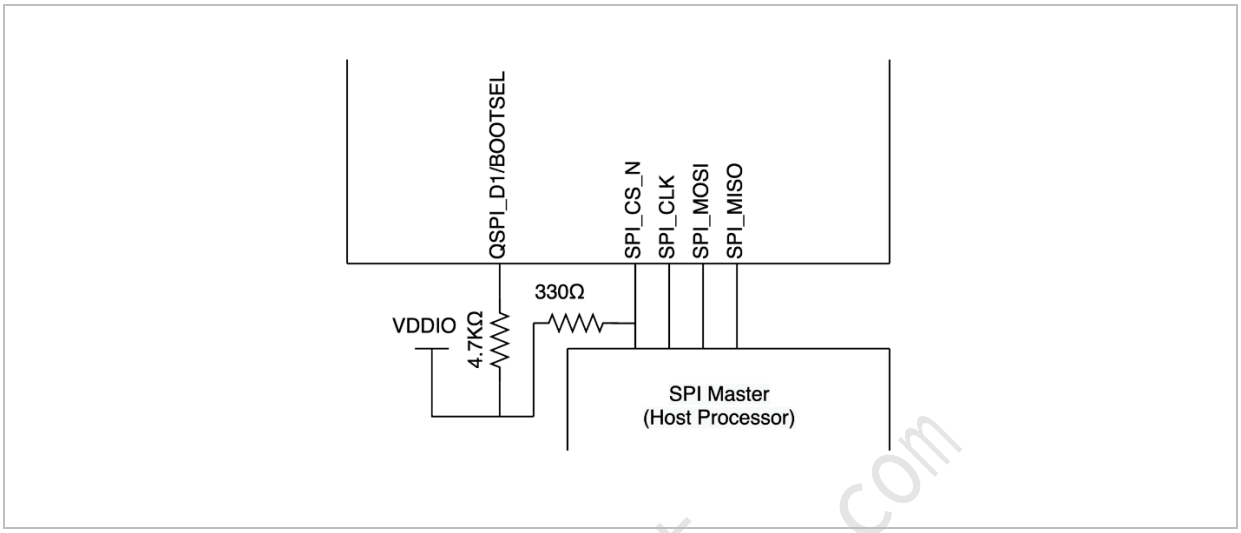

Figure 3-2 XVF3610 SPI slave boot configuration

The SPI pins are shown below in the table below.

Table 3-2 SPI signals

SIGNAL	DESCRIPTION	COMMENT	PIN	I/O
SPI_CLK	SPI Clock		5	I
SPI_CS_N	SPI Chip Select	Pull high externally to the device using a 4.7k ohm resistor	6	I
SPI_MOSI	SPI Master Out Slave In		7	I
SPI_MISO	SPI Master In Slave Out	May be left floating if not required	47	O

3.4. INTEGRATED USB INTERFACE

USB Audio Class 1.0 running at Full Speed (12Mbps) is used to deliver processed voice audio to the host processor, stereo reference audio from the host and as a control interface. In this mode the adaptive USB Audio endpoint is used to generate an MCLK synchronised to the USB host. This is driven out of MCLK.

Table 3-3 USB connections

NAME	DESCRIPTION	PIN
USB_DP	Connect to USB connector	29
USB_DM	Connect to USB connector	28
USB_VBUS_DET	Do not connect Self-powered operation is not supported by current device firmware	43
USB_VDD18	1.8V supply for USB-PHY - May be left floating if the USB interface is not used.	31
USB_VDD33	3.3V supply to the USB-PHY May be left floating if the USB interface is not used.	30

The table below shows the signals required to implement a USB interface using the XVF3610: Currently the -UA firmware only supports use in a bus powered configuration.

3.5. I2S

The XVF3610 operates as an I2S slave outputting audio to the host processor and receiving reference audio signal. This bidirectional flow of audio samples must be synchronised to a single set of I2S clocks, see Table below:

Table 3-4 I2S signals

SIGNAL	DESCRIPTION	COMMENT	PIN	I/O
MCLK	Master audio clock		14	I
I2S_BCLK	I2S bit synchronisation clock	Configurable for 16KHz (1.024MHz) and 48KHz (3.072MHz) sample rates	13	I
I2S_LRCK	I2S Left/Right clock	48kHz or 16KHz clock derived as I2S_BLCK/64.	10	I
I2S_DIN	I2S Data In	Reference audio data from I2S device	53	I
I2S_DOUT	I2S Data Out	Audio data out to host processor	9	O

The I2S audio samples are transmitted serially with a one I2S_BCLK delay between the change of I2S_LRCK phase and the start (MSB) of the audio sample for that channel. This the standard alignment for I2S systems.

3.6. I2C

The I2C Slave interface is used to control and configure the parameters on the XVF3610.

NOTE: I2C commands received prior to I2S clocks being activated will not be processed and may result in undefined behaviour. Therefore, it is important to ensure that the I2S interface is activated before parameterisation of the device is undertaken.

The interface operates with the following specifications:

- 100 kbps SCL clock speed
- Register read/write
- Up to 56 byte I2C read/write

For more information on control and configuration of the XVF3610 please refer to the User Guide.

The device I2C address is 0x2C, and the pin connections are shown below.

Table 3-5 I2C Slave Connections

SIGNAL	DESCRIPTION	COMMENT	PIN	I/O
I2C_SCL	I2C serial clock line for receiving control command from I2C host		44	I/O
I2C_SDA	I2C serial data line for receiving control command from I2C host		45	I/O

3.7. GENERAL PURPOSE INPUT/OUTPUT

Four input and four output pins are provided to allow general-purpose I/O such as LEDs and button controls. Input pins can be individually read by the host using the control interface and configured to detect edge events. The output pins can be individually set, and they have configurable Pulse Width Modulated (PWM) brightness control with blinking sequences. The GPIO pins are shown in the table below.

Table 3-6 GPIO pin table

NAME	DESCRIPTION	PIN	I/O
IP_0	General purpose input	46	I
IP_1	General purpose input	50	I
IP_2	General purpose input	48	I
IP_3	General purpose input	51	I
OP_0	General purpose output	40	O
OP_1	General purpose output	54	O
OP_2	General purpose output	55	O
OP_3	General purpose output	56	O

For more information on configuring these inputs and outputs, please refer to the User Guide.

4. DEVICE OPERATION

4.1. POWER SUPPLIES

The XVF3610 has the following power supply pins:

Table 4-1 Power Pins

NAME	DESCRIPTION	PIN
VDD	Digital core power supply. 0.9V (nominal)	4, 12, 19, 27, 34, 42, 49, 57, 61-64
VDDIOL	Digital I/O power supply ** See Note A.	8
VDDIOR	Digital I/O power supply ** See Note A	38
VDDIOT	Digital I/O power supply ** See Note A	52
VDDIOB18	Digital I/O power supply. 1.8V (nominal)	17,26
PLL_AVDD	PLL analogue power. This 0.9V (nominal) PLL supply should be separated from the other supplies at the same voltage by a low pass filter.	22
USB_VDD18	Digital supply to the USB-PHY. 1.8V (nominal)	31
USB_VDD33	Analogue supply to the USB-PHY. 3.3V (nominal)	30
VSS	Device Ground	65 (Paddle)

NOTES:

A: I/O voltage depends on package variant

QF60A – VDDIOx is 1.8V nominal – pins 8, 38 and 52 should be connected to a 1.8V supply

QF60B – VDDIOx is 3.3V nominal – pins 8, 38 and 52 should be connected to a 3.3V supply

For both variants, VDDIOB18 – pins 17 & 26 - must be connected to 1.8V

B: All VDD power pins must be connected.

C: USB_VDDxx supplies can be left floating if USB is not used.

Refer to the XU316-1024-QF60(A/B) datasheets for further information.

4.2. CLOCKS

The XVF3610 device has an on-chip oscillator. To use the oscillator a crystal, two capacitors, and damping and feedback resistors to the device as shown in Figure 4-1.

Table 4-2 XVF3610 crystal oscillator

SIGNAL	DESCRIPTION	COMMENT	PIN	I/O
XIN	Crystal oscillator input		16	I

SIGNAL	DESCRIPTION	COMMENT	PIN	I/O
XOUT	Crystal oscillator output		15	O

Alternatively, the XVF3610 can be provided with a 24MHz, 1V8 clock input on the XIN pin. The clock must be running when the chip comes out of reset.

Table 4-3 XVF3610 clock signals

SIGNAL	DESCRIPTION	COMMENT	PIN	I/O
XIN	Master clock (system)	24MHz 1V8 clock signal	16	I
XOUT	N/C	Leave floating if clock input on XIN	15	O

Figure 4-1 Crystal oscillator or clock input configurations

For further information, and details on the calculation of R_f and R_d, please refer to the XU316-1024-QF60(A/B) datasheet.

4.3. RESET

The XVF3610 device has an on-chip Power-on-Reset (POR). This keeps the chip in reset whilst the supplies are coming up.

See XU316-1024-QF60(A/B) datasheet for further information.

Table 4-4 Reset Signal

SIGNAL	DESCRIPTION	COMMENT	PIN	I/O
RST_N	Device reset	Active low	21	I

4.4. BOOT MODES

On start-up and after a reset event, the XVF3610 is booted either using an externally connected QSPI flash memory or by transferring a boot image to the device via SPI from a host processor.

SLAVE BOOT MODE

The boot mode is specified using QSPI_D1/BOOTSEL. If this pin is tied high via a 4.7k ohm resistor on start-up, the XVF3610 will enable SPI Slave boot mode.

QSPI MASTER BOOT MODE

If the QSPI_D1/BOOTSEL pin is connected to a QSPI_D1 pin on a flash device, the XVF3610 will boot from a local QSPI flash in QSPI Master mode.

4.5. QSPI FLASH SUPPORT

Flash devices with the following specifications are supported by the XVF3610 (eg. Winbond W25Q16JWSNIM).

Table 4-5 Flash device specification supported by XVF3610

DEVICE CHARACTERISTIC	DESCRIPTION	VALUE
Page size	Size of flash page in bytes	256
Number of pages	Total number of pages	8192
Address size	Number of bytes used to represent the address	3
Read ID operation code	Operation code to read the device identification (ID) information	0x9F
Read ID dummy bytes	Number of dummy bytes after read command before ID is returned	0
ID size	Size of ID in bytes	3
Sector Erase operation code	Operation code for 4 KB Erase	0x20
Sector information	Arrangement of sectors	Regular (all equally sized - 4KB)
Write Enable operation code	Operation code for write enable	0x06
Write Disable operation code	Operation code for write disable	0x04
Page Program operation code	Operation code for page program	0x02
Fast Quad Read operation code	Operation code for Fast Quad I/O Read	0xEB
Fast Quad Read Dummy Bytes	Number of dummy bytes after setup of fast quad read that data is returned	1
Read Status Register operation code	Operation code for reading status register	0x05
Write Status Register operation code	Operation code for write to the status register	0x01
Write Status Register Busy Mask	Bit mask for operation in progress (device busy)	0x01

4.6. DEVICE FIRMWARE

Device Firmware Upgrade (DFU) is supported for devices that have QSPI flash connected and loaded with a firmware image. If the DFU process fails, the boot process safely falls back to the factory image allowing the user to re-attempt the upgrade. Images loaded via DFU can also be removed allowing the device to revert to the factory image.

For further information on the operation of the DFU mechanism refer to the User Guide.

5. ELECTRICAL AND THERMAL CHARACTERISTICS

For electrical characteristics refer to the XU316-1024-QF60(A/B) datasheets.

6. SWITCHING CHARACTERISTICS

For clock, reset and JTAG timing refer to the XU316-1024-QF60(A/B) datasheet. XVF3610 specific interface timings are detailed below.

6.1. QSPI MASTER (EXTERNAL FLASH FOR BOOT IMAGE STORAGE)

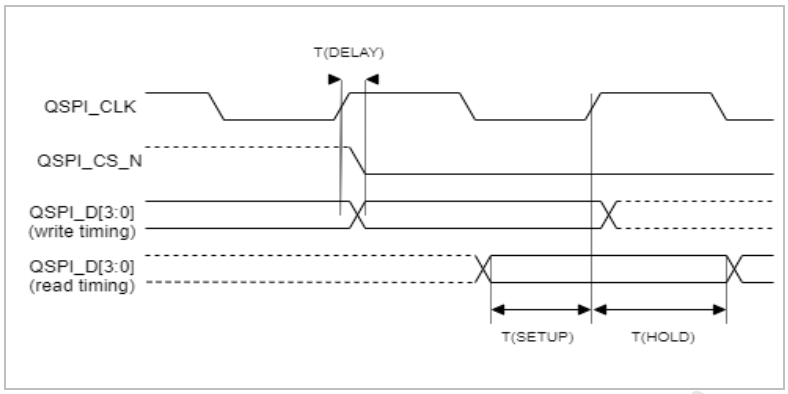

Figure 6-1 QSPI Timing

Table 6-1 QSPI Timing Requirements

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS
QSPI Clock frequency	f(QSPI_CLK)	-	TBC	50	MHz
QSPI_CLK to QSPI Data output delay	T(DELAY)	-2.7	-	2.7	ns
QSPI Data input to QSPI_CLK Setup time	T(SETUP)	22	-	-	ns
QSPI Data input to QSPI_CLK hold time	T(HOLD)	-11	-	-	ns

6.2. I2S SLAVE

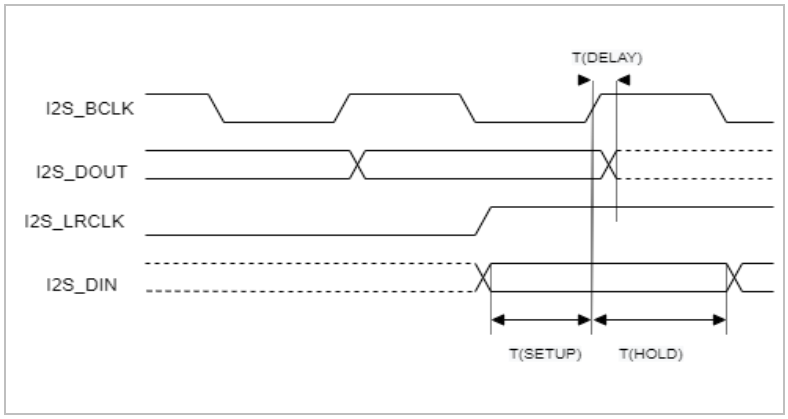

Figure 6-2 I2S Slave timing

Table 6-2 I2S Slave timing requirements

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS	NOTES
Master clock input frequency	f(MCLKin)	TBC	-	24.576	MHz	A
I2S Bit Clock frequency input	f(I2S_BCLK)	1.024	-	3.072	MHz	
I2S Data Input (LRCLK) to I2S_BCLK setup time	T(SETUP)	0	-	-	ns	B
I2S Data Input (LRCLK) to I2S_BCLK hold time	T(HOLD)	6	-	-	ns	B
I2S_BCLK to I2S Data output delay	T(DELAY)	11	-	21.3	ns	

A: Configurable input multiplier used to generate appropriate audio sample rates (16kHz / 48kHz)

B: Timing also applies to I2S Sample Clock (I2S_LRCLK)

6.3. SPI SLAVE (EXTERNAL PROCESSOR BOOT)

Table 6-3 SPI Slave Timing Requirements

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS	NOTES
SPI Clock frequency	f(SPI_CLK)	-	TBC	TBC	MHz	
SPI_CLK to MISO output delay	T(DELAY)	11	-	21.3	ns	
SPI Master Output Slave Input (MOSI) to SPI_CLK Setup time	T(SETUP)	0	-	-	ns	
SPI Master Output Slave Input to (MOSI) SPI_CLK hold time	T(HOLD)	6	-	-	ns	

A: Timing also applies to SPI Chip Select input (SPI_CS_N)

6.4. SPI MASTER (PERIPHERAL CONTROL)

Table 6-4 SPI Master Timing Requirements

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS	NOTES
SPI Clock frequency	f(SCLK)	-	TBC	TBC	MHz	
SPI CLK to SPI Master In Slave Out (MOSI) output delay	T(DELAY)	-2.7	-	2.7	ns	
SPI Master Out Slave In (MISO) Setup time	T(SETUP)	0	-	-	ns	
SPI Master Out Slave In (MISO) Hold time	T(HOLD)	6	-	-	ns	

7. DEVICE MARKINGS

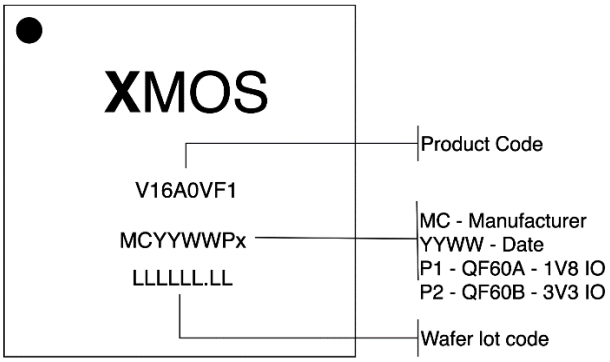

Figure 7-1 Part marking scheme

The two variants of the package (1.8V and 3.3V I/O) are distinguished by a P1 or P2 code after the date code (yyww) on the package

Table 7-1 Ordering codes

PRODUCT ORDER CODE	MARKING	DESCRIPTION
XVF3610-QF60A-C	V16A0VF1 MCYYWWP1	Commercial Temp range (0 °C – 70 °C), 1.8V IO
XVF3610-QF60B-C	V16A0VF1 MCYYWWP2	Commercial Temp range (0 °C – 70 °C), 3.3V IO
XVF3610-QF60A-I	V16A0VF1I MCYYWWP1	Industrial Temp range (-40 °C – 85 °C), 1.8V IO
XVF3610-QF60B-I	V16A0VF1I MCYYWWP2	Industrial Temp range (-40 °C – 85 °C), 3.3V IO

MC – Manufacturer, YY – Year code, WW – Week code

8. FURTHER INFORMATION

8.1. DOCUMENTATION

Table 8-1 Additional documentation

DOCUMENT TITLE	DOWNLOAD
XU316-1024-QF60A Datasheet	https://www.xmos.ai/file/xu316-1024-qf60a-xcore_ai-datasheet
XU316-1024-QF60B Datasheet	https://www.xmos.ai/file/xu316-1024-qf60b-xcore_ai-datasheet
XVF3610 User Guide	https://www.xmos.ai/view/xvf3610-user-guide
XTC Tools User Guide	https://www.xmos.ai/file/tools-user-guide
XK-VOICE-L71 Hardwarel	https://www.xmos.ai/file/xk-voice-l71-pcb-design-files
XVF3610 Getting Started	https://www.xmos.ai/file/xvf3610-quick-start-guide

8.2. DEVICE FIRMWARE AND DRIVERS

Table 8-2 Device firmware

DEVICE FIRMWARE & TOOLS	DOWNLOAD
XVF3610 firmware and host control applications	https://www.xmos.ai/file/xvf3610-release
XTC Programming Tools	https://www.xmos.ai/software-tools

9. REVISION HISTORY

Table 9-1 Revision history

DOCUMENT VERSION	RELEASE DATE	CHANGE DESCRIPTION
XM-014380-PC-1	9 March 2021	Preliminary Release
XM-014380-PC-2	8 July 2021	Added UA configuration and QF60B 3V3 IO package
XM-014380-PC-3	15 October 2021	Amended to short form, modified device marking
XM-014380-PC-4	11 February 2022	Corrected VDDIOR PIN on notes below table 4-1
XM-014380-PC-5	17 February 2022	Corrected USB_VDDxx pins on table 4.1 and 3.3 Reversed descriptions on D+/D- pins in table 2.1
XM-014380-PC-6	18 February 2022	Regenerated Table of Contents – no other changes
XM-014380-PC-7	26 May 2022	Added new part order code – Industrial qualification Extended list of web links in section 8