

0.1	Preliminary New release		2011-12-27

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LCD MODULE NUMBERING SYSTEM

XYF480272C-TP

XYF XYF TECHNOLOGY
480272 SERIALS NUMBER FOR SM 480 COLUMNS Vs. 272 ROWS
C VERSION OF PCB
TP Touch panel

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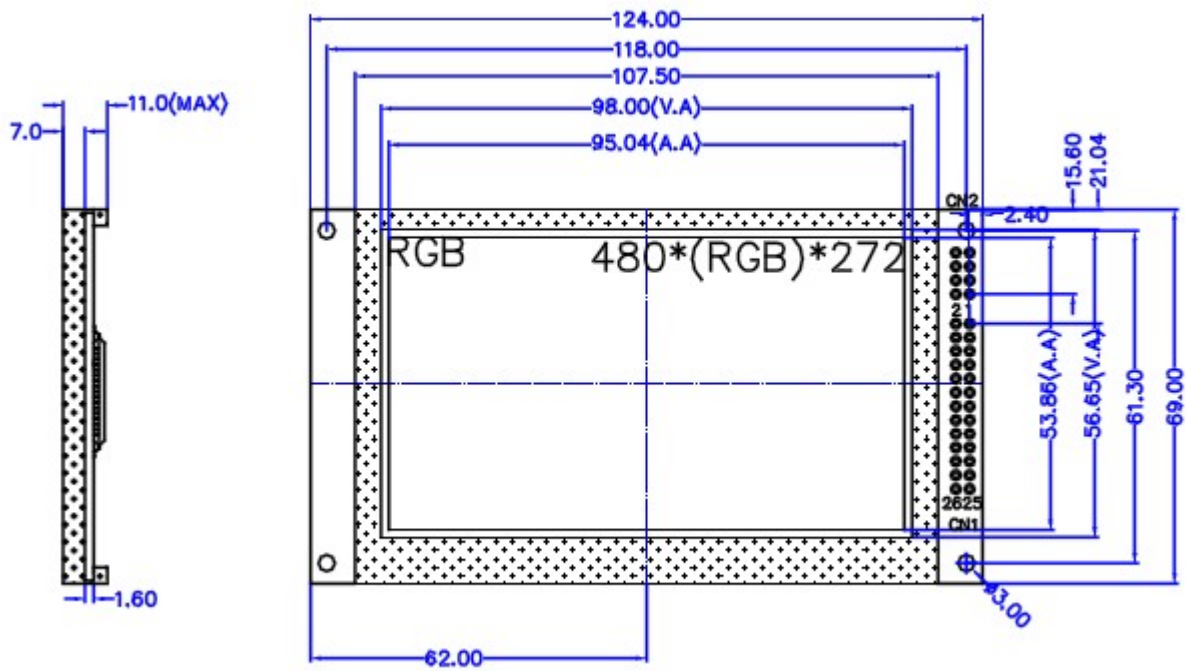
1. Basic Specifications

1. Supply Voltage: VDD= +3.3V ±2%。
2. dots: 480 (RGB) X272
3. 4.3 inch
4. Working temperature: -20℃--+70℃
5. Storage temperature: -30℃--+80℃
6. 4-Wire SPI Interface。

2. Mechanical Specifications

ITEM	SPECIFICATION	UNIT
OVERALL SIZE	124.0 X 69.0 X 10.6T	MM
VIEWING AREA	98.7 X 57.15	MM
DOT NUMBER	480(RGB) X272	DOTS

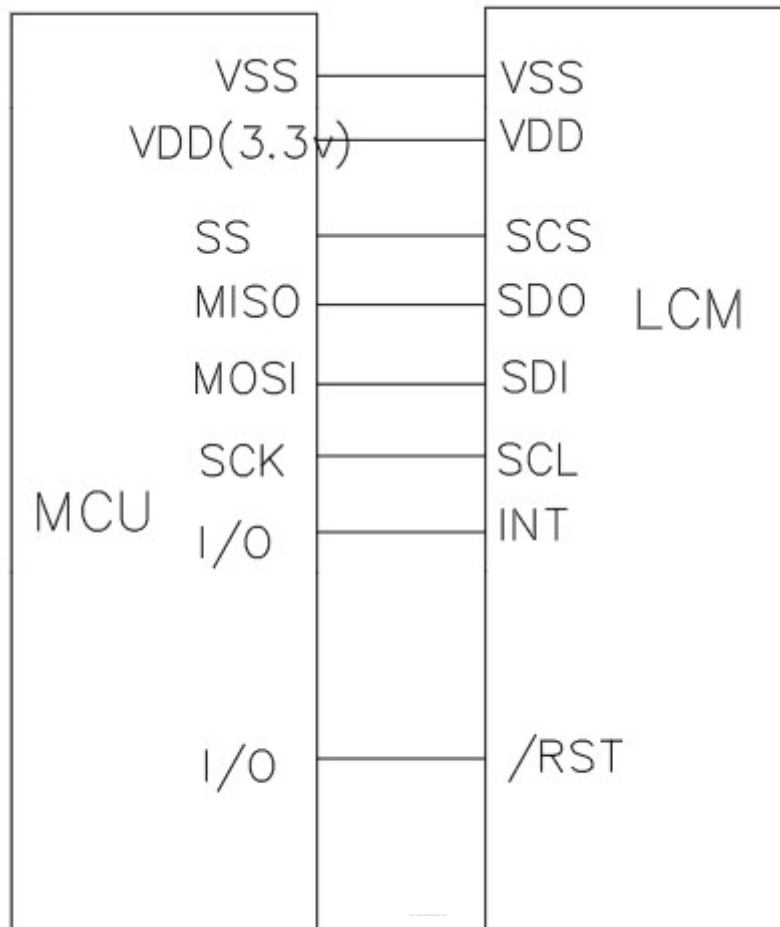
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Outline dimension drawing

3.4-wire SPI Interface

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The INT output for MCU to indicate the status of LCM

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4. Terminal Functions

模块引脚顺序及定义		
序号	名称	描述
1	VSS	Negative Power Supply, Ground(0V)
2	VDD	Positive Power Supply(+3.3V)
3	/RST	Reset Signal Input
4	SCS	SPI Chip Select
5	SDO	SPI Data Output
6	SDI	SPI Data Input
7	SCL	SPI Clock
8	INT	Interrupt Signal Output

5. Electrical Characteristics

1. Limit parameters

1.1 Electrical limit parameters

Items	Symbol	TYP	MIN	MAX	Unit
Operating Voltage	Vdd - Vss	3.3	2.8	3.8	V
Input High Voltage	Vi	-	2.7	3.8	V

1.2 Environmental limit parameters

Items	Symbol	Condition	MIN.	MAX.	Unit
Working Temp	Topr	-Normal temp.	-20	70	deg C
Storage Temp	Ttsg	version-	-30	80	deg C

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2. DC Characteristics

电气特性 at Ta=25 deg C, Vdd = 3.3V

Items	Symbol		MIN.	TYP.	MAX.	Unit
Operating Voltage	Vdd-Vss	-	2.8	3.3	3.5	V
Input Voltage (forSCS, SDO, SDI, SCK)	V-ih	“H” level	2.7	-	3.5	V
	V-il	“L” level	VSS	-	0.6	V
LCD 驱动电流	Idd	-	-	300	350	mA

6. Function Specifications

6.1 Introduction

XYF480272C-TP is a text/graphic mixed display with 2 layers TFT LCD. The Advanced geometric speed-up engine provides user an easy way to draw the programmable Geometric shapes by hardware, like line, square, circle and ellipse. Besides, for different End-user applications, many powerful functions are integrated with the lcm, such as scroll function, floating window display, graphic pattern and font enlargement function. These function will save user a large of effort during development period.

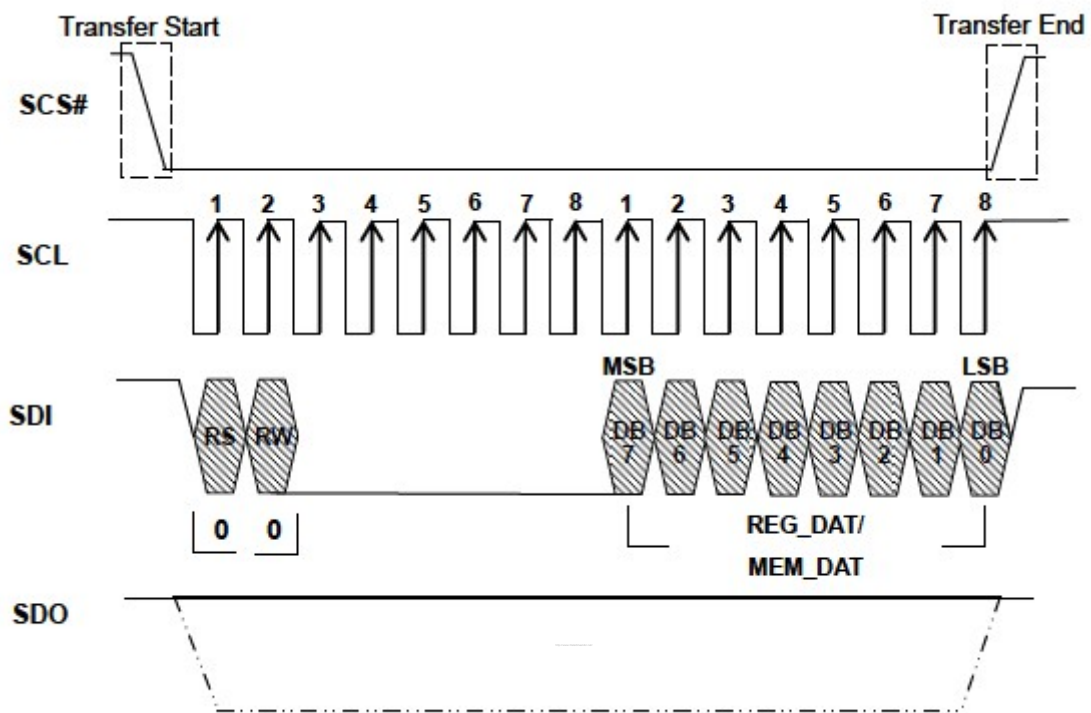
6.2 Resetting the LCD module

Before programming the LCM, it' s suggested that a reset process should be done. The LCM requires a reset low pulse at least 27us.

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6.3 Transmission protocol

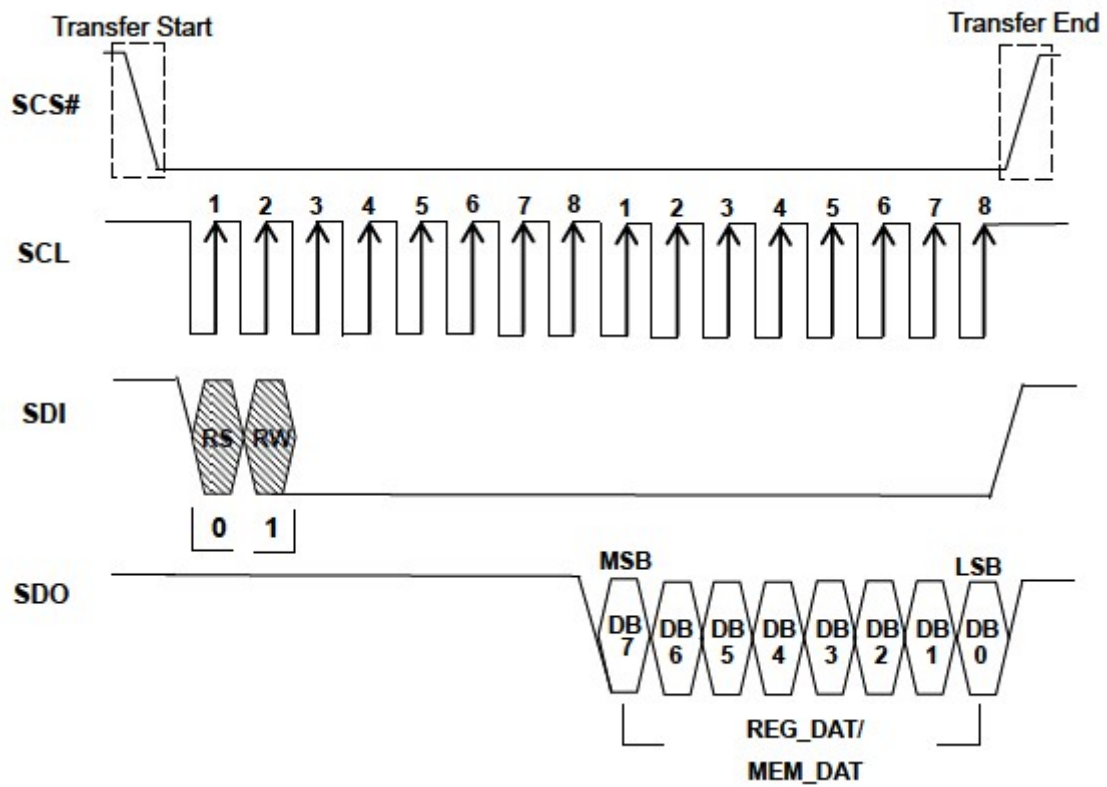
SDI is the data pin from the SPI master, SDO is the data output from the SPI slave. About the detail protocol, please refer to Figure.



Data Write on 4-Wire SPI-Bus

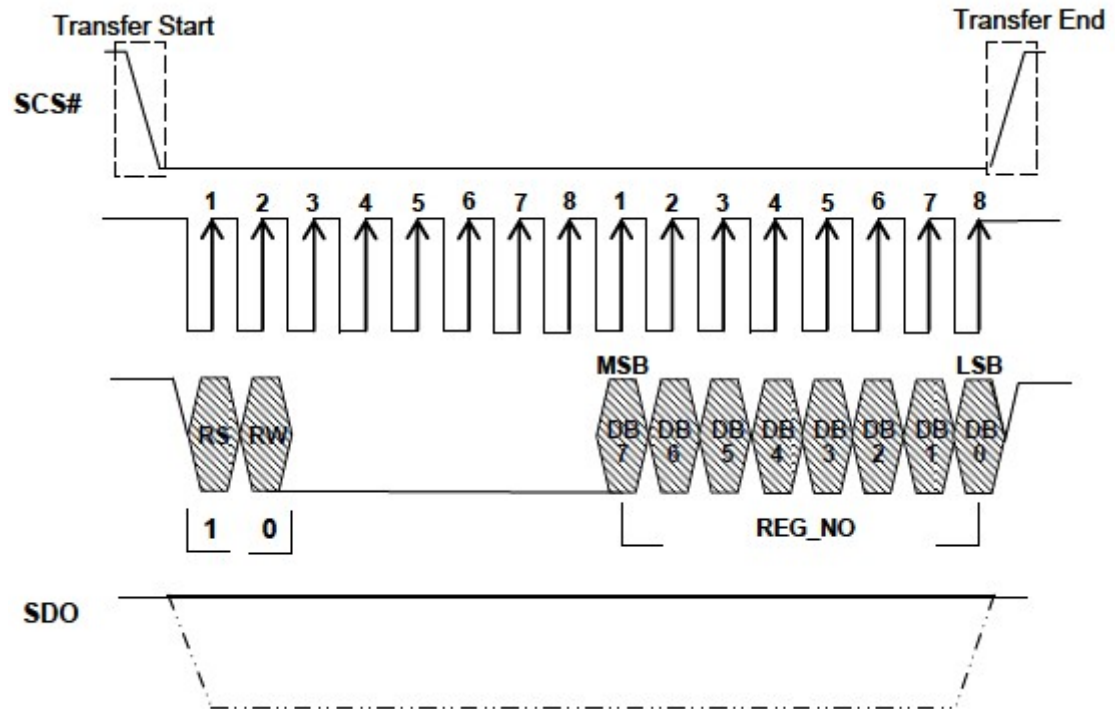
SCK<=4MHZ

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Data Read on 4-Wire SPI-Bus

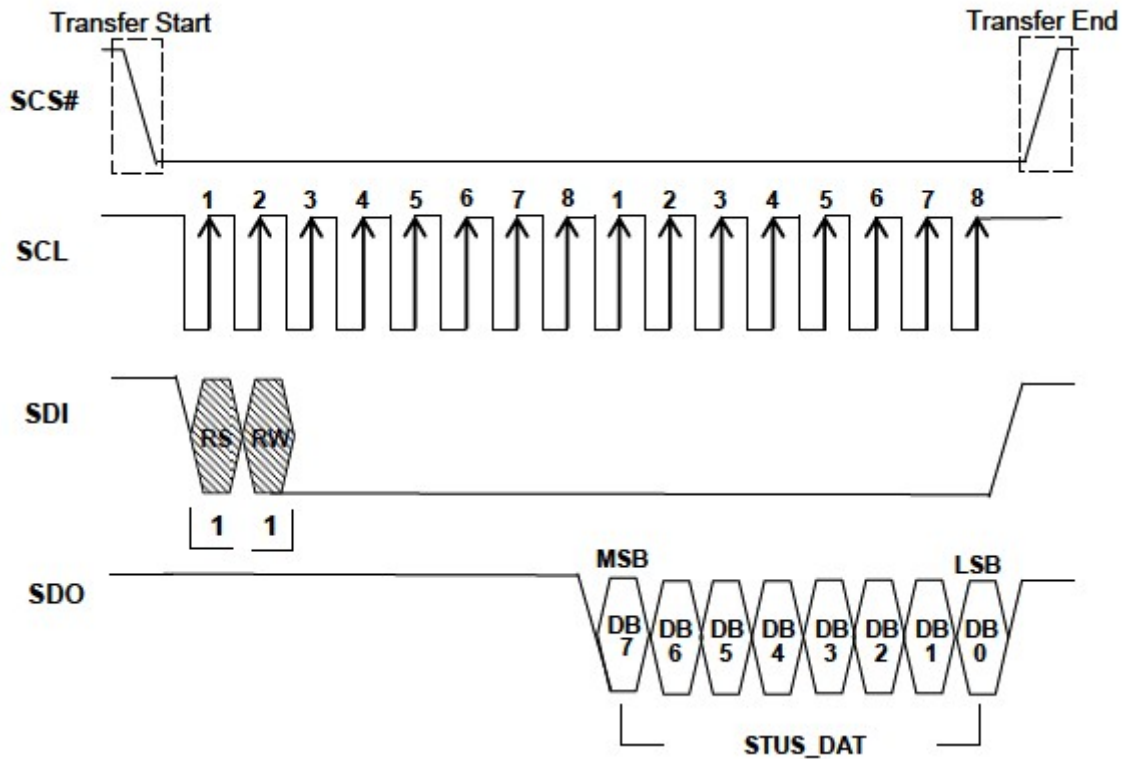
SCK<=4MHZ



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CMD (Command) Write on 4-Wire SPI-Bus

SCK ≤ 4MHz



Status Read on 4-Wire SPI-Bus

SCK ≤ 4MHz

6.4 Interrupt

There are 2 kinds of interrupt events for LCM, each maps to the corresponding status Bits in REG[F1h]:

- ◆ Touch event occurs. Bit 2 of REG[F1h] is set to 1.
- ◆ The font access is completed. Bit 0 of REG[F1h] is set to 1.

All of the above interrupts function can be enable/disable by setting INTC1(REG[F0h]), In addition, if the system of customer can not provide the hardware interrupt, The LCM also supports a software polling method, MCU can detect the

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interrupt status through the related status flag. When hardware interrupts of LCM are active, the related interrupt masks must be disabled first. There is an example for describing the interrupt procedure of Touch Panel as below:

- ◆ LCM sends an interrupt signal to MCU.
- ◆ When MCU receives interrupt signal, the program counter(PC) will jump to ISR Start address.
- ◆ In the mean time, the corresponding interrupt status flag of LCM will be set to “1” (REG[F1h]). For example, When Touch event generates an interrupt, The touch panel Interrupt Status bit will be set to “1” .
- ◆ After the ISR completes, the status flag should be cleared , i.e., Write “1” to The corresponding bit of status register.

By software interrupt, user can read INTC2 register for detecting interrupt event Without any external device. Besides, Interrupt mask function is only applied to Hardware interrupt, not to INTC2 status flag. It should be noted that, INTC2 status Flag must be cleared manually at the tail of ISR, i.e., writing the Bit2 of Register INTC2 (REG[F1h]) with 1, because the INTC2 status flag will not be cleared Automatically.

6.5 Data Format

The LCM supports the 16-bit color depth TFT-LCD Panle, .i.e 65K colors TFT LCD panel



Color illustrations for 8-bit Data Bus MCU

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7.Instructions

7-1: The Categories of the Instruction Registers

No.	Command Registers	Address
1	System and Configuration Registers	[01h],[02h],[04h],[10h]-[1Fh]
2	LCD Display Control Registers	[20h]-[29h]
3	Active Window Setting Registers	[30h]-[3Fh]
4	Cursor Setting Registers	[40h]-[4Eh]
5	Not used	[50h]-[67h]
6	Touch Panel Control Registers	[70h]-[74h]
7	Graphic Cursor Setting Registers	[80h]-[85h]
8	PLL Setting Registers	[88h]-[89h]
9	PWM Control Registers	[8Ah]-[8Eh]
10	Drawing Control Registers	[90h]-[ACh]
11	Floating Window Control Registers	[D0h]-[DBh]
12	Serial Flash Control Registers	[E0h]-[E2h]
13	Interrupt Control Registers	[F0h]-[F1h]

7-2 Status Register

Status Register(STSR)

Bit	说明	初始值	Access
7	Memory Read/Write Busy(Include Font Write Busy) 0: No Memory Read/Write event. 1: Memory Read/Write busy.	0	RO
6	NA	0	RO
5	Touch Panel Event Detected 0: Touch Panel is not touched 1: Touch Panel is touched. This bit comes from the TP controller ADET signal directly and not de-bounced.It's suggested to check the Validation for multiple polling.	0	RO
4	Sleep Mode Status 0: LCM in Normal mode. 1: LCM in Sleep mode	0	RO
3-0	NA	0	RO

Note:RO: Read(Read Only)。

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7-3 System & Configuration Register

REG[01h] Power and Display Controller Register(PWRR)

Bit	Description	Default	Access
7	LCD Display Off 0: Display off. 1: Display on.	0	RW
6-2	NA	0	RO
1	Sleep Mode 0: Normal mode. 1: Sleep mode.	0	RW
0	Software Reset 0: No action 1: Software Reset Note:The bit must be set to 1 and then set to 0 to complete a software reset.	0	RW

Note: RW:Read or Write.

REG[02h]Memory Read/Write Command(MRWC)

Bit	Description	Default	Access
7-0	Write Function: Memory Write Data. Read Function: Memory Read Data.	--	RW

REG[04h]Pixel Clock Register(PCSR)

Bit	Description	Default	Access
7	PCLK Inversion 0: PDAT is fetched at PCLK rising edge. 1: PDAT is fetched at PCLK falling edge.	0	RW
6-2	NA	0	RO
1-0	PCLK Period Setting 00b:PCLKperiod=System Clock period. 01b:PCLK period=2 times of System Clock period. 10b:PLCK period=4 times of System Clock period. 11b:PCLK period=8 times of System Clock period.	0	RW

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REG[05h]Serial ROM Configuration Register(SROC)

Bit	Description	Default	Access
7	NA	0	RW
6	Serial ROM Address Mode 0: 24 bits address mode 1: 32 bits address mode	0	RW
5	Serial ROM Waveform Mode 0: Mode 0. 1: Mode 3.	0	RW
4-0	NA	0	RW

REG[06h]Serial ROM CLK Setting Register(SFCLR)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Serial ROM Clock Frequency Setting 0xb:SFCL frequency=System clock frequency 10b:SFCL frequency= System clock frequency /2. 11b:SFCL frequency= System clock frequency /4.	0	RW

REG[10h]System Configuration Register(SYSR)

Bit	Description	Default	Access
7-4	NA	0	RW
3-2	Color Depth Setting 00b:8-bpp generic TFT,i.e.256 colors. 1*b:16-bpp generic TFT,i.e.65K colors.	0	RW
1-0	N	0	RW

REG[14h]LCD Horizontal Display Width Register(HDWR)

Bit	Description	Default	Access
7	NA	0	RO
6-0	Horizontal Display Width Setting Bit[6:0] The register specifies the LCD panel horizontal display width in the uint of 8 pixels resolution. Horizontal display width (pixel) =(HDWR+1)*8	0	RW

REG[15h]Horizontal Non-Display Period Fine Tuning Option Register(HNDFTR)

Bit	Description	Default	Access
7	DE Polarity 0: High active 1: Low active	0	RW
6-4	NA	0	RO

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3-0	Horizontal Non-Display Period Fine Tuning(HNDFT)[3:0] This register specifies the fine tuning for horizontal non-display period;it is used to support the SYNC mode panel.Each level of this modulation is 1-pixel	0	RW
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REG[16h]LCD Horizontal Non-Display Period Register(HNDR)

Bit	Description	Default	Access
7-5	NA	0	RO
4-0	Horizontal Non-Display Period(HNDP)Bit[4:0] This register specifies the horizontal non-display period. Horizontal Non-Display Period (pixel)=(HNDR+1)*8+HNDFTR	0	RW

REG[17h]HSYNC Start Position Register(HSTR)

Bit	Description	Default	Access
7-5	NA	0	RO
4-0	HSYNC Start Position[4:0] The starting position from the end of display area to the beginning of HSYNC.Each level of this modulation is 8-pixel. HSYNC Start Position(pixel)=(HSTR+1)*8	0	RW

REG[18h]HSYNC PWM Register(HPWR)

Bit	Description	Default	Access
7	HSYNC Polarity 0: Low active. 1: High active.	0	RW
6-5	NA	0	RO
4-0	HSYNC Pulse Width(HPW) [4:0] HSYN Pulse Width (pixel)=(HPWR+1)*8	0	RW

REG[19h]LCD Vertical Display Height Register(VDHR0)

Bit	Description	Default	Access
7-0	Vertical Display Height Bit[7:0] Vertical Display Height(line)={ VDHR1,VDHR0}+1	0	RW

REG[1Ah]LCD Vertical Display Height Register0(VDHR1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Vertical Display Height Bit[8] Vertical Display Height(line)={ VDHR1,VDHR0}+1	0	RW

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REG[1Bh]LCD Vertical Non-Display Period Register(VNDR0)

Bit	Description	Default	Access
7-0	Vertical Non-Display Period Bit[7:0] Vertical Non-Display Period(line)={ VNDR1,VNDR0}+1	0	RW

REG[1Ch]LCD Vertical Non-Display Period Register(VNDR1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Vertical Non-Display Period Bit[8] Vertical Non-Display Period(line)={ VNDR1,VNDR0}+1	0	RW

REG[1Dh]VSYNC Start Position Register(VSTR0)

Bit	Description	Default	Access
7-0	VSYNC Start Position [7:0] The starting position from the end of display area to the beginning of VSYNC. VSYNC Start Position(line)={ VSTR1,VSTR0}+1	0	RW

REG[1Eh]VSYNC Start Position Register{ VSTR1 }

Bit	Description	Default	Access
7-1	NA	0	RO
0	VSYNC Start Position [8] The starting from the end of display area to the beginning of VSYNC. VSYNC Start Position(line)={ VSTR1,VSTR0}+1	0	RW

REG[1Fh]VSYNC PWM Register(VPWR)

Bit	Description	Default	Access
7	VSYNC Polarity 0: Low active 1: High active	0	RW
6-0	VSYNC Pulse Width [6:0] VSYNC Pulse Width(line)=(VPWR+1)	0	RW

7-4 LCD Display Control Register

REG[20h]Display Configuration Register(DPCR)

Bit	Description	Default	Access
7	Layer Setting Control 0: One layer configuration is selected 1: Two layers configuration is selected	0	RW

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6-4	NA	0	RO
3	HDIR Horizontal Scan Direction,for n=SEG number. 0: SEG0 to SEG(n-1). 1: SEG(n-1) to SEG0.	0	RW
2	VDIR Vertical Scan direction,for n=COM number 0: COM0 to COM(n-1). 1: COM(n-1) to COM0.	0	RW
1-0	NA	0	RW

REG[21h]Font Control Register 0(FNCR0)

Bit	Description	Default	Access
7	CGRAM/CGROM Font Selection Bit in Text Mode 0: CGROM Font is selected. 1: CGRAM Font is selected.	0	RW
6	NA.	0	RW
5	External/Internal CGROM Selection Bit 0: Internal CGROM is selected(REG[2Fh] must be set 00h) 1: External CGROM is selected.	0	RW
4-2	NA	0	RW
1-0	Font Selection for internal CGROM 00: ISO8859-1. 01: ISO8859-2. 10: ISO8859-3. 11: ISO8859-4.	0	RW

REG[22h]Font Control Register1(FNCR1)

Bit	Description	Default	Access
7	Full Alignment Selection Bit 0: Full alignment is disable. 1: Full alignment is enable.	0	RW
6	Font Transparency 0: Font with background color. 1: Font with background transparency.	0	RW
5	NA	0	RW
4	Font Rotation 0: Normal 1: 90 degree display	0	RW
3-2	Horizontal Font Enlargement 00: *1 01: *2	0	RW

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	10: *3 11: *4		
1-0	Vertical Font Enlargement 00: *1 01: *2 10: *3 11: *4	0	RW

REG[23h]CGRAM Select Register(CGSR)

Bit	Description	Default	Access
7-0	CGRAM No.	0	RW

REG[24h]Horizontal Scroll Offset Register 0(HOFS0)

Bit	Description	Default	Access
7-0	Horizontal Display Scroll Offset[7:0] The display offset of the horizontal direction,changing the value will cause the effect of scrolling at horizontal direction	0	RW

REG[25h]Horizontal Scroll Offset Register 1(HOFS1)

Bit	Description	Default	Access
7-3	NA	0	RO
2-0	Horizontal Display Scroll Offset[10:8] The display offset of the horizontal direction,changing the value will cause the effect of scrolling at horizontal direction.	0	RW

REG[26h]Vertical Scroll Offset Register 1(VOFS0)

Bit	Description	Default	Access
7-0	Vertical Display Scroll Offset[7:0] The display offset of the vertical direction,changing the value will cause the effect fo scrolling at vertical direction.	0	RW

REG[27h]Vertical Scroll Offset Register 1(VOFS1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Vertical Display Scroll Offset[9:8] The display offset of the vertical direction,changing the value will cause the effect of scrolling at vertical direction.	0	RW

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REG[29h]Font Line Distance Setting Register(FLDR)

Bit	Description	Default	Access
7-5	NA	0	RO
4-0	Font Line Distance Setting Setting the font character line distance when setting memory font write cursor auto move(Unit:Pixel)。	0	RW

REG[2Ah]Font Write Cursor Horizontal Position Register 0(F_CURXL)

Bit	Description	Default	Access
7-0	Font Write Cursor Horizontal Position[7:0] The setting of the horizontal cursor position for font writing	0	RW

REG[2Bh]Font Write Cursor Horizontal Position Register 1(F_CURXH)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Font Write Cursor Horizontal Position[9:8] The setting of the horizontal cursor position for font writing	0	RW

REG[2Ch]Font Write Cursor Vertical Position Register 0(F_CURL)

Bit	Description	Default	Access
7-0	Font Write Cursor Vertical Position[7:0] The setting of the vertical cursor position for font writing	0	RW

REG[2Dh]Font Write Cursor Vertical Position Register 1(F_CURXH)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Font Write Cursor Vertical Position[9:8] The setting of the vertical cursor position for font writing	0	RW

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REG[2Eh]Font Write Type Setting Register

Bit	Description				Default	Access
7-6	Font Size Setting				0	RW
		Full Size	Half-Size	Variable Width		
	00b	16*16	8*16	N*16		
	01b	24*24	12*24	N*24		
	1*b	32*32	16*32	N*32		
5-0	Font to Font Width Setting 00h:Font width off 01h:Font to Font width=1 pixel 02h:Font to Font width=2 pixel : 3Fh::Font to Font width=63 pixels				0	RW

REG[2Fh]Serial Font ROM Setting

Bit	Description	Default	Access
7-5	100b	0	RO
4-0	NA	0	RW

7-5 Active Window & Scroll Window Setting Registers

REG[30h]Horizontal Start Point 0 of Active Window(HSAW0)

Bit	Description	Default	Access
7-0	Horizontal Start Point of Active Window[7:0]	0	RW

REG[31h]Horizontal Start Point 1 of Active Window(HSAW1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Horizontal Start Point of Active Window[9:8]	0	RW

REG[32h]Vertical Start Point 0 of Active Window(VSAW0)

Bit	Description	Default	Access
7-0	Vertical Start Point of Active Window[7:0]	0	RW

REG[33h]Vertical Start Point 1 of Active Window(VSAW1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Vertical Start Point of Active Window[8]	0	RW

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REG[34h]Horizontal End Point 0 of Active Window(HEAW0)

Bit	Description	Default	Access
7-0	Horizontal End Point of Active Window[7:0]	0	RW

REG[35h]Horizontal End Point 1 of Active Window(HEAW1)

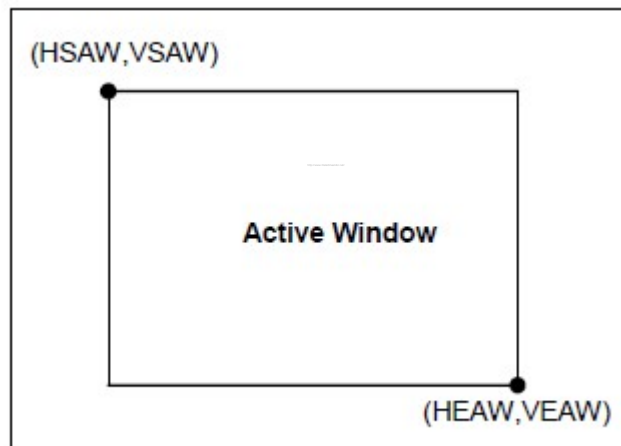
Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Horizontal End Point of Active Window[9:8]	0	RW

REG[36h]Vertical End Point of Active Window 0(VEAW0)

Bit	Description	Default	Access
7-0	Vertical End Point of Active Window[7:0]	0	RW

REG[37h]Vertical End Point of Active Window 1(VEAW1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Vertical End Point of Active Window[8]	0	RW



Active Window

REG[38h]Horizontal Start Point 0 of Scroll Window(HSSW0)

Bit	Description	Default	Access
7-0	Horizontal Start Point of Scroll Window[7:0]	0	RW

REG[39h]Horizontal Start Point 1 of Scroll Window(HSSW1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Horizontal Start Point of Scroll Window[9:8]	0	RW

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REG[3Ah]Vertical Start Point 0 of Scroll Window(VSSW0)

Bit	Description	Default	Access
7-0	Vertical Start Point of Scroll Window[7:0]	0	RW

REG[3Bh]Vertical Start Point 1 of Scroll Window(VSSW1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Vertical Start Point of Scroll Window[8]	0	RW

REG[3Ch]Horizontal End Point 0 of Scroll Window(HESW0)

Bit	Description	Default	Access
7-0	Horizontal End Point of Scroll Window[7:0]	0	RW

REG[3Dh]Horizontal End Point 1 of Scroll Window(HESW1)

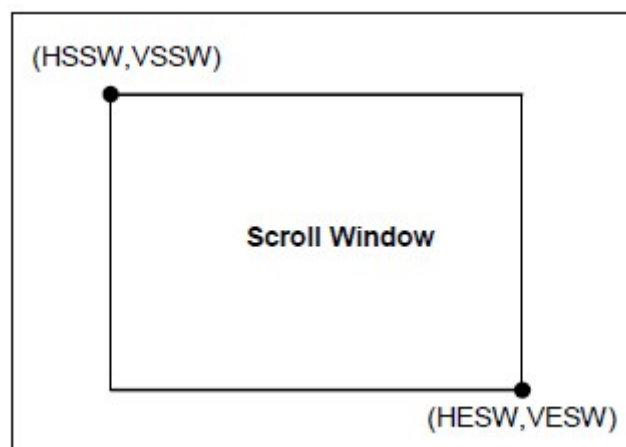
Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Horizontal End Point of Scroll Window[9:8]	0	RW

REG[3Eh]Vertical End Point 0 of Scroll Window(VESW0)

Bit	Description	Default	Access
7-0	Vertical End Point of Scroll Window[7:0]	0	RW

REG[3Fh] Vertical End Point 1 of Scroll Window(VESW1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Vertical End Point of Scroll Window[8]	0	RW



Scroll Window

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7-6 Cursor Setting Registers

REG[40h]Memory Write Control Register 0(MWCRO)

Bit	Description	Default	Access
7	Text Mode Enable 0: Graphic mode. 1: Text mode.	0	RW
6	Font Write Cursor/Memory Write Cursor Enable 0: Font write cursor/Text Write Cursor is not visible. 1: Font write cursor/Text Write Cursor is visible	0	RW
5	Font Write Cursor/Memory Write Cursor Blink Enable 0: Normal display 1: Blink display	0	RW
4	NA	0	RO
3-2	Memory Write Direction(Only for Graphic Mode) 00: Left->Right then Top->Down. 01: Right->Left then Top->Down. 10: Top->Down then Left->Right. 11: Down->Top then Left->Right.	0	RW
1	Memory Write Cursor Auto-Increase Disable 0: Cursor auto-increases when memory write. 1: Cursor doesn't auto-increases when memory write	0	RW
0	Memory Read Cursor Auto-Increase Disable 0: Cursor auto-increases when memory read. 1: Cursor doesn't auto-increases when memory read.	0	RW

REG[41h]Memory Write Control Register1(MWCR1)

Bit	Description	Default	Access
7	Graphic Cursor Enable 0: Graphic Cursor disable. 1; Graphic Cursor enable.	0	RW
6-4	Graphic Cursor Selection Bit Select one from eight graphic cursor types. 000: Graphic Cursor Set 1。 001: Graphic Cursor Set 2。 010: Graphic Cursor Set 3。 : : : : 111: Graphic Cursor Set 8.	0	RW
3-2	Write Destination Selection 00: Layer 1-2.	0	RW

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	01: CGRAM。 10: Graphic Cursor。 11: Pattern。		
1	NA	0	RO
0	Layer No.for Writing Selection 0:Layer 1. 1:Layer 2.	0	RW

REG[44h]Blink Time Control Register(BTCR)

Bit	Description	Default	Access
7-0	Text Blink Time Setting(Unit:Frame) 00h: 1 Frame time 01h: 2 Frame time 02h: 3 Frame time : : : FFh: 256 Frame time	0	RW

REG[45h]Memory Read Cursor Direction(MRCD)

Bit	Description	Default	Access
7-2	NA	0	RW
1-0	Memory Read Direction(Only for Graphic Mode) 00b:Left->Right then Top->Down. 01b:Right->Left then Top->Down. 10b:Top->Down then Left->Right. 11b:Down->Top then Left->Right.	0	RW

REG[46h]Memory Write Cursor Horizontal Position Register 0(CURH0)

Bit	Description	Default	Access
7-0	Memory Write Cursor Horizontal Location[7:0]	0	RW

REG[47h]Memory Write Cursor Horizontal Position Register 1(CURH1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Mememory Write Cursor Horizontal Location[9:8]	0	RW

REG[48h]Memory Write Cursor Vertical Position Register 0(CURV0)

Bit	Description	Default	Access
7-0	Memory Write Cursor Vertical Location[7:0]	0	RW

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REG[49h]Memory Write Cursor Vertical Position Register(CURV1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Memory Write Cursor Vertical Location[8]	0	RW

REG[4Ah]Memory Read Cursor Horizontal Position Register 0(RCURH0)

Bit	Description	Default	Access
7-0	Memory Read Cursor Horizontal Location[7:0]	0	RW

REG[4Bh]Memory Read Cursor Horizontal Position Register 1(RCURH01)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Memory Read Cursor Horizontal Location[9:8]	0	RW

REG[4Ch]Memory Read Cursor Vertical Position Register 0(RCURV0)

Bit	Description	Default	Access
7-0	Memory Read Cursor Vertical Location[7:0]	0	RW

REG[4Dh]Memory Read Cursor Vertical Position Register 1(RCURV1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Memory Read Cursor Vertical Location[8]	0	RW

REG[4Eh]Font Write Cursor and Memory Write Cursor Horizontal Size Register(CURHS)

Bit	Description	Default	Access
7-5	NA	0	RO
4-0	Font Write Cursor Vertical Size Setting[4:0] Unit:Pixel Note:When font is enlarged,the cursor setting will multiply the same times as the font enlargement.	0	RW

REG[4Eh]Font Write Cursor Vertical Size Register(CURVS)

Bit	说明	初始值	Access
7-5	NA	0	RO
4-0	字体光标垂直大小设定 注意：当文字被放大，文字光标垂直方向将放大同文字相同的倍数。	0	RW

7-7 Touch Panel Control Registers

REG[70h]Touch Panel Control Register 0(TPCR0)

--	--	--

Bit	Description	Default	Access
7	Touch Panel Enable Bit 0:Disable 1:Enable	0	RW
6-4	TP Sample Time Adjusting 000b:Wait 512 system clock period for ADC data ready. 001b: Wait 1024 system clock period for ADC data ready. 010b: Wait 2048 system clock period for ADC data ready. 011b: Wait 4096 system clock period for ADC data ready. 100b: Wait 8192 system clock period for ADC data ready. 101b: Wait 16384 system clock period for ADC data ready. 110b: Wait 32768 system clock period for ADC data ready. 111b: Wait 65536 system clock period for ADC data ready.	0	RW
3	Touch Panel Wakeup Enable 0:Disable the Touch Panel wake-up function. 1:Touch Panel can wake-up the sleep mode.	0	RW
2-0	ADC Clock Setting 000b:System CLK 001b: (System CLK) /2。 010b: (System CLK)/4 011b: (System CLK)/8 100b: (System CLK)/16 101b: (System CLK)/32 110b: (System CLK)/64 111b: (System CLK)/128	0	RW

REG[71h]Touch Panel Control Register 1(TPCR1)

Bit	Description	Default	Access
7	NA	0	RO
6	TP Manual Mode Enable 0:Auto mode. 1:Using the manual mode.	0	RW
5	TP ADC Reference Voltage Source 0:Vref generated from internal circuit. No external voltage is needed. 1:Vref from external source,1/2 VDD is needed for ADC.	0	RW
1-0	Mode Selection for TP Manual Mode 00b:IDLE mode: Touch Panel in idle mode. 01b:Wait for TP event,Touch Panel event could cause the interrupt or be read from REG[F1h]Bit2. 10b:Latch X data,in the phase,X Data can be latched in REG[72h] and REG[74h]. 11b:Latch Y data,in the phase, Y Data can be latched in REG[73h] and REG[74h].	0	RW

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REG[72h]Touch Panel X High Byte Data Register(TPXH)

Bit	Description	Default	Access
7-0	Touch Panel X Data Bit[9:2]	0	RW

REG[73h]Touch Panel Y High Byte Data Register(TPYH)

Bit	Description	Default	Access
7-0	Touch Panel Y Data Bit[9:2]	0	RW

REG[74h]Touch Panel X/Y Low Byte Data Register(TPXYL)

Bit	Description	Default	Access
7	ADET Touch Event Detector 0:Touch Panel is touched. 1:Touch Panel is not touched.	1	RO
6-4	NA	0	RO
3-2	Touch Panel Y Data Bit[1:0]	0	RW
1-0	Touch Panel X Data Bit[1:0]	0	RW

7-8 Graphic Cursor Setting Registers

REG[80h]Graphic Cursor Horizontal Position Register 0(GCHP0)

Bit	Description	Default	Access
7-0	Graphic Cursor Horizontal Location[7:0]	0	RW

REG[81h]Graphic Cursor Horizontal Position Register 1(GCHP1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Graphic Cursor Horizontal Location [9:8]	0	RW

REG[82h]Graphic Cursor Vertical Position Register 0(GCVP0)

Bit	Description	Default	Access
7-0	Graphic Cursor Vertical Location[7:0]	0	RW

REG[83h]Graphic Cursor Vertical Position Register 1(GCVP1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Graphic Cursor Vertical Location [8]	0	RW

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REH[84h]Graphic Cursor Color 0(GCC0)

Bit	Description	Default	Access
7-0	Graphic Cursor Color 0 with 256 Colors RGB Format[7:0]=RRRGGBB.	0	RW

REG[85h]Graphic Cursor Color 1(GCC1)

Bit	Description	Default	Access
7-0	Graphic Cursor Color 1 with 256 Colors RGB Format[7:0]=RRRGGBB.	0	RW

7-9 PLL Setting Registers

REG[88h]PLL Control Register 0(PLLC0)

Bit	Description	Default	Access
7	PLLDIVM 0: divided by 1. 1: divided by 2. $SYS_CLK=FIN*(PLLDIVN[4:0]+1)/((PLLDIVM+1)*(2^{PLLDIVK(2:0)})$	0	RW
6-5	NA	0	RO
4-0	PLLDIVN[4:0] PLL input parameter,the value should be 1-31.	07h	RW

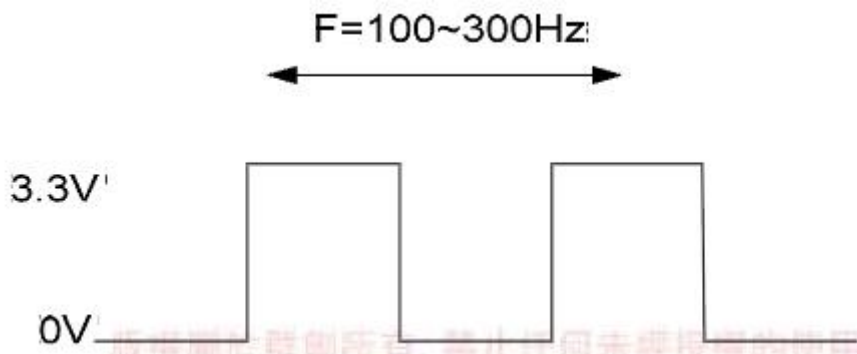
REG[89h] PLL Control Register 1(PLLC1)

Bit	Description	Default	Access
7-3	NA	0	RO
2-0	PLLDIVK[2:0] PLL Output divider 000: divided by 1。 001: divided by 2。 010: divided by 4。 011: divided by 8。 100: divided by 16。 101: divided by 32。 110: divided by 64。 111: divided by 128。	02h	RW

7-11 PWM Control Registers

XYF480272C-TP use pwm control the Backlight.

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REG[8Ah]PWM Control Register(P1CR)

Bit	Description	Default	Access
7	PWM1 Enable 0: Disable. 1: Enable.	0	RW
6	PWM1 Disable Level 0: PWM1 is Normal L when PWM disable or Sleep mode. 1: PWM1 is Normal H when PWM disable or Sleep mode. The bit is only usable when P1CR bit 4 is 0.	0	RW
5	Reserved	0	RO
4	PWM Function Selection 0: PWM function. 1: PWM output a fixed frequency signal and it is equal to 1/16 oscillator clock. PWM=Fin/16		RW
3-0	PWM Clock Source Divide Ratio 0000b:SYS_CLK/1 1000b:SYS_CLK/256 0001b:SYS_CLK/2 1001b:SYS_CLK/512 0010b:SYS_CLK/4 1010b:SYS_CLK/1024 0011b:SYS_CLK/8 1011b:SYS_CLK/2048 0100b:SYS_CLK/16 1100b:SYS_CLK/4096 0101b:SYS_CLK/32 1101b:SYS_CLK/8192 0110b:SYS_CLK/64 1110b:SYS_CLK/16384 0111b:SYS_CLK/128 1111b:SYS_CLK/32768	0	RW

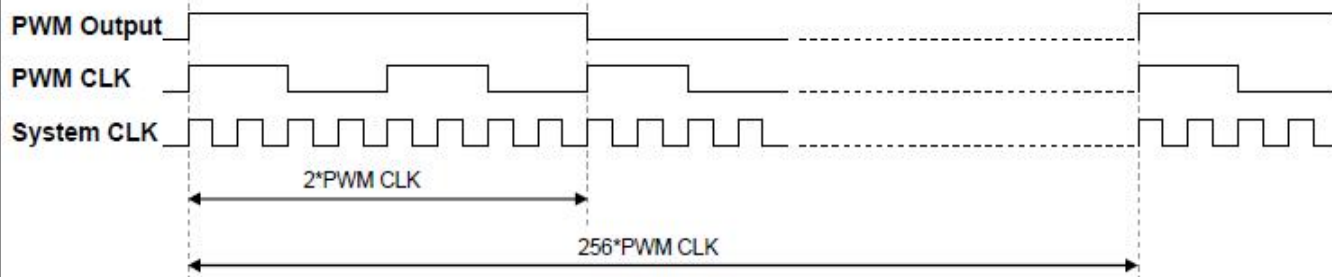
REG[8Bh]PWM Duty Cycle Register(P1DCR)

Bit	Description	Default	Access
7-0	PWM Cycle Duty Selection Bit 00h:1/256 Duty with PWM1 clock source. 01h:2/256 Duty with PWM1 clock source. 02h:3/256 Duty with PWM1 clock source.	0	RW

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FEh:255/256 Duty with PWM1 clock source.
FFh:256/256 Duty with PWM1 clock source.



Ex : PWM source CLK = System CLK/4 and 2/256 High Period

PWM Waveform

REG[8Eh]Memory Clear Control Register(MCLR)

Bit	Description	Default	Access
7	Memory Clear Function 0: End or Stop. When write 0 to this bit LCM will stop the Memory clear function. Or if read back this bit is 0, it indicates that Memory clear function is complete. 1: Start the memory clear function.	0	RW
6	Memory Clear Area Setting 0: Clear the full window. 1: Clear the active window	0	RW
5-0	NA	0	RO

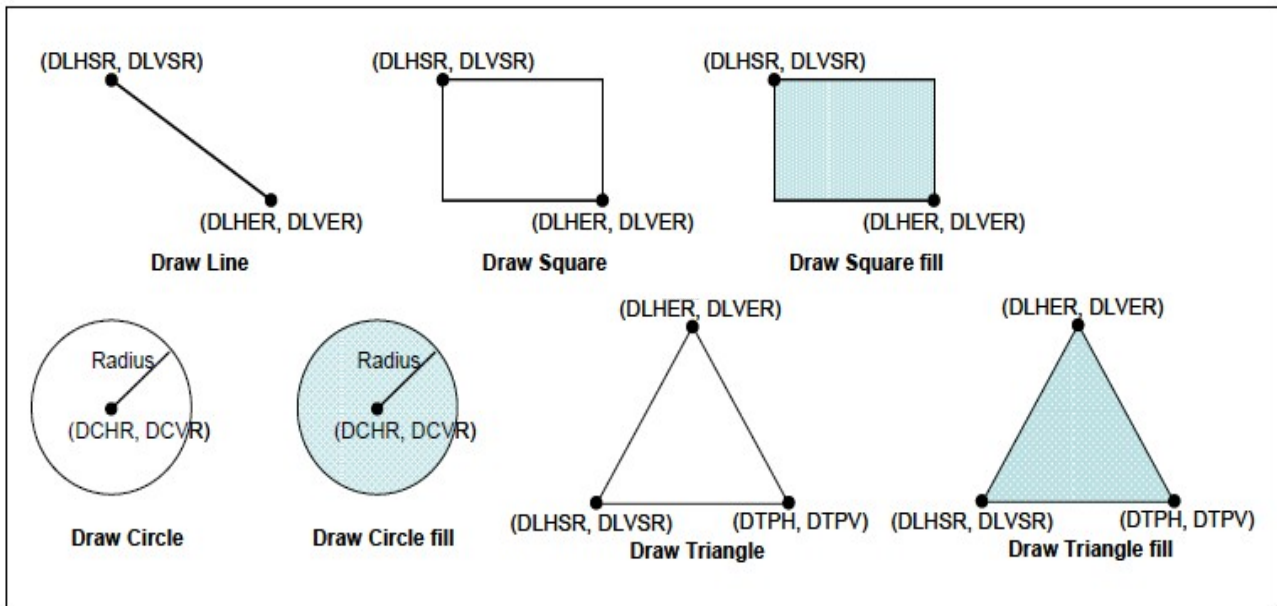
7-12 Drawing Control Registers

REG[90h]Draw Line/Circle/Square Control Register(DCR)

Bit	Description	Default	Access
7	Draw Line/Square/Triangle Start Signal Write Function 0: Stop the drawing function. 1: Start the drawing function. Read Function 0: Drawing function complete. 1: Drawing function is processing.	0	RW
	Draw Circle Start Signal Write Function		

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6	0: Stop the circle drawing function. 1: Start the circle drawing function. Read Function 0: Circle drawing function complete. 1: Circle drawing function is processing.	0	RW
5	Fill the Circle/Square/Triangle Signal 0: Non fill. 1: Fill.	0	RW
4	Draw Line or Square Select Signal 0: Draw line. 1: Draw square.	0	RW
3-1	NA	0	RO
0	Draw Triangle or Line/Square Select Signal 0: Draw Line or Square 1: Draw Triangle	0	RW



Drawing Function Parameter

REG[91h]Draw Line/Square Horizontal Start Address Register 0(DLHSR0)

Bit	Description	Default	Access
7-0	Draw Line/Square Horizontal Start Address[7:0]	0	RW

REG[92h]Draw Line/Square Horizontal Start Address Register 1(DLHSR1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Draw Line/Square Horizontal Start Address[9:8]	0	RW

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REG[93h]Draw Line/Square Vertical Start Address Register 0(DLVSR0)

Bit	Description	Default	Access
7-0	Draw Line/Square Vertical Start Address[7:0]	0	RW

REG[94]Draw Line/Square Vertical Start Address Register 1(DLVSR1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Draw Line/Square Vertical Start Address[8]	0	RW

REG[95h]Draw Line/Square Horizontal End Address Register 0(DLHER0)

Bit	Description	Default	Access
7-0	Draw Line/Square Horizontal End Address[7:0]	0	RW

REG[96h]Draw Line/Square Horizontal End Address Register 1(DLHER1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Draw Line/Square Horizontal End Address [9:8]	0	RW

REG[97h]Draw Line/Square Vertical End Address Register 0(DLVER0)

Bit	Description	Default	Access
7-0	Draw Line/Square Vertical End Address[7:0]	0	RW

REG[98h]Draw Line/Square Vertical End Address Register 1(DLVER1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Draw Line/Square Vertical End Address [8]	0	RW

REG[99h]Draw Circle Center Horizontal Address Register 0(DCHR0)

Bit	Description	Default	Access
7-0	Draw Circle Center Horizontal Address[7:0]	0	RW

REG[9Ah]Draw Circle Center Horizontal Address Register 1(DCHR1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Draw Circle Center Horizontal Address [9:8]	0	RW

REG[9Bh]Draw Circle Center Vertical Address Register 0(DCVR0)

Bit	Description	Default	Access
7-0	Draw Circle Center Vertical Address[7:0]	0	RW

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REG[9Ch]Draw Circle Center Vertical Address Register 1(DCVR1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Draw Circle Center Vertical Address [8]	0	RW

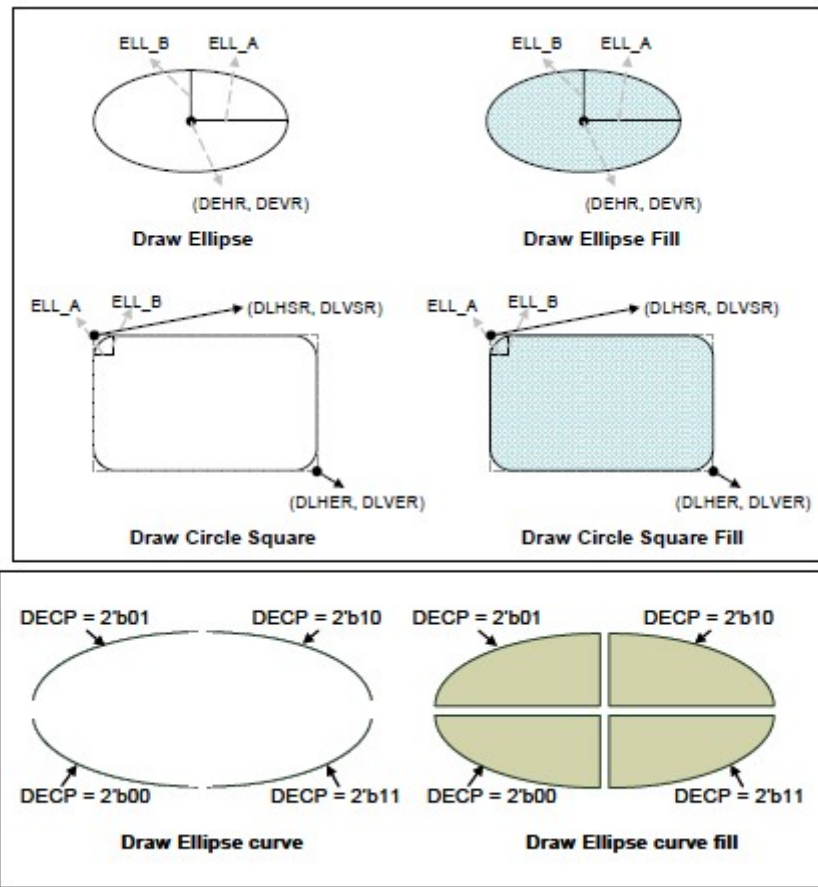
REG[9Dh]Draw Circle Radius Register(DCRR)

Bit	Description	Default	Access
7-0	Draw Circle Radius[7:0]	0	RW

REG[A0h]Draw Ellipse/Ellipse Curve/Circle Square Control Register

Bit	Description	Default	Access
7	<p>Draw Ellipse/Circle Square Start Signal Write Function</p> <p>0: Stop the drawing function. 1: Start the drawing function.</p> <p>Read Function</p> <p>0: Drawing function complete. 1: Drawing function is processing.</p>	0	RW
6	<p>Fill the Ellipse/Circle Square Signal</p> <p>0: Non fill. 1: fill.</p>	0	RW
5	<p>Draw Ellipse/Ellipse Curve or Circle Square Select Signal</p> <p>0: Draw Ellipse/Ellipse Curve. (Depend on bit4) 1: Draw Circle Square.</p>	0	RW
4	<p>Draw Ellipse or Ellipse Curve Select Signal</p> <p>0: Draw Ellipse 1: Draw Ellipse Curve</p>	0	RW
3-2	NA	0	RO
1-0	Draw Ellipse Curve Part Select(DECP)	0	RW

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画图功能图

REG[A1h]Draw Ellipse/Circle Square Long axis Setting Register(ELL_A0)

Bit	Description	Default	Access
7-0	Draw Ellipse/Circle Square Long axis[7:0]	0	RW

REG[A2h]Draw Circle Radius Register(ELL_A1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Draw Ellipse/Circle Square Long axis [9:8]	0	RW

REG[A3h]Draw Ellipse/Circle Square Short axis Setting Register(ELL_B0)

Bit	Description	Default	Access
7-0	Draw Ellipse/Circle Square Short axis [7:0]	0	RW

REG[A4h]Draw Ellipse/Circle Square Short axis Setting Register(ELL_B1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Draw Ellipse/Circle Square Short axis [8]	0	RW

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REG[A5h]Draw Ellipse/Circle Square Center Horizontal Address Register0(DEHR0)

Bit	Description	Default	Access
7-0	Draw Ellipse/Circle Square Center Horizontal Address[7:0]	0	RW

REG[A6h]Draw Ellipse/Circle Square Center Horizontal Address Register1(DEHR1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Draw Ellipse/Circle Square Center Horizontal Address [9:8]	0	RW

REG[A7h]Draw Ellipse/Circle Square Center Vertical Address Register0(DEVR0)

Bit	Description	Default	Access
7-0	Draw Ellipse/Circle Square Center Vertical Address [7:0]	0	RW

REG[A8h]Draw Ellipse/Circle Square Center Vertical Address Register1(DEVR1)

Bit	Description	Default	Access
7-1	NA	0	RO
1-0	Draw Ellipse/Circle Square Center Vertical Address [8]	0	RW

REG[A9h]Draw Triangle Point 2 Horizontal Address Register0(DTPH0)

Bit	Description	Default	Access
7-0	Draw Triangle Point 2 Horizontal Address[7:0]	0	RW

REG[AAh]Draw Triangle Point 2 Horizontal Address Register1(DTPH1)

Bit	Description	Default	Access
7-2	NA	0	RO
1-0	Draw Triangle Point 2 Horizontal Address [9:8]	0	RW

REG[ABh]Draw Triangle Point 2 Vertical Address Register0(DTPV0)

Bit	Description	Default	Access
7-0	Draw Triangle Point 2 Vertical Address [7:0]	0	RW

REG[ACh]Draw Triangle Point 2 Vertical Address Register1(DTPV1)

Bit	Description	Default	Access
7-1	NA	0	RO
0	Draw Triangle Point 2 Vertical Address [8]	0	RW

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7-13 Floating Window Control Registers

REG[D0h]Floating Windows Start Address XA 0(FWSAXA0)

Bit	Description	Default	Access
7-0	Floating Windows Start Address XA[7:0]	0	RW

REG[D1h]Floating Windows Start Address XA1(FWSAXA1)

Bit	Description	Default	Access
7-2	NA	0	RW
1-0	Floating Windows Start Address XA[9:8]	0	RW

REG[D2h] Floating Windows Start Address YA0 (FWSAYA0)

Bit	Description	Default	Access
7-0	Floating Windows Start Address YA[7:0]	0	RW

REG[D3h]Floating Windows Start Address YA1(FWSAYA1)

Bit	Description	Default	Access
7-1	NA	0	RW
0	Floating Windows Start Address YA[8]	0	RW

REG[D4h] Floating Windows Width 0 (FWW0)

Bit	Description	Default	Access
7-0	Floating Windows Width Setting[7:0]	0	RW

REG[D5h]Floating Windows Width1(FWW1)

Bit	Description	Default	Access
7-2	NA	0	RW
1-0	Floating Windows Width Setting [9:8]	0	RW

REG[D6h] Floating Windows Height 0 (FWH0)

Bit	Description	Default	Access
7-0	Floating Windows Height Setting[7:0]	0	RW

REG[D7h]Floating Windows Height1(FWH1)

Bit	Description	Default	Access
7-2	NA	0	RW
1-0	Floating Windows Height Setting [9:8]	0	RW

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REG[D8h] Floating Windows Display X Address 0 (FWDXA0)

Bit	Description	Default	Access
7-0	Floating Windows Display X Address[7:0]	0	RW

REG[D9h] Floating Windows Display X Address1(FWDXA1)

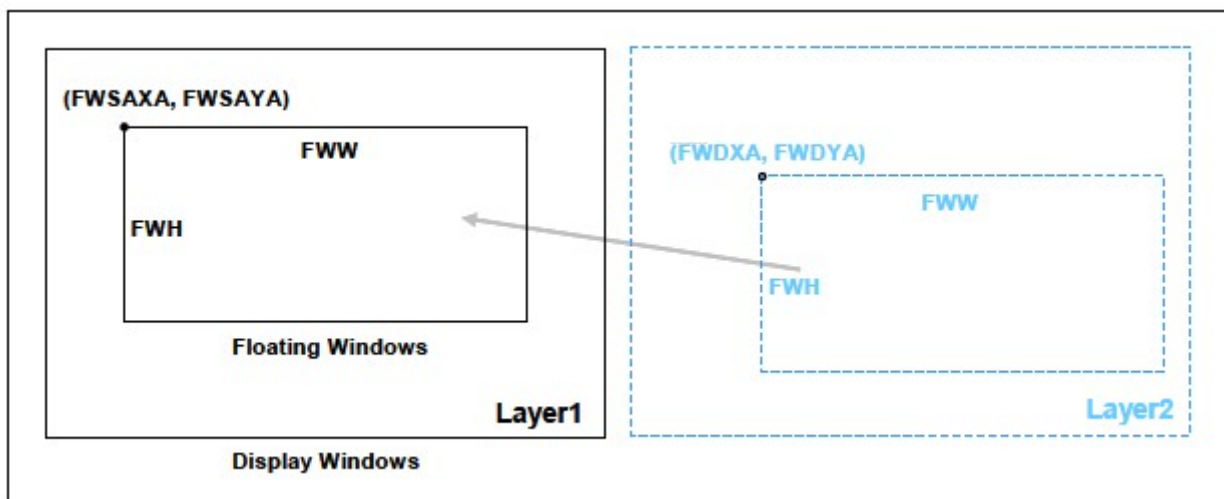
Bit	Description	Default	Access
7-2	NA	0	RW
1-0	Floating Windows Display X Address [9:8]	0	RW

REG[DAh] Floating Windows Display Y Address 0 (FWDYA0)

Bit	Description	Default	Access
7-0	Floating Windows Display Y Address [7:0]	0	RW

REG[DBh] Floating Windows Display Y Address1(FWDYA1)

Bit	Description	Default	Access
7-1	NA	0	RW
0	Floating Windows Display Y Address [8]	0	RW



浮动窗口

7-13 Interrupt Control Registers

REG[F0h] Interrupt Control Register1(INTC1)

Bit	Description	Default	Access
7-3	NA	0	RO
2	Touch Panel Interrupt Enable Bit 0:Disable Touch interrupt. 1:Enable Touch interrupt.	0	RW
1-0	NA	0	RW

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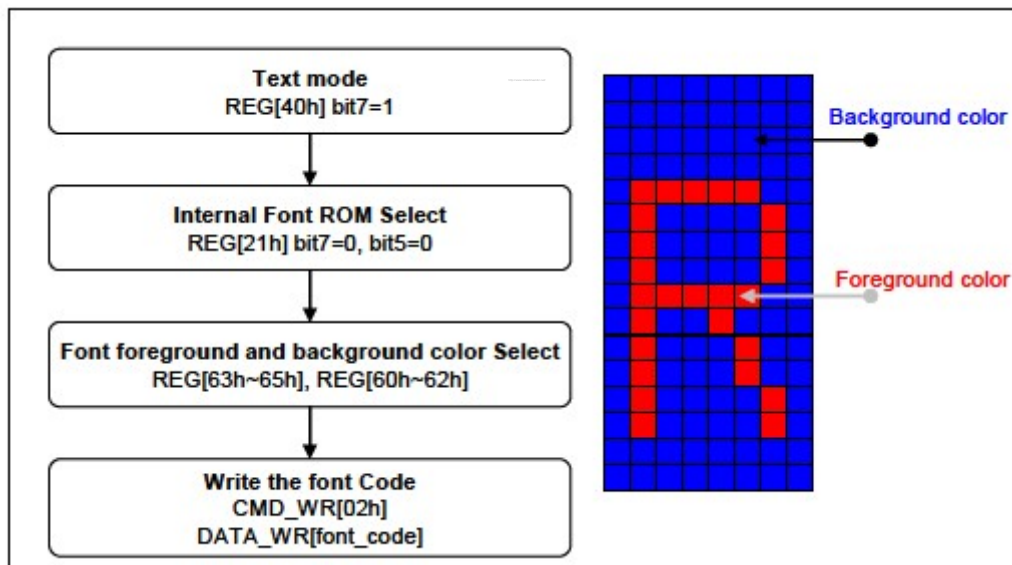
REG[F1h]Interrupt Control Register2(INTC2)

Bit	Description	Default	Access
7-3	NA	0	RO
2	Write Function->Touch Panel Interrupt Clear Bit 0:No operation. 1:Clear the touch interrupt Read Function->Touch Panel Interrupt Status 0:No Touch Panel interrupt happens 1:Touch Panel interrupt happens.	0	RW
1-0	NA	0	RW

八.Font

8-1 Internal Font ROM

XYF480272C-TP embedded 8*16 dots ASC || Font ROM that provides user a convenient way to input characters by code.The embedded character set support ISO/IEC 8859-1~4 coding standard..Besides,user can choose the font foreground color by setting the REG[60h~62h] and background color by setting the REG[63h~65h].For the procedure of characters writing please refers to below figure:



h

ASC || Font ROM Programming Procedure

表 1 shows the standard character encoding of ISO/IEC 8859-1.ISO means International Organization for Standardization.The ISO/IEC 8859-1,generally called”Latin-1”,is the first 8-bit coded character sets that developed by the ISO.It refers to ASCII that consisting of 192 characters from the Latin script in range 0xA0-0xFF.This character encoding is used throughout Western Europe,includes

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Albanian,Afrikaans,Breton,Faroese,Frisian,Galician,German,Greenlandic,Icelandic,Irish,Italian,Latin,Luxembourgish,Norwegian,Portuguese,Rhaeto-Romanic,Scottish Gaelic,Spanish,Swedish.English letters with no accent marks also can use ISO/IEC 8859-1.

In addition,it is also commonly used in many languages outside Europe,such as Swahili,Indonesian,Malaysian and Tagalog.

H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		☺	☹	♥	♦	♣	♠	●	◻	◯	♁	♂	♀	♪	♫	☀
1	▶	◀	↕	!!	¶	§	■	↑	↓	→	←	↔	▲	▼		
2	SP	!	"	#	\$	%	&	'	()	*	+	,	-	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[\]	^	_
6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z	{		}	~	
8																
9																
A		ı	ç	€	¤	¦	§	¨	©	ª	«	¬	®	¯		
B	°	±	²	³	´	µ	¶	·	¸	¹	º	»	¼	½	¾	¿
C	À	Á	Â	Ã	Ä	Å	Æ	Ç	È	É	Ê	Ë	Ì	Í	Î	Ï
D	Ð	Ñ	Ò	Ó	Ô	Õ	Ö	×	Ø	Ù	Ú	Û	Ü	Ý	Þ	ß
E	à	á	â	ã	ä	å	æ	ç	è	é	ê	ë	ì	í	î	ï
F	ð	ñ	ò	ó	ô	õ	ö	÷	ø	ù	ú	û	ü	ý	þ	ÿ

表 1: ASC || Block 1(ISO 8859-1)

表 2 shows the standard characters of ISO/IEC 8859-2.ISO/IEC 8859-2 also cited as Latin-2 is the part 2 of the 8-bit coded character sets developed by ISO/IEC 8859.These code values can be used in almost any data interchange system to communicate in the following European languages:Croatian,Czech,Hungarian,Polish,Slovak,Slovenian,and Upper Sorbian.The Serbian,English, German,Latin can use ISO/IEC 8859-2 as well.Furthermore it is suitable to represent some western European languages like Finnish(with the exception for a used in Swedish and Finnish)

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H\I	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0		☺	☹	♥	♠	♣	♣	♣	♣	♣	♣	♣	♣	♣	♣	♣
1	▶	◀	↕	!!	¶	§	■	↑	↓	→	←	↔	▲	▼		
2	SP	!	"	#	\$	%	&	'	()	*	+	,	-	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[\]	^	_
6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z	{		}	~	
8																
9																
A	SP	À	Á	Â	Ã	Ä	Å	Æ	Ç	È	É	Ê	Ë	Ï	Ð	
B	à	á	â	ã	ä	å	æ	ç	è	é	ê	ë	ï	ð		
C	Á	À	Ä	Å	Æ	Ç	È	É	Ê	Ë	Ï	Ð				
D	Ð	Ñ	Ń	Ó	Ô	Õ	Ö	×	Ŕ	Ū	Ú	Ū	Ū	Ý	Ţ	ß
E	ř	á	â	ã	ä	å	î	ç	ç	é	ę	ë	ë	í	î	đ
F	č	ň	ň	ó	ô	õ	ö	÷	ř	ű	ú	ű	ű	ý	ı	·

Figure 2

Figure 3 Shows the standard characters of ISO/IEC 8859-3. ISO/IEC 8859-3 also known as Latin-3 or "South European" is an 8-bit character encoding, third part of the ISO/IEC 8859 standard. It was designed originally to cover Turkish, Maltese and Esperanto, though the introduction of ISO/IEC 8859-9 superseded it for Turkish. The encoding remains popular with users of Esperanto and Maltese, though it also supports English, German, Italian, Latin and Portuguese.

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H/L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0		☺	☹	♥	♦	♣	♠	●	◻	◯	◼	♁	♀	♫	♬	☼
1	▶	◀	↕	!!	¶	§	■	⤴	⤵	⤶	→	←	↔	▲	▼	
2	SP	!	"	#	\$	%	&	'	()	*	+	,	-	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[\]	^	_
6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z	{		}	~	
8																
9																
A	SP	Ħ	˘	£	¤		Ħ	§	˘	İ	Ş	Ğ	Ĵ			Ž
B	˘	ħ	²	³	˘	//	h	.	.	ı	ş	ğ	ĵ	½		ž
C	À	Á	Â		Ã	Ç	Ç	Ç	È	È	È	È	Ì	Ì	Ì	Ì
D		Ñ	Ò	Ó	Ô	Ğ	Ö	×	Ğ	Ū	Ū	Ū	Ū	Ū	Š	ß
E	à	á	â		ã	ç	ç	ç	è	è	è	è	ì	ì	ì	ì
F		ñ	ò	ó	ô	ğ	ö	÷	ğ	û	û	û	û	û	š	·

Figure 3

Figure 4 Shows the standard characters of ISO/IEC 8859-4. ISO/IEC 8859-4 is known as Latin-4 or “North European” is the fourth part of the ISO/IEC 8859 8-bit character encoding. It was designed originally to cover Estonian, Greenlandic, Latvian, Lithuanian, and Sami. This character set also supports Danish, English, Finnish, German, Latin, Norwegian, Slovenian, and Swedish.

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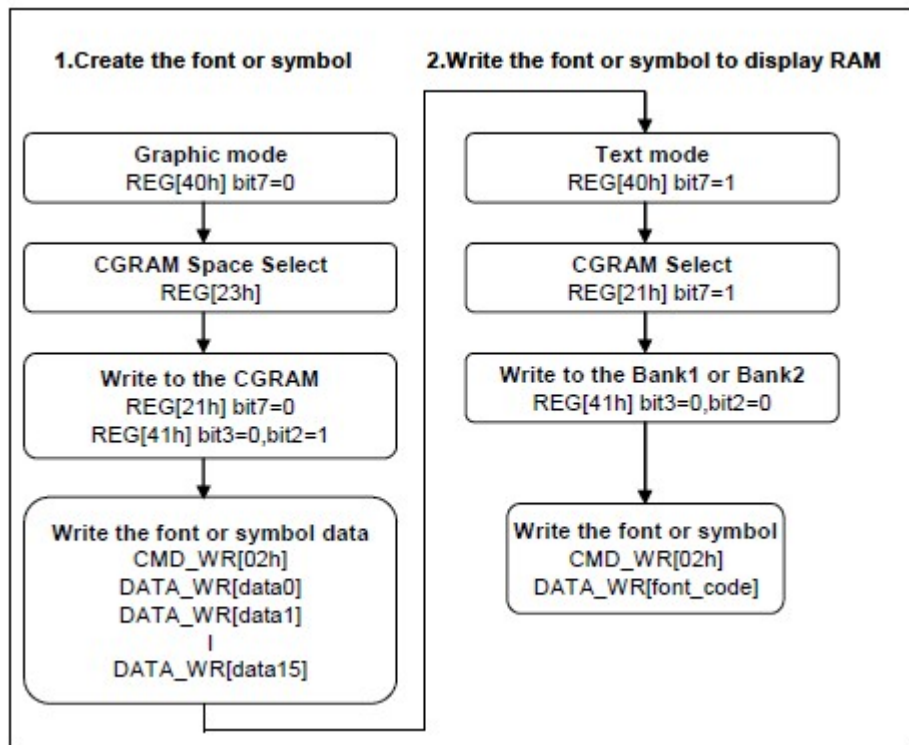
H/L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0		☺	☹	♥	♦	♣	♠	●	◻	◯	◼	♂	♀	♪	♫	☀
1	▶	◀	↕	!!	¶	§	■	↑	↓	→	←	↔	▲	▼		
2	SP	!	"	#	\$	%	&	'	()	*	+	,	-	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[\]	^	_
6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z	{		}	~	
8																
9																
A	SP	À	Á	Â	Ã	Ä	Å	Æ	Ç	È	É	Ê	Ë	Ï	Î	Ï
B	°	à	á	â	ã	ä	å	æ	ç	è	é	ê	ë	ï	î	ï
C	À	Á	Â	Ã	Ä	Å	Æ	Ç	È	É	Ê	Ë	Ï	Î	Ï	
D	Ð	Ñ	Ò	Ó	Ô	Õ	Ö	×	Ø	Ù	Ú	Û	Ü	Ý	Û	ß
E	ā	á	â	ã	ä	å	æ	ç	è	é	ê	ë	ï	î	ï	
F	đ	ñ	ō	ķ	ō	ö	÷	ø	ų	ú	û	ü	Û	ü	ü	•

Figure 4

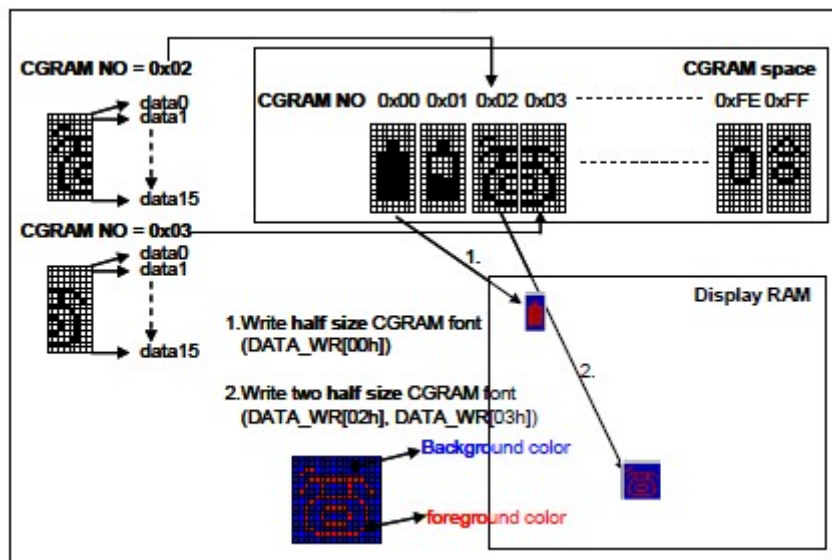
8-2 CGRAM

XYF480272C-TP supports 256 half size space that lets user can create fonts or symbols the want. User just writes the font or symbol data to the indicated space and then writes the corresponding font code, LCM will write the font or symbol to the DDRAM. Also, user can choose the font foreground color by setting the REG[63h~65h] and background color by setting the REG[60h~62h]. The procedure of creating and writing just refers to below figure:

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CGRAM Programming Procedure



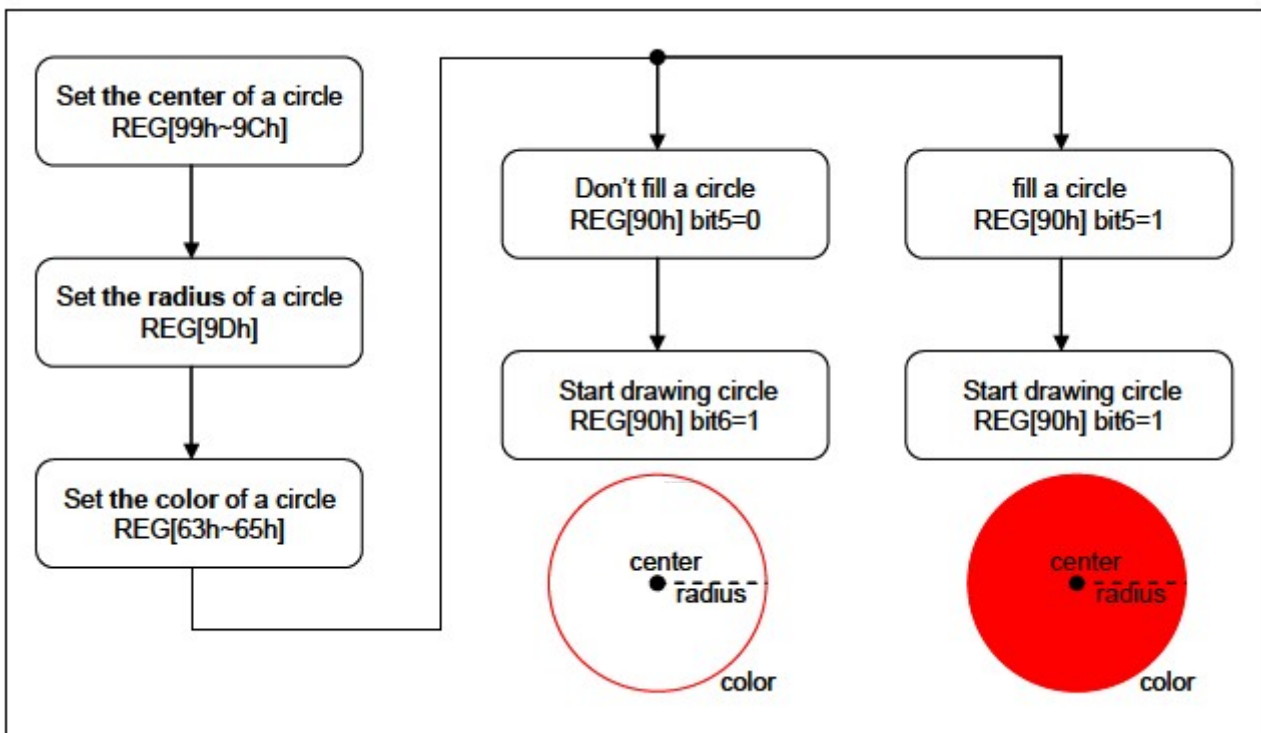
CGRAM Description

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9. Geometric Pattern Drawing Engine

9-1 Circle Input

XYF480272C-TP supports hardware circle drawing function on the DDRAM. User can largely reduce the effort MCU by the function. By setting the center of circle REG[99h~9Ch], the radius of a circle REG[9Dh] and the color of circle REG[63h~65h], and then setting start draw REG[90h]Bit6=1, LCM will implements a corresponding circle on the DDRAM automatically. Moreover, user can decide whether to fill the circle by setting REG[90h]Bit5 as 0(not fill) or 1(fill). The procedure of drawing circle just refers to the below figure:

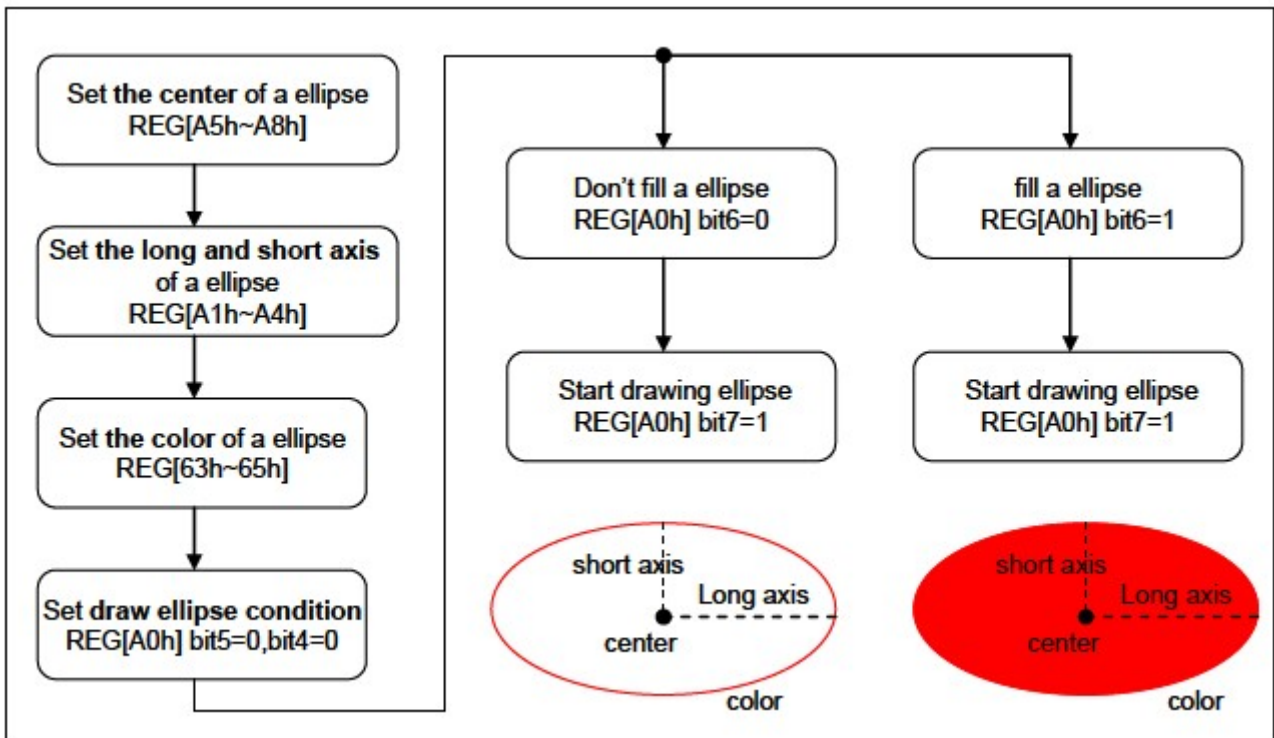


Geometric Pattern Drawing-Draw Circle

9-2 Ellipse Input

XYF480272C-TP supports draw ellipse drawing function makes user to draw ellipse on the DDRAM only use bu few MCU cycles. By setting the center of ellipse REG[A5h~A8h], the long and short axis of ellipse REG[A1h~A4], the color of ellipse REG[63h~65h], the draw ellipse condition REG[A0h]Bit5=0 and Bit4=0, and then setting start draw REG[A0h]Bit7=1, LCM will draw a corresponding Ellipse on the DDRAM. Moreover, user can fill the circle by setting REG[A0h]Bit6=1. The procedure of Drawing ellipse just refers to the below figure:

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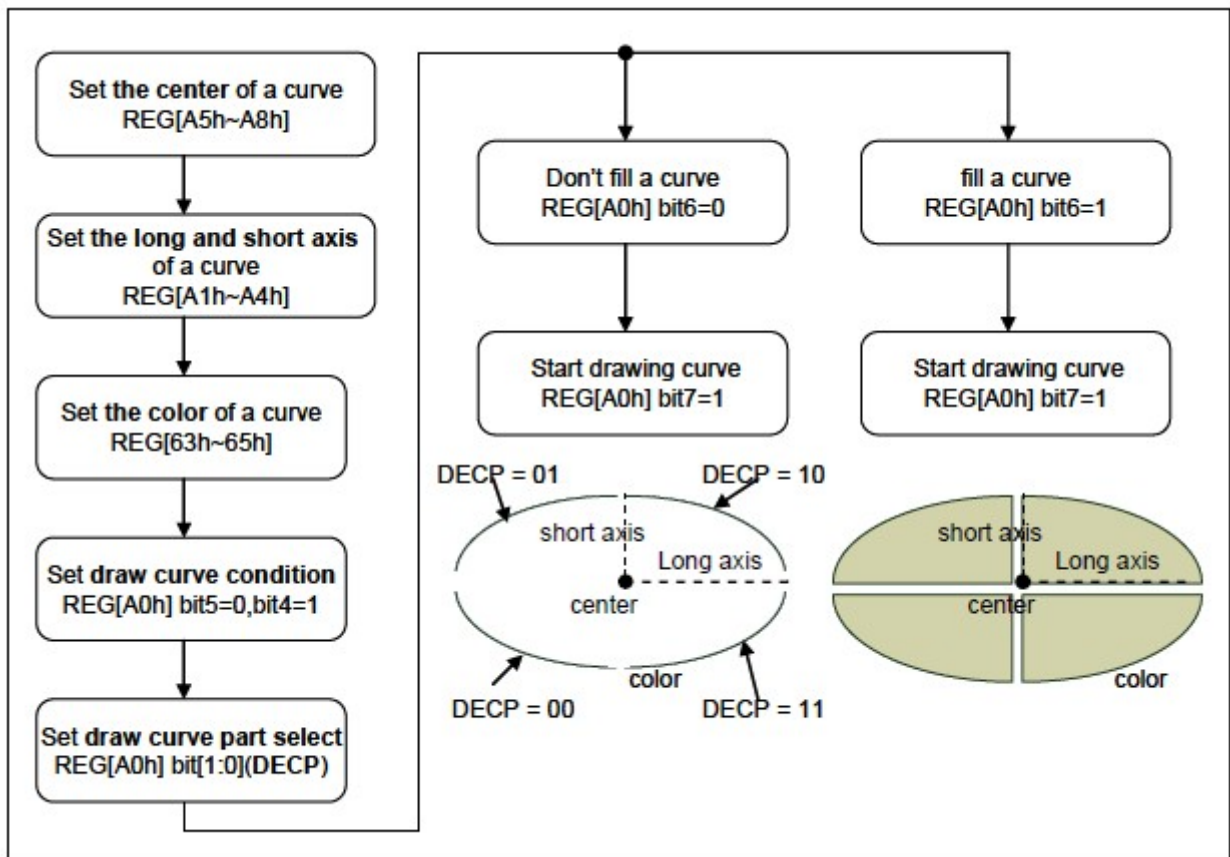


Figure

9-3 Curve Input

XYF480272C-TP supports curve drawing function for user to draw curve on the DDRAM only by few MCU cycles. By setting the center of a curve REG[A5-A8h], the long and short axis of a curve REG[A1-A4], the color of curve REG[63h-65h], the draw curve condition REG[A0h]Bit5=0 and Bit4=1, the curve part of the ellipse REG[A0h]Bit[1:0], and then setting start draw REG[A0h]Bit7=1, LCM will draw a corresponding curve on the DDRAM. Moreover, user can fill the curve by setting REG[A0h] Bit6 =1. The procedure of drawing circle just refers to the below figure:

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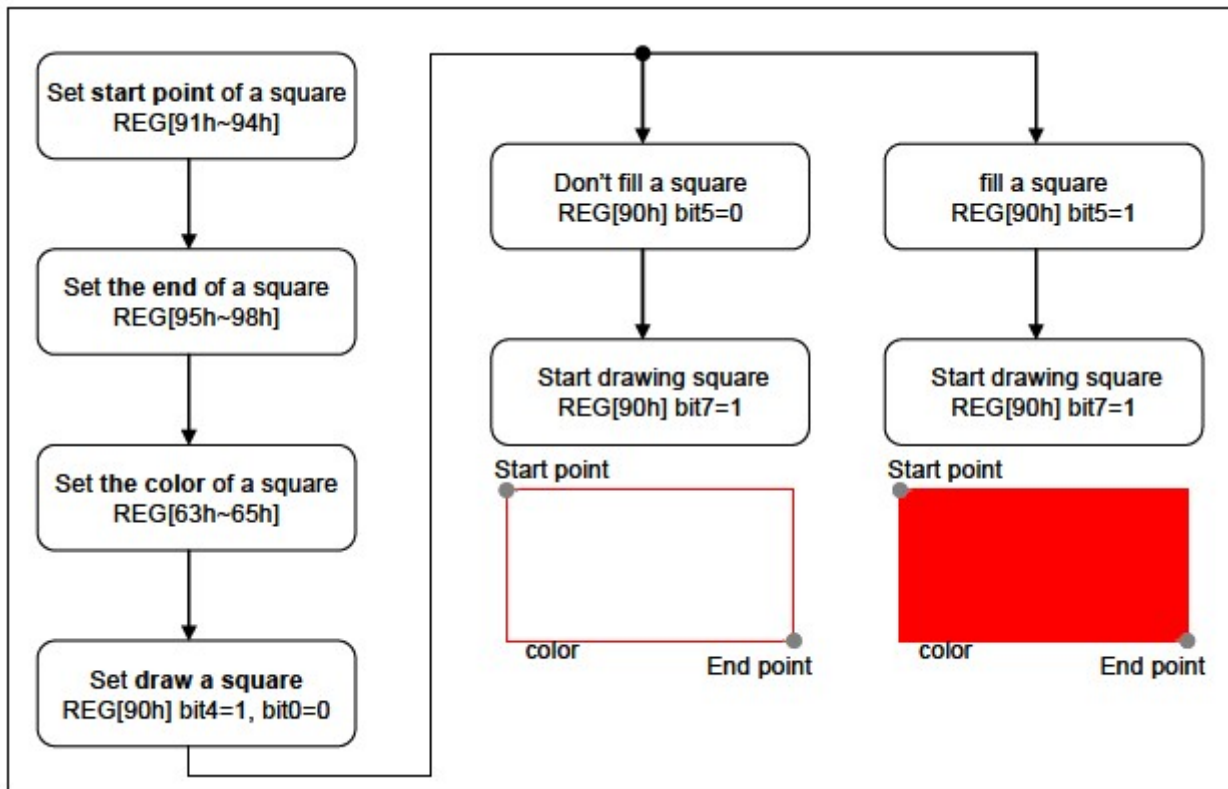


Figure

9-4 Square Input

XYF480272C-TP supports square drawing function for user to draw curve on the DDRAM only by few MCU cycles. By setting the center of a curve REG[91h~94h], the end point of a square REG[95h~98h] and the color of a square REG[63h~65h], then setting draw a square REG[90h]Bit4=1, Bit0=0 and start draw REG[90h]Bit7=1, LCM will draw a corresponding square on the DDRAM. Moreover, user can fill the square by setting REG[90h]Bit5=1. The procedure of drawing square just refers to the below figure:

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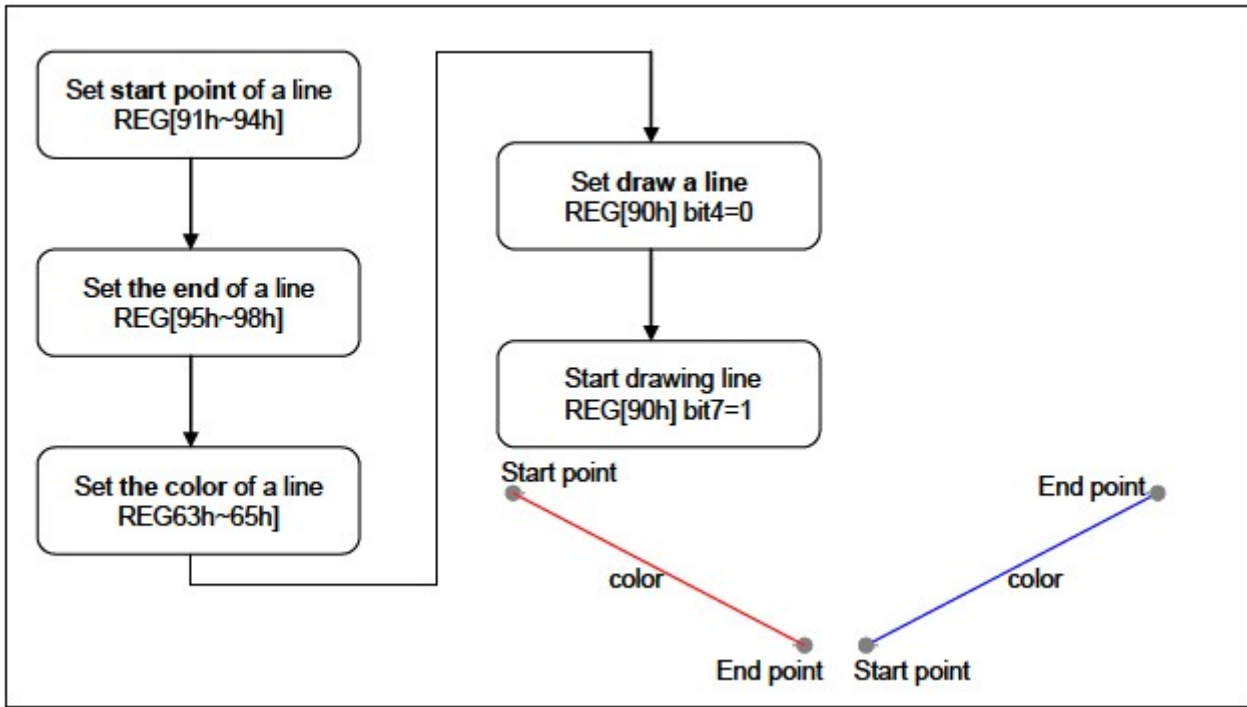


Geometric Pattern Drawing—Draw Rectangle

9-5 Line Input

XYF480272C-TP supports line drawing function for user to draw curve on the DDRAM only by few MCU cycles. By setting the start point of a line REG[91~94h], the end point of a line REG[95h~98h] and the color of a line REG[63h~65h], then setting draw a square REG[90h]Bit4=0, Bit0=0 and start draw REG[90h]Bit7=1, LCM will draw a corresponding line on the DDRAM. The procedure of drawing square just refers to the below figure:

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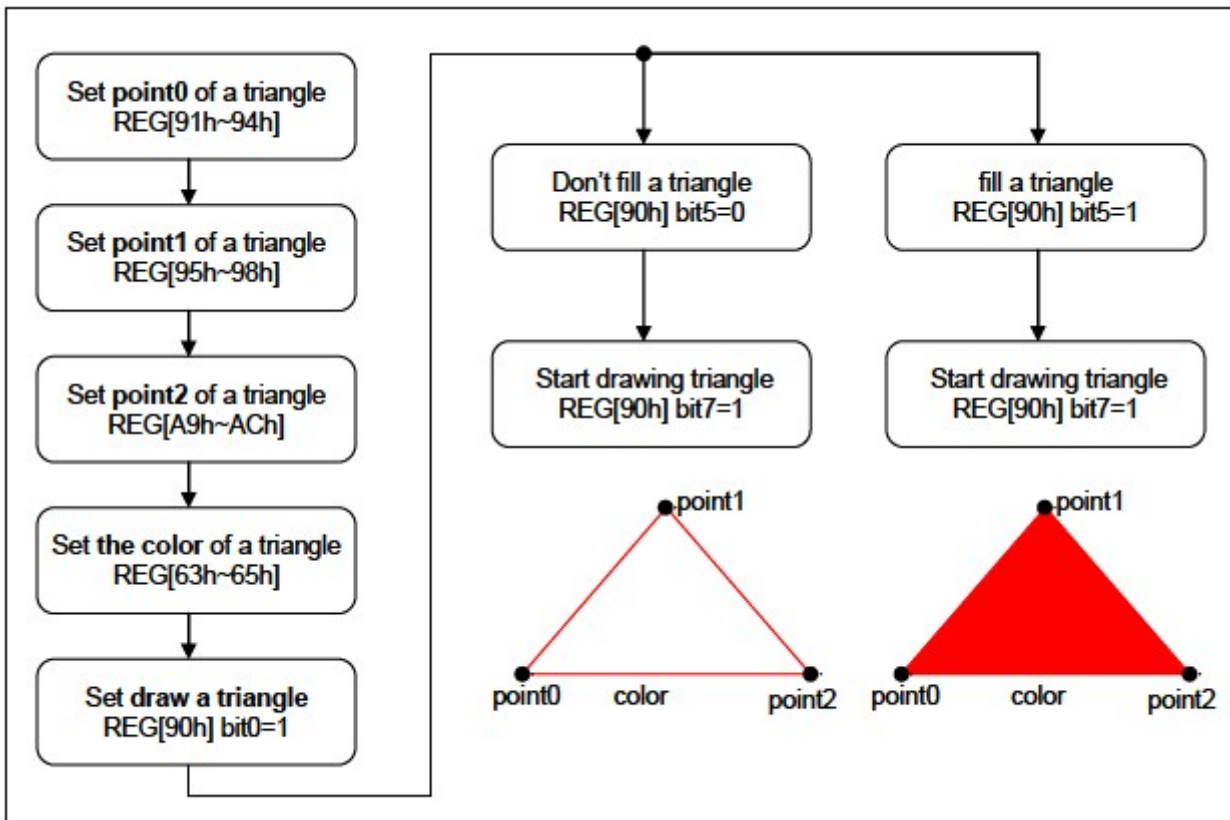


Geometric Pattern Drawing-Draw Line

9-6 Triangle Input

XYF480272C-TP supports square drawing function for user to draw line on the DDRAM only by few MCU cycles. By setting the point0 of a triangle REG[91h-94h], the point1 of a triangle REG[95h-98h], the point2 of a triangle REG[A9h-Ach] and the color of a triangle REG[63h-65h], then setting draw a triangle REG[90h]Bit7=1, LCM will draw a corresponding triangle on the DDRAM. Moreover, user can fill the square by setting REG[90h]Bit5=1. The procedure of drawing square just refers to the below figure:

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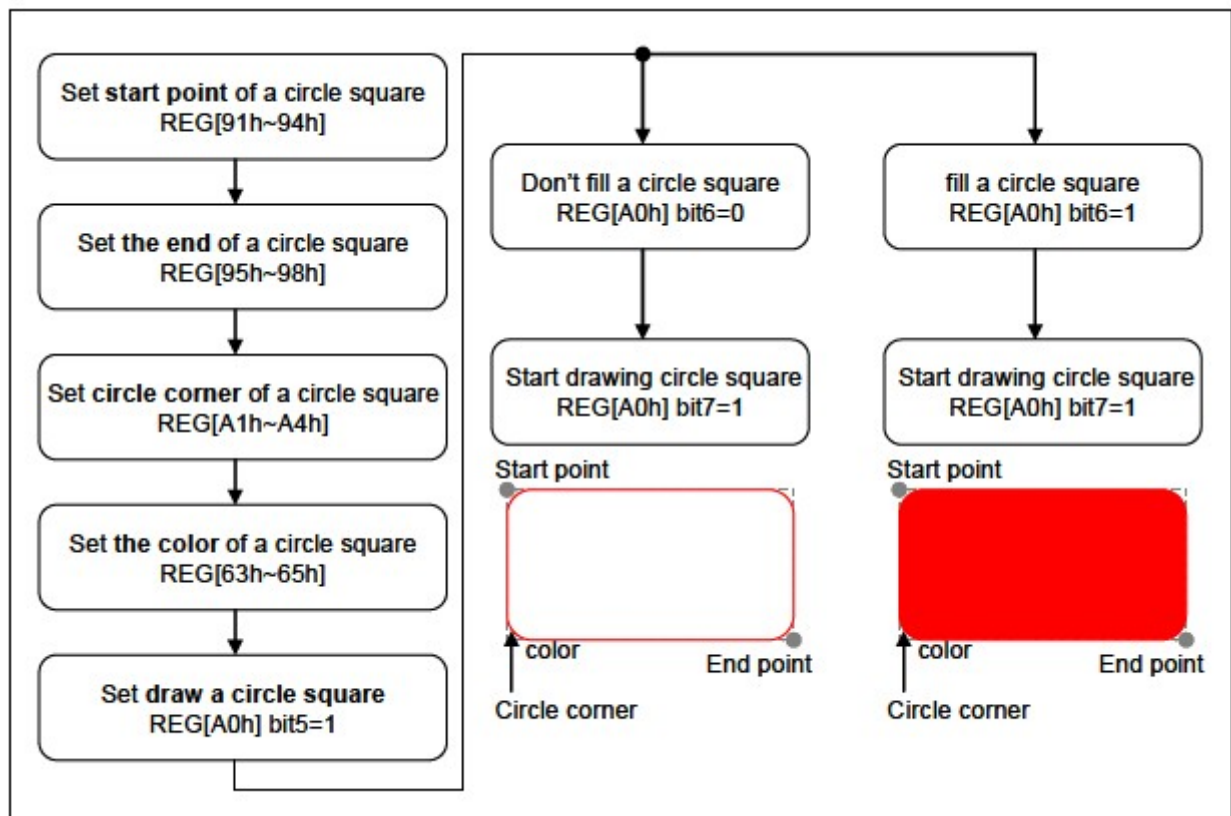


Figure

9-7 Square Of Circle Corner Input

XYF480272C-TP supports circle-square drawing function for user to draw circle square on the DDRAM only by few MCU cycles. By setting the point of a square REG[91h-94h], the end point of a square REG[95h-98h] circle corner REG[A1h-A4h] and the color of a circle square REG[63h-65h], then setting draw a circle square REG[A0h]Bit5=1 and start draw REG[A0h]Bit7=1, LCM will draw a corresponding circle square on the DDRAM. Moreover, user can fill the square by setting REG[A0h]Bit6=1. The procedure of drawing square just refers to the below figure:

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Figure

10.Touch Panel Function

There are 2 detection methods provided by LCM.Hardware interrupt mode or software polling Mode.

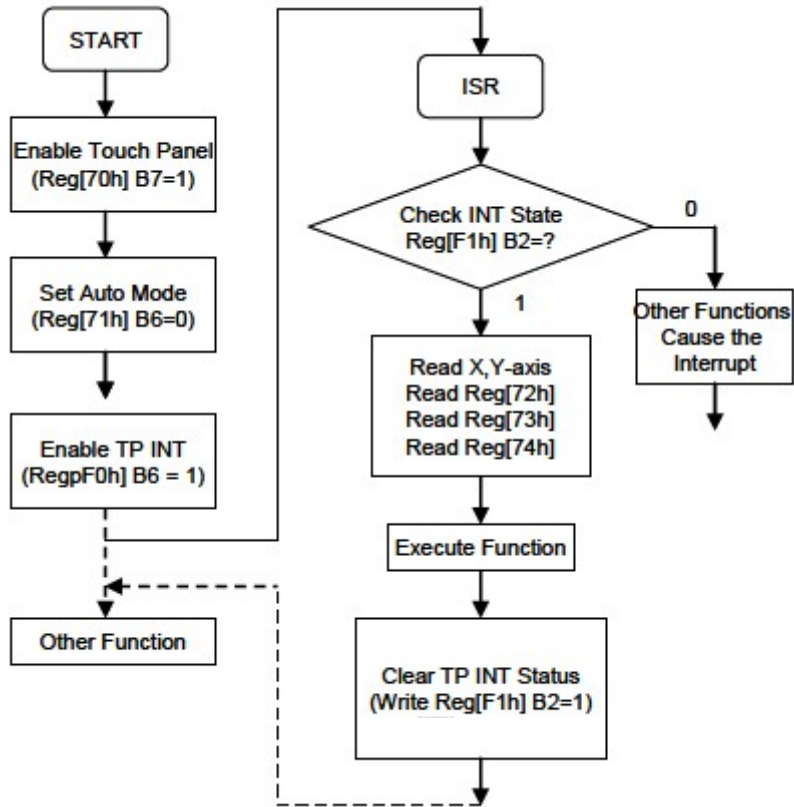
10-1-1 Auto Mode

Auto mode is the easiest way to implement Touch Panel application.User only needs to enable the related Register and LCM will execute the touch panel function and latch the touch data automatically. .

Operation Mode	Event Detection	Description
Auto	Interrupt	When touch event happens,read the corresponding X,Y coordination.
	Polling	Polling the touch event,read the correspondingX,Y coordination.
Manual	Interrupt	Set the operation state to “Checking touch event”for checking the touch event,when touch event interrupt happens,set the state to ‘Latch_X_data”and”Latch_Y_data”for latching the corresponding X,Y coordination,then read the X,Y data

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		and set operation state to “Idle state”
	Polling	持续轮询触控事件，之后切换触摸屏的相位，再读回对应的 XY 坐标值。



Auto mode Flowchart for Touch Panel

Reg.	Bit_Num	Description	Reference
TPCR0	Bit7	Enable Touch Panel function	REG[70h]
TPCR1	Bit6	“Auto-Mode”=0	REG[71h]
	Bit2	Set de-bounce enable for ADET	
TPXH	Bit[7:0]	Touch Panel SEG data MSB byte	REG[72h]
TPYH	Bit[7:0]	Touch Panel COM data MSB byte	REG[73h]
TPXYL	Bit[3:2]	Touch Panel COM data LSB 2bit	REG[74h]
	Bit[1:0]	Touch Panel SEG data LSB 2bit	

10-1-2 Manual Mode

Under the “Manual Mode”, user needs to justify the validation of the touch event by continue polling the status of register. Generally, an enough times of continue accessing the activity of touch event from status register will be confirmed as a valid touch event. The method allows more flexibility and less mistake of justification for different application, but more MCU resource will be occupied.

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Reg.	Bit_Num	Description
TPCR0	Bit7	Enable Touch Panel function
TPCR1	Bit6	“Manual-Mode=1”
	Bit2	Set de-bounce function for ADET
	Bit[1:0]	Mode Selection for TP Manual Mode
TPXH	Bit[7:0]	Touch Panel SEG data MSB byte
TPYH	Bit[7:0]	Touch Panel COM dat MSB byte
TPXYL	Bit[3:2]	Touch Panel COM data LSB 2bit
	Bit[1:0]	Touch Panel SEG data LSB 2bit

10-1-3 External Interrupt Mode

Under this mode LCM hardware interrupt pin(INT) must be connected correctly to the MCU interrupt input pin first. The major processes are listed as follows:

1. Enable Touch Panel function. (REG[70h]Bit7=1)。
2. Set operation mode for TP controller as Auto mode or Manual Mode(REG[71h]Bit6=1)。
3. Enable Touch Panel Interrupt.(REG[F0h]Bit6=1)。
4. When interrupt asserts,the IP jumps to the entry of ISR and check if TP interrupt。
5. If yes,according to the operation mode,doing the data latch for X,Y axis。
6. Process the corresponding jobs for the touch event。
7. Clear the interrupt status bit。

10-1-4 Software Polling Mode

Under the “Polling Mode”,no interrupt pin is needed for connection.The status of touch event can be read from 3 methods.Listed as follows:

1. From the status register(STSR)bit5. (REG[70h]Bit7=1)。
2. From TPXYL(REG[74h])bit7.
3. From the INTC2(REG[F1h])bit2.

10-1-5 Touch Panel Sampling Time Refernce Table

When using the auto mode of Touch Panel function,and the touch event occurring,LCM adapts a specific wait time for X,Y data stability.It is recommended to select a suitable T/P sampling time to avoid the mistake of ADC data latch.Please refer to the following table for the ADC sampling time.

Touch Panel Sampling Time-REG[70h]Bit[6:4]					
SYS-CLK	10M	20M	30M	40M	50M

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REG[70h][2:0]					
000	000	--	--	--	--
001	000	--	--	--	--
010	000	000	000	--	--
011	001	001	000	000	000
100	010	010	001	001	001
101	011	011	010	010	010
110	100	100	011	011	011
111	101	101	100	100	100

Note: The clock source of ADC can not exceed 10MHZ

11. Design and Handling Precaution

1. The LCD panel is made by glass .Any mechanical shock will damage the LCD module.
2. Do not add excessive force on the surface of the display,which may cause the display color change Abnormally.
3. The polarizer on the LCD is easily get scratched.If possible,do not remove the LCD protective film Untile the last step of installation.
4. Never attempt to disassemble or rework the LCD module.
- 5.Only Clean the LCD with Isopropyl Alcohol or Ethy Alcohol.Other solvents may damage the LCD.

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