

CURRENT MODE PWM CONTROL CIRCUITS—YD3843

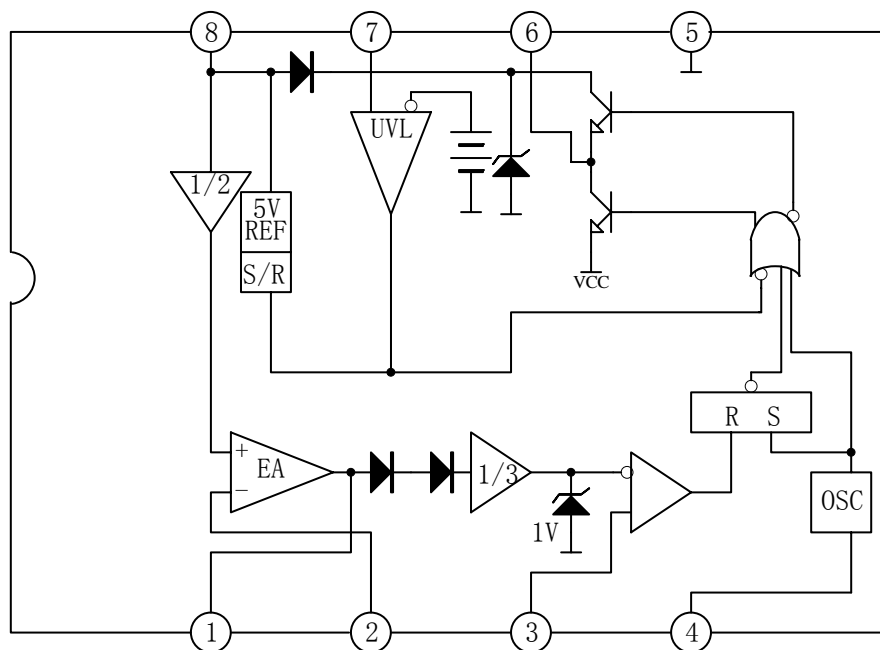
DESCRIPTION

The YD3843 provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count.

FEATURES

- *Optimized for off-line and DC to DC converts
- *Low start up current(<1mA)
- *Automatic feed forward compensation
- *Pulse-by-Pulse current limiting
- *Enhanced load response characteristic
- *Under-voltage lookout with hysteresis.
- *Double pulse Suppression
- *High current totem pole output
- *Internally trimmed band-gap reference
- *500kHz operation
- *Low Ro error amp

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS($T_{amb}=25^{\circ}\text{C}$)

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage(Low impedance Source)	V_{cc}	30	V
Supply Voltage($I_{cc}<30\text{mA}$)	V_{cc}	Self Limiting	V
Output Current	I_o	± 1	A
Output Energy(Capacitive Load)		5	μJ
Analog Inputs(pin 2, 3)	$V_{I(ANA)}$	-0.3 to +6.3	V
Error Amplifier Output Sink Current	$I_{SINK(EA)}$	10	mA
Power Dissipation	P_D	At $T_{amb}\leq 25^{\circ}\text{C}$ 1.0	W
Lead Temperature	T_{lead}	300	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-65—+150	$^{\circ}\text{C}$

Note 1: $T_a > 25^{\circ}\text{C}$, P_D derated with $8\text{mW}/^{\circ}\text{C}$.

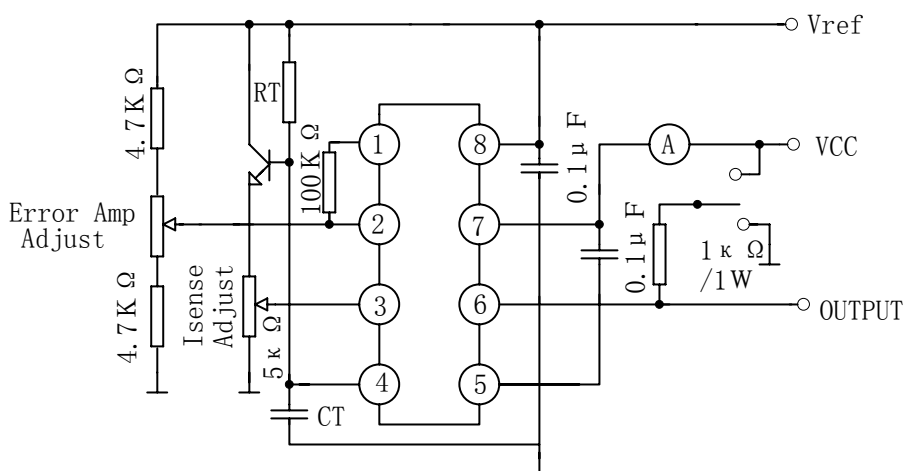
ELECTRICAL CHARACTERISTICS

($V_{cc}=15\text{V}$, $R_T=10\text{k}\Omega$, $C_T=3.3\text{nF}$, $T_{amb}=0^{\circ}\text{C}\sim 70^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Section						
Output Voltage	V_{REF}	$T_j=25^{\circ}\text{C}$, $I_o=1\text{mA}$	4.90	5.00	5.10	V
Line Regulation	ΔV_{REF}	$12\leq V_{IN}\leq 25\text{V}$		6	20	mV
Load Regulation	ΔV_{REF}	$1\leq I_o=20\text{mA}$		6	25	mV
Output Noise Voltage	V_{ose}	$10\text{Hz}\leq f\leq 10\text{kHz}$, $T_j=25^{\circ}\text{C}$ (note 2)		50	6	mV
Long Term Stability		$T_a=25^{\circ}\text{C}$, 1000Hrs(note 2)		5	25	mV
Output Short Circuit	I_{sc}		-30	-100	-180	mA
Oscillator Section						
Initial Accuracy	f	$T_j=25^{\circ}\text{C}$	47	52	57	kHz
Voltage Stability	$\Delta f/\Delta V_{cc}$	$12\leq V_{cc}\leq 25\text{V}$		0.2	1	%
Temp Stability		$T_{min}\leq T_A\leq T_{max}$ (note 2)		5		%
Amplitude	V_{osc}	$V_{pin 4}$ peak to peak		1.7		V
Error Amplifier Section						
Input Voltage	$V_{I(EA)}$	$V_{pin 1}=2.5\text{V}$	2.42	2.50	2.58	V
Input Bias Current	I_{BIAS}			-0.3	-2	μA
A_{VOL}		$2\leq V_o\leq 4\text{V}$	60	90		dB
Unity Gain Bandwidth		$T_j=25^{\circ}\text{C}$ (note 2)	0.7	1	6.0	mHz
PSRR		$12\leq V_{cc}\leq 25\text{V}$	60	70		dB
Output Sink Current	I_{sink}	$V_{pin 2}=2.7\text{V}$, $V_{pin 1}=1.1\text{V}$	2	6		mA

Output Source Current	I _{source}	V _{pin 2} =2.3V, V _{pin 1} =5V	-0.5	-0.8		mA
V _{out} High	V _{OH}	V _{pin 2} =2.3V, R _L =15k Ω to GND	5	6		V
V _{out} Low	V _{OL}	V _{pin 2} =2.7V, V _{pin 1} =1.1V		0.7	1.1	V
Current Sense Section						
Gain	G _v	(note 3, 4)	2.85	3	3.15	V/V
Maximum Input Signal	V _{I(MAX)}	V _{pin 1} =5V(note 3)	0.9	1	1.1	V
PSRR		12 \leq V _{cc} \leq 25V		70		dB
Input Bias Current	I _{BIAS}			-2	-10	μ A
Delay to Output		V _{pin 3} =0 to 2V		150	300	ns
Output Section						
Output Low Level	V _{OL}	I _{sink} =20mA		0.1	0.4	V
		I _{sink} =200mA		1.5	2.2	V
Output High Level	V _{OH}	I _{source} =20mA	13	13.5		V
		I _{source} =200mA	12	13.5		V
Rise Time	t _r	T _j =25 $^{\circ}$ C, C _L =1nF (note 2)		50	150	ns
Fall Time	t _f	T _j =25 $^{\circ}$ C, C _L =1nF(note 2)		50	150	ns
UVLO Saturation		V _{cc} =5V, I _{sink} =10mA		0.7	1.2	V
Under-Voltage Lockout Output Section						
Start Threshold	V _{TH(ST)}		7.8	8.4	9.0	V
Min. Operating Voltage After Turn On	V _{OPR(min)}		7.6	8.0	8.4	V
PWM Section						
Maximum Duty Cycle	D _(MAX)		95	07	100	%
Minimum Duty Cycle	D _(MIN)				0	%
Total Standby Current						
Start-up Current	I _{ST}			0.5	1	mA
Operating Supply Current	I _{CC(OPR)}	V _{pin 2} =V _{pin 3} =0V		11	17	mA
V _{cc} Zener Voltage	V _Z	I _{cc} =25mA		34		V

APPLICATION CIRCUIT



OUTLINE DRAWING

DIP-8

unit:mm

