DUAL OPERATIONNAL AMPLIFIER—YD4560

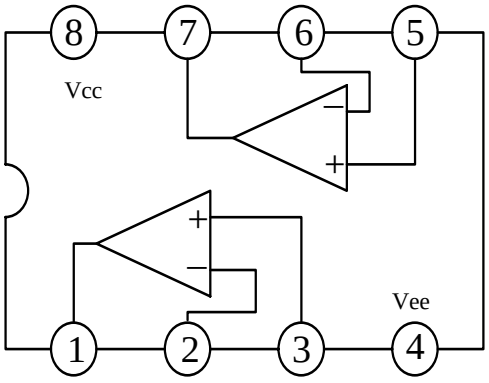
DESCRIPTION

The YD4560 is a monolithic integrated circuit designed for dual operational amplifier.

FEATURES

*Operating Voltage (±4V～±18V);
*NO frequency compensation required;
*Slew Rate (4V/μs typ);
*Internally frequency compensated
*Low noise input transistors(Vni=1.2μV)
*Package Outline DIP8,SOP8;
*Bipolar Technology。

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS(Tamb=25℃)

CHARACTERISTIC		SYMBOL	VALUE	UNIT
Supply Voltage		Vcc	±18	V
Differential input Voltage		V_{ID}	±30	V
Power Dissipation	DIP8	P_D	500	mW
	SOP8		300	
Input Voltage		V_I	±15	V
Operating Temperature		T_{OPR}	-20～+75	℃
Storage Temperature		T_{STG}	-40～+125	℃

ELECTRICAL CHARACTERISTICS

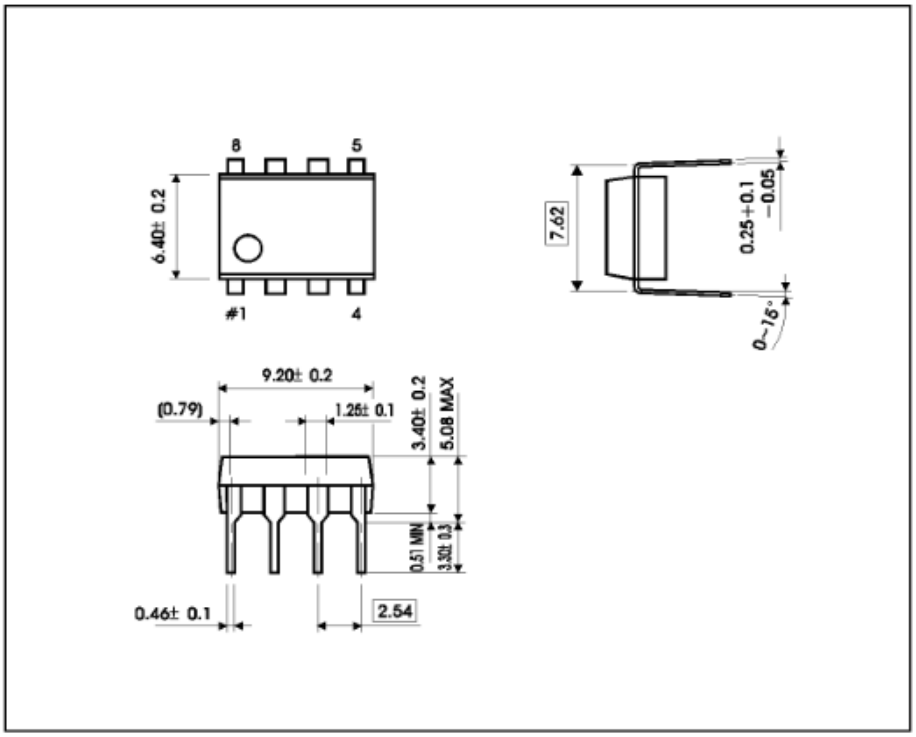
（Vcc=15V, Vee=-15V, Tamb=25℃, Unless otherwise specified）

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Supply Current	I_{CC}			4.3	5.7	mA
Input offset Voltage	V_{IO}	R_S＜10kΩ		0.5	6	mV
Input offset Current	I_{IO}			5	200	nA
Input bias current	I_B			40	500	nA
Input Resistance	R_{IN}		0.3	5		MΩ
Large signal voltage gain	A_V	Vo=±10V, R_L=2kΩ	86	100		dB
Common Mode Input Voltage Range	V_{ICM}		±12	±14		V
Maximum Output Voltage1	V_{OM1}	R_L≥2kΩ	±12	±14		V
Maximum Output Voltage1	V_{OM2}	Io=25mA	±10	±11.5		V
Common Mode Rejection Ratio	K_{CMR}		70	90		dB
Supply Voltage Rejection Ratio	K_{SVR}		76.5	90		dB
Gain Bandwidth Product	GB			10		MHz
Slew Rate	SR			4.0		V/μs
Equivalent Input Noise Voltage	V_{NI}	Rs=2kΩ，f=30Hz～30kHz		1.2		μVrms

OUTLINE DRAWING

DIP-8

unit:mm



SOP-8

unit:mm