



YDA145

D-4H

MONAURAL 2.1W Non-Clip DIGITAL AUDIO POWER AMPLIFIER

■ Overview

YDA145 (D-4H) is a digital audio power amplifier IC with maximum output of 2.1W ($R_L=4\Omega$) \times 1ch.

YDA145 has a "Pure Pulse Direct Speaker Drive Circuit" which directly drives speakers while reducing distortion of pulse output signal and reducing noise on the signal, and realizes the highest standard low distortion rate characteristics and low noise characteristics among digital amplifier ICs for mobile use.

In addition, circuit design with fewer external parts can be made depend on the condition of use because corresponds to filter less.

The YDA145 features Yamaha original non-clip output control function which detects output signal clip due to the over level input signal and suppress the output signal clip automatically. Also the non-clip output control function can adapt the output clip caused by power supply voltage down with battery. This is the difference from the traditional AGC (Auto Gain Control) or ALC (Auto Level Control) circuit.

YDA145 has the power-down function which can minimize the power consumption in the standby state.

As for protection function, overcurrent protection function for speaker output terminal, overtemperature protection function for inside of the device, and low supply voltage malfunction preventing function are prepared.

■ Features

- Maximum output
 - 2.1 W \times 1ch ($V_{DD}=5.0V$, $R_L=4\Omega$, THD+N=10%)
 - 0.75 W \times 1ch ($V_{DD}=3.6V$, $R_L=8\Omega$, THD+N=10%)
- Distortion Rate (THD+N)
 - 0.03 % ($V_{DD}=3.6V$, $R_L=8\Omega$, $P_o=0.4W$, 1kHz)
- Residual Noise
 - 45 μ Vrms ($V_{DD}=3.6V$, $A_v=18dB$)
- Efficiency
 - 84 % ($V_{DD}=3.6V$, $R_L=8\Omega$, $P_o=600mW$)
 - 78 % ($V_{DD}=3.6V$, $R_L=8\Omega$, $P_o=100mW$)
- S/N Ratio
 - 94dB ($V_{DD}=3.6V$, $A_v=18dB$)
- Over-current Protection function
- Thermal Protection function
- Low voltage Malfunction Prevention function
- Pop noise reduction function
- Power-down control function
- Power-down High speed Recovery function
- Package
 - Lead-free 9-ball WLCSP (YDA145-PZ)

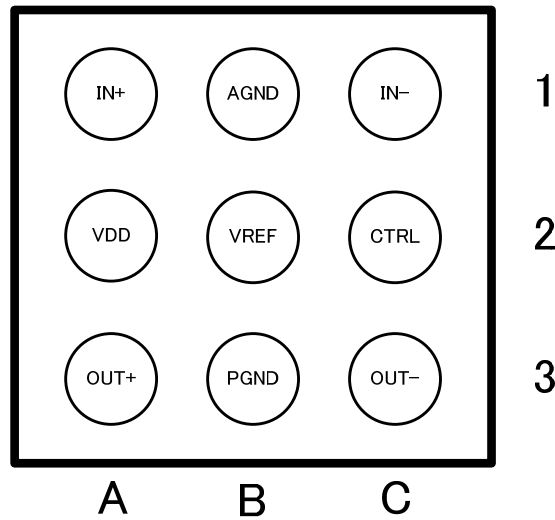
YAMAHA CORPORATION

YDA145 CATALOG

CATALOG No.:LSI-4DA145A30

2007.10

■ Terminal configuration



<9-ball WLCSP Bottom View>

■ Terminal function

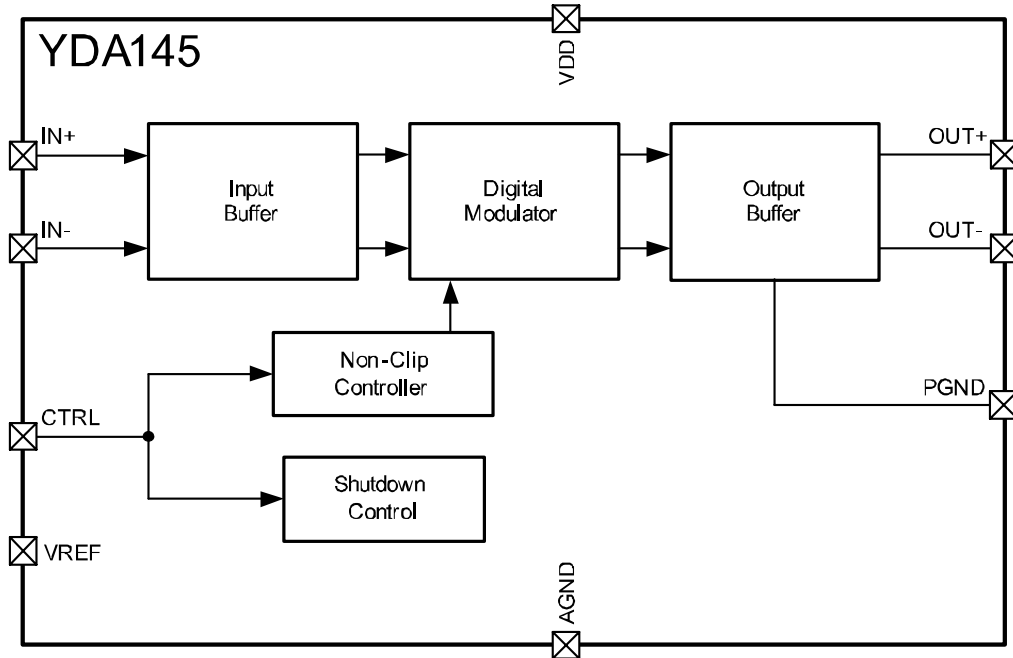
No.	Name	I/O	Protection circuit composition	Function
A1	IN+	A	PN	Positive input terminal (differential +)
A2	VDD	Power	-	Power supply
A3	OUT+	O	-	Positive output terminal (differential +)
B1	AGND	GND	-	GND for analog circuits
B2	VREF	A	PN	Analog reference power supply terminal
B3	PGND	GND	-	GND for output
C1	IN-	A	PN	Negative input terminal (differential -)
C2	CTRL	I	N	Power down and Non-clip control terminal
C3	OUT-	O	-	Negative output terminal (differential -)

(Note) I: Input terminal O: Output terminal A: Analog terminal

When a voltage that is bigger than the AVDD potential is impressed to the terminal of PN (protection circuit is composed of PMOS and NMOS), the leakage current flows through the protection circuit of PMOS.

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■Block diagram



■ Description of operating functions

● Digital Amplifier Function

YDA145 has digital amplifiers with analog input, PWM pulse output, and maximum output of $2.1W(R_L=4\Omega)\times 1ch$.

Distortion of PWM pulse output signal and noise of the signal is reduced by adopting “Pure Pulse Direct Speaker Drive Circuit”.

In addition, YDA145 has been designed so that high-efficiency can be maintained within an average power range (100mW or so) that is used for mobile terminal.

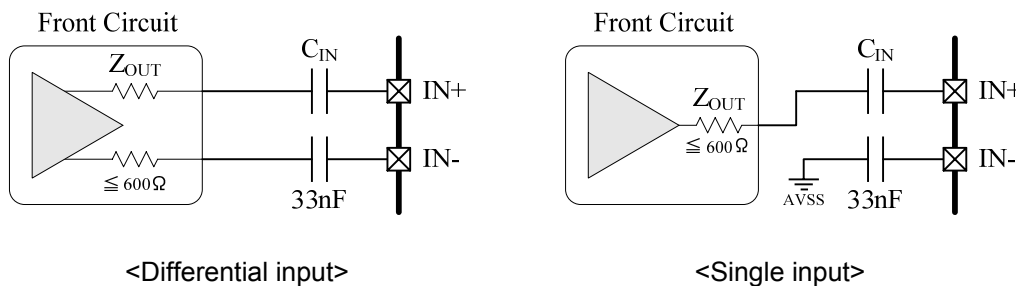
Analog signal input

For a differential input, input signals to IN+ and IN- pins via DC-cut capacitors (C_{IN}).

The input signal gain is $+18dB^{*1)}$. And, with an input impedance of $28.5k\Omega$ (typ.), a lower cut-off frequency of an input signal becomes 169Hz at $C_{IN}=33nF$.

For a single-ended input, input a signal to IN+ via a DC-cut capacitor (C_{IN}). At this time, IN- pin should be connected to AVSS via a DC-cut capacitor (C_{IN}) with the same capacitance. Gain and a lower Cut-off frequency are the same as the above case.

In addition, the output impedance (Z_{out}) of the former source circuit, including signal paths up to INL+ terminal and IN- terminal should be designed to become 600Ω or lower^{*1)}.



Use a capacitance of $0.1\mu F$ or less as a DC-cut capacitor (C_{IN}) to reduce pop noise.

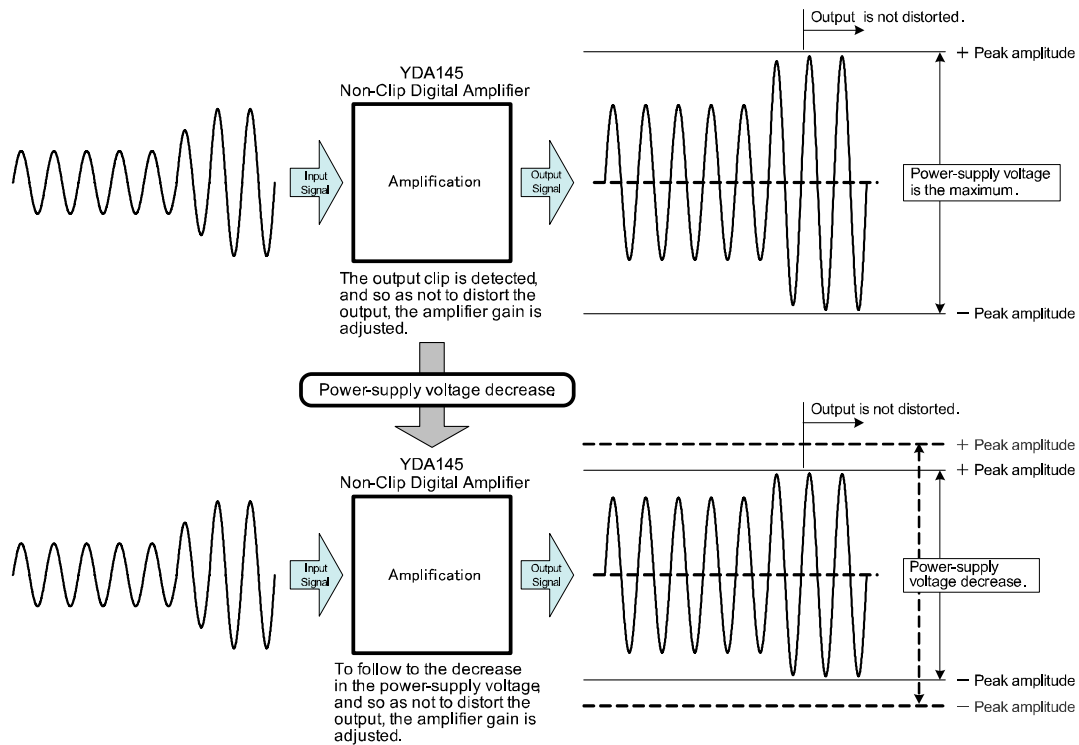
*1)

By limiting supply voltage V_{DD} , operating ambient temperature T_a , DC-cut capacitor C_{IN} , and power-down setting time T_{PD} , gain can be set by the control of the input resistance. For details, please contact us.

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● Non-Clip control Function

This is the function to control the output in order to obtain a maximum output level without distortion when an excessive input which causes clipping at the differential signal output is applied. That is, with the Non-Clip function, YDA145 lowers the Gain of the digital amplifier to an appropriate value so as not to cause the clipping at the differential signal output. And, YDA145 follows also to the clip of the output wave form due to the decrease in the power-supply voltage.



<Operation outline of Non-Clip control function>

The attack time and the release time of Non-Clip control are fixation two levels, and selects with the CTRL terminal. The Attack time is a time interval until gain falls to target attenuation gain -3dB with a big signal input enough. And, the Release Time is a time from target attenuation gain to not working of Non-Clip.

Attack time and Release time

Non-Clip mode	Attack time	Release time
1(Recommendation)	45ms	2.6s
2	10ms	1.2s

● Protection Function

YDA145 has the following protection functions for the digital amplifier: Over-current Protection function, Thermal Protection function, and Low voltage Malfunction Prevention function.

Over-current Protection function

This is the function to establish the over-current protection mode when detecting a short circuit between YDA145 differential output terminal and VSS, VDD, or another differential output. In the over current protection mode, the differential output terminal becomes a high impedance state.

The over current protection mode can be cancelled by power down or turning on the power again.

Thermal Protection function

This is the function to establish the thermal protection mode when detecting excessive high temperature of YDA145 itself. In the thermal protection mode, the differential output terminal becomes Weak Low state (a state grounded through high resistivity). And, when YDA145 gets out of such condition, the protection mode is cancelled.

Low voltage Malfunction Prevention function

This is the function to establish the low voltage protection mode when VDD terminal voltage becomes lower than the detection voltage (V_{UVLL}) for the low voltage malfunction prevention and to cancel the protection mode when VDD terminal voltage becomes higher than the threshold voltage (V_{UVLH}) and by return procedure from power down for its deactivation.

(In sag state, this function works, and YDA145 becomes a low voltage protection mode.)

In the low voltage protection mode, the differential output pin becomes Weak Low state (a state grounded through high resistivity). YDA145 will start up within the start-up time (T_{STUP}) when the low voltage protection mode is cancelled.

● Control Function

VREF terminal output

The voltage of $VDD/2$ is output from the VREF terminal. Capacitor ($1\mu F$) is connected between the VREF terminal and GND for stabilization.

Power down and Initialization function

When CTRL terminal is connected to GND potential, the IC goes to the power-down mode. In the mode, all the circuit functions stop and its current consumption becomes the lowest. And, the output terminals become Weak Low (A high resistance grounded state).

When in the power-down mode, the level of the terminal must not be changed from GND level during t_{PD} .

On the contrary, when CTRL terminal is set to H level, the power-down mode is canceled and the IC starts up after startup time (t_{STUP}).

Caution:

Please start up the former source circuit first to stabilize the DC bias point (See Figure1-②) and then cancel the power-down state of YDA145. The time (T_{DLY}) required to stabilize the voltage can be found by the formula (See (1) shown below). And, signal variation in the former source circuit should be a value lower than PVDD.

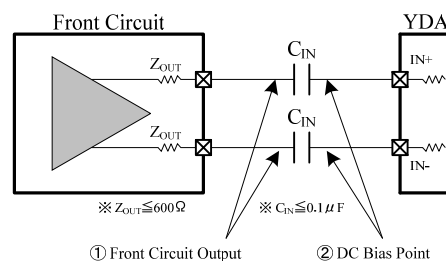


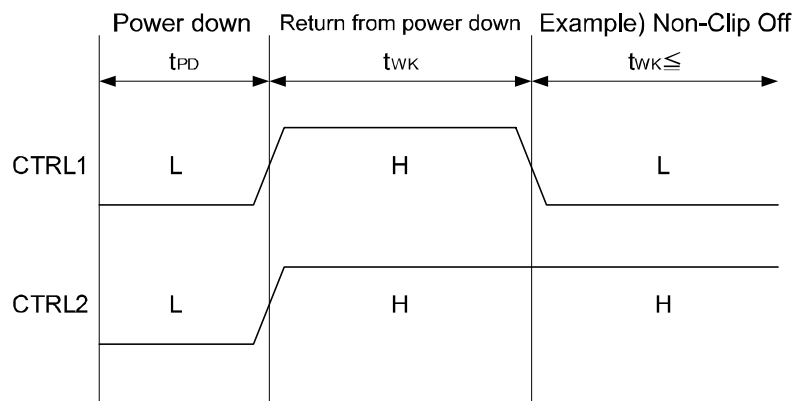
Figure 1 Circuit Diagram

$$T_{DLY} \geq C_{IN} \times 330 \times 10^3 \times 3 \quad \dots (1)$$

Example) $T_{DLY} \geq 33$ [msec] ($C_{IN} = 0.033$ [μF])

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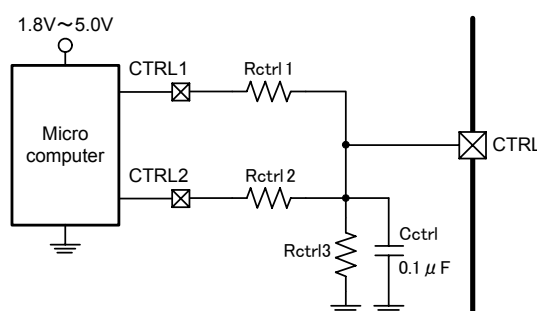
In order to return from the power-down mode a desired mode needs to be set after setting both CTRL1 and CTRL2 to H level during t_{WK} . In addition, at startup, cancel the power-down mode after supply voltages has been sufficiently stabilized.



CTRL terminal function

By connection external resistors (R_{ctrl1} , R_{ctrl2} , and R_{ctrl3} : Accuracy of 1%) to CTRL terminal, and impression setting threshold voltage of each mode to CTRL terminal, the followings can be set: Non-Clip1, Non-Clip2, Non-Clip OFF, and power-down mode. **When turning on the supply voltage or cancelling the power-down mode, control the CTRL terminal according to procedure for cancelling power-down (See Page 6).** A pulse shorter than t_{PD} must not be input.

Connect the terminal to the ground through a capacitor C_{ctrl} (a ceramic capacitor of $0.1\mu F$ or more).



CTRL1	CTRL2	Function
H	H	Non-Clip 1 mode
H	GND	Non-Clip 2 mode
GND	H	Non-Clip Off mode
GND	GND	Power-down mode

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“H” level indicates a microcomputer’s I/O port H level output voltage that is input to CTRL1 and CTRL2 terminals and GND indicates GND of the microcomputer.

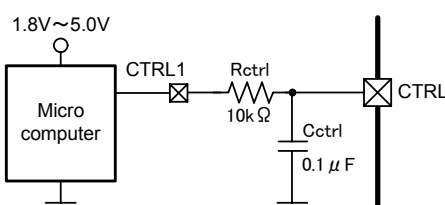
GND level of the microcomputer must be the same as that of YDA145.

The control of CTRL terminal is based on I/O port H level output voltage of microcomputer that is connected. Set resistance constants according to I/O port H level output voltage of each microcomputer as shown below.

I/O port H level output voltage of microcomputer	1.8V	2.6V	3.0V	3.3V	5.0V
R_{ctrl1}	27k Ω	33k Ω	33k Ω	33k Ω	56k Ω
R_{ctrl2}	56k Ω	68k Ω	68k Ω	68k Ω	120k Ω
R_{ctrl3}	82k Ω	27k Ω	22k Ω	18k Ω	15k Ω

Functions of CTRL pin are designed with their control by two control pins (CTRL1 and CTRL2).

Only a switching control between Non-Clip1 mode and Power-down mode is available when a single control terminal is used. A setting voltage should be set according to V_{MOD1} and V_{MOD4} , and use a RC filter with time constant of 1msec or more in order to eliminate noise at transmission side such as Micon etc. (Example. $R_{ctrl1}=10k\Omega$ and $C_{ctrl}=0.1\mu F$).



CTRL1	Function
H	Non-Clip 1 mode
GND	Power-down mode

● Pop noise reduction function

The Pop Noise Reduction Function works in the cases of Power-on, Power-off, Power-down on, and Power-down off. And, the pop-noise can be suppressed according to control the power down by the following procedure.

- Power down mode is cancelled after power-on and the power supply is stabilized enough.
- Power down mode is set before Power-off.

● Snubber Circuit and schottky barrier diode

It is necessary to connect the snubber circuit and schottky barrier diode with the output terminal to prevent IC destruction by the output short-circuit when using it on the following conditions. The constant and the circuit are as follows.

Power supply voltage range	Load conditions	Snubber Circuit	Schottky barrier diode
$2.7V \leq VDD \leq 4.5V$	Wiring inductance $> 4\mu H$	Between OUT+ and OUT- $R_s=1.5\Omega$, $C_s=330pF$	Need less
$4.5V < VDD \leq 5.25V$	—	Between OUT+ and OUT- $R_s=1.5\Omega$, $C_s=680pF$	Between OUT* and VDD

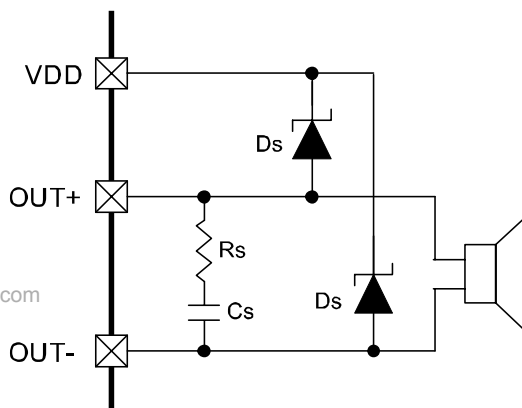
Wiring inductance and wiring length: about $1\mu H/1m$

Recommended parts

Schottky barrier diode: ROHM, RB161VA-20(or ROHM RB550VA-30)

Forward current surge peak = 5A or more, Average forward current = 1A or more,

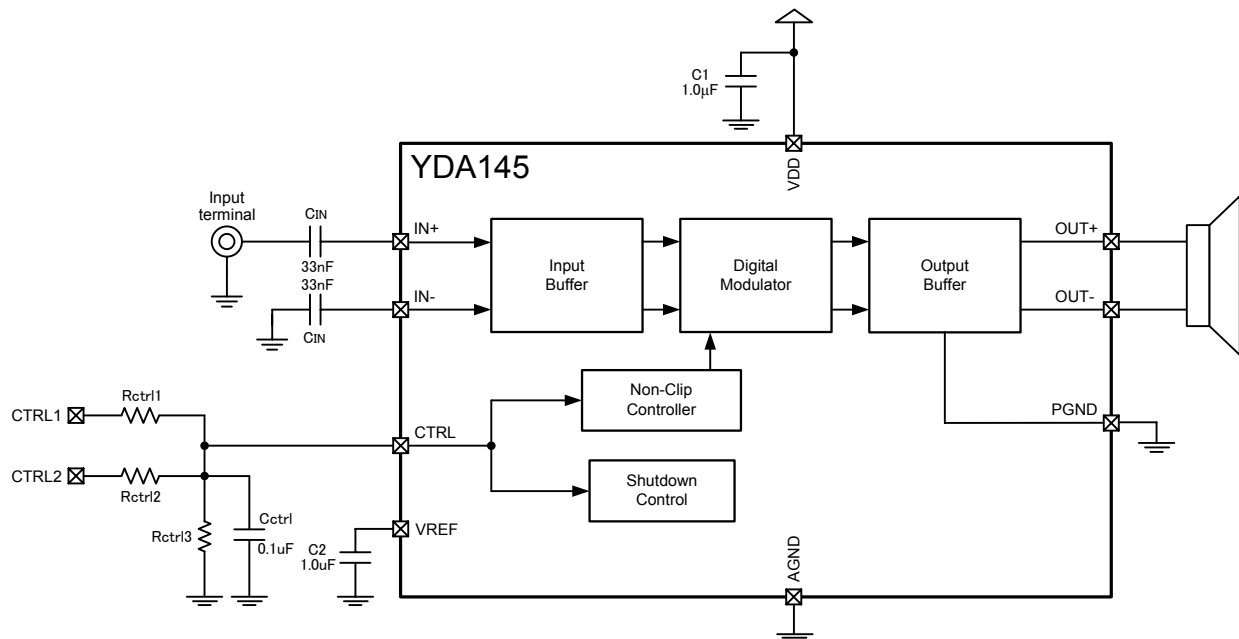
Forward voltage ($I_F=1A$) = 0.38V or less



<Snubber circuit and Schottky barrier diode>

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■ Application circuit examples



Use a capacitance of 0.1 μ F or less (e.g. 33nF), $\pm 10\%$ as a DC-cut capacitor (C_{IN}) to reduce pop noise.

Explanation of the capacitance (C1) between VDD and GND:

Use the capacitor (1 μ F or more) with low enough ESR (Equivalent Series Resistance).

When it is used at $R_L=4\Omega$ or a supply voltage of more than 4.5V, another capacitor (10 μ F or more) with low enough ESR (Equivalent Series Resistance) should be added to use. In addition, place the capacitor as close as possible within 3mm from the IC.

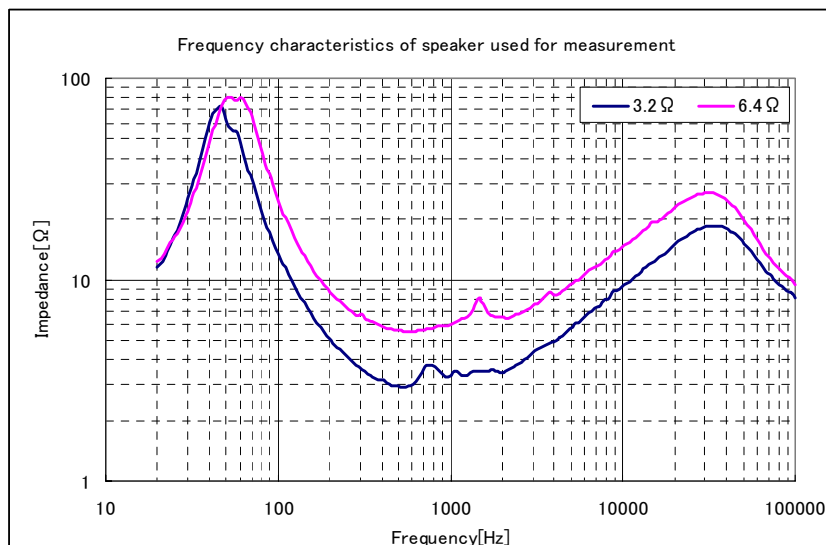
■ Cautions for Safety

Please observe the following restrictions to use YDA145 safely and obtain an enough analog characteristic.

- The snubber circuit should be laid out within 3mm from the IC on the component side.
- The schottky barrier diode and bypass capacitor which is connected between VDD and GND should be laid out within 3mm from the IC.
- Bypass capacitor which is connected between PVDD and GND:
 - Use the capacitor (1 μ F or more) with enough low ESR (Equivalent Series Resistance).
 - When it is used at less than 8 Ω or a supply voltage of more than 4.5V, another capacitor (10 μ F or more) with low enough ESR (Equivalent Series Resistance) should be added to use. In addition, place the capacitor as close as possible within 3mm from the IC.
- When a LC filter is used, consider the following.

With a system of which an input signal in excess of a resonance frequency of a LC filter could be input, be sure to place a snubber circuit (insert 15 Ω +470nF at the LC filter output) after the LC filter to prevent an over-current condition. The purpose is to prevent an over-current from flowing because an impedance of the speaker increases at the resonance frequency.

(The inserted snubber circuit constant might be different according to the impedance frequency characteristics of the speaker. The snubber circuit constant of the description is confirmed with the speaker of the following characteristic. Therefore, when the speaker of frequency characteristics different from the following is used, an enough evaluation is necessary.)



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- With a system of which a voltage at an input pin might exceed a supply voltage of V_{DD}/GND , use an external diode etc. to assure that the voltage does not exceed the absolute maximum rating.

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■Electrical Characteristic

●Absolute Maximum Ratings^{*1)}

Item	Symbol	Min.	Max.	Unit
Power supply terminal voltage range	V_{DD}	-0.3	6.0	V
Input terminal voltage range (Analog input terminal: IN+, IN-)	V_{IN}	$V_{SS}-0.6$	$V_{DD}+0.6$	V
Input terminal voltage range (Input terminals except IN+, IN-)	V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
Allowable dissipation ($T_a=25^{\circ}\text{C}$) ^{*2)}	P_{D25}		1.67	W
Allowable dissipation ($T_a=85^{\circ}\text{C}$) ^{*2)}	P_{D85}		0.67	W
Junction Temperature	T_{JMAX}		125	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-50	125	$^{\circ}\text{C}$

Note) *1: Absolute Maximum Ratings is values which must not be exceeded to guarantee device reliability and life, and when using a device in excess even a moment, it may immediately cause damage to device or may significantly deteriorate its reliability
 With a system of which a voltage at an input pin might exceed a supply voltage of V_{DD}/GND , use an external diode etc. to assure that the voltage does not exceed the absolute maximum rating.

*2: $\theta_{ja}=60.0^{\circ}\text{C}/\text{W}$, Conditions: YDA145 Evaluation board (4 layers), dead calm

●Recommended Operating Condition

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}		2.7	3.6	5.25	V
Operating Ambient Temperature	T_a	$t_{PD}(\text{Min.})=50\text{ms}$	-20	25	85	$^{\circ}\text{C}$
		$t_{PD}(\text{Min.})=80\text{ms}$	-30			
Speaker Impedance	R_L		4			Ω

Note) Do not use under a condition other than the recommended operating conditions.

The rising time of V_{DD} should be more than $1\mu\text{s}$.

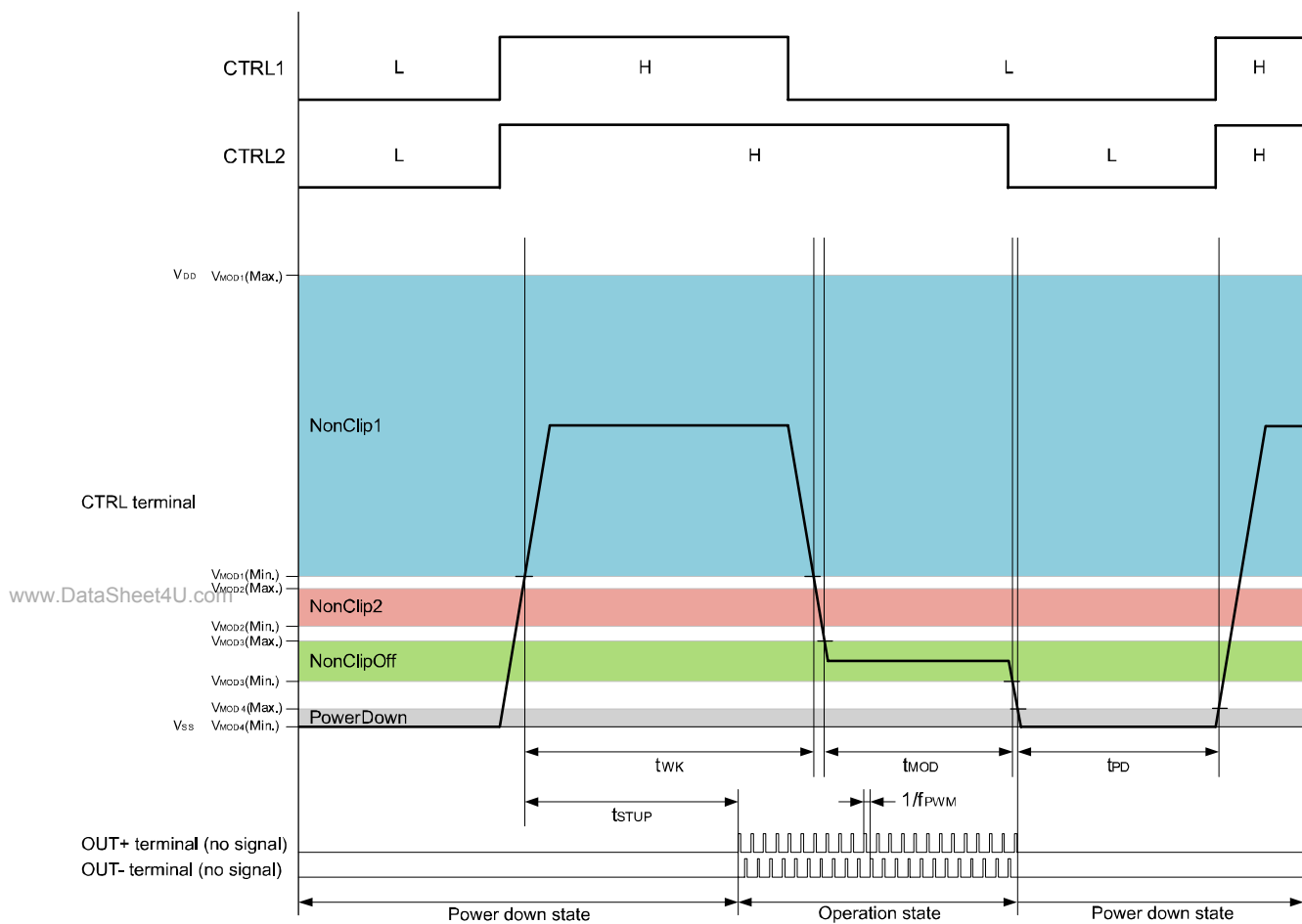
Please note not falling below than the power supply shut-down threshold voltage.

●DC Characteristics ($V_{SS}=0\text{V}$, $V_{DD}=2.7\text{V}$ to 5.25V , $T_a=-30^{\circ}\text{C}$ to 85°C , unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply start-up threshold voltage	V_{UVLH}			2.2		V
Power supply shut-down threshold voltage	V_{UVLL}			2.0		V
Non-Clip 1 mode setting threshold voltage	V_{MOD1}		1.20		V_{DD}	V
Non-Clip 2 mode setting threshold voltage	V_{MOD2}		0.80		1.10	V
Non-Clip Off mode setting threshold voltage	V_{MOD3}		0.36		0.68	V
Power-down mode setting threshold voltage	V_{MOD4}		V_{SS}		0.14	V
Consumption current	I_{DD}	$V_{DD}=3.6\text{V}$, no load, no signal input		4.0		mA
Consumption current in power-down mode	I_{PD}	$\text{CTRL}=V_{SS}$, $T_a=25^{\circ}\text{C}$		0.1		μA
VREF voltage	V_{REF}			$V_{DD}/2$		V

● AC characteristics ($V_{SS}=0V$, $V_{DD}=2.7V$ to $5.25V$, $T_a=-30^{\circ}C$ to $85^{\circ}C$, unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Start-up time (Power-down release)	t_{STUP}			3.5		ms
Input cut-off frequency	f_C	$C_{IN}=33nF$, $A_v=18dB$		169		Hz
Attack time 1	t_{AT1}	$V_{DD}=3.6V$, $g=10dB$		45		ms
Release time 1	t_{RL1}	$V_{DD}=3.6V$, $g=10dB$		2.6		s
Attack time 2	t_{AT2}	$V_{DD}=3.6V$, $g=10dB$		10		ms
Release time 2	t_{RL2}	$V_{DD}=3.6V$, $g=10dB$		1.2		s
Wake-up mode setting time	t_{WK}		6			ms
Power down setting time	t_{PD}	$T_a(\text{Min.})=-20^{\circ}C$	50			ms
		$T_a(\text{Min.})=-30^{\circ}C$	80			
Each mode setting time (Except power down)	t_{MOD}		0.1			ms
Carrier clock frequency	f_{PWM}			1.0		MHz



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● Analog Characteristics

($V_{SS}=0V$, $V_{DD}=3.6V$, $A_v=18dB$, $T_a=25^\circ C$, $C_{IN}=33nF$, Non-Clip Off, no snubber circuit, no schottky barrier diode, unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Maximum output	P_O	$R_L=4\Omega$, $V_{DD}=5V$		2.1		W
		$R_L=8\Omega$		0.75		W
Total Harmonic Distortion Rate (BW:20kHz)	THD+N	$R_L=4\Omega$, $P_O=0.65W$, $f=1kHz$		0.03		%
		$R_L=8\Omega$, $P_O=0.4W$, $f=1kHz$		0.03		%
Residual Noise (BW:20kHz A-Filter)	N	$A_v=18dB$		45		μV_{rms}
Signal /Noise Ratio (BW:20kHz A-Filter)	SNR	$A_v=18dB$		94		dB
Power supply rejection ratio	PSRR	217Hz		-75		dB
Maximum Efficiency	η	$R_L=8\Omega$, $P_O=0.6W$		84		%
		$R_L=8\Omega$, $P_O=0.1W$		78		%
Output offset voltage	V_o			± 20		mV
Frequency characteristics	f_{RES}	$C_{IN}=0.1\mu F$, $f=100Hz$ to 20kHz	-3	-	1	dB
Non-Clip maximum attenuation gain	Aa			-10		dB

Note) All the values of analog characteristics were obtained by using our evaluation circumstance.

Depending upon parts and pattern layout to use, characteristics may be changed.

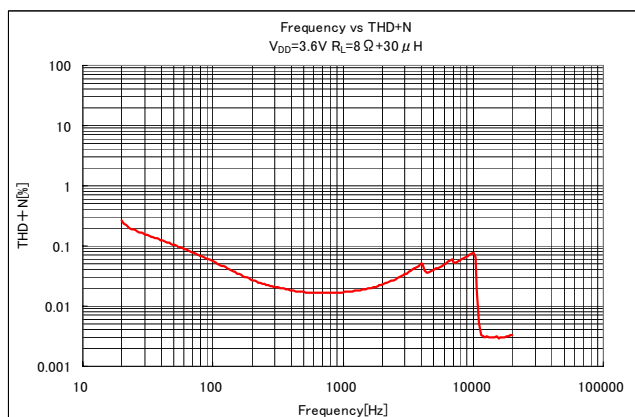
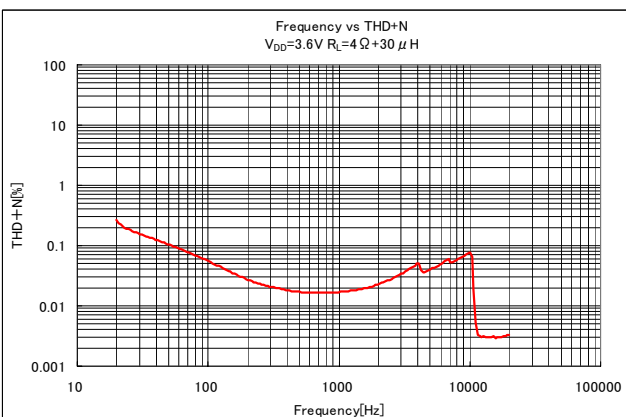
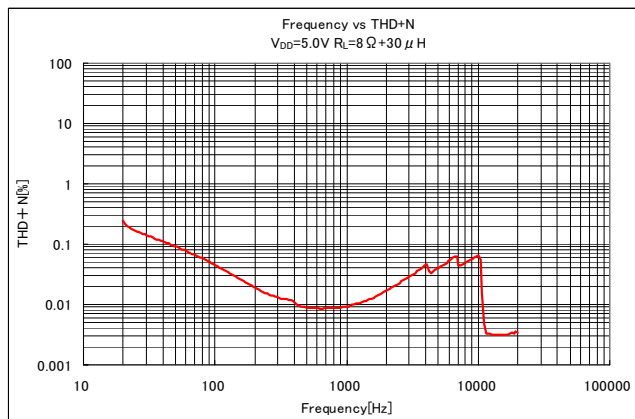
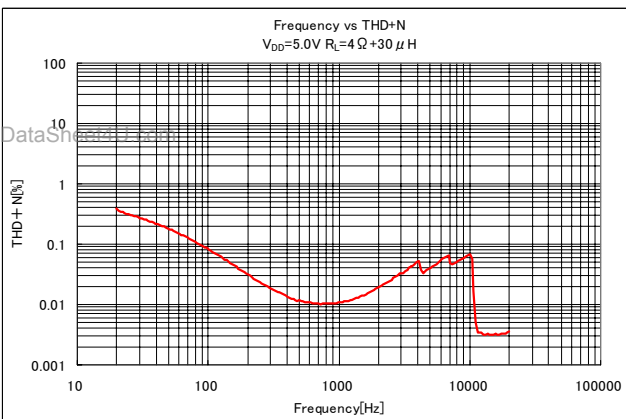
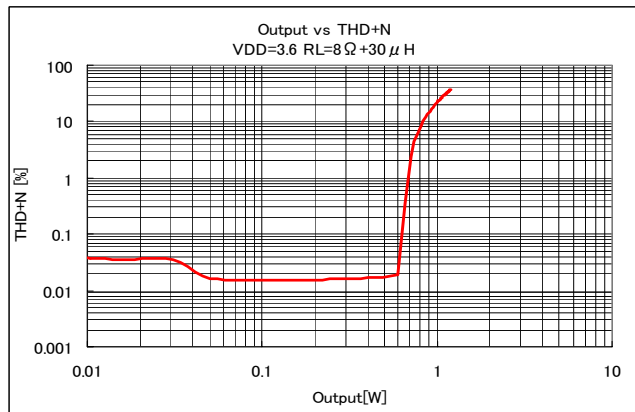
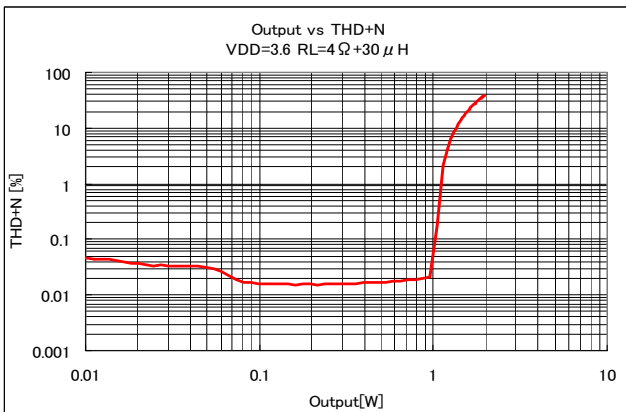
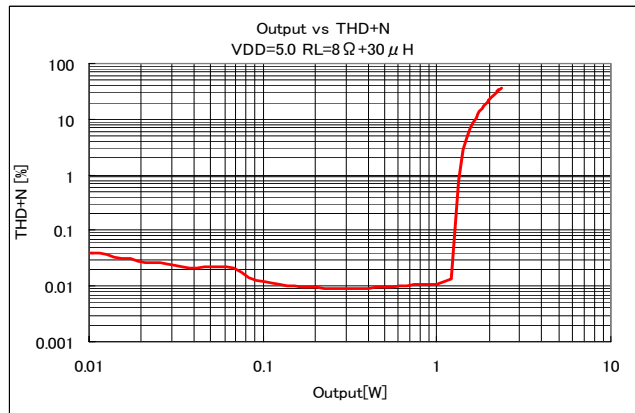
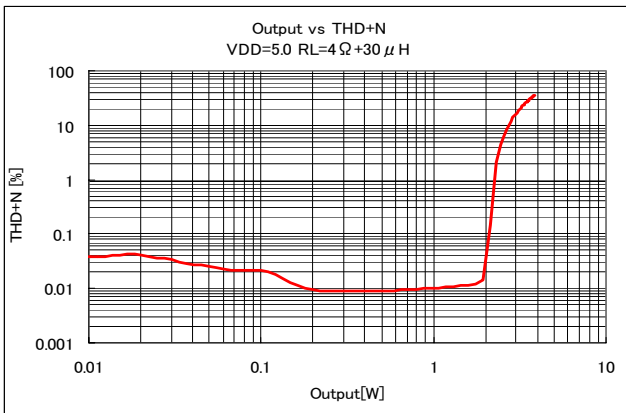
8 Ω or 4 Ω resistor and 30 μH coil are used as an output load in order to obtain various digital amplifier characteristics.

● Typical characteristics examples

$V_{DD}=5V$: Gain=18dB, Snubber circuit and schottky barrier diode are added.

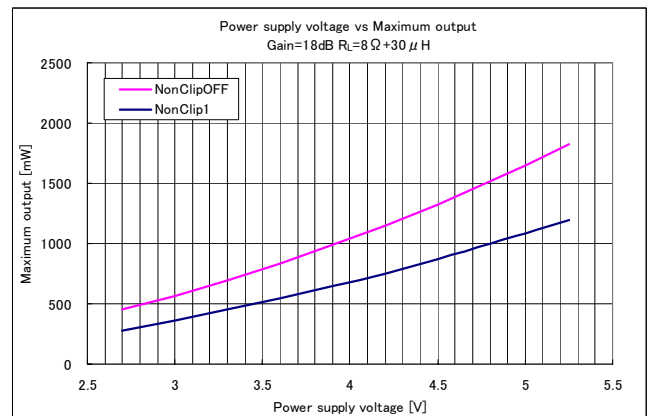
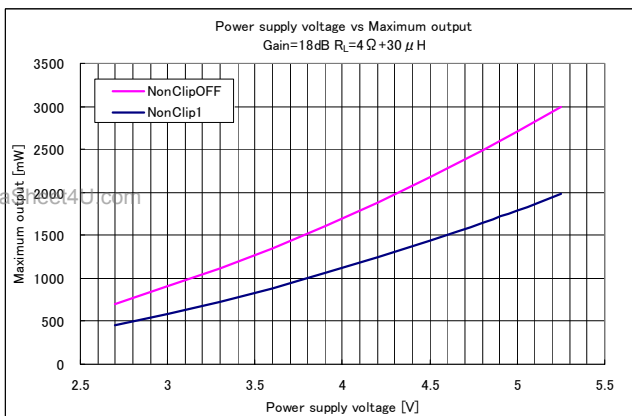
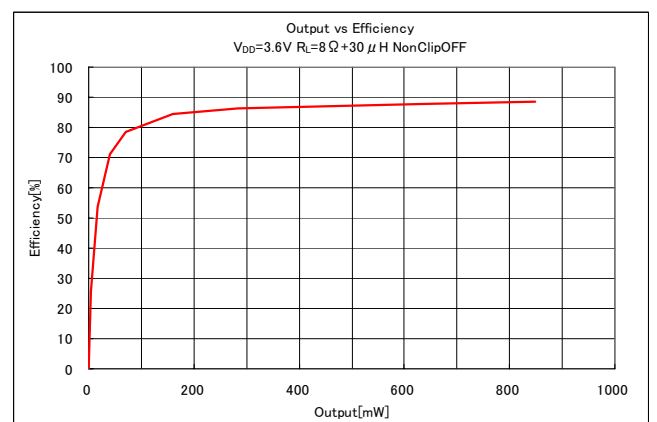
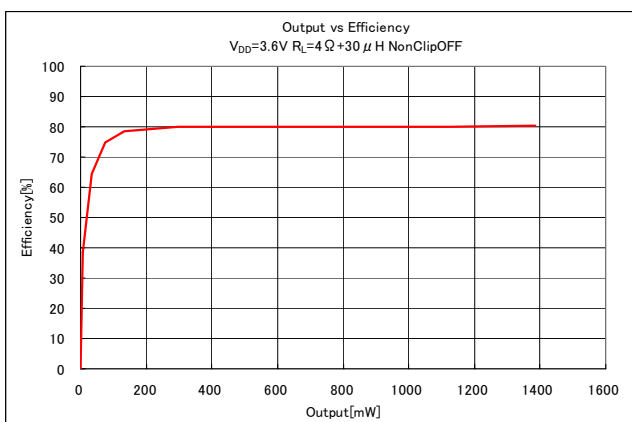
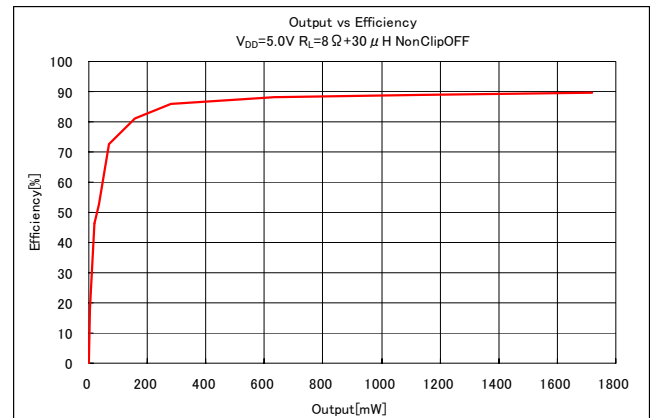
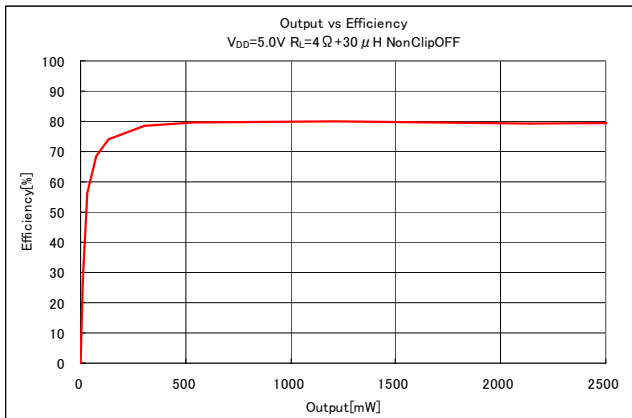
$V_{DD}=3.6V$: Gain=18dB, no Snubber circuit, no schottky barrier diode.

($V_{SS}=0V$, $T_a=25^{\circ}C$, Non-Clip Off, $C_{IN}=33nF$, unless otherwise specified)



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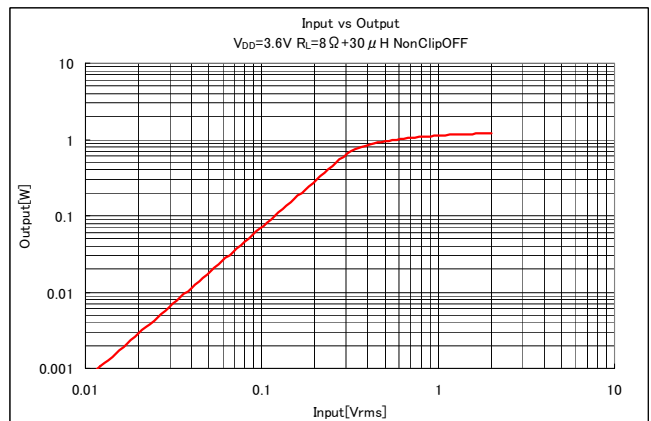
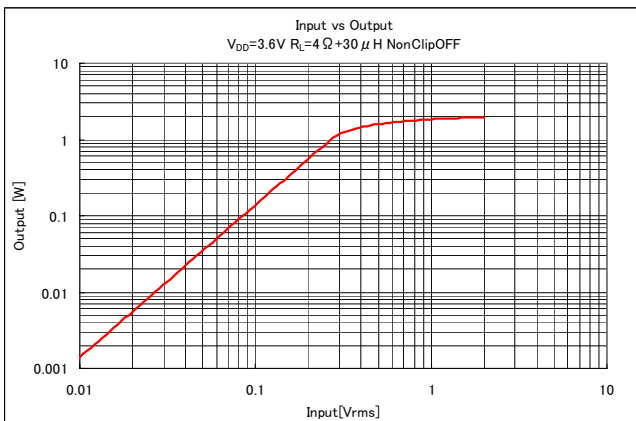
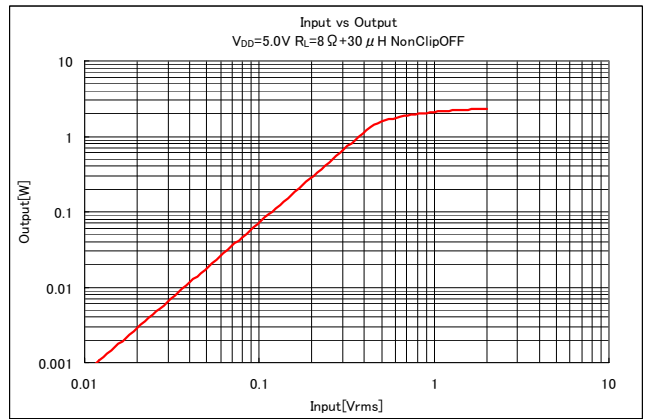
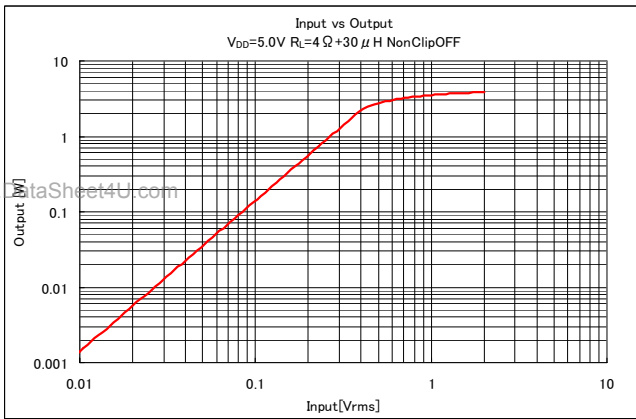
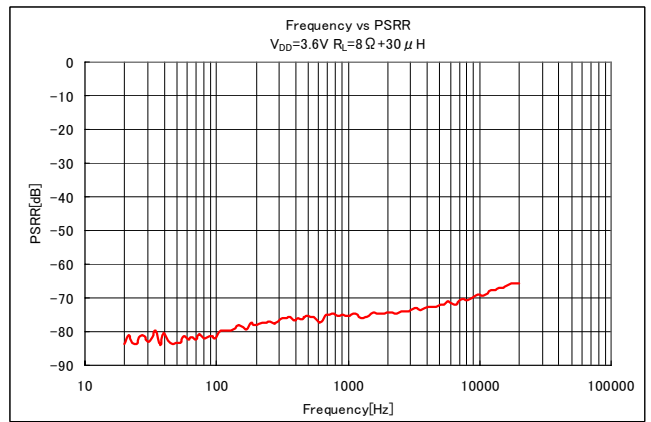
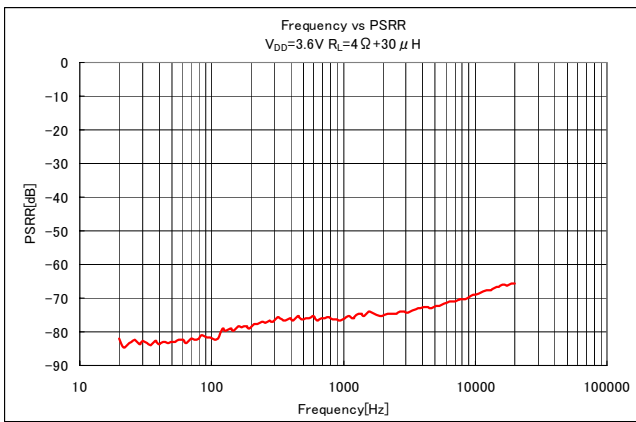
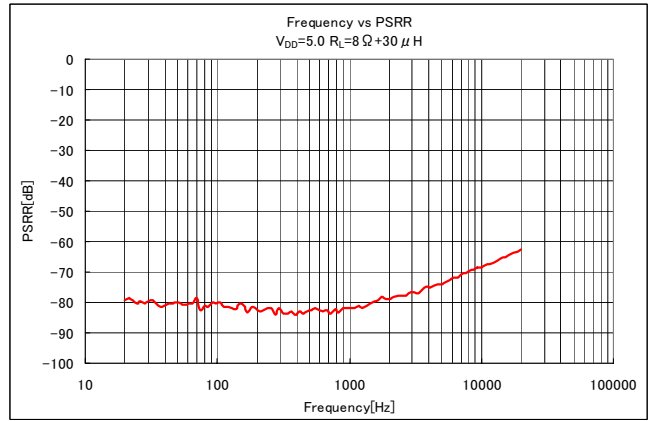
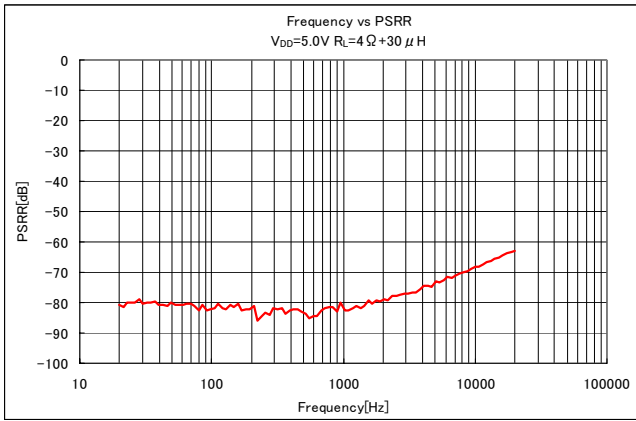
Note) The definition of the maximum output is different in “NonClipOFF” and “NonClip1”.

NonClipOFF: Output when THD+N=10%.

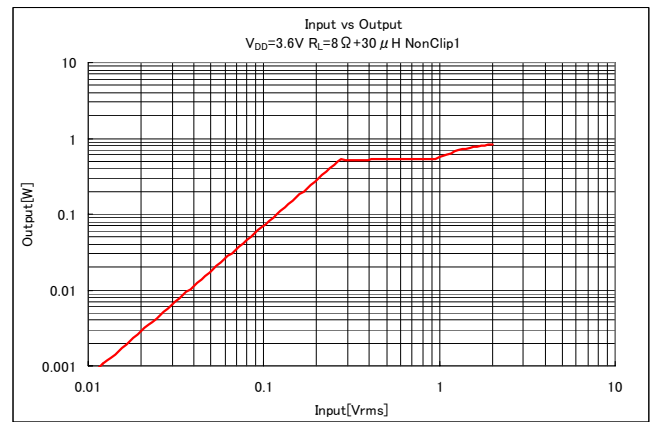
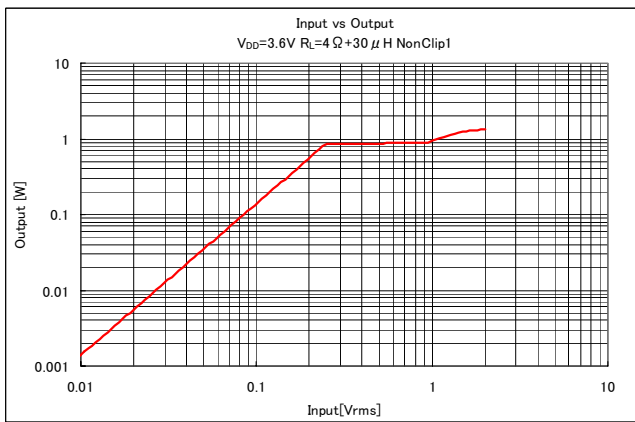
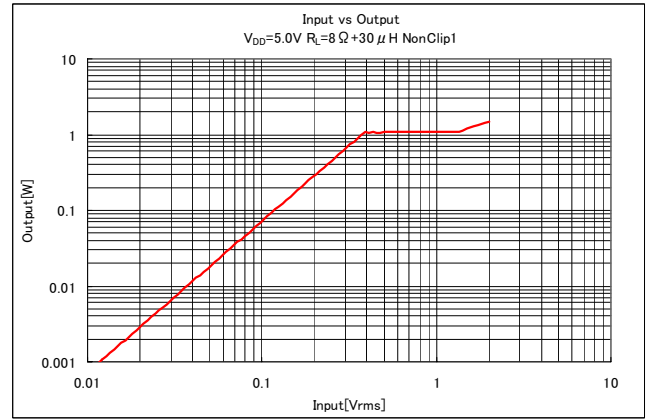
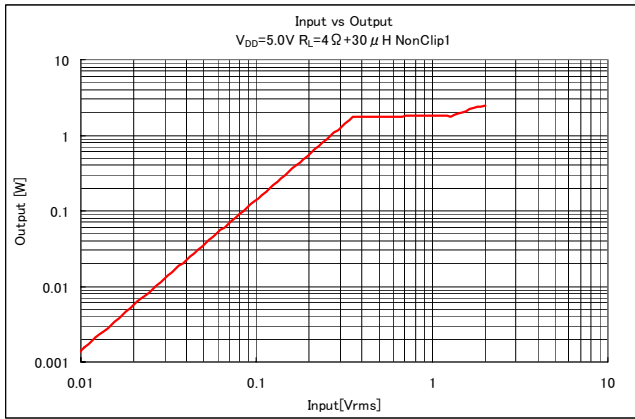
NonClip1: Output when "NonClip" functions.



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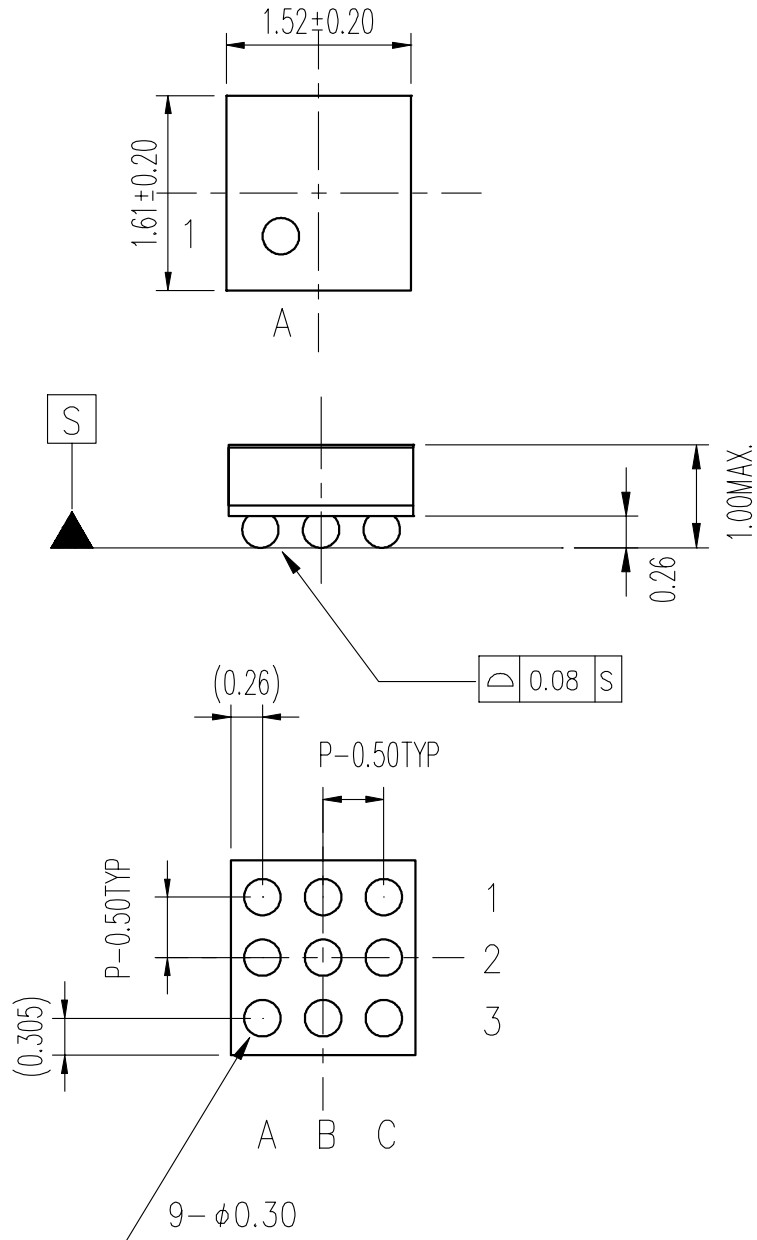


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■ Package Outline

C-PK9PP1-2



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カッコ内の寸法値は参考値です。
外形寸法はバリを含みます。
単位：mm

The figure in the parentheses () should be used as a reference.
The dimensions include burr.
UNIT: mm

注) 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせください。

Note: The storage and soldering of LSIs for surface mounting need special consideration.
For detailed information, please contact your local Yamaha agent.



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MEMO

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The specifications of this product are subject to improvement changes without prior notice.

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