PRELIMINARY

YDA176

Application Manual

D-507DL DIGITAL INPUT STEREO 15W DIGITAL AUDIO POWER AMPLIFIER

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YAMAHA CORPORATION

YDA176 APPLICATION MANUAL
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	WARNING
Prohibited	Do not use the device under stresses beyond those listed in Absolute Maximum Ratings. Such stresses may become causes of breakdown, damages, or deterioration, causing explosion or ignition, and this may lead to fire or personal injury.
Prohibited	Do not mount the device reversely or improperly and also do not connect a supply voltage in wrong polarity. Otherwise, this may cause current and/or power-consumption to exceed the absolute maximum ratings, causing personal injury due to explosion or ignition as well as causing breakdown, damages, or deterioration. And, do not use the device again that has been improperly mounted and powered once.
Prohibited	Do not short between pins. In particular, when different power supply pins, such as between high-voltage and low-voltage pins, are shorted, smoke, fire, or explosion may take place.
Instructions	As to devices capable of generating sound from its speaker outputs, please design with safety of your products and system in mind, such as the consequences of unusual speaker output due to a malfunction or failure. A speaker dissipates heat in a voice-coil by air flow accompanying vibration of a diaphragm. When a DC signal (several Hz or less) is input due to device failure, heat dissipation characteristics degrade rapidly, thereby leading to voice-coil burnout, smoking or ignition of the speaker even if it is used within the rated input value.

	CAUTION
Prohibited	Do not use Yamaha products in close proximity to burning materials, combustible substances, or inflammable materials, in order to prevent the spread of the fire caused by Yamaha products, and to prevent the smoke or fire of Yamaha products due to peripheral components.
Instructions	Generally, semiconductor products may malfunction and break down due to aging, degradation, etc. It is the responsibility of the designer to take actions such as safety design of products and the entire system and also fail-safe design according to applications, so as not to cause property damage and/or bodily injury due to malfunction and/or failure of semiconductor products.
Instructions	The built-in DSP may output the maximum amplitude waveform suddenly due to malfunction from disturbances etc. and this may cause damage to headphones, external amplifiers, and human body (the ear). Please pay attention to safety measures for device malfunction and failure both in product and system design.
Instructions	As semiconductor devices are not nonflammable, overcurrent or failure may cause smoke or fire. Therefore, products should be designed with safety in mind such as using overcurrent protection circuits to control the amount of current during operation and to shut off on failure.
Instructions	Products should be designed with fail safe in mind in case of malfunction of the built-in protection circuits. Note that the built-in protection circuits such as overcurrent protection circuit and high-temperature protection circuit do not always protect the internal circuits. In some cases, depending on usage or situations, such protection circuit may not work properly or the device itself may break down before the protection circuit kicks in.
Instructions	Use a robust power supply. The use of an unrobust power supply may lead to malfunctions of the protection circuit, causing device breakdown, personal injury due to explosion, or smoke or fire.
Instructions	Product's housing should be designed with the considerations of short-circuiting between pins of the mounted device due to foreign conductive substances (such as metal pins etc.). Moreover, the housing should be designed with spatter prevention etc. due to explosion or burning. Otherwise, the spattered substance may cause bodily injury.
Instructions	The device may be heated to a high temperature due to internal heat generation during operation. Therefore, please take care not to touch an operating device directly.

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1. Overview

YDA176(D-507DL) is a high-performance digital audio amplifier IC that delivers up to 15W×2ch, which has a digital audio interface, and is capable of operating at a supply voltage ranging from 5V[*1)] to 18V. YDA176, with Yamaha original "Pure Pulse Direct Speaker Drive Circuit," allows a speaker to be directly connected to the output. In addition, this amplifier is insusceptible to supply voltage fluctuation because of a feedback-type digital amplifier, and have the feature with high power supply noise tolerance. As a result, power supply can be simplified and allowing a simple amplifier system with less external components to be configured. YDA176 has the following functions: gain setting function, power limit function, pop noise reduction function, overcurrent protection function for speaker output pins, internal overtemperature protection function, under voltage lockout, and DC detection function.

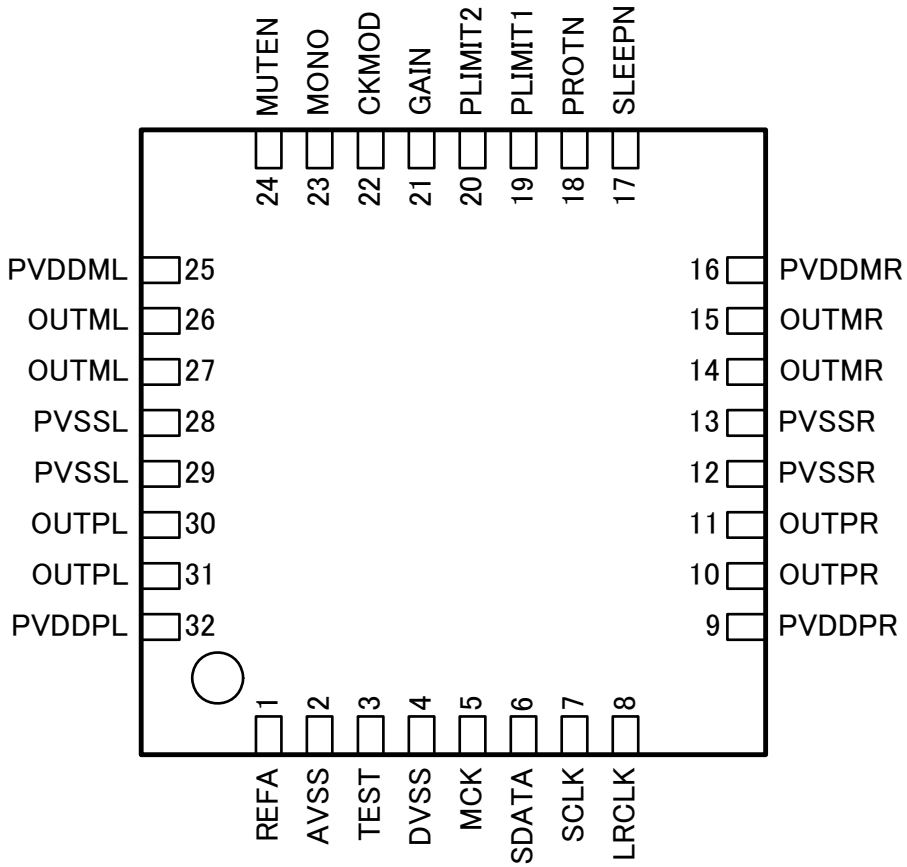
(Note) *1: When operating below 8V (V_{DDP}), the speaker impedance must be 8Ω or higher.

2. Features

- Supply Voltage Range V_{DDP} 5V[*1)] to 18V
- Input Digital Audio Interface (Stereo)
  Sampling Frequency: 32kHz, 44.1kHz, 48kHz
  Left-justified, MSB first, 1-bit delay, Digital Audio Data 24-bits
- Max. Instantaneous Output 15W×2ch (V_{DDP}=15V, R_L=8Ω, THD+N=10%)
  10W×2ch (V_{DDP}=12V, R_L=8Ω, THD+N=10%)
  10W[*2)]×2ch (V_{DDP}=12V, R_L=6Ω)
  10W[*2)]×2ch (V_{DDP}=12V, R_L=4Ω)
- Max. Continuous Output 15W[*3)]×2ch (V_{DDP}=15V, R_L=8Ω, Ta=70 ºC, 4-layer Board)
  10W[*3)]×2ch (V_{DDP}=12V, R_L=8Ω, Ta=70 ºC, 4-layer Board)
  10W[*2) *3)]×2ch (V_{DDP}=12V, R_L=6Ω, Ta=70 ºC, 4-layer Board)
- Distortion Ratio (THD+N) 0.05% (V_{DDP}=12V, R_L=8Ω, Po=4.5W, 1kHz)
- Residual Noise 50μVrms (V_{DDP}=12V, R_L=8Ω, A-Weighted Filter)
- S/N Ratio 105dB (V_{DDP}=12V, R_L=8Ω, A-Weighted Filter)
- Efficiency 92% (V_{DDP}=12V, R_L=8Ω, Po=10W)
- Channel Separation 90 dB (V_{DDP}=12V, R_L=8Ω, 1kHz)
- Power Limit Function
- Gain Setting Function
- Stereo/Monaural Switching Function
- Output Mute Function (Quick Mute/Quick Start)
- Sleep Function
- Pop Noise Reduction Function
- Overcurrent Protection Function (OCP)
- Over Temperature Protection Function (OTP)
- Under Voltage Lockout (UVLO)
- DC Detection Function (DCDET)
- Clock Detection Function (CKDET)
- Package Lead-free 32-pin Plastic QFN (Exposed die pad) : YDA176-QZ

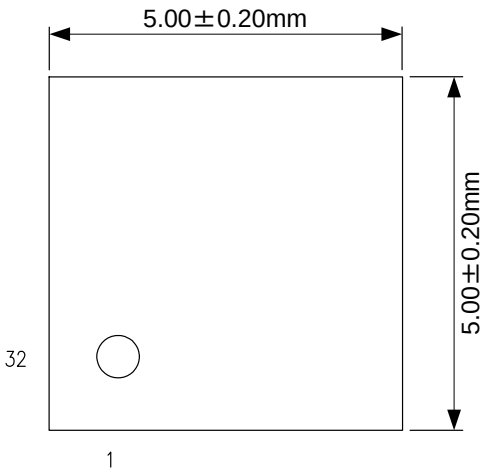
(Note) *1: When operating below 8V (V_{DDP}), the speaker impedance must be 8Ω or higher.
*2: The maximum output power when driving 4Ω and 6Ω loads must be 10W or less.
*3: These values are based on evaluations on a Yamaha's PCB board implementation.
Please refer to Absolute Maximum Rating (Note) *4 on page 33.

3. Pin Assignments

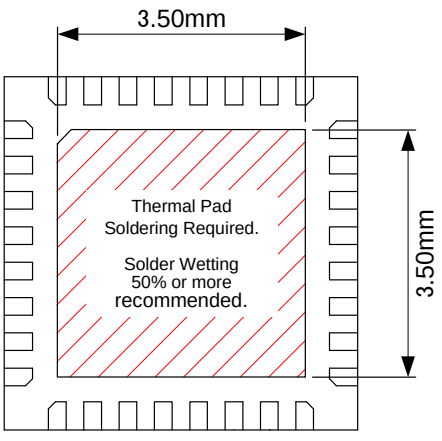


< Figure 3-1 32 pin QFN Top View >

A thermal pad for heat dissipation purpose is provided on the bottom as shown below. This pad should be soldered to your board. The solder wetting not less than 50% is preferable.



<Figure 3-2 QFN Top >



< Figure 3-3 QFN Bottom >

4. Pin Descriptions

The table below shows the pin function list.

Table 4-1 Pin Function

No.	Name	I/O*1)	Function
1	REFA	AO	Internal Regulator Output pin
2	AVSS	GND	Analog GND pin
3	TEST	I	This pin must be connected to GND.
4	DVSS	GND	Digital GND pin
5	MCK	I	Master Clock Input Pin
6	SDATA	I	Audio Data Input Pin
7	SCLK	I	Bit Clock Input Pin
8	LRCLK	I	Word Clock Input Pin
9	PVDDPR	PVDD power	Power pin for the digital amplifier output (Rch+)
10	OUTPR	O	Digital Amplifier Output pin (Rch+)
11	OUTPR	O	Digital Amplifier Output pin (Rch+)
12	PVSSR	GND	GND pin for the digital amplifier output (Rch)
13	PVSSR	GND	GND pin for the digital amplifier output (Rch)
14	OUTMR	O	Digital Amplifier Output pin (Rch-)
15	OUTMR	O	Digital Amplifier Output pin (Rch-)
16	PVDDMR	PVDD power	Power pin for the digital amplifier output (Rch-)
17	SLEEPN	I	Sleep Reset pin *2)
18	PROTN	O/D	Error Flag Output pin
19	PLIMIT1	A	Power Limit Setting Pin 1.
20	PLIMIT2	A	Power Limit Setting Pin 2.
21	GAIN	A	Gain Setting Pin.
22	CKMOD	I	Clock Mode setting pin
23	MONO	A	Stereo/Mono Setting Pin.
24	MUTEN	I	Mute pin
25	PVDDML	PVDD power	Power pin for the digital amplifier output (Lch-)
26	OUTML	O	Digital Amplifier Output pin (Lch-)
27	OUTML	O	Digital Amplifier Output pin (Lch-)
28	PVSSL	GND	GND pin for the digital amplifier output (Lch)
29	PVSSL	GND	GND pin for the digital amplifier output (Lch)
30	OUTPL	O	Digital Amplifier Output pin (Lch+)
31	OUTPL	O	Digital Amplifier Output pin (Lch+)
32	PVDDPL	PVDD power	Power pin for the digital amplifier output (Lch+)

(Note) *1: I: Input pin, O: Output pin, A: Analog pin, O/D: Open-Drain output pin
PVDD power pins should be connected each other on the board. Likewise, GND pins should be also connected each other on it.
Each output pin with the same name (OUTPR, OUTMR, OUTPL, and OUTML) should be connected on the board.

*2: A voltage for supplying SLEEPN pin with “H” level should be applied from an external power supply. Do not apply from REFA pin output.

4.1. Pin Internal Circuit

The tables 4-2 to 4-3 show the internal circuit configuration of each pin.

Table 4-2 Pin Internal Circuit

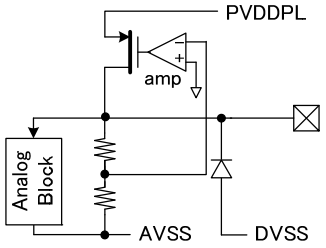
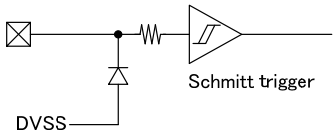
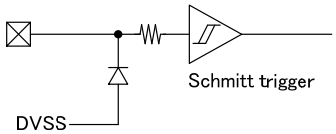
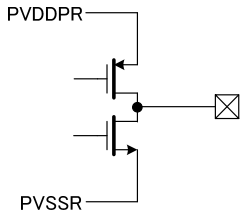
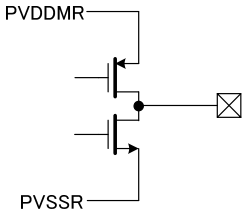
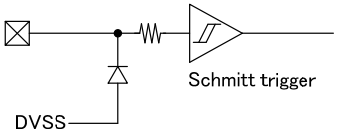
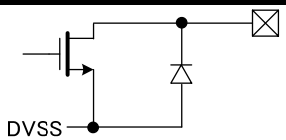
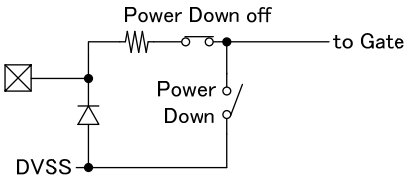
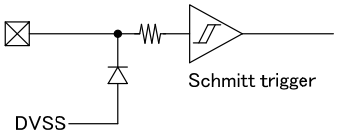
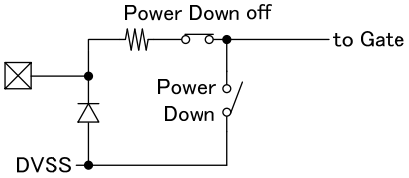
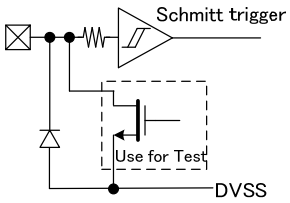
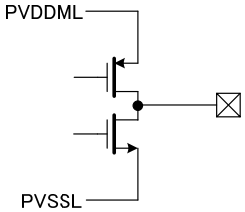
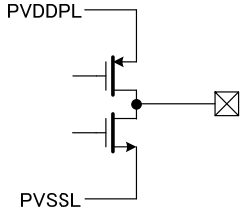
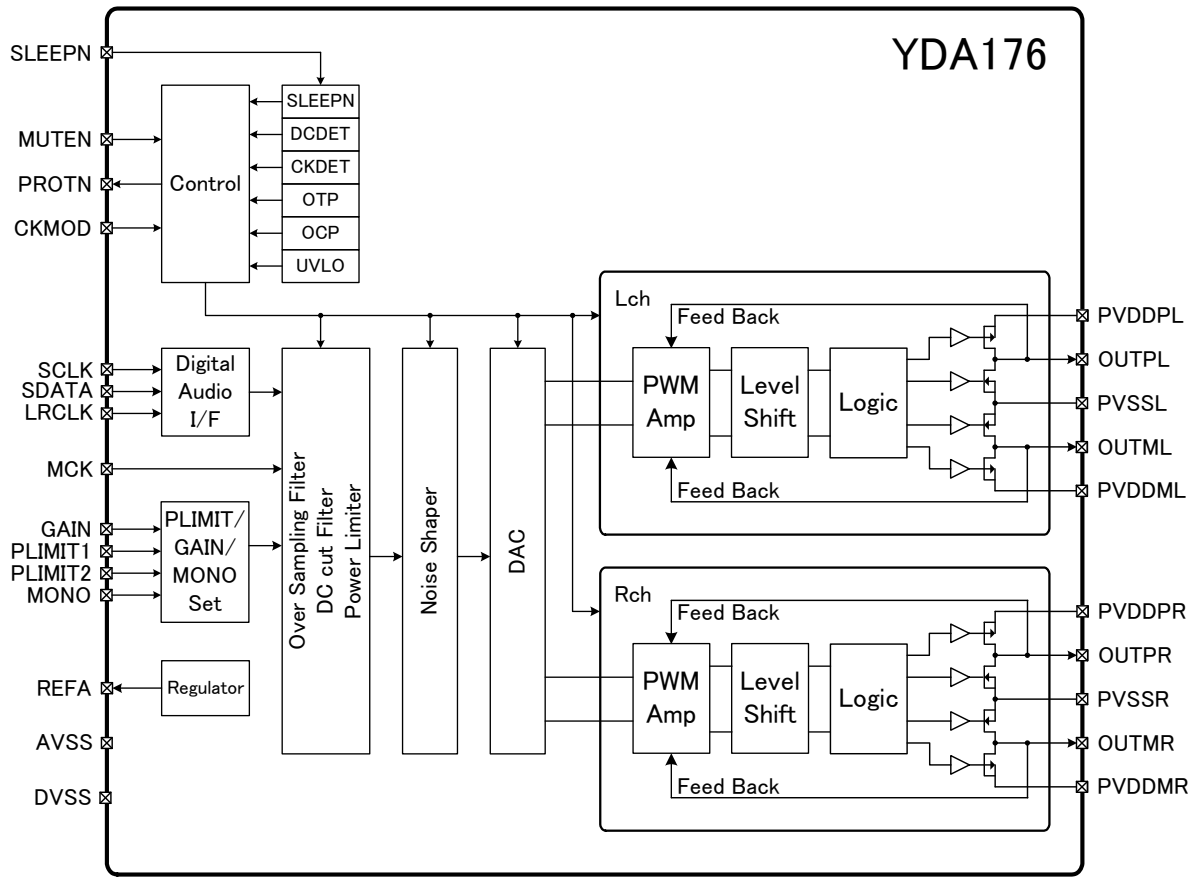
Pin No.	Name	Equivalent Circuit
1	REFA	
2	AVSS	—
3	TEST	
4	DVSS	—
5	MCK	
6	SDATA	
7	SCLK	
8	LRCLK	
9	PVDDPR	—
10,11	OUTPR	
12,13	PVSSR	—
14,15	OUTMR	
16	PVDDMR	—
17	SLEEPN	

Table 4-3 Pin Internal Circuit

Pin No.	Name	Equivalent Circuit
18	PROTN	
19	PLIMIT1	
20	PLIMIT2	
21	GAIN	
22	CKMOD	
23	MONO	
24	MUTEN	
25	PVDDML	—
26,27	OUTML	
28,29	PVSSL	—
30,31	OUTPL	
32	PVDDPL	—

5. Block Diagram



< **Figure 5-1 Block Diagram** >

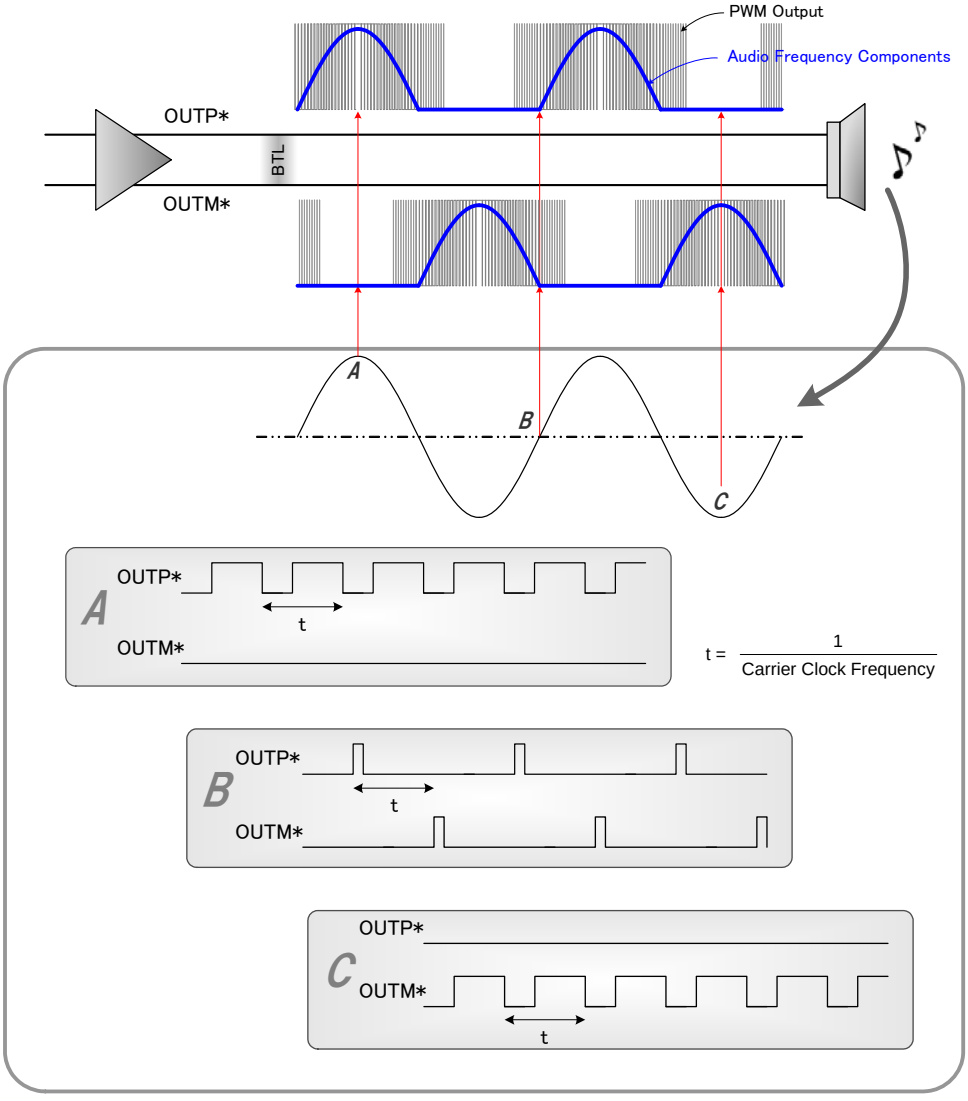
6. Operations Description

The description below shows YDA176 functions and operations.

6.1. Digital Amplifier Modulation Method

YDA176 has a 15W (max.) × 2ch digital amplifier with digital input and PWM pulse output.
YDA176, with Yamaha original "Pure Pulse Direct Speaker Drive Circuit," allows a speaker to be directly connected to the output.

The pulse frequency that appears between OUTP* and OUTM* pins is called "Carrier Clock Frequency."
The figure below shows the output waveform for when a sine wave is input, because of the characteristics of Yamaha unique modulation method.
As shown in B of the figure, the frequency that appears between GND and OUTP* pins and between GND and OUTM* pins at no-signal input becomes the half of a carrier clock frequency.
As shown in A, C of the figure, when the output power increases, one side stops its switching and the other serves as a carrier clock frequency.



< **Figure 6-1 Modulation Method with Pure Pulse Direct Speaker Drive Circuit** >

6.2. Maximum Output

The maximum output power for each condition (load impedance, supply voltage) is as follows:

・Instantaneous Max. Output:	15W×2ch	(V_{DDP}=15V, R_L=8Ω, THD+N=10%)
	10W×2ch	(V_{DDP}=12V, R_L=8Ω, THD+N=10%)
	10W[*1)]×2ch	(V_{DDP}=12V, R_L=6Ω)
	10W[*1)]×2ch	(V_{DDP}=12V, R_L=4Ω)
・Max. Continuous Output:	15W[*2)]×2ch	(V_{DDP}=15V, R_L=8Ω, T_A=70 ºC, 4-layer board)
	10W[*2)]×2ch	(V_{DDP}=12V, R_L=8Ω, T_A=70 ºC, 4-layer board)
	10W[*1)*2)]×2ch	(V_{DDP}=12V, R_L=6Ω, T_A=70 ºC, 4-layer board)

The instantaneous maximum output means the maximum output without consideration of the heat of IC package. "Max. Continuous Output" means the maximum output under the following conditions: continuous sine waveform output, Tjmax: less than 150 ºC at a specified ambient temperature T_A.

(Note) *1: The maximum output power when driving 4Ω and 6Ω loads must be 10W or less.

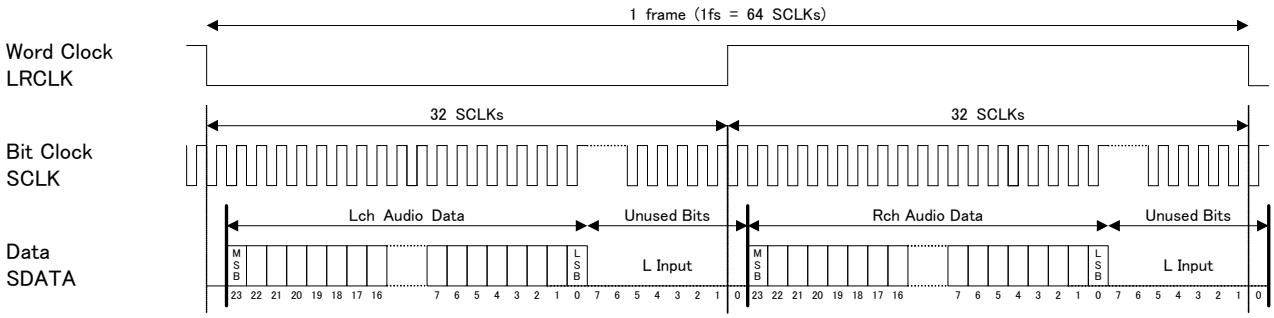
*2: These values are based on evaluations on a Yamaha's PCB board implementation.

Please refer to Absolute Maximum Rating (Note) *4 on page 33.

6.3. Digital Audio Interface

YDA176 receives digital audio data using SCLK, LRCLK, and SDATA pins.
The following sampling frequencies are supported: 32kHz, 44.1kHz, and 48kHz
Audio signal format: Left-justified format, MSB first, 1-bit delay, 24 bits.
LRCLK and SDATA are loaded at the rising edge of SCLK.
The number of valid SDATA bits is up to 24 bits.

24bit×2ch audio data are input through SDATA pin during one sample period. Fill the unused bits after 24th bit with "L" data.



< **Figure 6-2 Digital Audio Interface Timing** >

6.4. Carrier Clock Frequency Control Function

This is the function to set a carrier frequency with the following control pins. The way to control the frequency is as follows:

・LRCLK, SCLK, MCK pins
According to condition used, input clock to LRCLK, SCLK, and MCK pins as shown in Table 6-1.
・CKMOD pin
CKMOD pin is the clock mode setting pin. It should be set as shown in the table according to MCK frequency to input.

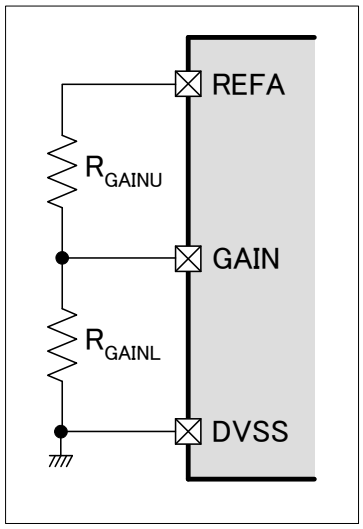
Frequencies and pin settings other than the listed values are not available.
MCK frequency must be just an integral multiple of SCLK frequency. And, the frequencies must be derived from the same oscillator. There is no restriction about the phase relationship of MCK and SCLK.
To change SCLK and LRCLK frequencies, MUTEN pin must be set to “L”.
To change MCK frequencies and CKMOD pin setting, SLEEPN pin must be set to “L” or power must be down.

Table 6-1 Carrier Clock Frequency

fs [kHz]	LRCLK(1fs) [kHz]	SCLK(64fs) [kHz]	MCK [kHz]	MCK [fs]	CKMOD	Carrier Clock Frequency [kHz]
32	32	2048	24576	768	L	768
32	32	2048	16384	512	H	1024
32	32	2048	12288	384	H	768
44.1	44.1	2822.4	22579	512	L	705.6
44.1	44.1	2822.4	11290	256	H	705.6
48	48	3072	24576	512	L	768
48	48	3072	12288	256	H	768

6.5. Gain Setting Function

Two discrete resistors on the GAIN pin select YDA176's amplifier gain from one of eight values.
Gain setting circuit is shown below.



< Figure 6-3 Gain Setting Circuit >

The amplifier gain can be set to one of the three fixed levels (*Mode* 6 through 8 in *Table 6-2*), or a level that satisfies full scale output distortion figures of less than 1 %, or at 5 %, 10 %, 20 %, or 30 % (*Mode* 1 through 5 in *Table 6-2*).
To change GAIN pin setting, MUTEN pin must be set to “L” or power must be down.
Table 6-2 shows digital amplifier gain setting.

Table 6-2 Gain Setting

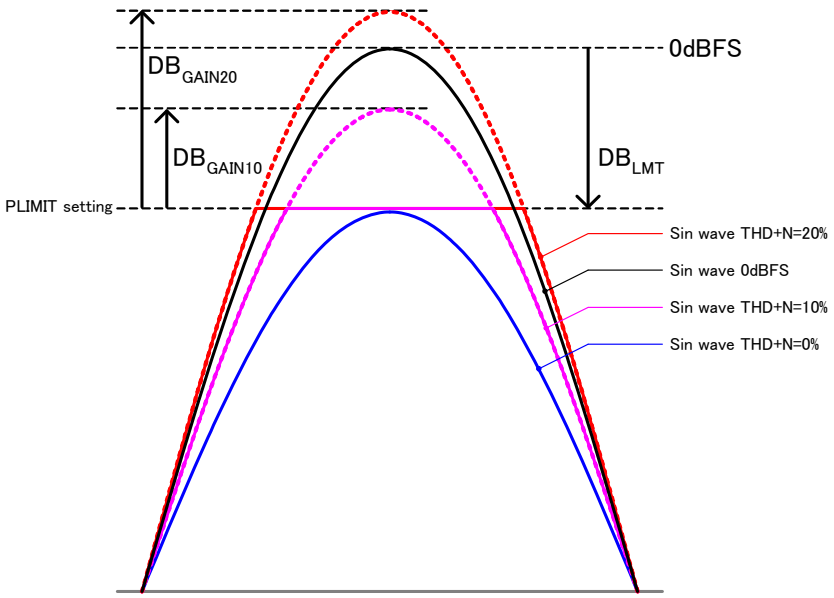
Mode	GAIN pin level	GAIN pin Voltage range	Resistance Value Setting (E12 series 1% accuracy)		DB_{GAIN**}[dB]	Output level [dBV] When –20dBFS input	Power Limiter bounded (at the 0 dBFS distortion figure)
	REFA voltage ratio	(When REFA=3.4V)	R_{GAINU}	R_{GAINL}			
1	55% to 100%	1.80V to 3.40V	Short	Open	DB_{GAIN10}: 2.473	2.30＋(DB_{LMT}+ DB_{GAIN10}) *1)	10% *2)
2	44% to 55%	1.45V to 1.80V	22kΩ	22kΩ	DB_{GAIN30} : 9.159	2.30＋(DB_{LMT}+ DB_{GAIN30}) *1)	30% *2)
3	35% to 44%	1.15V to 1.45V	22kΩ	15kΩ	DB_{GAIN20} : 5.197	2.30＋(DB_{LMT}+ DB_{GAIN20}) *1)	20% *2)
4	26% to 35%	0.85V to 1.15V	27kΩ	12kΩ	DB_{GAIN5} : 1.376	2.30＋(DB_{LMT}+ DB_{GAIN5}) *1)	5% *2)
5	17% to 26%	0.55V to 0.85V	56kΩ	15kΩ	DB_{GAIN0} : 0	2.30＋(DB_{LMT}+ DB_{GAIN0}) *1)	<1% *2)
6	9% to 17%	0.30V to 0.55V	68kΩ	10kΩ	–	–3.70	–
7	3% to 9%	0.10V to 0.30V	68kΩ	4.7kΩ	–	8.30	–
8	0% to 3%	0.00V to 0.10V	Open	Short	–	2.30	–

(Note): Gain setting resistors (R_{GAINU}, R_{GAINL}) draw current when not in sleep state (SLEEPN = "L").

The external resistance should use the above-mentioned value and the 1% accuracy.

*1: DB_{LMT} values are described in *Table 6-4 Power Limiter Setting Examples.*

*2: These distortion figures do not apply if the PWM outputs cause clipping.

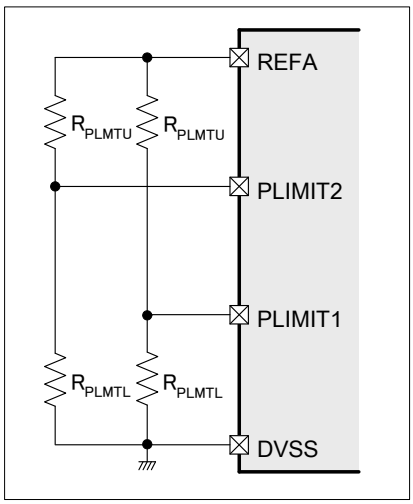


< Figure 6-4 Power Limiter bounded gain controls >

6.6. Power Limit Function

This function, limiting the output peak voltage, protects an external speaker and controls the increase of internal temperature.

PLIMIT1 and *PLIMIT2* can be strapped to one of 8 *Modes* in *Table 6-3, A* through *H* and *1* through *8* respectively with two external resistors on each pin as shown in *Figure 6-5.*
The combination of *PLIMIT1 Mode* and *PLIMIT2 Mode* configures 63 Power Limiter levels as shown in *Table 6-4.* The figure 6-5 shows PLIMIT1 and PLIMIT2 pin setting circuit.



< Figure 6-5 PLIMIT1, PLIMIT2 pin Setting Circuit >

To change PLIMIT1 and PLIMIT2 pin setting, MUTEN pin must be set to "L" or power must be down.
Table 6-3 shows power limit setting example.

Table 6-3 Power Limit Setting

Mode		PLIMIT1,2 pin Voltage range		Resistance Value Setting (E12 series 1% accuracy)	
PLIMIT2 pin	PLIMIT1 pin	REFA Voltage ratio	PLIMIT pin Voltage range (When REFA=3.4V)	R_{PLMTU}	R_{PLMTL}
1	A	55% to 100%	1.80V to 3.40V	Short	Open
2	B	44% to 55%	1.45V to 1.80V	22kΩ	22kΩ
3	C	35% to 44%	1.15V to 1.45V	22kΩ	15kΩ
4	D	26% to 35%	0.85V to 1.15V	27kΩ	12kΩ
5	E	17% to 26%	0.55V to 0.85V	56kΩ	15kΩ
6	F	9% to 17%	0.30V to 0.55V	68kΩ	10kΩ
7	G	3% to 9%	0.10V to 0.30V	68kΩ	4.7kΩ
8	H	0% to 3%	0.00V to 0.10V	Open	Short

(Note): The external resistance should use the above-mentioned value and the 1% accuracy.

Table 6-4 shows sample Power Limiter levels using the Mode combinations.
Power Limiter levels for 8 Ω, 6 Ω, or 4 Ω loads, and stereo or mono output configuration are shown.

Table 6-4 Power Limiter levels using the Mode combinations (TBD)

PLIMIT2 Power Limit Setting (min, THD+N=10%)			PLIMIT1 Power Limit Setting (min, THD+N=10%)								
		Load	A	B	C	D	E	F	G	H
1	Stereo	8Ω	4.000W	TBD	TBD	TBD	TBD	TBD	TBD	10.000W
		6Ω	5.333W							–
		4Ω	8.000W							–
	Mono	8Ω	4.000W							10.000W
		6Ω	5.333W							13.333W
		4Ω	8.000W							20.000W
	DB_{LMT}[dB]		−7.86							−3.88
2	Stereo	8Ω	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
		6Ω								
		4Ω								
	Mono	8Ω								
		6Ω								
		4Ω								
	DB_{LMT}[dB]									
3	Stereo	8Ω	TBD	TBD	TBD	TBD	TBD	TBD	TBD	2.500W
		6Ω								3.333W
		4Ω								5.000W
	Mono	8Ω								2.500W
		6Ω								3.333W
		4Ω								5.000W
	DB_{LMT}[dB]									−9.90
4	Stereo	8Ω	2.750W	2.625W	3.375W	4.125W	4.875W	5.500W	6.250W	3.000W
		6Ω	3.667W	3.500W	4.500W	5.500W	6.500W	7.333W	8.333W	4.000W
		4Ω	5.500W	5.250W	6.750W	8.250W	9.750W	–	–	6.000W
	Mono	8Ω	2.750W	2.625W	3.375W	4.125W	4.875W	5.500W	6.250W	3.000W
		6Ω	3.667W	3.500W	4.500W	5.500W	6.500W	7.333W	8.333W	4.000W
		4Ω	5.500W	5.250W	6.750W	8.250W	9.750W	11.000W	12.500W	6.000W
	DB_{LMT}[dB]		−9.49	−9.69	−8.60	−7.73	−7.00	−6.48	−5.92	−9.11
5	Stereo	8Ω	3.250W	6.375W	6.500W	7.000W	7.125W	8.250W	8.500W	3.500W
		6Ω	4.333W	8.500W	8.667W	9.333W	9.500W	–	–	4.667W
		4Ω	6.500W	–	–	–	–	–	–	7.000W
	Mono	8Ω	3.250W	6.375W	6.500W	7.000W	7.125W	8.250W	8.500W	3.500W
		6Ω	4.333W	8.500W	8.667W	9.333W	9.500W	11.000W	11.333W	4.667W
		4Ω	6.500W	12.750W	13.000W	14.000W	14.250W	16.500W	17.000W	7.000W
	DB_{LMT}[dB]		−8.76	−5.84	−5.75	−5.43	−5.36	−4.72	−4.59	−8.44
6	Stereo	8Ω	4.250W	9.000W	9.500W	9.750W	10.500 W	11.000 W	11.250 W	4.500W
		6Ω	5.667W	–	–	–	–	–	–	6.000W
		4Ω	8.500W	–	–	–	–	–	–	9.000W
	Mono	8Ω	4.250W	9.000W	9.500W	9.750W	10.500 W	11.000 W	11.250 W	4.500W
		6Ω	5.667W	12.000W	12.667W	13.000W	14.000W	14.667W	15.000W	6.000W
		4Ω	8.500W	18.000W	19.000W	19.500W	21.000W	22.000W	22.500W	9.000W
	DB_{LMT}[dB]		−7.60	−4.34	−4.11	−3.99	−3.67	−3.47	−3.37	−7.35
7	Stereo	8Ω	4.750W	11.500W	13.000W	13.500 W	14.000W	14.500W	Reserved	5.000W
		6Ω	6.333W	–	–	–	–	–		6.667W
		4Ω	9.500W	–	–	–	–	–		10.000W
	Mono	8Ω	4.750W	11.500 W	13.000W	13.500 W	14.000W	14.500W		5.000W
		6Ω	6.333W	15.333W	17.333W	18.000W	18.666W	19.333W		6.667W
		4Ω	9.500W	23.000W	26.000W	27.000W	28.000W	29.000W		10.000W
	DB_{LMT}[dB]		−7.12	−3.28	−2.74	−2.58	−2.42	−2.27		−6.89
8	Stereo	8Ω	3.750W	5.625W	6.000W	7.500W	8.000W	12.000 W	12.500W	15.000W
		6Ω	5.000W	7.500W	8.000W	10.000 W	–	–	–	–
		4Ω	7.500W	–	–	–	–	–	–	–
	Mono	8Ω	3.750W	5.625W	6.000W	7.500W	8.000W	12.000 W	12.500W	15.000W
		6Ω	5.000W	7.500W	8.000W	10.000 W	10.667W	16.000W	16.667W	20.000W
		4Ω	7.500W	11.250W	12.000W	15.000W	16.000W	24.000W	25.000W	30.000W
	DB_{LMT}[dB]		−8.14	−6.38	−6.10	−5.13	−4.85	−3.09	−2.91	−2.12

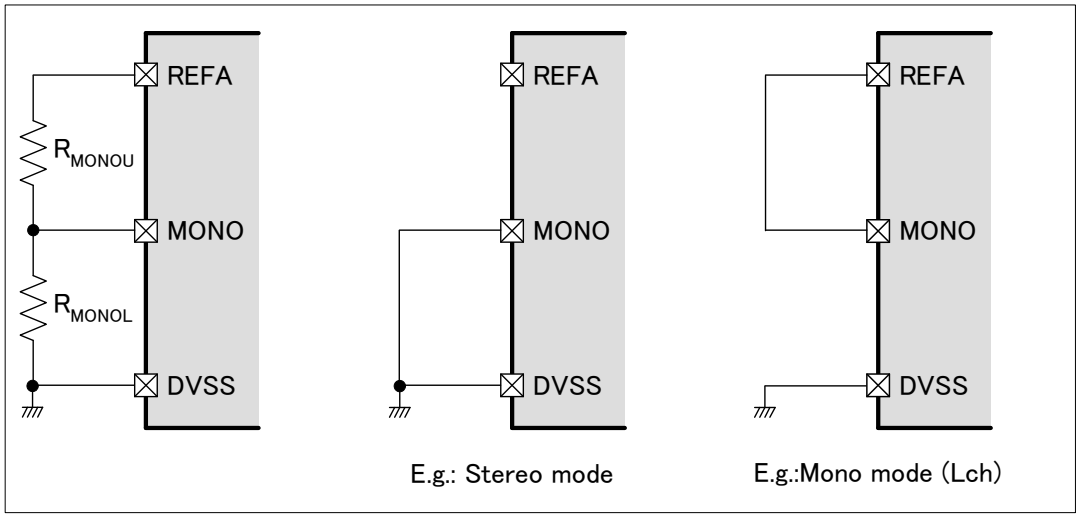
(Note): Current flows through the voltage divide resistor (R_{PLMTU},R_{PLMTTL}), including the time when SLEEPN pin is "L" (SLEEP state).

Parasitic DC resistances of signal traces and inductors are taken into account for each loading condition as follows.

8Ω load: 0.10Ω, 6Ω load: 0.075Ω, 4Ω load: 0.05Ω

6.7. Stereo mode / Monaural mode Setting Function

YDA176 can be configured as stereo or mono amplifier by external resistors on *MONO* pin.
The figure 6-6 shows MONO pin setting circuit.



< **Figure 6-6 MONO pin Setting Circuit** >

YDA176 can be configured as stereo or mono amplifier by external resistors on *MONO* pin.
For mono configuration, these resistors also determine which mono channel is used as the mono source. The source signal is amplified and put on both L- and R-channel outputs.

Table 6-5 MONO pin Setting

Mode	MONO pin Voltage range		Resistance Value Setting (E12 series 1% accuracy)	
	REFA Voltage ratio	MONO pin Voltage range (When REFA=3.4V)	R_{MONOU}	R_{MONOL}
Mono mode (Rch)	45% to 55%	1.45V to 1.80V	22kΩ	22kΩ
Mono mode (Lch+Rch,-6dB)	35% to 44%	1.15V to 1.45V	22kΩ	15kΩ
Mono mode (Lch)	55% to 100%	1.80V to 3.40V	Short	Open
Stereo mode	0% to 3%	0.00V to 0.10V	Open	Short

(Note): The external resistance should use the above-mentioned value and the 1% accuracy.

When using in stereo mode, this device should be connected as shown in “Stereo Mode” of “7.1 Application Circuit Examples.”
When using in monaural mode, OUTPL and OUTML should be connected to OUTPR and OUTMR respectively as shown in “Monaural Mode” of “7.1 Application Circuit Examples.”
Be sure to turn off the power before selecting stereo or monaural mode or making the appropriate connection.

6.8. Quick Mute/Quick Start Function

Quick Mute/Quick Start function allows intermittent sound to be reduced significantly and uncomfortable feeling to be removed by varying the output envelope at a slow rate at the time of MUTE ON/OFF.

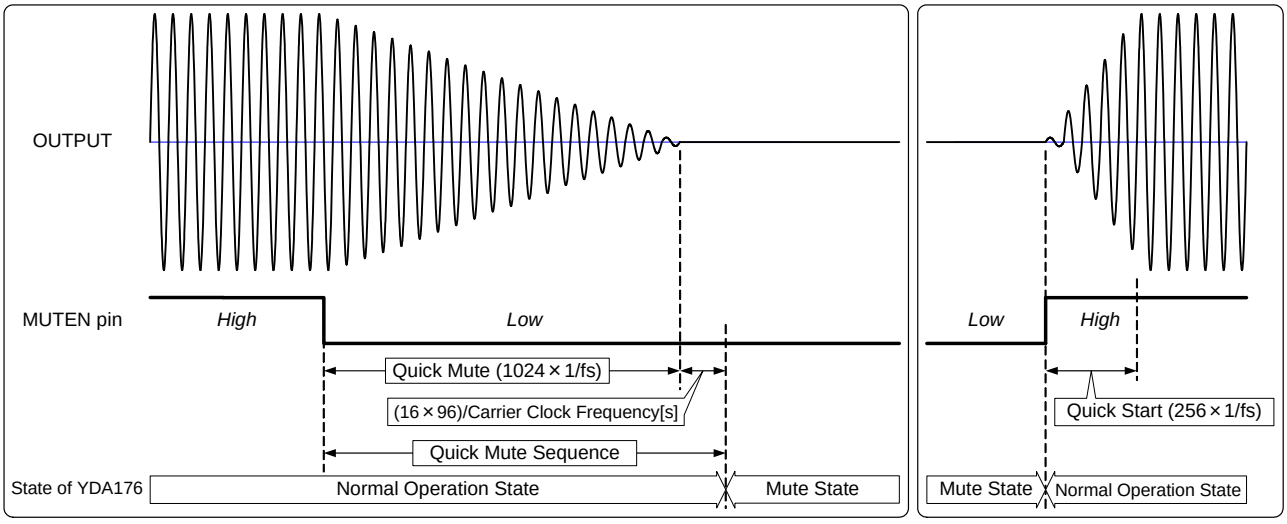
Table 6-6 MUTEN pin setting

MUTEN pin	Mode
L	Digital Amplifier Mute State
H	Normal Operation State

By setting MUTEN pin to "L", YDA176 performs Quick Mute operation (Decreasing the volume linearly by taking 1024×1/fs), (16×96) / (carrier clock frequency)[s] later, it sets the digital amplifier output to WL (Weak Low: a state grounded through a high-value resistance), resulting in Mute state (Output Disabled).

By setting MUTEN pin to "H", YDA176 moves from the mute state to normal operation state while turned down volume. Afterwards, the quick start operation (where the volume is increased linearly over 256×1/fs) is executed. Mute recovery time from Mute state is t_{mrcv}(typ.).
If the mute state is cancelled during the Quick Mute Sequence, Quick Start Sequence will start after the quick mute sequence.

When the voltage at PVDD pin becomes lower than PVDD pin Shutdown Threshold Voltage (V_{HUVLL}) in the mute state, for shutting down the system safely, the amplifier output is set to WL (Weak Low : a state grounded through a high-value resistance) after outputting a low signal for a given period of time.



< **Figure 6-7 Quick Mute / Quick Start Function** >

6.9. Sleep Function

In Sleep state, all circuit functions are stopped and consumption current becomes the minimum (I_{DDPS}). And, REFA pin outputs is pulled down.

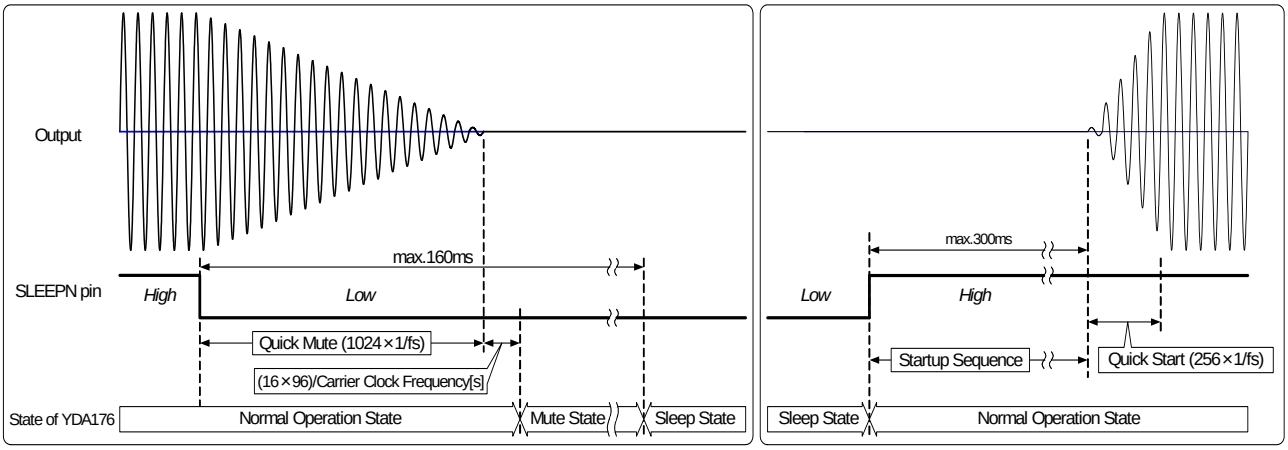
Table 6-7 SLEEPN pin setting

SLEEPN pin	Mode
L	Sleep State
H	Normal Operation State

By setting SLEEPN pin to “L”, YDA176 performs Quick Mute operation (Decreasing the volume linearly by taking 1024×1/fs), (16×96) / (carrier clock frequency) [s] later, it sets the digital amplifier output to WL(Weak Low: a state grounded through a high-value resistance).

YDA176 goes to Sleep state when max.160ms has passed after setting SLEEPN pin to "L."
When going to sleep mode while some protection state is being activated, this protection mode is cancelled and PROTN pin output goes to Hi-Z state.

With PVDD pin output being higher than the threshold voltage to cancel the low-voltage malfunction preventing function, when changing the state of SLEEPN pin from “L” to “H,” the digital amplifier terminates the sleep state, simultaneously starts the Startup Sequence and does the quick start (raises the volume level linearly by taking 256×1/fs) to activate the oscillation after max.300ms.



< **Figure 6-8 Sleep Function** >

6.10. DC-cut Function

YDA176 includes DC-cut filter (cut-off frequency=10Hz) for input digital audio data.

6.11. Supply Voltage Regulation

YDA176 adopts a circuit method that feeds back the output signal. This method allows the deterioration in distortion characteristics to be minimized even when a supply voltage fluctuates (in case of a power supply not regulated). Whereas, with a non-feedback type digital amplifier, a power supply with high-regulation capability is required because this fluctuation is added to the output waveform.

6.12. REFA Voltage Output Function

YDA176 includes series regulator. The voltage inputted from a PVDD power supply pin is supplied to a regulator. REFA pin outputs the voltage (V_{REFA}) regulated from the voltage coming from PVDD pin.
For its stabilization, connect a bypass capacitor of 1.0μF to 4.7μF between REFA and AVSS pins. (0.8μF or more should be secured including its variation and temperature change.)
REFA pin must not be connected to other devices.

6.13. Digital Amplifier Startup/Shutdown Procedure

It is recommended to use the following sequences as digital amplifier start and shutdown procedure.
With different sequence, unusual sound or pop noise may occur.

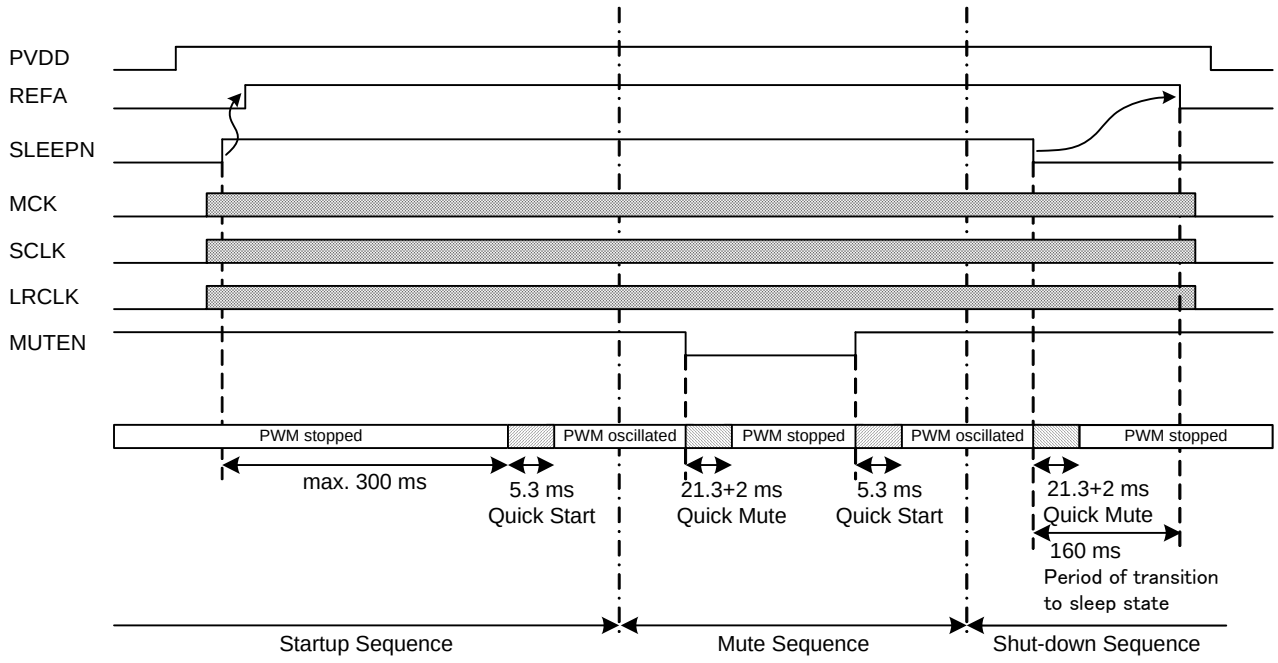
6.13.1 Recommended Digital Amplifier Startup Sequence

1. Supply the power to PVDD pin.
2. When the supply voltage reaches at the recommended voltage range, input clocks to MCK, SCLK, and LRCLK pins.
3. Change the logical state of SLEEPN pin from “L” to “H”.

6.13.2 Recommended Digital Amplifier Shutdown Sequence

1. Change the logical state of SLEEPN pin from “H” to “L”.
2. After 160ms or more, stop input the signal to the input pins and shut down the power to PVDD pin.

* As long as SLEEPN pin was changed from “H” to “L” and Quick Mute {1024×1/fs + (16×96) / (Carrier Clock Frequency)}[s]” has elapsed, unusual sound or pop noise is not generated even if the power is shut down.



*Quick Start and Quick Mute are those at fs=48kHz as an example.

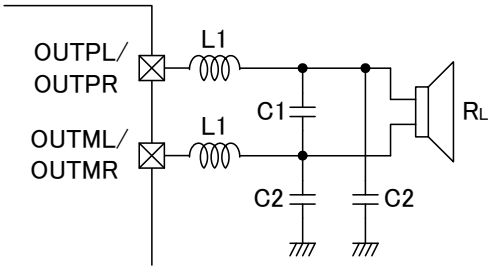
< **Figure 6-9 Recommended Digital Amplifier Startup / Shutdown Sequence** >

6.14. LC Filter

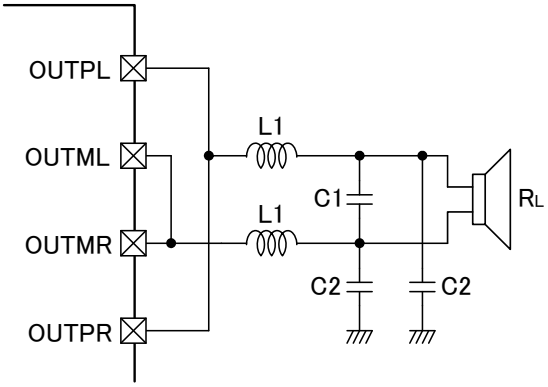
On the other hand, when using a LC filter, the output circuit as shown in Figure 6-10, 6-11 should be used with the constants listed in Table 6-8. The use of these constants enables the filter to be a low-pass filter with its cut-off frequency being 50kHz or so and Q being 0.6 or so.

When disconnecting a speaker, turn off the power in advance.

When operating the device without a speaker, consumption current may increase or overcurrent detection circuit may work due to the resonance in LC filter. When removing a speaker during operation, SLEEPN or MUTEN pin should be set to "L" or PVDD should be shut down.



< **Figure 6-10 LC Filter Circuit (Stereo)** >



< **Figure 6-11 LC Filter Circuit (Mono)** >

Table 6-8 LC Filter Constants

R_L	L1	C1	C2	fc	fc (to GND)	Q
4Ω	10μH	0.33μF	0.22μF	53.7kHz	107kHz	0.59
6Ω	15μH	0.22μF	0.1μF	55.9kHz	130kHz	0.57
8Ω	22μH	0.22μF	0.1μF	46.2kHz	107kHz	0.63
16Ω	47μH	0.1μF	0.047μF	46.7kHz	107kHz	0.58

$$f_C = \frac{1}{2\pi\sqrt{L_1 \times (2 \times C_1 + C_2)}}$$

$$f_C(toGND) = \frac{1}{2\pi\sqrt{L_1 C_2}}$$

$$Q = \frac{\sqrt{\frac{2 \times C_1 + C_2}{L_1}} \times R_L}{2}$$

When using YDA176 with a speaker connected directly without connecting LC filters, or when using it with EMI countermeasure components, such as ferrite beads etc., in addition to a speaker, a speaker with an inductance higher than 20μH should be used. Otherwise, loss of the speaker and YDA176 may increase.

6.15. Protection Function

YDA176 has the following protection functions.

Table 6-9 Protection Function List

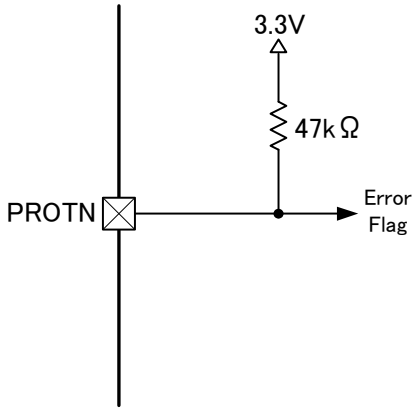
Protection Function	PROTN Pin Output	Digital Amplifier Output	Quick Mute	Automatic Recovery
Overcurrent Protection	L	WL *3)	–	Applicable *1)
Over Temperature Protection	L *2)	WL *3)	–	Not Applicable (However, it returns when the temperature decreases.)
Under Voltage Lock Out (PVDD pin)	H	WL *3)	–	Not Applicable (However, it recovers from the lock out once the voltage level rise after startup sequence.)
DC Detection	L	WL *3)	–	Applicable *1)
Clock Detection (MCK, SCLK pin)	H	WL *3)	–	Not Applicable (However, it returns when the clock input.)

(Note) *1: Automatic recovery is performed 2.7 to 5.4 seconds (at fs=48kHz) after a protecting function is activated, and then PROTN pin goes to "H."

*2: When an over temperature condition is cleared, PROTN is returned to "H."

*3: WL=Weak Low (a state grounded through a high-value resistance)
For shutting down the system safely, the amplifier output is set to WL after outputting a low or high signal for a given period of time.

PROTN pin has an open-drain output.
Use a resistor of 47kΩ to pull up the pin with respect to an external power supply source lower than 3.3V.
In order to prevent the current in excess of 2mA from being flowed into PROTN pin being in L state.
If multiple YDA176s are used, all the PROTNs can be tied together for wired OR connection.
PROTN pin must not connect to pins of YDA176.
PROTN pin should be left open when not used.



< **Figure 6-12 PROTN pin Pull-up Termination** >

6.15.1 Digital Amplifier Overcurrent Protection Function (OCP)

This function, detecting an overcurrent condition at the digital amplifier output, enables the overcurrent protection state, in which the following short-circuiting conditions are detected: VSS short (Ground or any other lower-potential point), PVDD short (supply voltage or a higher-potential point), or short-circuiting between ±output pins.
The detection current, for pin-to-pin short-circuiting, is 8A (typ.,V_{DDP}=12V) and 10A (typ.,V_{DDP}=15V).

In this state, digital amplifier outputs are forced to "WL" state (Weak Low: a state grounded through a high-value resistance) and PROTN pin goes to "L."
The automatic recovery operation is performed 2.7 to 5.4 seconds (at fs=48kHz) after the protection state is activated.
When detected eight times in all, the protection state is held without being cancelled.
The held protection state can be cancelled by setting SLEEPN pin to "L" temporarily or shutting down the power.
This protection state is provided not for guarantee of IC protection in case of exceeding the maximum rating (speaker impedance) but for safety in case of unusual conditions.

6.15.2 Over Temperature Protection Function (OTP)

This function, detecting an unusual high-temperature condition in the chip, and protect IC by output disable.

In this over temperature protection state, in which digital amplifier outputs are forced to "WL" state (Weak Low : a state grounded through a high-value resistance) and PROTN pin goes to "L".
When such unusual temperature in the chip is lowered, this protection state is cancelled and PROTN goes to "Hi-Z.". At the same time, normal operation will start again after a quick start.
This protection function is provided not for guaranteeing the protection in case of exceeding the maximum ratings (junction temperature) but for ensuring safety in case of unusual conditions.

6.15.3 PVDD Under Voltage Lock Out Function (UVLO)

This function, detecting an unusual condition where the voltage at PVDD pin becomes lower than "PVDD pin Shutdown Threshold Voltage", and prevent malfunction etc.

In this low-voltage protection state, digital amplifier outputs become WL state (Weak Low: a state grounded through a high-value resistance).
When voltages at PVDD pin become higher than low-voltage cancel threshold voltage (V_{HUVLH}), the low-voltage protection state is cancelled and the normal operation starts after max. 300ms.
This function does not guarantee all operations even if PVDD pin voltage is over the startup threshold voltage V_{HUVLH}. Be sure to use this IC within the recommended supply voltage.

6.15.4 DC Detection Function (DCDET)

This function is activated when detecting a DC signal in excess of 3.3V (V_{DDP}=15V) for a given period of time (0.67s to 1.33s) at the digital amplifier output and stops the output.

In DC protection state, digital amplifier outputs are forced to WL state (Weak Low: a state grounded through a high-value resistance) and also L level is output to PROTN pin.
The automatic recovery operation is performed 2.7 to 5.4 seconds (at fs=48kHz) after the activation of this protection state.
When detected eight times in all, the protection state is held without being cancelled.
The held protection state can be cancelled by setting SLEEPN pin to "L" temporarily or shutting down the power.
This protection function does not guarantee the protection of the speaker, and provided for ensuring safety.

6.15.5 Clock Detection Function (CKDET)

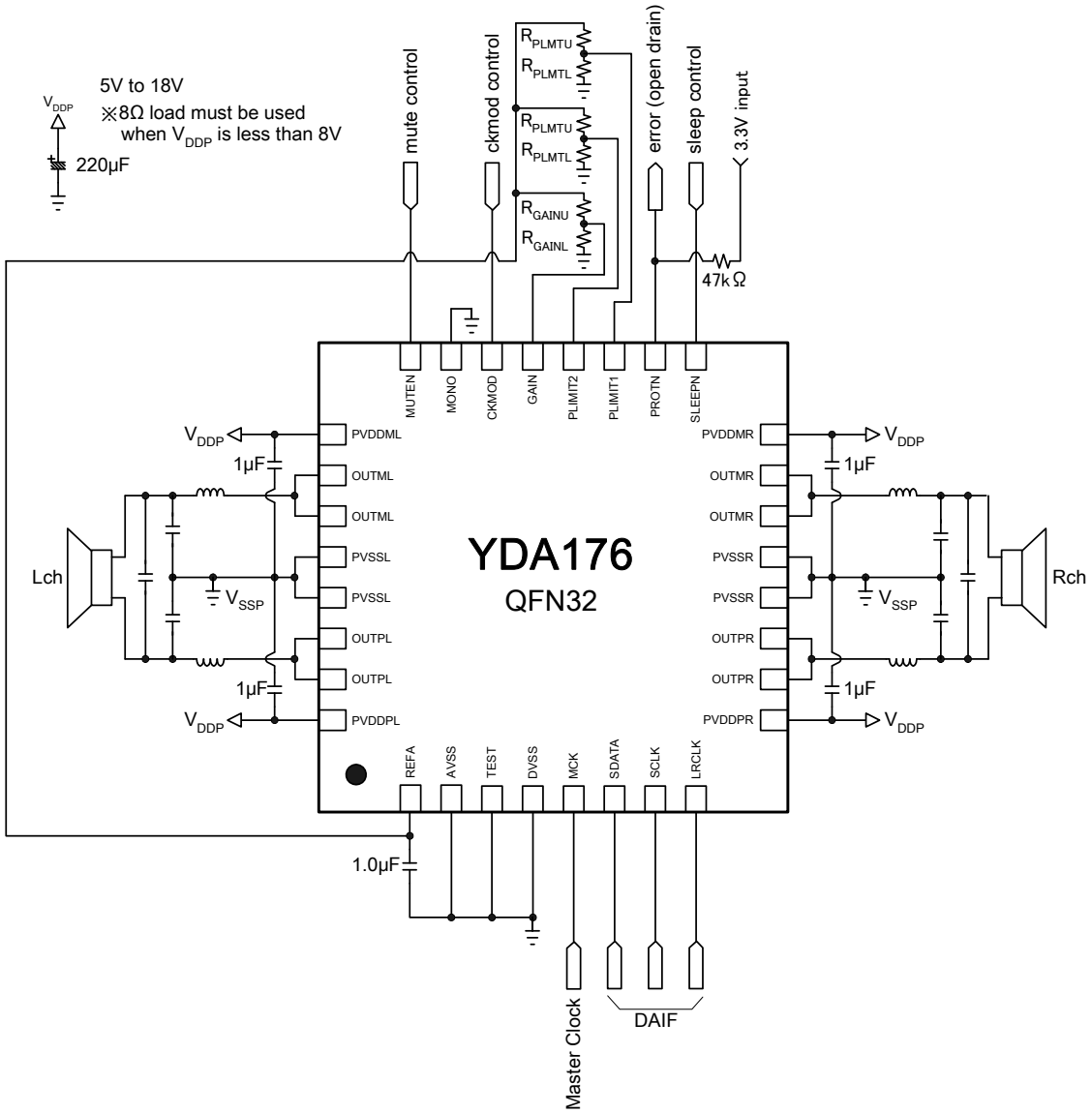
This is the function to prevent DC signals from being transmitted in case any clock to SCLK or MCK pin is stopped during the playback.

When any clock is stopped, the internal free-running clock supersedes it and the digital amplifier output are forced to WL state (Weak Low: a state grounded through a high-value resistance). And, when a clock is received again at SCLK or MCK pin, the operation shifts to the normal operation state.
This protection function is provided for ensuring safety, and does not guarantee the protection of the speaker.

7. Application Information

7.1. Application Circuit Examples

・Stereo Mode



< Figure 7-1 Application Circuit Example Stereo >

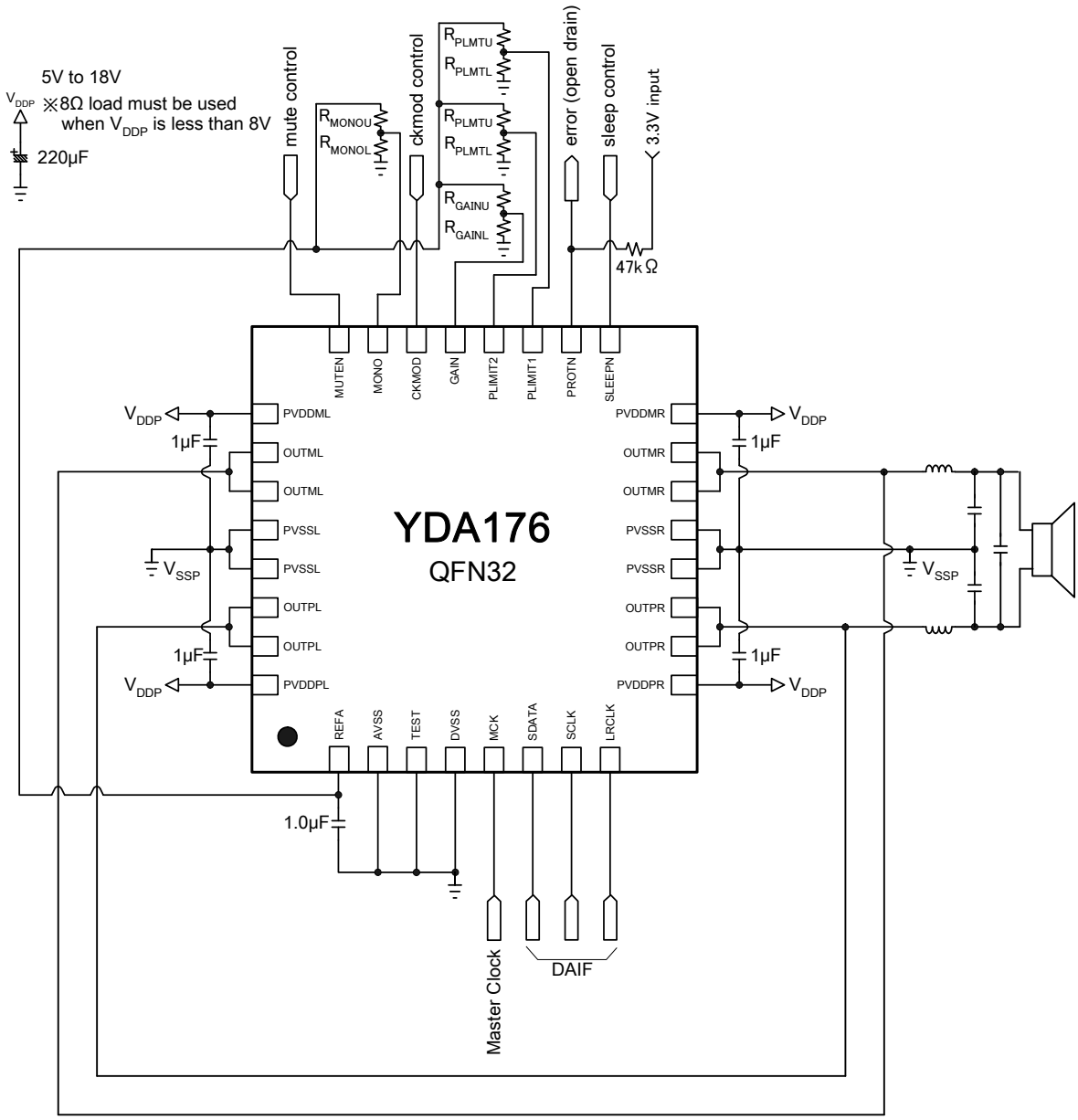
(Note) Connect a bypass capacitor (ceramic capacitor) between the following terminals.

REFA pin and AVSS pin	: 1.0μF to 4.7μF (0.8μF or more should be secured including its variation and temperature change.)
PVDD** pin and PVSS* pin	: 1μF

A bypass capacitor should be placed as closely to a pin as possible.

If TEST, PLIMIT1, PLIMIT2, GAIN, and MONO pins are connected to GND, it will become the same operational mode as YDA175 (D-507D).

・Mono Mode



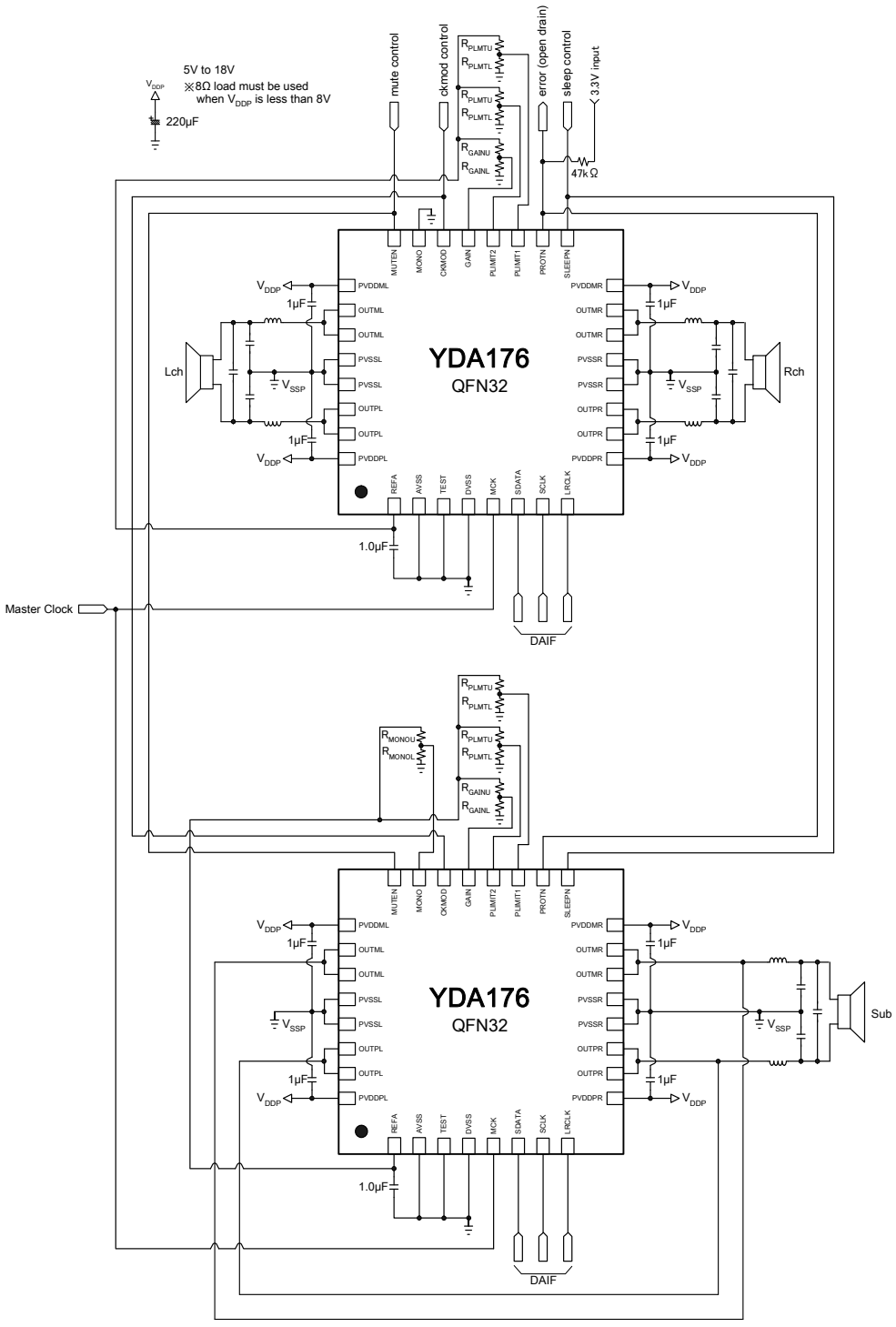
< Figure 7-2 Application Circuit Example Mono >

(Note) Connect a bypass capacitor (ceramic capacitor) between the following terminals.

REFA pin	and	AVSS pin	: 1.0μF to 4.7μF (0.8μF or more should be secured including its variation and temperature change.)
PVDD** pin	and	PVSS* pin	: 1μF

A bypass capacitor should be placed as closely to a pin as possible.

・2.1ch (Stereo Mode ×1 + Mono Mode ×1)



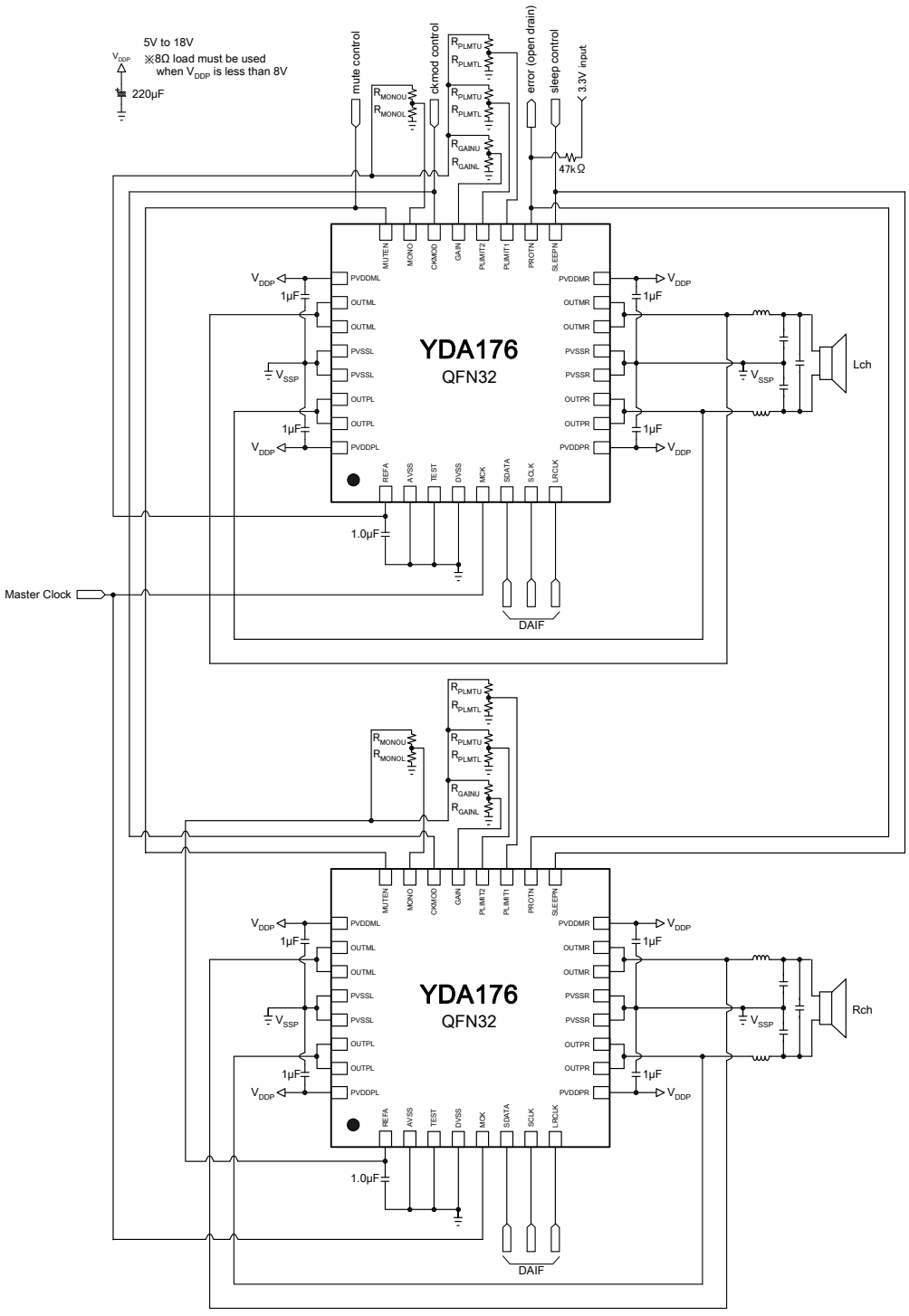
< Figure 7-3 Application Circuit Example 2.1ch >

(Note) Connect a bypass capacitor (ceramic capacitor) between the following terminals.

REFA pin and AVSS pin	: 1.0μF to 4.7μF (0.8μF or more should be secured including its variation and temperature change.)
PVDD** pin and PVSS* pin	: 1μF

A bypass capacitor should be placed as closely to a pin as possible.

・Mono Mode ×2



< Figure 7-4 Application Circuit Example Mono Mode ×2 >

(Note) Connect a bypass capacitor (ceramic capacitor) between the following terminals.

REFA pin and AVSS pin	: 1.0μF to 4.7μF (0.8μF or more should be secured including its variation and temperature change.)
PVDD** pin and PVSS* pin	: 1μF

A bypass capacitor should be placed as closely to a pin as possible.

8. Electrical Characteristics

8.1. Absolute Maximum Ratings[*1)]

Item	Symbol	Condition		Min.	Max.	Unit
Power Supply pin (PVDD) Voltage Range	V_{DDP}	–		–0.3	21.6	V
Input Pin Voltage Range[*2)]	V_{IN1}	–		–0.3	4.6	V
Junction Temperature	T_{jmax}	–		–	150	ºC
Storage Temperature	T_{STG}	–		–40	150	ºC
Power Dissipation	P_{D25}	4-layer Board, θja =23.6 ºC /W θjc(ψjt) =0.2 ºC /W	T_A[*3)]=25 ºC	–	5.2[*4)]	W
	P_{D70}		T_A[*3)]=70 ºC	–	3.3[*4)]	W
	P_{D85}		T_A[*3)]=85 ºC	–	2.7[*4)]	W
	P_{D25}	2-layer board, θja =35.2 ºC /W θjc(ψjt) =0.4 ºC /W	T_A[*3)]=25 ºC	–	3.5[*5)]	W
	P_{D70}		T_A[*3)]=70 ºC	–	2.2[*5)]	W
	P_{D85}		T_A[*3)]=85 ºC	–	1.8[*5)]	W
Speaker Impedance	R_{LS}	$V_{DDP} \geqq 8V$		3.2	–	Ω
	R_{LS}	$V_{DDP} < 8V$		6.4	–	Ω

(Note) *1: Absolute Maximum Ratings are values which must not be exceeded to guarantee device reliability and life, and when using a device in excess of the ratings for even a moment, it may immediately cause damage to the device or may significantly deteriorate its reliability.

*2: Input Pins: MUTEN, MCK, SCLK, LRCLK, SDATA, SLEEPN, CKMOD, TEST, GAIN, MONO, PLIMIT1, and PLIMIT2.

*3: T_A: Air temperature of an open space as far away from the device under test as its contribution can be ignored.

*4: Using the thermal resistance θja of 23.6 °C/W obtained from a board described below.
Board layer: 4 layers, Size: 136[mm]× 85[mm], copper foil thickness: 35[µm],
Copper foil ratio: 377%, Thermal Pad: Soldered to the board,
Thermal via (φ0.5mm): 9 from the exposed stage side to internal layers (VSS layer) and B side

*5: Using the thermal resistance θja of 35.2 °C/W obtained from a board described below.
Board layer: 2 layers, Size: 136[mm] × 85[mm], copper foil thickness: 35[µm],
Copper foil ratio: 185%, Thermal Pad: Soldered to the board,
Thermal via (φ0.5mm) : 9 from the exposed stage side to B side

8.2. Recommended Operating Conditions

Item	Symbol	Condition	Min.	Max.	Unit
Supply Voltage (PVDD)	V_{DDP}	5*1)	–	18	V
Digital pins*2) Input Voltage H level	V_{IN}	2.0	3.3	3.6	V
SLEEPN pin Input Voltage H level	V_{IN}	2.2	3.3	3.6	V
Ambient Operating Temperature	T_A	–40	25	85	ºC

(Note) *1: When operating below 8V (V_{DDP}), the speaker impedance must be 8Ω or higher.

*2: Digital Pins: MUTEN, MCK, SCLK, LRCLK, SDATA, and CKMOD

8.3. DC Characteristics

(V_{DDP} = 5V to 18V, V_{SS} = 0V, T_A = –40 ºC to 85 ºC, unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
PVDD pin	Startup Threshold Voltage	V_{HUVLH}	–	–	3.8	–	V
	Shutdown Threshold Voltage	V_{HUVLL}	–	–	3.7	–	V
Digital pins*1)	Input Voltage H level	V_{IH}	–	2.0	-	–	V
	Input Voltage L level	V_{IL}	–	–	-	0.8	V
	Input Impedance	R_{IN_D}	–	3.3	-	–	MΩ
SLEEPN pin	Input Voltage H level	V_{IH}	–	2.2	-	–	V
	Input Voltage L level	V_{IL}	–	–	-	0.5	V
	Input Impedance	R_{IN_D}	–	3.3	-	–	MΩ
PROTN pin Output Voltage		V_{OL}	I_{OL}=2mA	–	-	0.4	V
REFA pin Output Voltage		V_{REFA}	–	–	3.4	–	V
Current drawn from PVDD	at idling state	I_{DDPP}	V_{DDP} =12V, No load	–	31	–	mA
	at power-down state (SLEEPN="L")	I_{DDPS}	V_{DDP} =12V, No load, T_A = 25 ºC	–	7	–	μA
	at mute state (MUTEN="L")	I_{DDPM}	V_{DDP} =12V, No load	–	21	–	mA

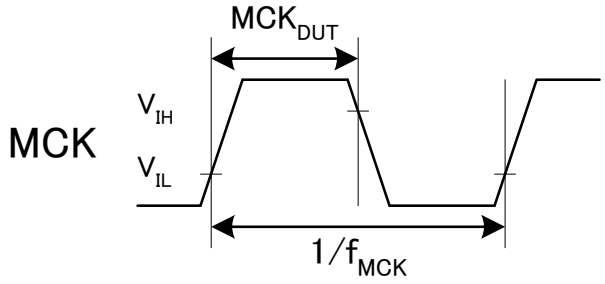
(Note) *1: Digital Pins: MUTEN, MCK, SCLK, LRCLK, SDATA, and CKMOD

8.4. AC Characteristics

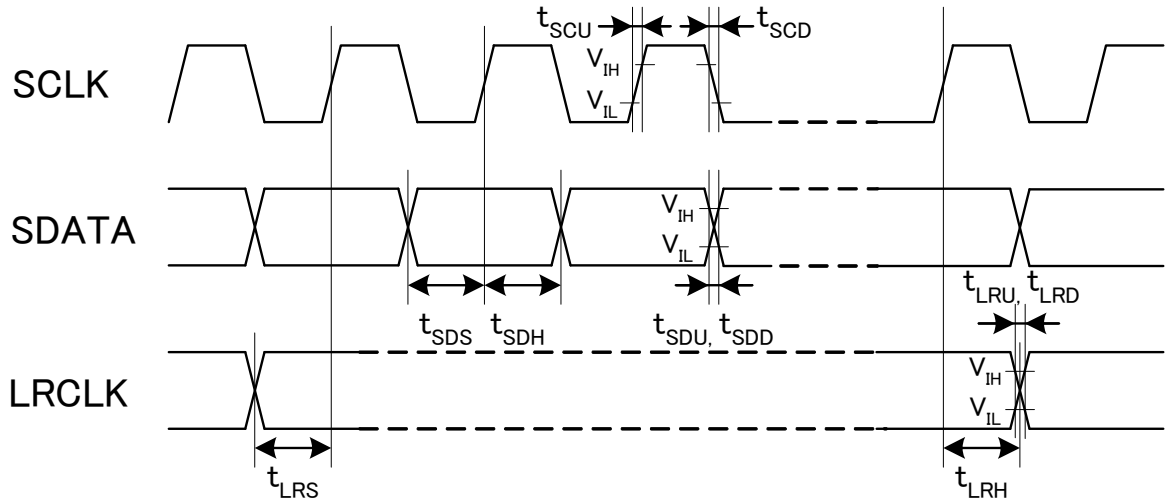
(V_{DDP} = 5V to 18V, V_{SS} = 0V, T_A = –40 ºC to 85 ºC, unless otherwise specified)

Item		Symbol	Min.	Typ.	Max.	Unit
MCK	Input Frequency*1)	f_{MCK}	typ × 0.95	11.290 12.288 16.384 22.579 24.576	typ × 1.05	MHz
	Duty	MCK_{DUT}	40	–	60	%
SCLK	Input Frequency	f_{SCLK}	–	64×fs	–	–
	Rise Time	t_{SCU}	–	–	15	ns
	Fall Time	t_{SCD}	–	–	15	ns
LRCLK	Input Frequency	f_S	–	32 44.1 48	–	kHz
	Setup Time	t_{LRS}	10	–	–	ns
	Hold Time	t_{LRH}	10	–	–	ns
	Rise Time	t_{LRU}	–	–	15	ns
	Fall Time	t_{LRD}	–	–	15	ns
SDATA	Setup Time	t_{SDS}	10	–	–	ns
	Hold Time	t_{SDH}	10	–	–	ns
	Rise Time	t_{SDU}	–	–	15	ns
	Fall Time	t_{SDD}	–	–	15	ns
MUTE Recovery Time (fs=48kHz)		t_{mrcv}	–	5.3	–	ms

(Note) *1: Refer to “Table 6-1 Carrier Clock Frequency” at page 15 for the MCK Input Frequency.



< Figure 8-1 Master Clock Input Timing >



< Figure 8-2 Digital Audio Interface Timing >

8.5. Analog Characteristics

(V_{DDP} = 12V, V_{SS} = 0V, T_A= 25 ºC, R_L=8Ω, unless otherwise specified)

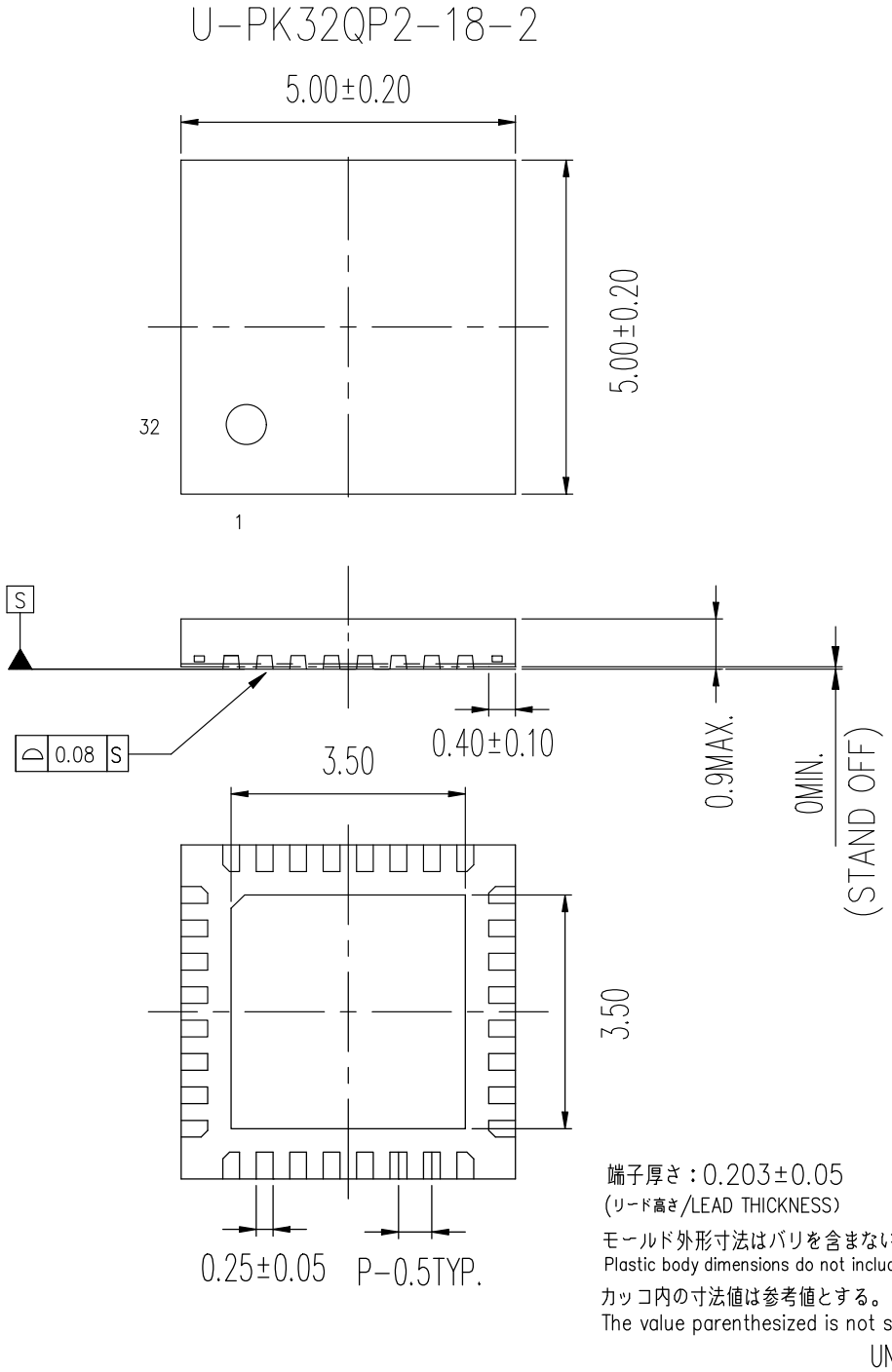
Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum Instantaneous Output	Stereo	Po	V_{DDP}=15V, R_L=8Ω, THD+N=10%	–	15	–	W
			V_{DDP}=12V, R_L=8Ω, THD+N=10%	–	10	–	W
			V_{DDP}=12V, R_L=6Ω	–	10*1)	–	W
			V_{DDP}=12V, R_L=4Ω	–	10*1)	–	W
Maximum Continuous Output	Stereo	Po	V_{DDP}=15V, R_L=8Ω, T_A=70 ºC, 4-layer board	–	15	–	W
			V_{DDP}=12V, R_L=8Ω, T_A=70 ºC, 4-layer board	–	10	–	W
			V_{DDP}=12V, R_L=6Ω, T_A=70 ºC, 4-layer board	–	10*1)	–	W
Total Harmonic Distortion	Stereo	THD+N	R_L=8Ω, Po=4.5W	–	0.05	–	%
Residual Noise	Stereo	Vn	R_L=8Ω, A-Weighted Filter	–	50	–	μVrms
S/N Ratio	Stereo	SNR	R_L=8Ω, A-Weighted Filter	–	105	–	dB
Channel Separation (L vs R)		CS	R_L=8Ω, 1kHz	–	90	–	dB
PSRR	Stereo	PSRR	PVDD applied, Vripple=200mVpp, f=1kHz	–	70	–	dB
Maximum Efficiency	Stereo	η	R_L=8Ω, Po=10W	–	92	–	%
			R_L=4Ω, Po=10W	–	85	–	%
Output Offset Voltage (Stereo)*2)		Vo	–	–	2	6	mV
Frequency Characteristics		f	20Hz	–1	0	1	dB
			20kHz	–3	0	1	dB

(Note) All analog characteristics were measured by using Yamaha evaluation board. Depending upon pattern layout etc., its characteristics may vary.

*1: The maximum output power when driving 4Ω and 6Ω loads must be 10W or less.

*2: An offset voltage is represented by taking typ. as σ and max. as 3σ.

9. Package Information



注） 1. 表面実装LSIは、保管条件、および、半田付けについての特別な配慮が必要です。
2. 組立工場により、寸法や形状などが異なる場合があります。
詳しくはヤマハ代理店までお問い合わせください。

Note: 1. Special attention needs to be paid to the storage conditions and soldering method of the surface mount IC.
2. Dimension, form, etc. may differ depending on assembly plants.
For details, please contact your local Yamaha agent.

10. Appendix

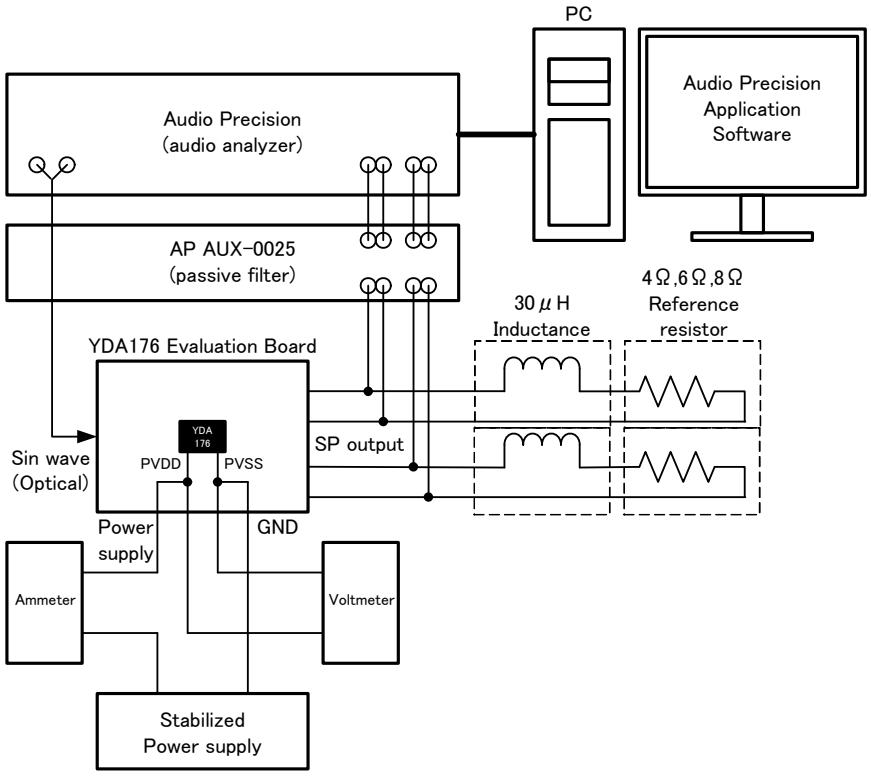
・This chapter describes reference data for user to use this product effectively. Before actual use, please evaluate the product under your use conditions sufficiently.
・The information described in this chapter are not those provided for guaranteeing your product's performance and quality.
・This information is subject to change without notice for improvement etc.

10.1. Various Audio Characteristics

10.1.1 Measurement Environment

Various audio characteristics are measured under the following system using YDA176 evaluation board.

When using an LC filter, a reference resistor of 4Ω, 6Ω, or 8Ω is used as the load resistance.
When not using the filter, a reference resistor of 4Ω, 6Ω, or 8Ω connecting in series with an inductance of 30μH is used as a model of general 15W-class full range speaker.
A digital audio signal for the measurement is directly input into YDA176 Evaluation Board from Audio Precision audio analyzer (2700 series).
YDA176 output signals are sent to the audio analyzer via Audio Precision AUX-0025 (low-pass filter).
In general, AES17 filter is used for audio characteristics measurement.
A-Weighted filter is used for Noise measurement.
A stabilized power supply is used for this power supply.
(Note) *1 : Contact our sales agent for details of the evaluation board.



< Figure 10-1 Audio Characteristics Measurement Environment >

NOTICE The information provided is preliminary, and subject to change without notice.
Please check for the latest information when using this product in your design.

AGENT

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