Osptek Display

TFT LCD SPECIFICATION

Model No:

YDP399B002-V4

1. Introduction

1.1 Scope of application

This specification applies to the LCD module that is supplied by Shenzhen Osprey Optoelectronics Technology Co., Ltd.
LCD specification: Dots 400xRGBx960
As to basic specification of the driver IC, refer to the IC (Sitronix：ST7701SN-G5-1) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

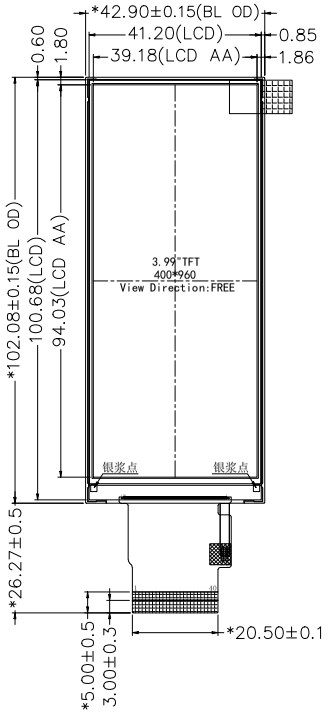
Structure: TFT PANNEL+IC +FPC+BL;
ALL Viewing Type LCD
400 dot-segment and 960 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
3line SPI or 18bit RGB interface

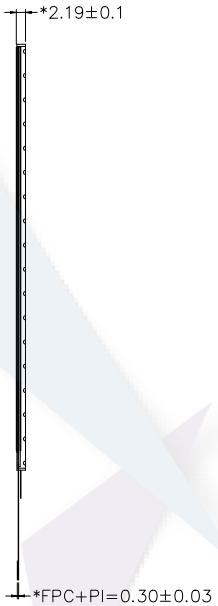
1.3 Applications:

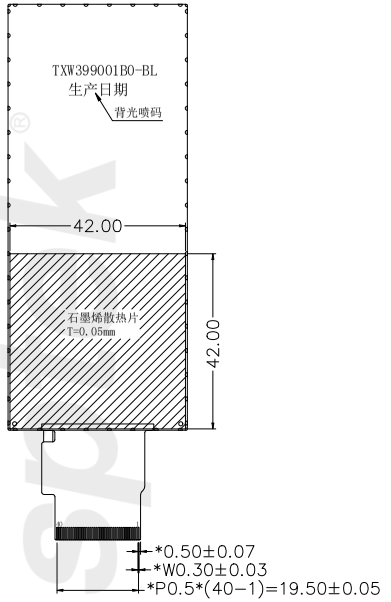
2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	400*3RGB(H)X960(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.108(H) × 0.108(V)	mm
Active area	39.18(H) x 94.03(V)	mm
Viewing direction	ALL Viewing	--
TFT Driver IC	ST7701SN-G5-1	--
TFT interface	3line SPI or 18bit RGB Interface	--
Approx. Weight	TBD	g
Module Size(W*H*T)	42.90(W) ×102.08(H) ×2.19(T)	mm
Touch structure	--	--
Touch Driver IC	--	--
Touch Interface	--	--

REV	DESCRIPTION	DRG DATE	DRAWN BY
00	First Design	2023.08.29	





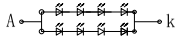


FPC展开出货

1	LEDA
2	LEDK1
3	LEDK2
4	GND
5	VCI 2.8V
6	RESET
7	NC
8	NC
9	SDA
10	SCK
11	CS
12	PCLK
13	DE
14	VSYNC
15	HSYNC
16	DB0
17	DB1
18	DB2
19	DB3
20	DB4
21	DB5
22	DB6
23	DB7
24	DB8
25	DB9
26	DB10
27	DB11
28	DB12
29	DB13
30	DB14
31	DB15
32	DB16
33	DB17
34	GND
35	TP_INT(NC)
36	TP_SDA(NC)
37	TP_SCL(NC)
38	TP_RESET(NC)
39	TP_VCI(NC)
40	GND

NOTES:
1. DISPLAY TYPE: 3.99", 480*960 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: Free
4. DRIVER IC:ST7701SN-G5-1
5. LCM (White 9 AVG 1/9) :
   Brightness: 500cd/m² (TYP)
   Uniformity:80%(MIN)
6. BACK LIGHT: 8 chip white LEDs If=40mA,Vf=22.4V~25.6V
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS

LED CIRCUIT DIAGRAM:



深圳市鱼鹰光电科技有限公司

Mobile: 0755-26810170

PART NO.:	YDP399B002-V4	MODULE NO.:	00
DRAWN BY:	LYH	DATE:	2023.08.29
CHECKED BY:		DATE:	
APPROVED BY:		DATE:	
PROJECTION:			
SCALE:N.T.S	UNIT: mm		
SHEET: 1 OF 1			

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+70	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for(DC/DC)	VCC	2.5	2.8	3.3	V

4.2 Back-Light Unit Characeristics

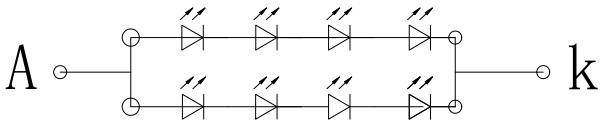
The back-light system is an edge-lighting type with 8 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	22.4	--	25.6	V	--
Forward current	I_F	--	40	--	mA	--
Luminance(With LCD)	Lv	--	500	--	cd/m^2	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	LCM Functional	Notes
1	LEDA	Power supply for backlight anode input terminal.	
2	LEDK1	Power supply for backlight cathode input terminal.	
3	LEDK2	Power supply for backlight cathode input terminal.	
4	GND	Power Ground	
5	VCI 2.8V	Power Supply For LCD.	
6	RESET	Reset signal input terminal. Active at 'L'.	
7	NC	No Connection.	
8	NC	No Connection.	
9	SDA	Serial data input/output pin.	
10	SCK	Serial clock signal.	
11	CS	Chip selection signal.	
12	PCLK	Dot clock signal for RGB interface operation.	
13	DE	Data enable signal for RGB interface operation.	
14	VSYNC	Vertical (Frame) synchronizing input signal for RGB interface operation.	
15	HSYNC	Horizontal (Line) synchronizing input signal for RGB interface operation.	
16	DB0	RGB interface data bus.	
17	DB1	RGB interface data bus.	
18	DB2	RGB interface data bus.	
19	DB3	RGB interface data bus.	
20	DB4	RGB interface data bus.	
21	DB5	RGB interface data bus.	
22	DB6	RGB interface data bus.	
23	DB7	RGB interface data bus.	
24	DB8	RGB interface data bus.	
25	DB9	RGB interface data bus.	
26	DB10	RGB interface data bus.	
27	DB11	RGB interface data bus.	
28	DB12	RGB interface data bus.	
29	DB13	RGB interface data bus.	
30	DB14	RGB interface data bus.	
31	DB15	RGB interface data bus.	
32	DB16	RGB interface data bus.	
33	DB17	RGB interface data bus.	
34	GND	Power Ground	
35	TP-INT(NC)	No Connection.	
36	TP-SDA(NC)	No Connection.	
37	TP-SCL(NC)	No Connection.	
38	TP-RESET(NC)	No Connection.	
39	TP-VCI(NC)	No Connection.	
40	GND	Power Ground	

6. Timing Characteristics

POWER ON/OFF SEQUENCE

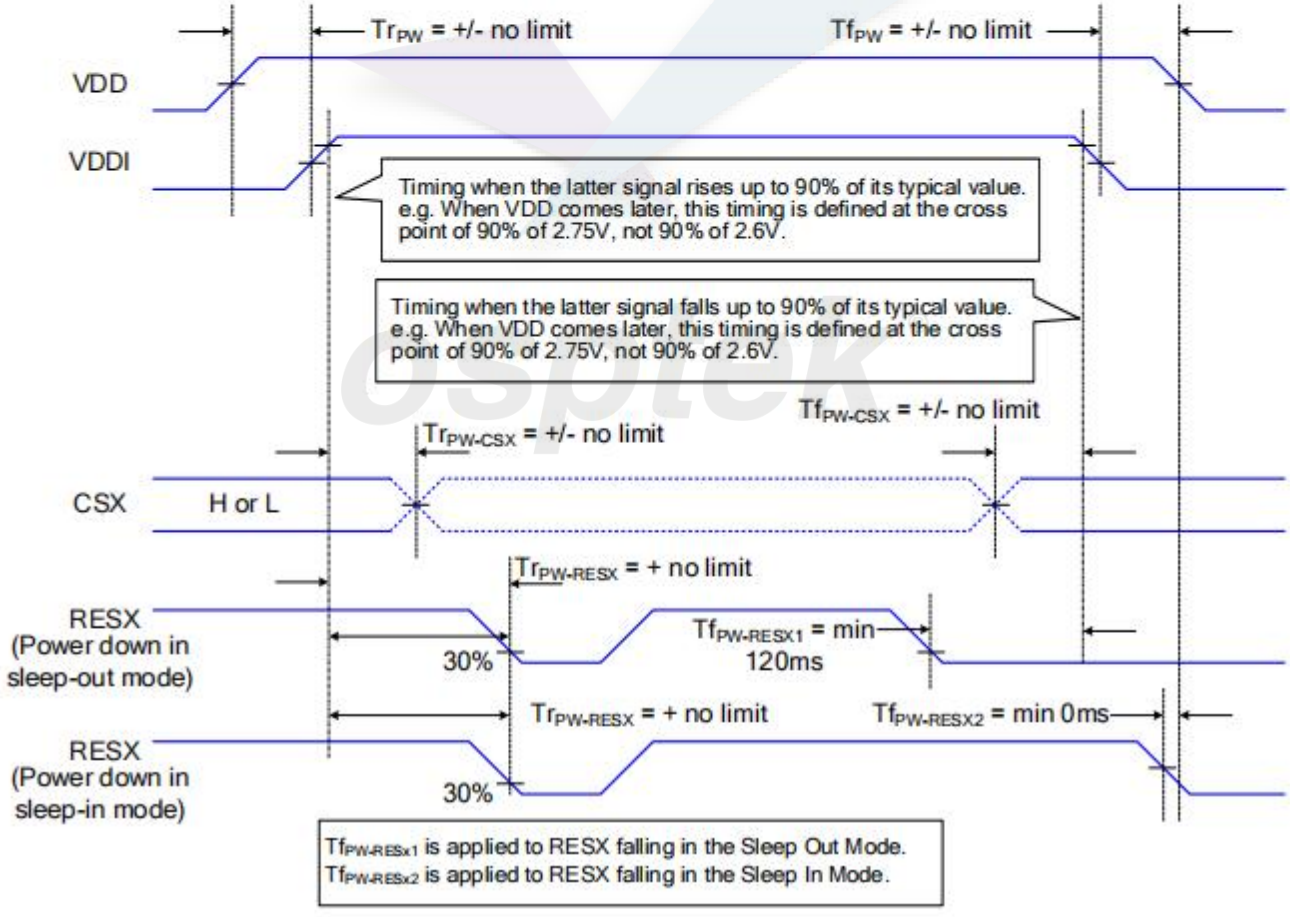
VDDI and VDDA can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec. If the LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after the RESX is released.

CSX can be applied at any timing or can be permanently grounded. RESX has high priority over CSX.

Notes:

1. There will be no damage to the ST7701SN if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.

The power on/off sequence is illustrated below



Serial Interface Characteristics (3-line serial):

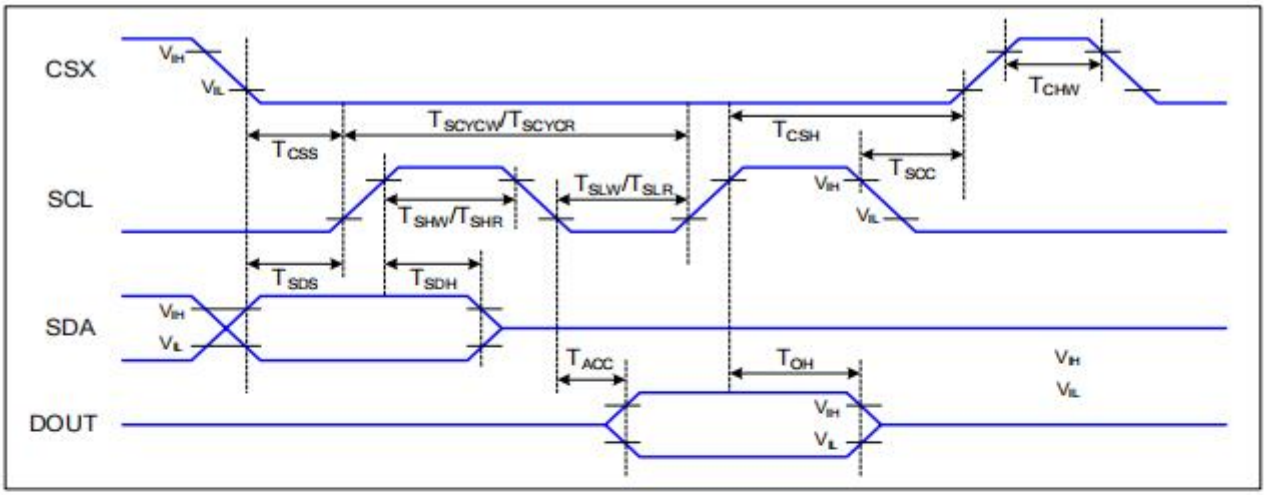


Figure 1 3-line serial Interface Timing Characteristics

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	60		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	

Table 4 3-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

RGB Interface Characteristics :

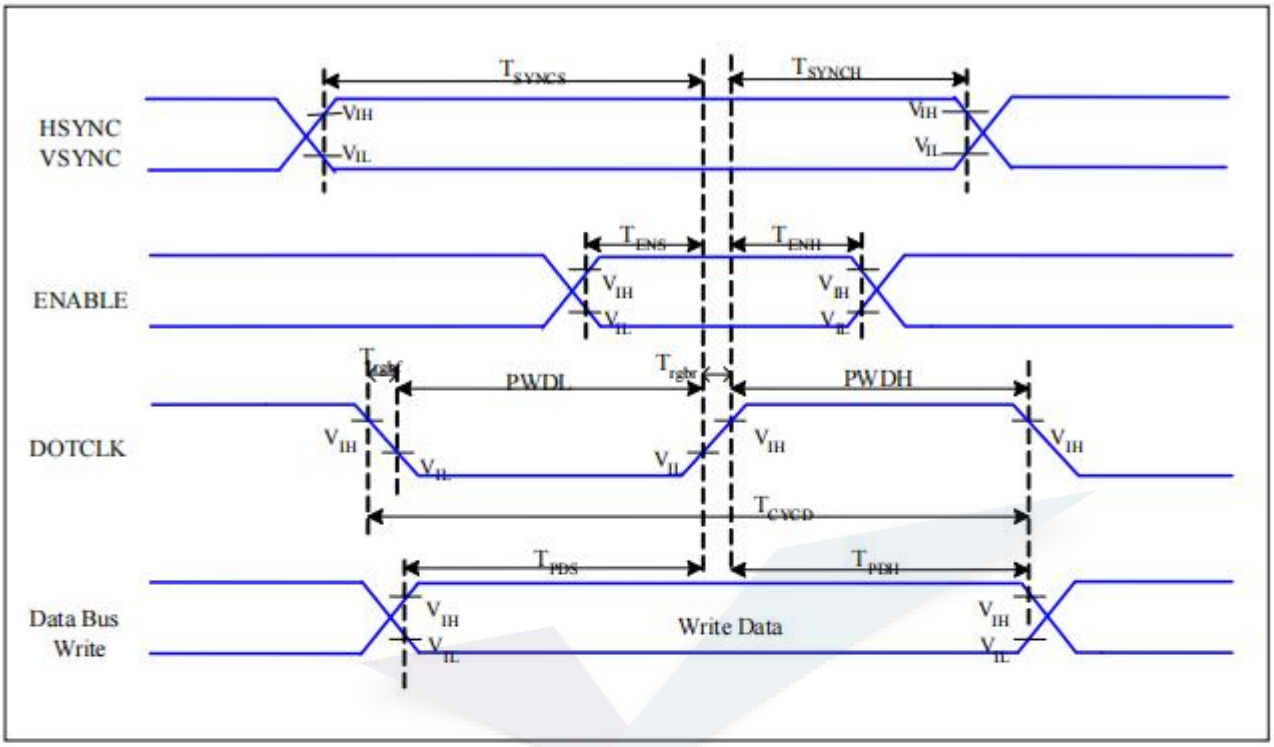


Figure 3 RGB Interface Timing Characteristics

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	5	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	5	-	ns	
	T_{ENH}	Enable Hold Time	5	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	33	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	5	-	ns	
	T_{PDH}	PD Data Hold Time	5	-	ns	

Table 6 18/16 Bits RGB Interface Timing Characteristics

Reset Description:

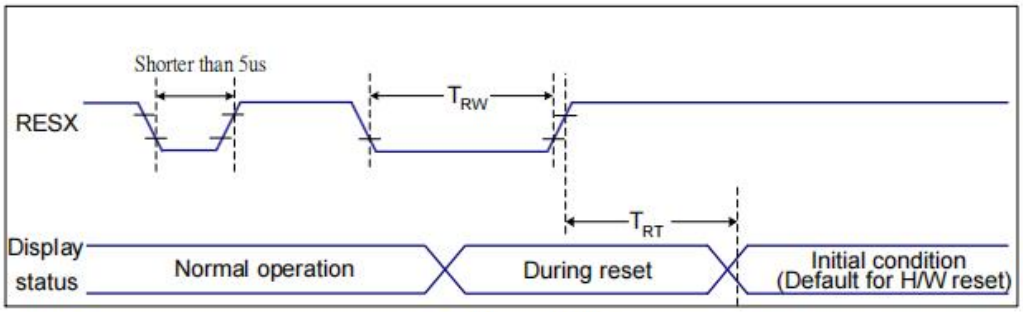


Figure 9 Reset Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

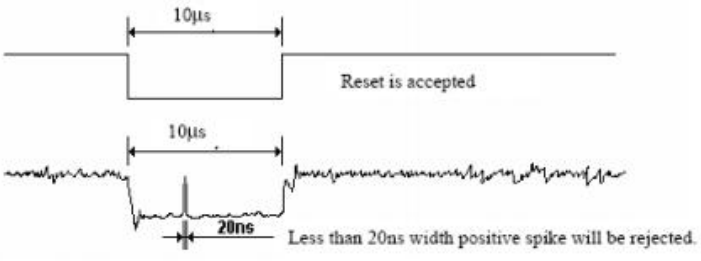
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

Optical Specification

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	80	85	-	Deg.	Note 1
		Θ_9		80	85	-	Deg.	
	Vertical	Θ_{12}		80	85	-	Deg.	
		Θ_6		80	85	-	Deg.	
Contrast ratio		CR	$\Theta = 0°$	550	800	-		Note 2
Transmittance		Tr.		3.34	3.93	-	%	Without APF Note 3
White Chromaticity		x_w		0.277	0.292	0.307		Note 4 CF Glass Base on C Light
		y_w		0.318	0.333	0.348		
Reproduction of color (C light)	Red	R_x						
		R_y						
	Green	G_x						
		G_y						
	Blue	B_x						
		B_y						
Response Time (Rising + Falling)		$T_r + T_f$	Ta= 25° C $\Theta = 0°$	-	35	-	ms	Note 5

Note:

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the Value with Polarizer

4. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

5. The electro-optical response time measurements shall be made as FIGURE 3 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

Figure 1. The Definition of Vth & Vsat

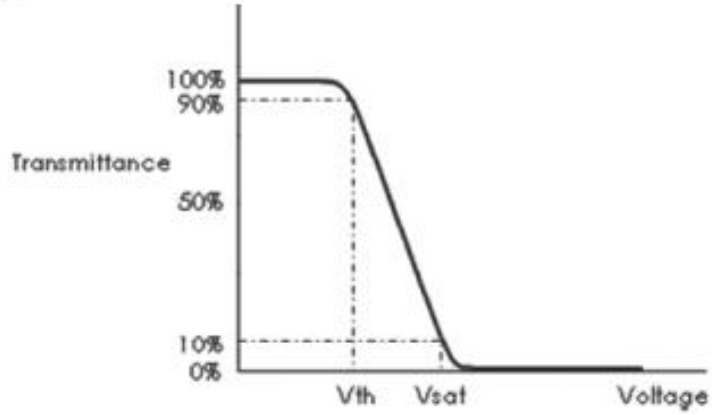


Figure 2. Measurement Set Up

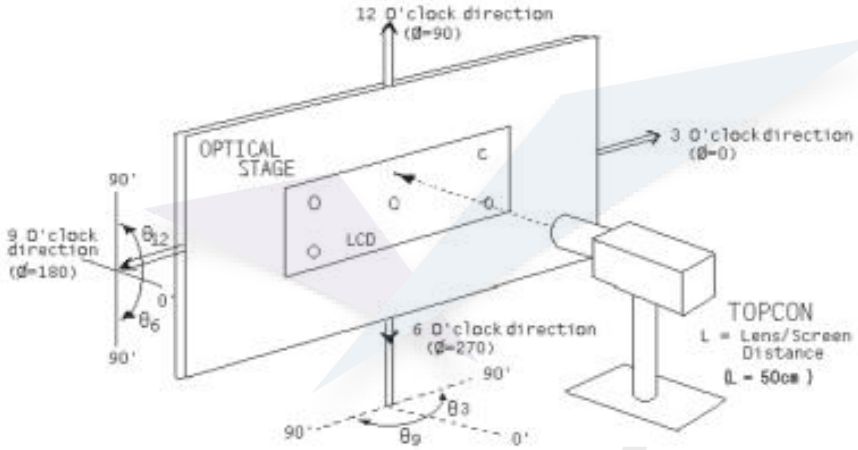
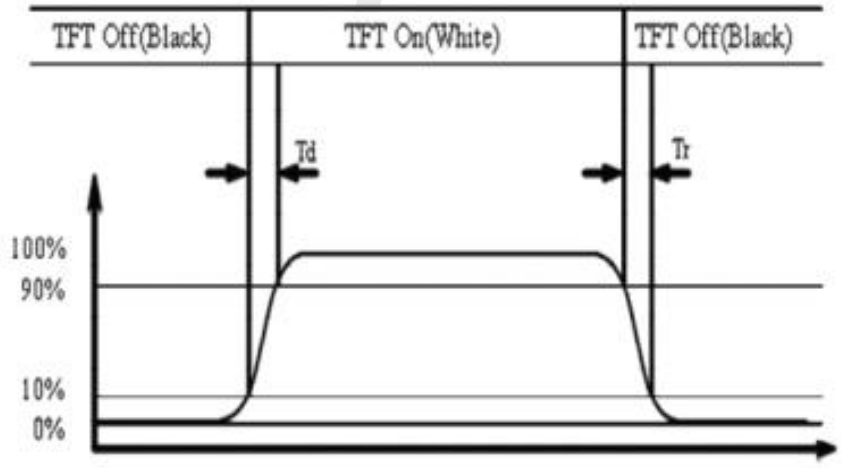


Figure 3. Response Time Testing



8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state，-20℃（30min）~60℃（30min），10 cycles	

9. Packing Method----TBD

- END -