Osptek Display

4.58" TFT LCD SPECIFICATION

Model No:

YDP458B001-V4

1. Introduction

1.1 Scope of application

This specification applies to the LCD module that is supplied by Shenzhen Osprey Optoelectronics Technology Co., Ltd.
LCD specification: Dots 320xRGBx960
As to basic specification of the driver IC, refer to the IC (ST7701S) specification and data book.
All material & processing of the LCD module should be Lead Free.

1.2 TFT features:

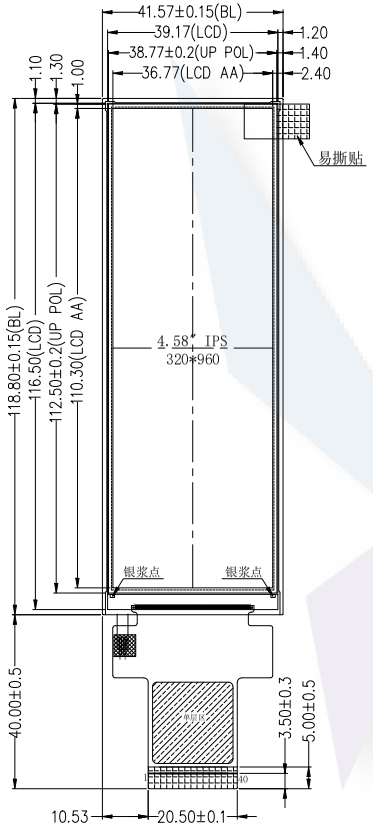
Structure: TFT PANNEL+IC +FPC1+BL;
ALL O'CLOCK Type LCD
320 dot-segment and 960 dot-common outputs;
16.7M Color can be selected by software;
White LED back light;
24RGB interface

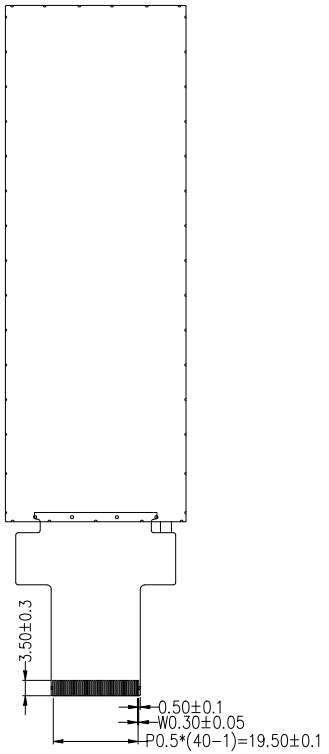
1.3 Applications:

2. LCM General specification

ITEM	Sandard value	Unit
LCD Type	Normally Black	--
Drive element	TFT active matrix	--
Number of pixels	320*3RGB(H)X960(V)	Dots
Pixel arrangement	RGB Vertical Stripe	--
Pixel Pitch (W*H)	0.1149 (H) x 0.1149 (V)	mm
Active area	36.77(H) x 110.30(V)	mm
Viewing direction	ALL O'CLOCK	--
TFT Driver IC	ST7701S	--
TFT interface	24RGB Interface	--
Module Size(W*H*T)	41.57(W) ×118.80(H) ×2.50(T)	mm
Approx. Weight	TBD	g
Touch structure	--	--
Touch Driver IC	--	--
Touch Interface	--	--

REV	DESCRIPTION	DRG DATE	DRAWN BY
	First Desing	2022.04.19	

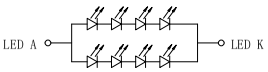




FPC展开出货

NO.	SYMBOL
01	LEDA
02	LEDK
03	VCC(3.3V)
04	GND
05	GND
06	DEN
07	VSYNC
08	HSYNC
09	CLK
10	B7
11	B6
12	B5
13	B4
14	B3
15	B2
16	B1
17	B0
18	G7
19	G6
20	G5
21	G4
22	G3
23	G2
24	G1
25	G0
26	R7
27	R6
28	R5
29	R4
30	R3
31	R2
32	R1
33	R0
34	RESET
35	CS
36	SCL
37	SDA
38	GND
39	VCC(3.3V)
40	GND

NOTES:
1. DISPLAY TYPE: 4.58", 320*960 TFT LCD
2. DISPLAY MODE: transmissive Normally Black
3. VIEWING DIRECTION: ALL
4. DRIVER IC:ST7701S
5. LCM (White 9 AVG 1/9) :
   Brightness: 500cd/m² (TYP)
   Uniformity:80%(MIN)
6. BACK LIGHT:4 chip white LEDs If=40mA,Vf=11.2V-12.8V
7. OPERATING TEMP: -20° C TO 70° C,STORAGE TEMP: -30° C TO 80° C
8. * Critical Parameter,( ) ref Parameter,[ ] cpk Parameter
   Unspecified Tolerances:±0.20mm
   Modification mark:
9. SUGGESTION:TP window size unilateral increase 0.3~0.5mm than LCM A.A
10. REQUIREMENTS ENVIRONMENTAL PROTECTION: RoHS



V=12V If=40mA

深圳市鱼鹰光电科技有限公司

PART NO.:	YDP458B001-V4			MODULE NO.:	00
DRAWN BY:	LYH	DATE:	2022.04.19	PROJECTION:	
CHECKED BY:		DATE:		SCALE:N.T.S	UNIT: mm
APPROVED BY:		DATE:		SHEET: 1 OF 1	

Shenzhen Osprey Optoelectronics Technology Co., Ltd. 0755-26810170 https://www.osptek.com

3.Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit
LCM Operating Temperature	T_{OPR}	-20	+70	°C
LCM Storage Temperature	T_{STG}	-30	+80	°C
Humidity	RH	--	90	%

4.Electrical Characteristics

4.1 TFT DC Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage for I/O	VCCIO	--	--	--	V
Supply Voltage for(DC/DC)	VCC	2.5	3.3	3.3	V
Supply Voltage for(DC/DC)	AVDD	--	--	--	V
Supply Voltage for(DC/DC)	AVEE	--	--	--	V

4.2 Back-Light Unit Characeristics

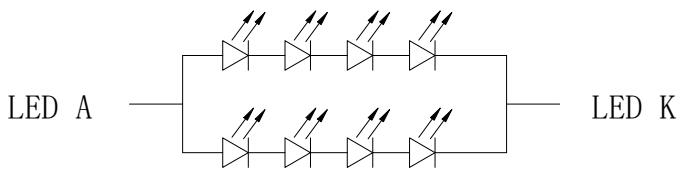
The back-light system is an edge-lighting type with 8 white LEDs. The characteristics of the back-light are shown in the following tables.

Characteristics	Symbol	Min.	Type	Max.	Unit	Notes
Forward Voltage	V_F	11.2	--	12.8	V	--
Forward current	I_F	--	40	--	mA	--
Luminance(With LCD)	Lv	--	500	--	cd/m^2	--
LED life time	N/A	--	30,000	--	Hr	Note 1

Note:

(1) The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20mA/LED. The LED life time could be decreased if operating I_L is larger than 25mA/LED.

Backlight circuit diagram shown in below:



5. Module Function Description

Pin No.	Symbol	Functional	Notes
1	LEDA	POWER SUPPLY+ FOR BACKLIGHT ANODE	
2	LEDK	POWER SUPPLY- FOR BACKLIGHT cathode	
3	VCC(3.3V)	Power supply 2.5V ~ 3.3V	
4~5	GND	Power Ground	
6	DE	Data enable signal in RGB I/F mode 1	
7	VSYNC	Vertical sync. Signal in RGB I/F	
8	HSYNC	Horizontal sync. Signal in RGB I/F	
9	CLK	Pixel clock signal in RGB I/F	
10~17	B7~B0	Blue data	
18~25	G7~G0	Green data	
26~33	R7~R0	Red data	
34	RESET	Reset signal input terminal. Active at 'L'.	
35	CS	A chip select signal	
36	SCL	Serial clock input for SPI interface.	
37	SDA	Serial data input/output pin.	
38	GND	Power Ground	
39	VCC(3.3V)	Power supply 2.5V ~ 3.3V	
40	GND	Power Ground	

6. Timing Characteristics

POWER ON/OFF SEQUENCE

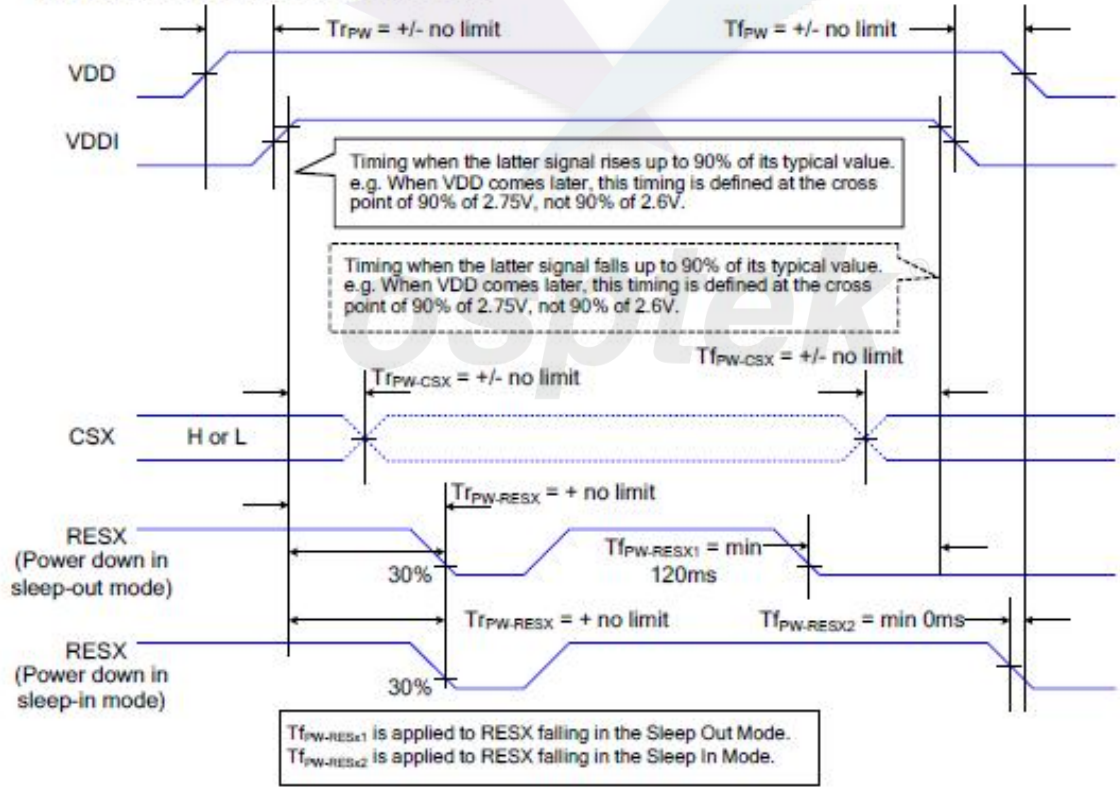
VDDI and VDDA can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec. If the LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after the RESX is released.

CSX can be applied at any timing or can be permanently grounded. RESX has high priority over CSX.

Notes:

1. There will be no damage to the ST7701S if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.

The power on/off sequence is illustrated below



Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until "Power On Sequence" powers it up.

RGB Interface Characteristics :

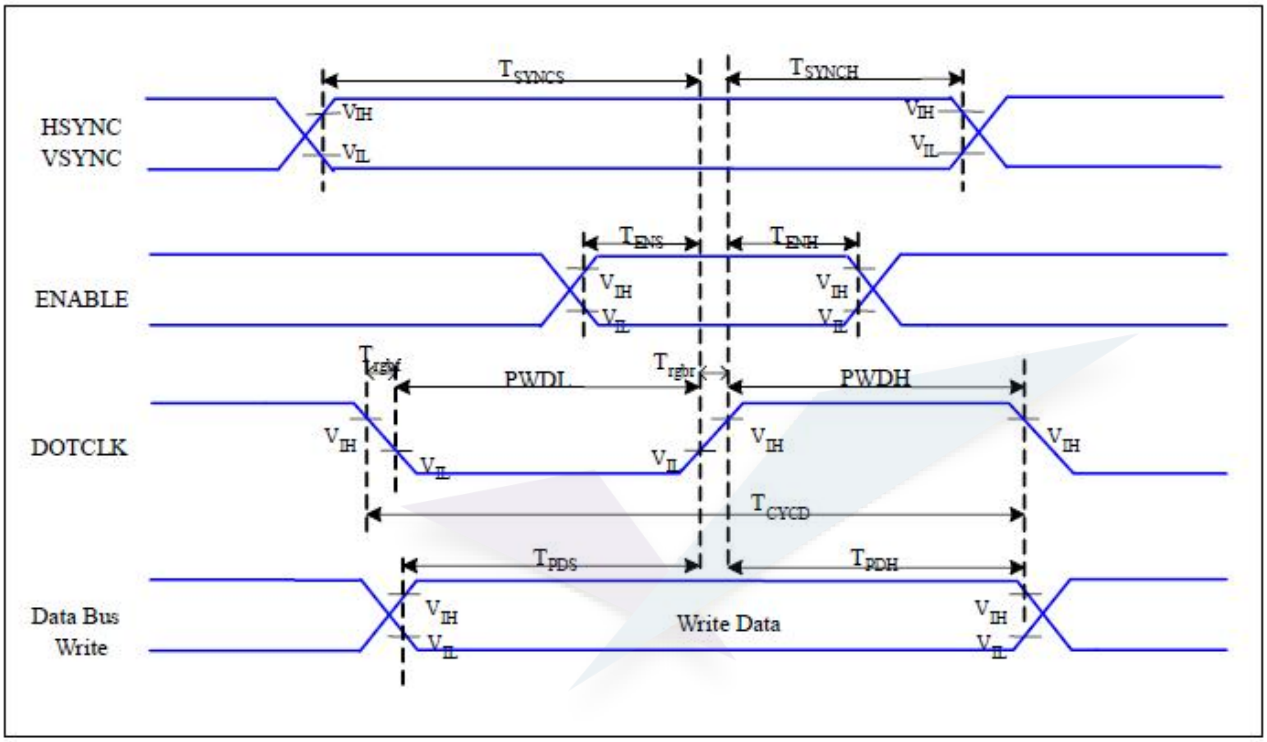


Figure 3 RGB Interface Timing Characteristics

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	5	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	5	-	ns	
	T_{ENH}	Enable Hold Time	5	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	33	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	5	-	ns	
	T_{PDH}	PD Data Hold Time	5	-	ns	

Table 6 18/16 Bits RGB Interface Timing Characteristics

Reset Description:

Reset Timing:

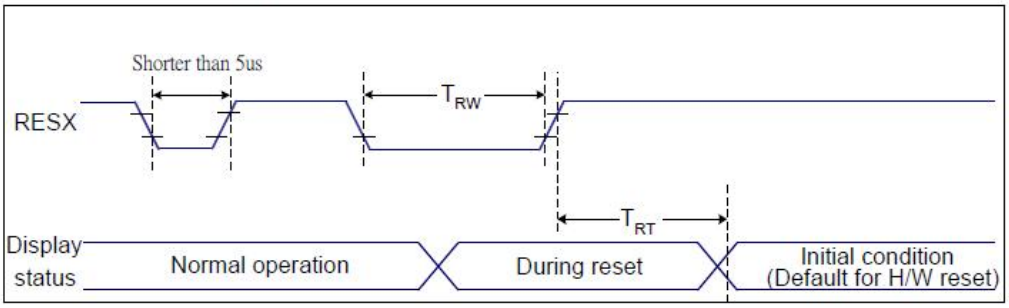


Figure 9 Reset Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

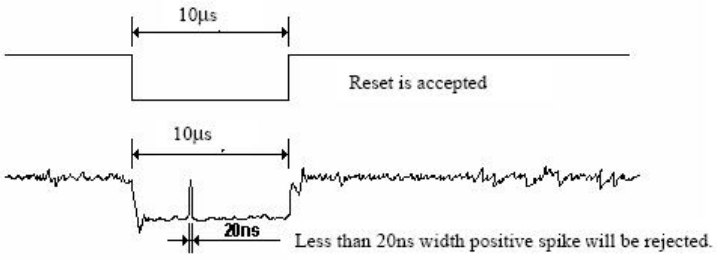
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.Optical Characteristics

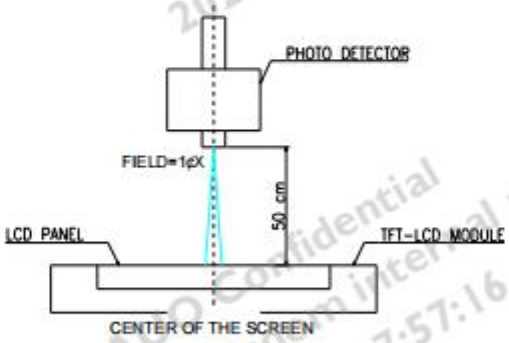
Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time		Tr+Tf	θ=0° Φ=0°	--	25	35	ms	Note 3
Contrast ratio		CR	At optimized viewing	1000	1200	--	--	Note 4
NTSC		%	θ=0°	45	50	--	%	Base on JF LED Silicate F50
Viewing Angle	Top		CR ≧10	70	80	--	deg.	Note 5
	Bottom					--		
	Left					--		
	Right					--		
Transmittance		%	θ=0°	5.75	--		%	Silicate F50 w/o APCF
Crosstalk	%	25℃		--	--	2.0	%	Note 7
Chromaticity	White	X	θ=0°	0.272	0.302	0.332		Base on JF LED Silicate F50
		Y	θ=0°	0.289	0.319	0.349		
	Red	X	θ=0°	0.560	0.590	0.620		
		Y	θ=0°	0.317	0.347	0.377		
	Green	X	θ=0°	0.310	0.340	0.370		
		Y	θ=0°	0.551	0.581	0.611		
	Blue	X	θ=0°	0.123	0.153	0.183		
		Y	θ=0°	0.074	0.104	0.134		

Note 1: Measured under Ambient temperature =25℃±2℃ in the dark room.

Note 2: To be measured on the center area of panel with a viewing cone of 1° by luminance meter, after 15 minutes operation.

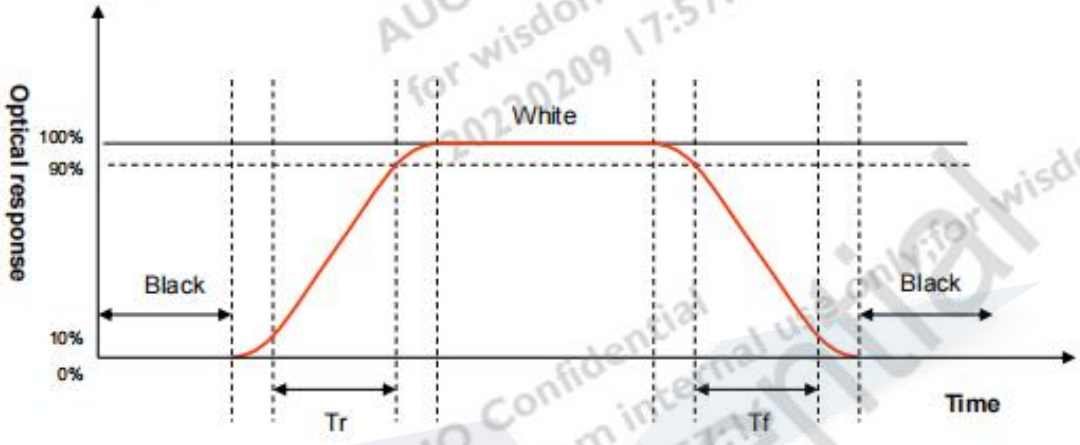


Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are

changed from "black" to "white" (rising time) and from "white" to "black" (falling time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

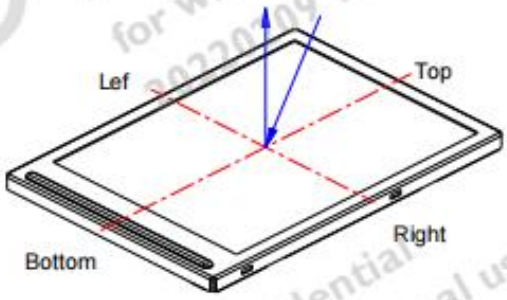


Note 4. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

Note 5. Definition of viewing angle, θ, Refer to figure as below.



Note 6: The spec in table is for reference, different polarizer and APCF would make different performance for it. Transmitace will be adjusted 1st Sample

Note 7: Cross-talk ratio is measuring by follow pattern and formula

8. Reliability Test Item

No.	Test Item	Test Condition	Notes
1	High Temp. Storage	+80°C / 96H	1. Functional test isOK. Missing Segment,short, unclear segment non-display,display abnormally and liquid crystal leakare un-allowed. 2. No low temperature bubbles,end seal loose andfall, frame rainbow.
2	Low Temp. Storage	-30°C / 96H	
3	High Tempe. Operating	+70°C / 96H	
4	Low Tempe. Operating	-20°C / 96H	
5	High Temperature /Humidity storage	50°C x 90%RH /96H	
6	Thermal and cold shock	Static state，-20℃（30min）~60℃（30min），50 cycles	

9. Packing Method----TBD

- END -