YAMAHA LSI

YGV617B

AVDP3

Advanced Video Display Processor 3

■OUTLINE

YGV617B has a built-in PLL circuit which allow to superimpose the images outputted by the device over an external video signals easier.

Since this device has a high speed drawing function and character drawing function and is able to specify vertical and horizontal size of the screen optionally, it is applicable to controlling display units such as a wide screen TV and liquid crystal displays.

These features make this device best suited to uses such as multi-vision display of automobile audio system, display of automobile navigation system, OSD of wide screen TV, video editing equipment and karaoke equipment.

This device has I/O pins for RGB (YUV) data, with which it is also suited to digital video applications such as DVD player and set-top-boxes.

■FEATURES

[Functions]

- Bit map plane is able to display images simultaneously using 16 colors, 256 colors or 32768 colors.
- A sprite is able to use 32 x 32 dots.
- The sprite plane can be used as a crosshair line cursor.
- A monitor synchronization frequency, dot clock frequency and display screen resolution can be specified optionally.
- High resolution display and interlaced scanning can be used.
- All direction smooth scroll (spherical scroll) function can be used.
- Has a built-in color look up table of 256 words x 16 bits, where display colors can be selected from 32768 colors.
- Linear RGB output is obtained with the built-in DAC.
- The built-in PLL circuit enables the device to generate clock signals that is synchronized with external video signals.
- By generating dot clock signals that are synchronized with sub carrier clock signals, the device makes clear image at an optional resolution without misalignment of colors.
- Provides various drawing command functions.

[CPU Interface]

- 16 bit or 8 bit asynchronous interface
- Registers and various I/O ports are mapped on the 16 byte I/O space.
- Video memory up to 2 Mbytes can be mapped directly on the memory space of the system.
- Has a built-in drawing data FIFO, and CPU interrupt function.
- When connected with an external DMA controller, command drawing data can be transferred through DMA.

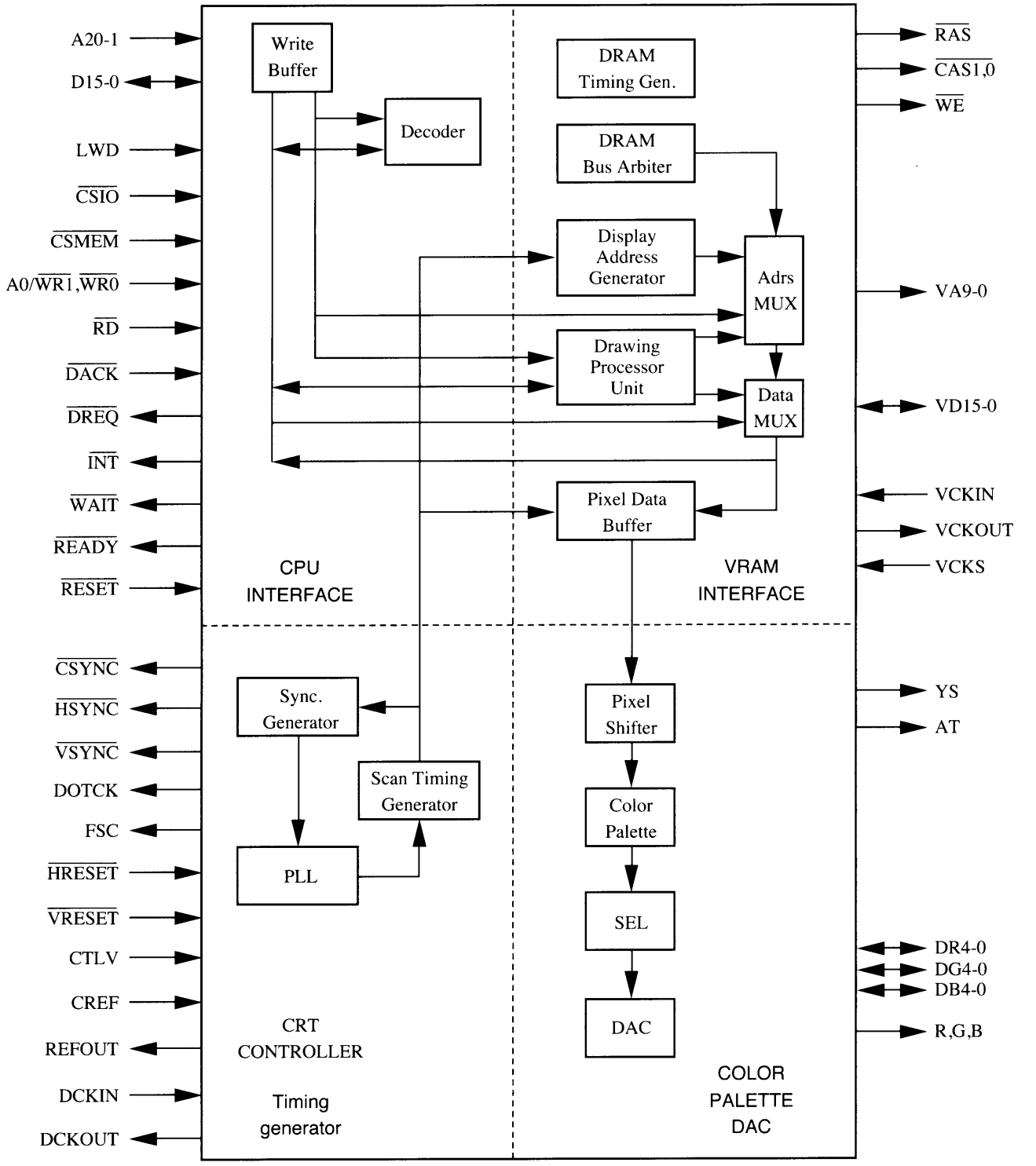
[Other Features]

- One unit of 4 M or 16 M DRAM with 16 bit configuration can be connected.
- Since clock signals for video memory can be inputted in addition to clock signals for display, an access speed that is the most suitable to the DRAM to be connected can be specified.
- The built-in FIFO for display data has reduced overhead at draw data access, achieving high speed drawing.
- Has digital RGB I/O pins, YS pin and attribute output pin.
- 144 pin plastic SQFP.
- CMOS and 5 V single power supply

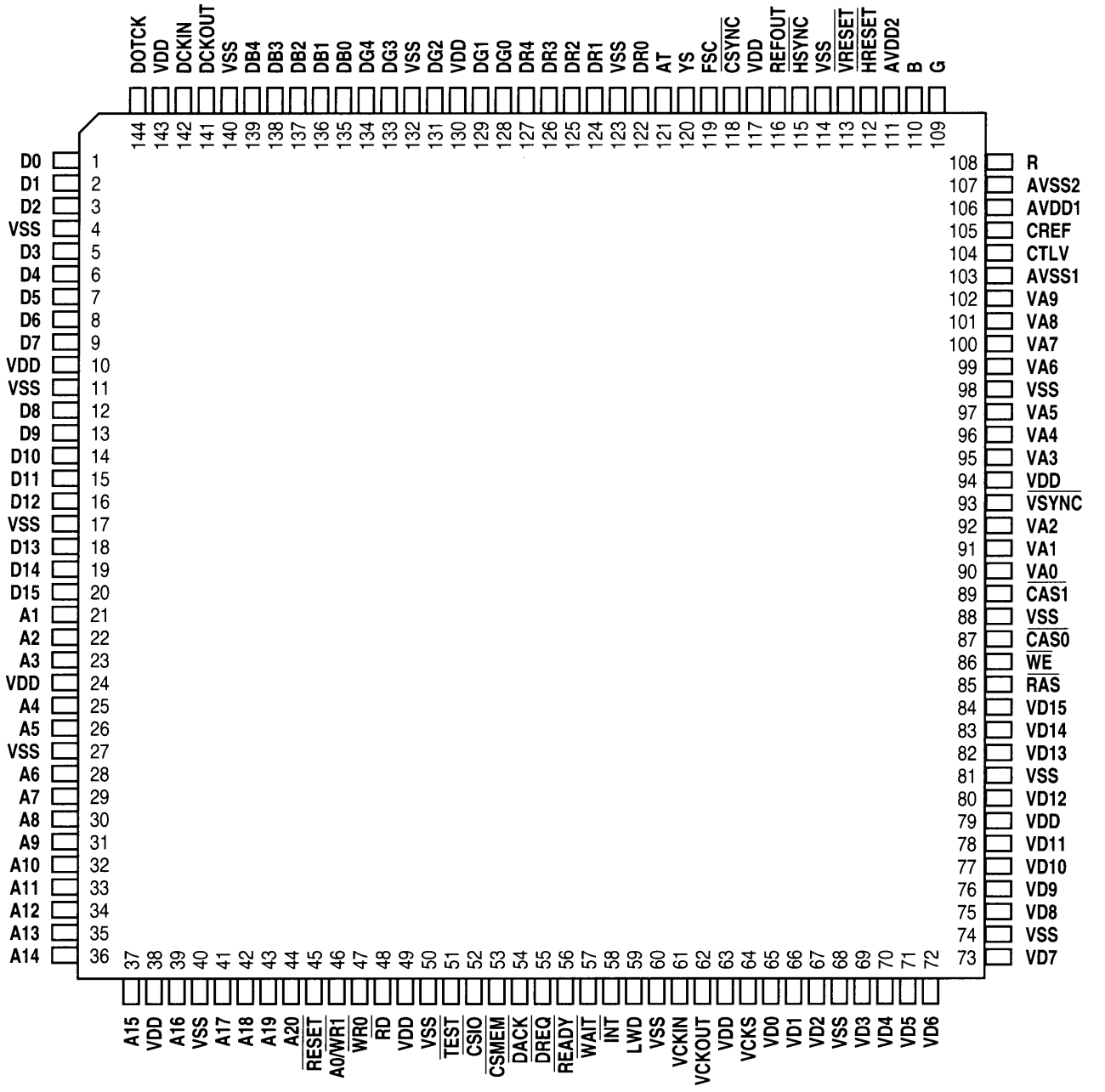
YAMAHA CORPORATION

YGV617B CATALOG
CATALOG No. : LSI-4GV617B2
1998. 1

■BLOCK DIAGRAM



■PIN ASSIGNMENT



TOP VIEW

■PIN FUNCTIONS

<CPU interface>

- D15-0 (I/O : Pull Up)

  These pins comprise a CPU data bus. D15-D8 pins are to be kept open in case of 8 bit CPU that does not use the pins.

- A20-1 (I)

  These pins comprise a CPU address bus. Input to A20-4 pins is ignored when accessing $\overline{\text{CSIO}}$ space. Unused pins are to be pulled up or down.

- $\overline{\text{CSIO}}$ (I)

  This is a chip select signal input for determining I/O space. An I/O port in AVDP3 is accessed by the write/read pulses that are inputted when this signal is active. When the address is inputted with this signal at low level, input to A20-4 pins is ignored.

- $\overline{\text{CSMEM}}$ (I)

  This is a chip select signal input for determining video memory port. Video memory controlled by AVDP3 is directly accessed by the write/read pulses that are inputted when this signal is active. The video memory can also be accessed from I/O space without using this pin if a high level signal is inputted to this pin.

- A0/$\overline{\text{WR1}}$, $\overline{\text{WR0}}$ (I)

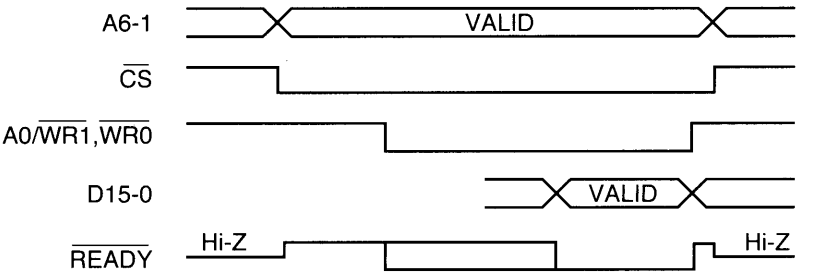
  These signals are used to control writing into AVDP3 when the chip select input is active. A0/$\overline{\text{WR1}}$ controls D15-8, and $\overline{\text{WR0}}$ controls D7-D0.
  In case of 8 bit CPU, A0/$\overline{\text{WR1}}$ functions as the CPU address bit 0.

- $\overline{\text{RD}}$ (I)

  This signal controls reading from AVDP3 when the chip select input is active. D15-0 pins are in output state in the period where both this signal and the chip select signal are active.

- $\overline{\text{READY}}$ (O : Pull Up, 3 state output)

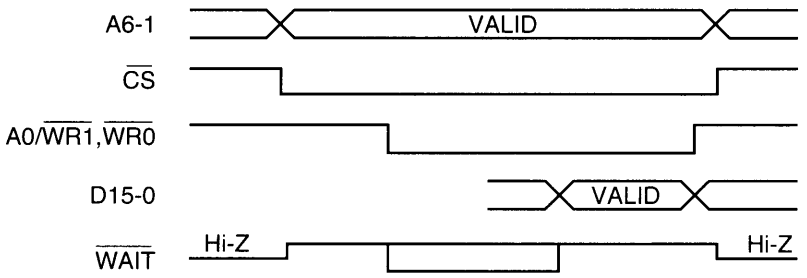
  This is the data ready signal output to CPU. When internal state of AVDP3 becomes accessible, this signal becomes active. This pin becomes high impedance state when $\overline{\text{CSIO}}$ pin or $\overline{\text{CSMEM}}$ pin (hereafter called $\overline{\text{CS}}$ pin) is not active, or this pin outputs high level signal when $\overline{\text{CS}}$ pin is active and $\overline{\text{RD}}$ or A0/$\overline{\text{WR1}}$ and $\overline{\text{WR0}}$ pins are not active.
  Some CPU must use $\overline{\text{WAIT}}$ signal instead of this signal.



State of $\overline{\text{READY}}$ signal at write access

- $\overline{\text{WAIT}}$ (O : Pull Up, 3 state output)

  This is the data wait signal outputted to CPU. When $\overline{\text{CS}}$ pin is active, this pin outputs $\overline{\text{WAIT}}$ signal responding to the $\overline{\text{RD}}$ or A0/$\overline{\text{WR1}}$ and $\overline{\text{WR0}}$ signals, and then clears the $\overline{\text{WAIT}}$ signal when the CPU has become accessible.
  When $\overline{\text{CS}}$ pin is not active, this pin becomes high impedance state.
  When $\overline{\text{CS}}$ pin is active and $\overline{\text{RD}}$ or A0/$\overline{\text{WR1}}$ and $\overline{\text{WR0}}$ pins are not active, the level of this pin becomes high.
  Some CPU must use $\overline{\text{READY}}$ signal instead of this signal.



State of $\overline{\text{WAIT}}$ signal at write access

- $\overline{\text{INT}}$ (O : Open drain output)

  Outputs an interrupt request signal to CPU. This signal becomes active when the internal state of AVDP3 coincides with the conditions set in the registers. It is reset when registers of AVDP3 have been accessed.

- LWD (I)

  This signal selects the width of data bus according to CPU. When high level signal is inputted, this device complies with 16 bit system, or when low level signal is inputted, it complies with 8 bit system.

- $\overline{\text{RESET}}$ (I : Pull Up)

  This pin accepts an initial reset signal. Internal registers of AVDP3 is cleared to "0" when this signal has been inputted. (Some registers are loaded with initial value.) Make sure to input the reset signal at power on.

- $\overline{\text{DREQ}}$ (O)

  Outputs command data request signal to an external DMA controller.

- $\overline{\text{DACK}}$ (I : Pull Up)

  When an external DMA controller has received $\overline{\text{DREQ}}$ signal, it returns command data transfer permit signal to this device through this pin.

<Video Memory Interface>

- VA9-VA0 (O)

  These pins comprise an address bus for VRAM. This bus outputs low address and column address of DRAM used by AVDP3 based on time sharing. This pin becomes high impedance when in VRAM halt state.

- VD15-VD0 (I/O : Pull Up)

  These pins comprise an data bus for VRAM. Data of DRAM used by AVDP3 are transferred through this bus. This pin becomes high impedance when in VRAM halt state.

- $\overline{\text{RAS}}$ (O)

  This pin outputs DRAM row address strobe signals for VRAM. This pin becomes high impedance when in VRAM halt state.

- $\overline{\text{CAS1,0}}$ (O)

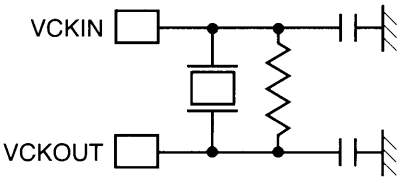
  These pins output DRAM column address strobe signals for VRAM. $\overline{\text{CAS1}}$ and $\overline{\text{CAS0}}$ are respectively related to data buses VD15-8 and VD7-0. These pins become high impedance when in VRAM halt state.

- $\overline{WE}$ (O)

  Outputs DRAM write strobe signal for VRAM. This pin becomes high impedance when in VRAM halt state.

- VCKIN (I), VCKOUT (O)

  Crystal oscillator generates clock for video memory access timing is connected to these pins. This clock is supplied to the blocks including VRAM interface, CPU interface and drawing processor. When low level signal is inputted to VCKS pin, be sure to input a low or high level signal to VCKIN pin. VCKOUT pin may be kept open.



- VCKS (I : Pull Up)

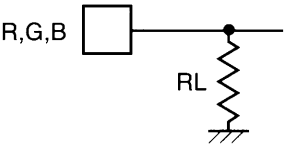
  When clock inputted from DCKIN and DCKOUT pins is used, input low level signal to this pin. VRAM clock and dot clock are generated. In this case, it is not necessary to feed clock into VCKIN pin. When clock inputted from VCKIN and VCKOUT pins is used, VCKS pin may be kept open.

  When the level of this pin is low, it is necessary to input a stable clock into DCKIN pin. Therefore, when clock generated by the built-in PLL is used as dot clock, be careful not to make them unstable.

<Display Monitor Interface>

- R, G, B (O : Analog output)

  These pins output linear red, green and blue signals respectively. Connect a terminating resistor of 390 ohms so that the pin outputs voltage amplitude of 1 Vp-p at the resolution of 5 bit (32 levels).



- DR4-0, DG4-0, DB4-0 (I/O : Pull Up)

  These are I/O pins for digital R, G and B signals respectively.

- $\overline{CSYNC}$ (O)

  Outputs composite synchronization signal for an external monitor. In interlace mode, this pin outputs an equalizing pulse.

- $\overline{VSYNC}$ (O)

  Outputs vertical synchronization signal for an external monitor.

- $\overline{HSYNC}$ (O)

  Outputs horizontal synchronization signal for an external monitor.

- DOTCK (O)

  Outputs clock for transferring display data. The display data changes synchronizing with this clock.

- FSC (O)

  Outputs sub carrier clock for video encoder. This pin is able to output a clock with frequency of 1/1, 1/2, 1/4 or 1/8 of that of DCKIN pin input signal. For example, when the frequency of a signal inputted to DCKIN pin is 14.318 MHz and it is divided by 4, the sub-carrier with frequency of 3.58 MHz is obtained.

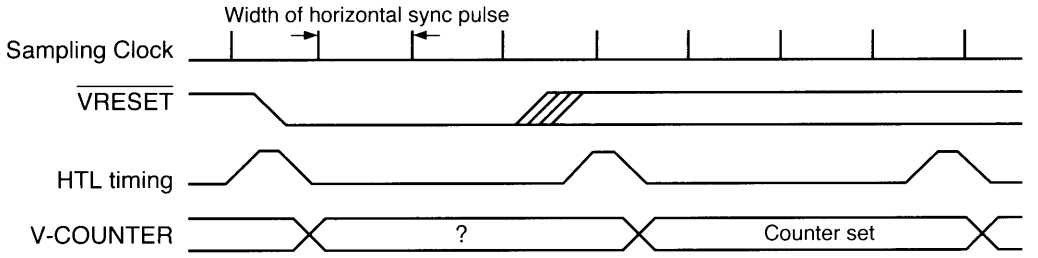
- $\overline{\text{VRESET}}$ (I : Pull Up)

  Resets vertical timing of CRT controller block of AVDP3.

  This input signal is sampled at the cycle equal to pulse width of horizontal synchronization signal. When three low levels have been detected successively, the internal V counter is set at HLT timing (horizontal synchronization signal start timing) immediately after the third low level.

  In interlace mode, current field is identified, and the internal V counter is set into the field where the signal has been inputted. With these operations, the internal counter can be reset at vertical synchronization timing even if composite synchronization signal is inputted to this pin. In case the $\overline{\text{VRESET}}$ is inputted in the display period, the display data in the next one field is not guaranteed.

  This pin may be kept open if this function is not used.



- $\overline{\text{HRESET}}$ (I : Pull Up)

  Resets horizontal timing of CRT controller block of AVDP3. This signal is sampled according to the main clock. The horizontal timing is set to horizontal synchronization start position at fall moment from high level to low level, and at the same time, phase of dot clock is reset.

  When the built-in PLL is operated in the external sync mode, the frequency of dot clock is given by multiplying the frequency of $\overline{\text{HRESET}}$ by the value set in the internal register, and HSYNC signal generated in the CRT control block is locked by $\overline{\text{HRESET}}$ signal.

  In case this signal is inputted in the display period, the display data in the next one line is not guaranteed.

  This pin may be kept open if this function is not used.

- YS (O)

  This signal is used to control switching between the external video signal and an image signal outputted by YGV617 when in superimposing. The reversed signal of YSN bit at the selected address on the Color palette is outputted to this pin. During the border display period, the reversed signal of setting value of border YS data is outputted to this pin.

  In 32768 color display mode, the reversed signal of YS data set in VRAM is outputted to this pin.

- AT (O)

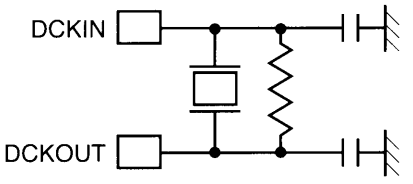
  A bit information of internal registers or that of color palette is outputted to this pin.

- DCKIN (I), DCKOUT (O)

  A reference clock is inputted to these pins when PLL is operated in FSC sync mode. In this case, frequency of the reference clock is four times of fsc.

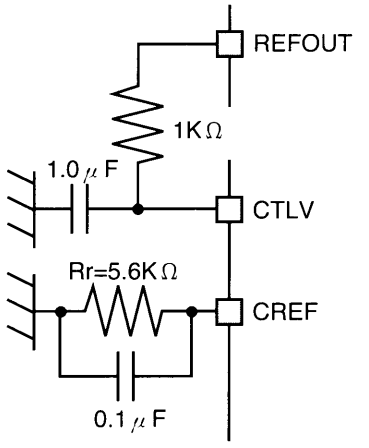
  When PLL function is not used, this inputted clock is supplied to CRTC block and display data control block as it is.

  When a low level signal is inputted to VCKS pin, the clock is supplied also to blocks including VRAM interface, CPU interface and drawing processor.



- CTLV (I), CREF (I), REFOUT (O)

These pins are used to connect external resistors and capacitors when the built-in PLL circuit is used.



Notes:

1. For the circuit between REFOUT and CTLV, the layout should be determined so that the parasitic capacitance is minimizes and no signal interference can occur.
2. For the circuit between CREF and Rr, the layout should be determined so that the parasitic capacitance is minimizes and no signal interference can occur.
3. PLL may fail to lock in case there is a time difference between rise moment of AVDD (for PLL) and rise moment of VDD (for Digital Logic).
4. When PLL is not used , open the REFOUT pin, ground the CTLV pin and pull down the CREF pin using a 5.6 kΩ resistor.

<Other pins>

- TEST (I)

This pin is used for testing. Be sure to keep this pin open in normal operation.

- AVDD1, AVSS1 (I)

These pins supply electric power to analog circuit of AVDP3's built-in PLL section.
+5 V is to be added to AVDD1 pin, and AVSS1 is to be grounded.

- AVDD2, AVSS2 (I)

These pins supply electric power to analog circuit of AVDP3's built-in DAC section.
+5 V is to be added to AVDD2 pin, and AVSS2 is to be grounded.

- VDD, VSS (I)

These pins supply electric power to digital circuit of AVDP3.
+5 V is to be added to VDD pin, and VSS is to be grounded.
AVDP3 has more than two VDD and VSS pins, all of which must be supplied with power. Place a bypass condenser as a noise killer between VDD and VSS as close as possible to these pins.

■ELECTRICAL CHARACTERISTICS

●Absolute maximum ratings

Item	Symbol	Ratings	Unit
Supply voltage	VDD	-0.5～+7.0	V
Input terminal voltage	VI	-0.5～VDD+0.5	V
Output terminal voltage	VO	-0.5～VDD+0.5	V
Output terminal current	IO	-20～+20	mA
Storage temperature	Tstg	-50～+125	℃

●Recommended operating conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDD	4.75	5.00	5.25	V
Supply voltage	VSS		0		V
Low level input voltage (except for DCKIN and VCKIN terminal)	VIL	-0.3		0.8	V
High level input voltage (except for DCKIN and VCKIN terminal)	VIH	2.2		VDD+0.3	V
Low level input voltage (DCKIN and VCKIN terminal)	VIL	-0.3		0.3VDD	V
High level input voltage (DCKIN and VCKIN terminal)	VIH	0.7VDD		VDD+0.3	V
Ambient operating temperature	Top	-40		85	℃

●Electrical characteristics under recommended operating conditions

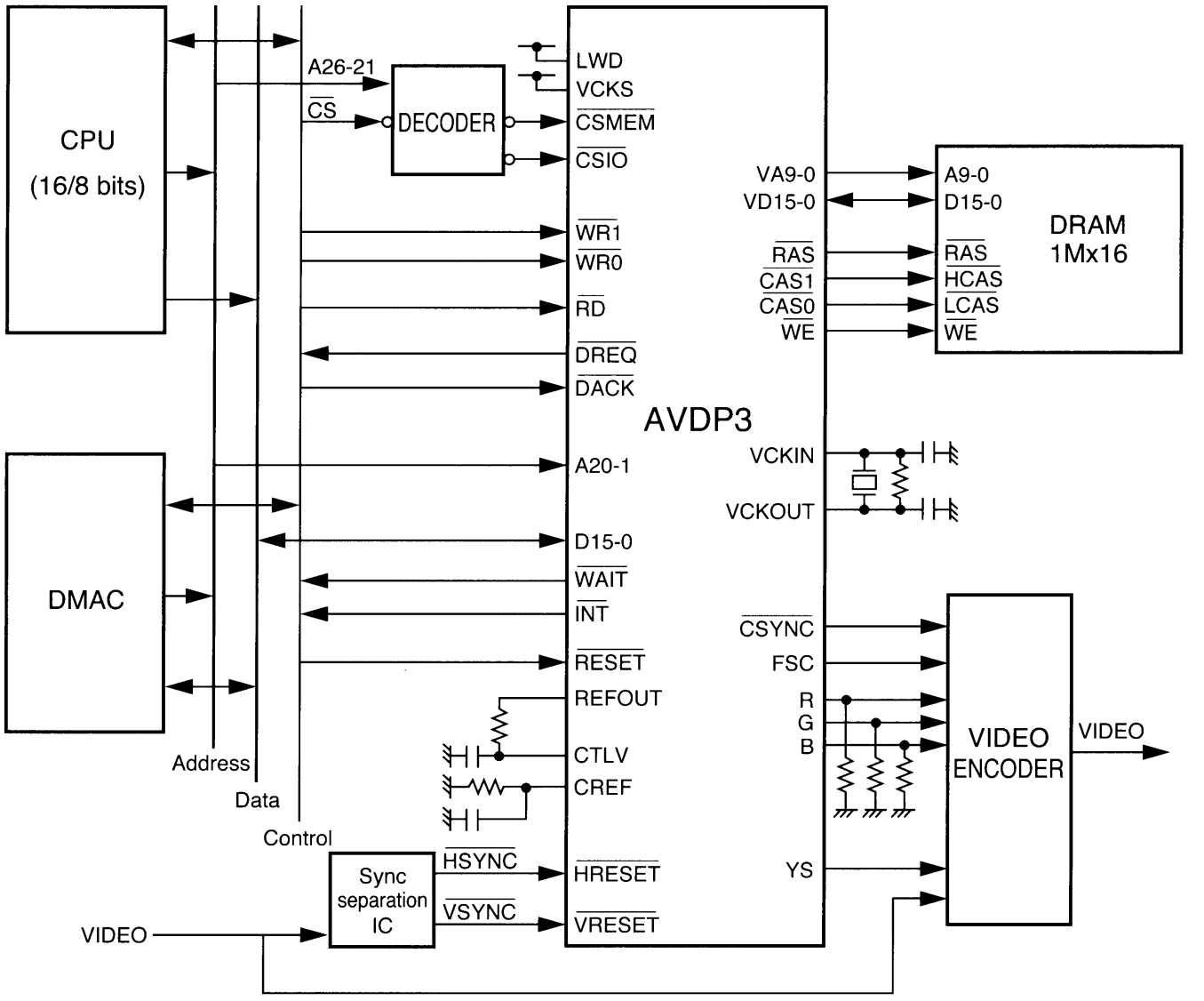
- DC characteristics

Item	Symbol	Measurement condition	Min.	Typ.	Max.	Unit
Low level output voltage (except for OPEN DRAIN terminal)	VOL	IOL=1.6mA			0.4	V
Low level output voltage (OPEN DRAIN terminal)	VOL	IOL=3.2mA			0.4	V
High level output voltage (except for OPEN DRAIN terminal)	VOH	IOH=-1.0mA	4.0			V
Input leakage current	ILI				10	μA
Output leakage current	ILO				25	μA
Power consumption	IDD			60		mA

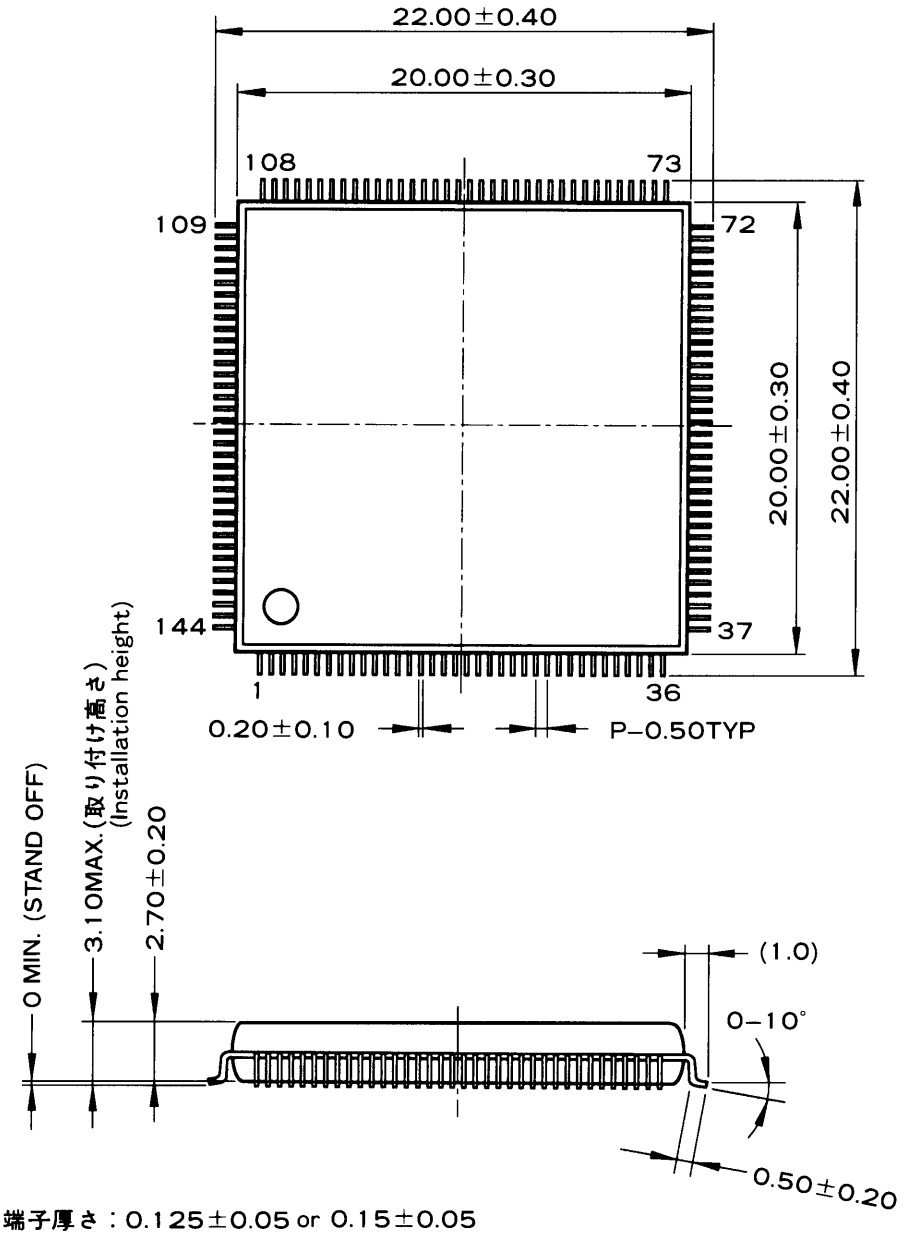
- Terminal capacity

Item	Symbol	Min.	Typ.	Max.	Unit
Input terminal capacity	CI	—	—	8	pF
Output terminal capacity	CO	—	—	10	
Input/Output terminal capacity	CIO	—	—	12	

■SYSTEM CONFIGURATION EXAMPLE



■EXTERNAL DIMENSIONS



端子厚さ：0.125±0.05 or 0.15±0.05
(LEAD THICKNESS)

モールドコーナー形状は、本図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値とする。
モールド外形寸法はバリを含まない。
単位(UNIT)：mm(millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

Note: The LSIs for surface mount need especial consideration on storage and soldering conditions. For detailed information, please contact your nearest agent of yamaha.

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AGENCY

YAMAHA CORPORATION

Address inquiries to:
Semiconductor Sales & Marketing Department

- Head Office: 203, Matsunokijima, Toyooka-mura, Iwata-gun, Shizuoka-ken, 438-0192 Tel. +81-539-62-4918 Fax. +81-539-62-5054
- Tokyo Office: 2-17-11, Takanawa, Minato-ku, Tokyo, 108-8568 Tel. +81-3-5488-5431 Fax. +81-3-5488-5088
- Osaka Office: Namba Tsujimoto Nissei Bldg. 4F 1-13-17, Namba Naka, Naniwa-ku, Osaka City, Osaka, 556-0011 Tel. +81-6-6633-3690 Fax. +81-6-6633-3691
- U.S.A. Office: YAMAHA Systems Technology 100 Century Center Court, San Jose, CA 95112 Tel. +1-408-467-2300 Fax. +1-408-437-8791