YAMAHA LSI

YGV619

AVDP6

Advanced Video Display Processor 6

■ Outline

YGV619 is a VDP (Video Display Processor) adopting OSD display control system which is best suited to the data broadcasting. The digital image interface of this device for connection with MPEG decoder has been improved. The use of this device allows screen composition that is suited to mobile information terminals, car navigation system, etc. Scan timing conforming to the display standard of digital TVs can be made.

Two built-in PLL circuits allows to realize superimposition of external image signal on original image signal, and to produce clock best suited to SDRAM that is adopted as external video memory.

■ Features

- Display planes**:** External digital image is overlaid with OSD images composed of regions.
  Up to four planes, which are individually composed of back drop plane (plane on which external images are inputted) + region, are available.
- OSD image format**:**
  8bit/dot palette mode, and 16 bit RGB or YCbCr format can be selected.
  YCbCr conforms to the conversion method of ITU601.
  Color palette (256 colors in 16777 k colors) can be specified by region.
- Digital image input format**:**
  · 18bitR6G6B6 (Max. dot clock frequency: 80 MHz)
  · 16bitYCbCr422 (Max. dot clock frequency: 80 MHz)
  · 8bitITU656 (Dot clock frequency 27 MHz)
- Digital image output format**:**
  · R6G6B6 + 2 bit AT
  · 18bitYCbCr444 + 2 bit AT
  · 16bitYCbCr422 + 2 bit AT
  · 8bitITU656 + 2 bit AT + 6 bit α blending coefficient
- Max. OSD resolution**:** 960 dots × 1080 lines
  (However, max. resolution of overlaid external image is 1920 ×1080 lines)
- Applicable digital TV image format**:**
  · 525i
  · 525p
  · 1125i
- Video capture function**:**
  · Draws external image input on the frame memory in real time.
  · Can convert resolution.
  · Provided with progressive scanning conversion

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YGV619 CATALOG
CATALOG No.: LSI-4GV619A1
2001.01

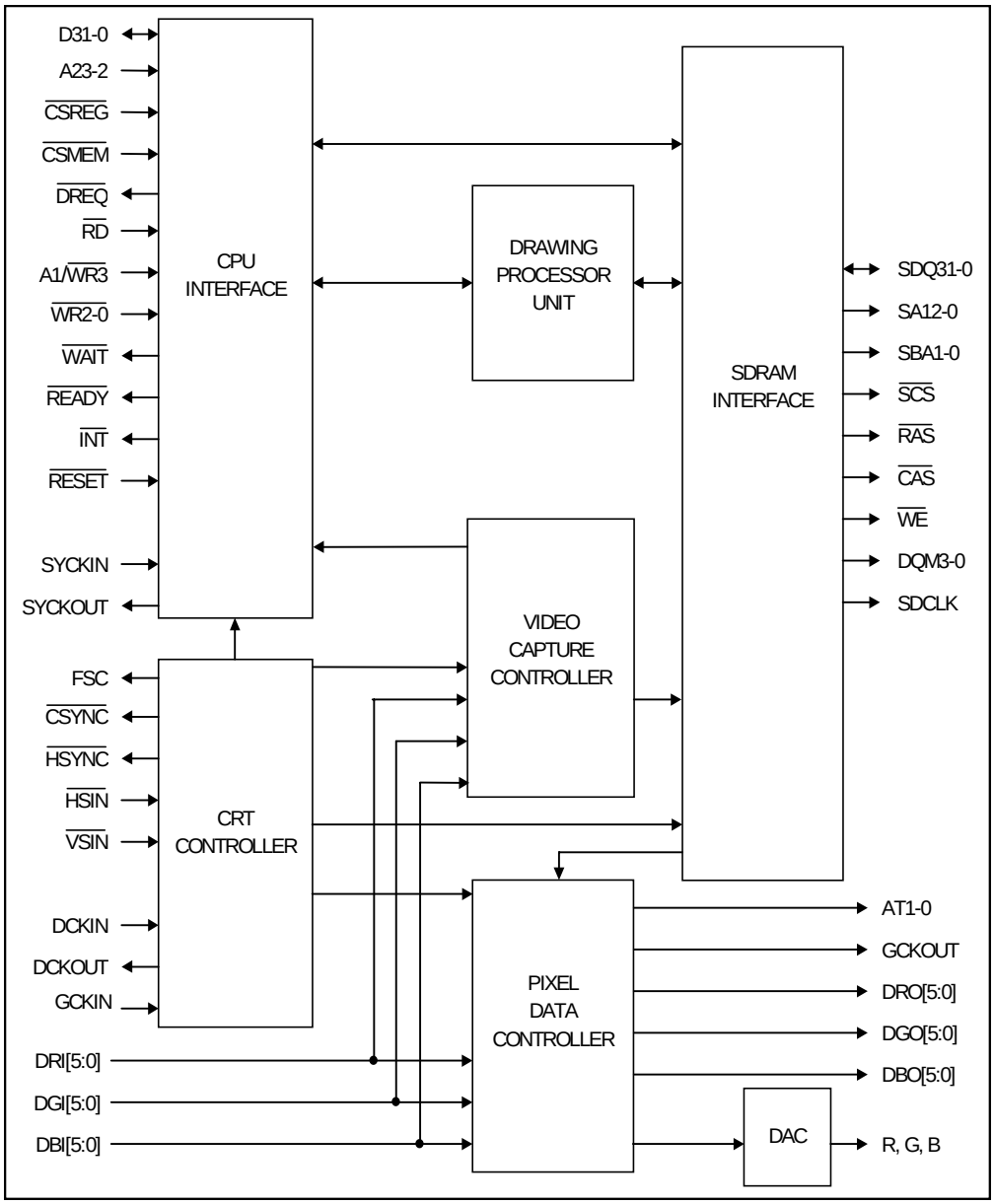
- Priority of display planes
  Regular priority: Plane D > Plane C > Plane B > Plane A > Back drop plane
  The priority can be changed by region.
- α blending function (64 intensity level)
  Blending weight can be set by dot.
- Flicker cancel filter is built in.
  Enabling / disabling flicker cancel function can be set by region.
- 8 bit DACs are built in for R, G and B individually. (Max. operating frequency: 80 MHz)
- Two PLLs are built in. (1: Generates SDRAM clock and system clock 2: Generates dot clock)
- Display monitor control
  · Display resolution and scanning frequency can be set optionally.
  This function is compatible with progressive scanning and interlaced scanning modes.
  NTSC subcarrier output
- SDRAM can be added externally as VRAM (SDRAM generation clock frequency: Max. 80 MHz.)
  ·16 bit bus
  512k words × 16 bits × 2 banks × 1 pc. (capacity: 2M bytes)
  1M words × 16 bits × 4 banks × 1 pc. (capacity: 8M bytes)
  2M words × 16 bits × 2 banks × 1 pc. (capacity: 8M bytes)
  ·32 bit bus
  512k words × 16 bits × 2 banks × 2 pcs. (capacity: 4M bytes)
  512k words × 32 bits × 4 banks × 1 pc. (capacity: 8M bytes)
  1M words × 16 bits × 4 banks × 2 pcs. (capacity: 16M bytes)
  2M words × 16 bits × 2 banks × 2 pcs. (capacity: 16M bytes)
- CPU interface
  Compatible with 16/32 bit CPU. Various built-in tables can be mapped on CPU space.
  Compatible with little endian and big endian
- Package: 240SQFP (YGV619-S)
- Operating temperature range: -45 to +85°C
- Power supply: 3.3V, single power supply

Supplementary information:
For YGV619, Application Manual that details the specifications of the device and the evaluation board (MSY619DB01) are available in addition to this brochure.
The evaluation board is equipped with an SDRAM of 16 MB as a video memory. A high performance system can be realized when it is used with Hitachi's CPU board, Super H Solution Engine.

The device driver provided by Yamaha and attached to the evaluation board consists of the main body of the driver and API related layers, allowing the user to build it into the system easily according to the environment.
For the details of these products, inquire of the sales agents or our business offices.

For CPU board, inquire of: Hitachi ULSI Systems Co., Ltd.
Tel:+81-42-351-6600

■ Block Diagram



AVDP6 performs parallel processing including operation of writing display data into video memory (SDRAM) connected on the local bus (drawing function) and operation of sequentially reading bit map image stored in the video memory in accordance with monitor scanning (display function).

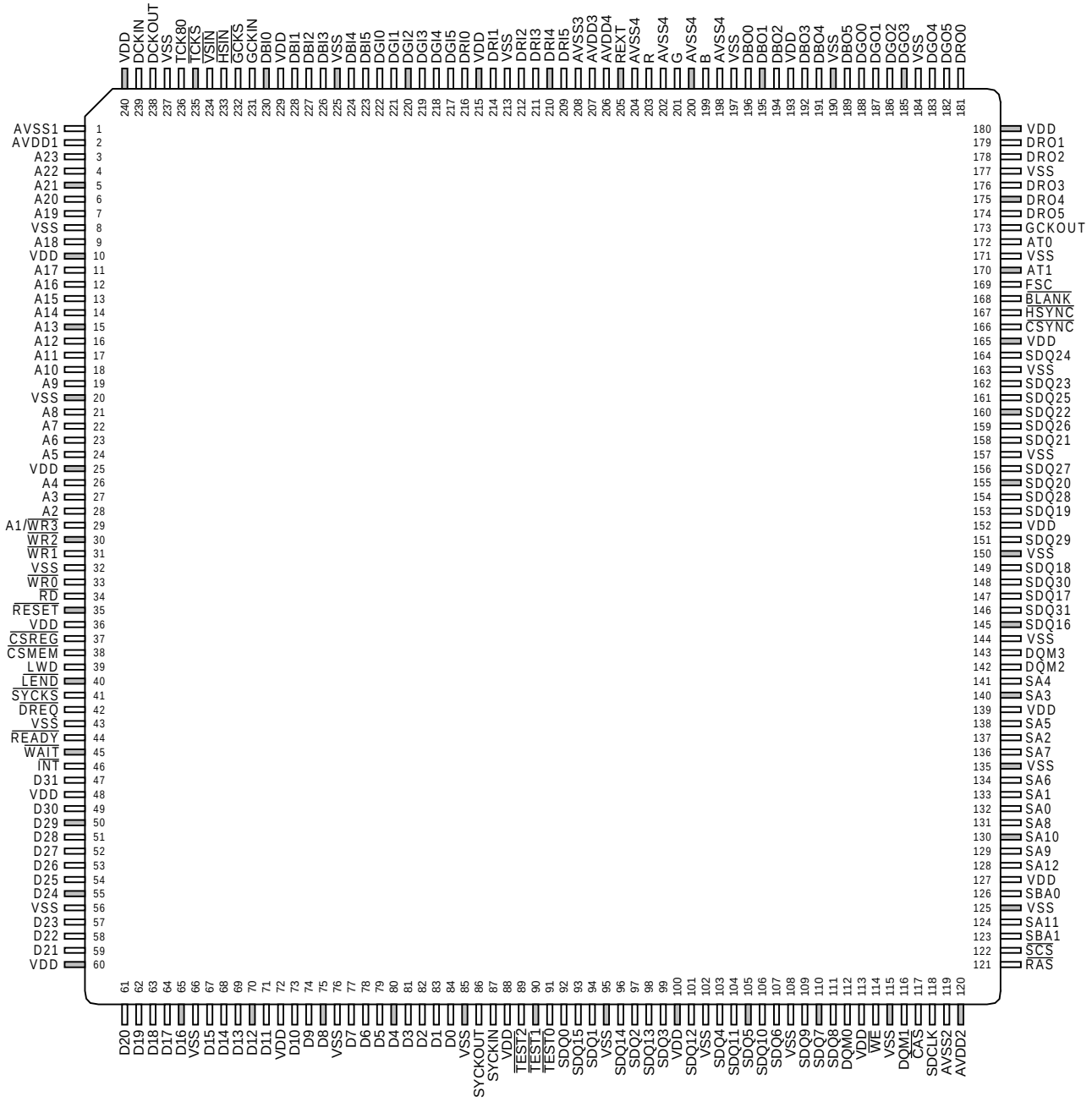
Drawing function**:**

This function transfers bit map image data configured on the external memory of CPU to video memory. For the transfer of the data, a method that maps the video memory as external memory managed by CPU and performs the transfer as the transfer between external memories of CPU, or a method that uses internal drawing processor of AVDP6 to configure the display image on the video memory can be used.

Display function**:**

This function displays the bit map image stored in the video memory in accordance with the display parameters that are stored in the internal registers of AVDP6 and the video memory. Basically, AVDP6 automatically sends out display data and refreshes SDRAM once initial setting for internal registers are completed. When performing dynamic processing such as scroll, the processing that synchronizes with the scanning of AVDP6 can be performed easily by using internal flag polling of AVDP6 or interrupt function.

■ Pin Assignment



Top view

■ Pin Functions

< CPU INTERFACE >

- **D31-0 (I/O: Pull Up)**

CPU data bus. D31-16 pins are not used for 16 bit CPU (LWD=0). These pins are provided with a pull-up resistor. Unused pins are to be open.

- **A23-8 (I: Pull Up), A7-2 (I)**

CPU address bus. When accessing $\overline{\text{CSREG}}$ space, signals inputted to A23-8 pins are ignored without regarding to the bus width of CPU. Internal registers are selected depending on the state of signals inputted to A7-2 for 32 bit CPU or A7-2 and A1 / $\overline{\text{WR3}}$ pin for 16 bit CPU. Systems that control AVDP6 only with $\overline{\text{CSREG}}$ do not use this address bus. However, A23-8 pins must be open because they are provided with pull-up resistor. All the addresses are valid when accessing $\overline{\text{CSMEM}}$ space.

- **$\overline{\text{CSREG}}$ (I)**

Chip select signal input to REG space. Internal registers of AVDP6 are accessed by a using write / read pulse that is inputted when the chip select signal is active.

When this signal is low, inputs to A23-8 pins are ignored.

- **$\overline{\text{CSMEM}}$ (I)**

$\overline{\text{CSMEM}}$ is made active when directly mapping the video memory connected to local bus of AVDP6 on the memory space of CPU. The video memory managed by AVDP6 is directly accessed using write / read pulse that is inputted with this chip select signal is active. The video memory can be accessed from REG space without using this pin, however, high level signal must be inputted to $\overline{\text{CSMEM}}$ in this case.

- **LWD (I: Pull Up)**

Selects a CPU data bus width. When high level signal is inputted to this pin, AVDP6 operates as CPU 32 bit device, or when low level signal is inputted to this pin, AVDP6 operates as CPU 16 bit device.

- **A1 / $\overline{\text{WR3}}$, $\overline{\text{WR2-0}}$ (I)**

Controls write access to AVDP6 when chip select input signal is active. A1 / $\overline{\text{WR3}}$ control D31-24, $\overline{\text{WR2}}$ controls D23-16, $\overline{\text{WR1}}$ controls D15-8, and $\overline{\text{WR0}}$ controls D7-0.

For 16 bit CPU, A1 / $\overline{\text{WR3}}$ function as A1 of CPU address. $\overline{\text{WR2}}$ is not used, and thus must be open because the pin is provided with a pull-up resistor.

- **$\overline{\text{RD}}$ (I)**

Controls read access to AVDP6 when chip select input signal is active. D31-0 pins are in output state while this signal and chip select signals are active. For 16 bit CPU, only D15-0 pins are in output state and D31-16 pins are in input states at all times.

- **$\overline{\text{WAIT}}$ (O: Pull Up, 3-state output)**

Data wait signal output to CPU. When $\overline{\text{CSREG}}$ pin or $\overline{\text{CSMEM}}$ pin (hereafter called "$\overline{\text{CS}}$ pin") is active, the $\overline{\text{WAIT}}$ signal is asserted once for $\overline{\text{RD}}$ or A1 / $\overline{\text{WR3}}$ and $\overline{\text{WR2-0}}$ signals, and then negated when AVDP6 becomes accessible. This pin becomes high impedance state when $\overline{\text{CS}}$ pin is not active, and outputs high level signal when $\overline{\text{CS}}$ pin is active and $\overline{\text{RD}}$ or A1 / $\overline{\text{WR3}}$ and $\overline{\text{WR2-0}}$ pins are not active. Use this pin or $\overline{\text{READY}}$ depending on the type of CPU.

- **$\overline{\text{READY}}$ (O: Pull Up, 3-state output)**

Data ready signal output to CPU. When AVDP6 becomes accessible, this signal is asserted. This pin becomes high impedance state when $\overline{\text{CS}}$ pin is not active, outputs high level signal when $\overline{\text{CS}}$ pin is active and $\overline{\text{RD}}$ or A1 / $\overline{\text{WR3}}$, $\overline{\text{WR2-0}}$ pins are not active. Use this pin or $\overline{\text{WAIT}}$ depending on the type of CPU.

- **$\overline{\text{INT}}$ (O)**

Interrupt request signal output to CPU. This pin becomes active when internal state of AVDP6 coincides with the setting conditions of the registers, and is reset when internal registers of AVDP6 are accessed.

● **$\overline{\text{DREQ}}$ (O)**

DMA request. This pin is asserted when AVDP6 becomes a state where it can accept the DMA transfer. The DMA transfer should be performed using regular $\overline{\text{WRn}}$ and $\overline{\text{RD}}$ pins. (Use Dual Address Mode of DMAC)

● **$\overline{\text{RESET}}$ (I: Schmidt input)**

Initial reset signal input. Inputting this signal clears the internal registers of AVDP6 to initialize the internal state of the device. (Some registers are loaded with initial value.)

● **$\overline{\text{LEND}}$ (I: Pull Up)**

Selects an endian of CPU. Big endian is selected when this pin is at high level, or little endian when the level is low.

● **$\overline{\text{SYCKS}}$ (I: Pull Up)**

Input high level to this pin or leave it open (because it is provided with pull-up resister) when clock inputted through DCKIN and DCKOUT pins are used as a system clock. VRAM clock and dot clock are generated from DCKIN. At this time, supply of clock to SYCKIN pin is not needed. Input low level signal to this pin when input clock from SYCKIN and SYCKOUT pins are used.

< SDRAM interface >

● **SDQ31-0 (I/O)**

Data bus for SDRAM. AVDP6 uses these pins for data input/out access to SDRAM. The data bus width for SDRAM can be set to 32 bits or 16 bits by using the register setting. SDQ31-16 pins are not used when SDRAM bus width of 16 bits is used. At this time, SDQ31-16 pins are in output state at all times.

● **SA12-0 (O)**

Address bus for SDRAM. This bus uses time-sharing method to output row address and column address of SDRAM used by AVDP6.

● **SBA1-0 (O)**

Outputs access bank of SDRAM and ACTIVE command at the same time.

SA12-0 and SBA1-0 pins output the signals as shown below depending on the type of SDRAM.

VRM	SBA1	SBA0	SA12	SA11	SA10	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
0	-	BA	-	-	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
	-	BA	-	-	-	-	-	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
1	BA1	BA0	-	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
	BA1	BA0	-	-	-	-	-	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
2	-	BA	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
	-	BA	-	-	-	-	-	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
3	-	BA	-	-	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
	-	BA	-	-	-	-	-	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
4	BA1	BA0	-	-	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
	BA1	BA0	-	-	-	-	-	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
5	BA1	BA0	-	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
	BA1	BA0	-	-	-	-	-	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
6	-	BA	RA12	RA11	RA10	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
	-	BA	-	-	-	-	-	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0

VRM shows the setting value of R#03:VRM[2:0]. Upper row shows the states of the pins when Active command is issued, and lower column shows the state when Read/Write command is issued.

● **$\overline{\text{SCS}}$ (O)**

Outputs chip select signal for SDRAM. A command is issued to SDRAM when this signal is active. When two 16 bit SDRAMs are used, connect this pin to both SDRAMs.

- **$\overline{\text{RAS}}$ (O)**

Outputs row address strobe signal for SDRAM.
When two 16 bit SDRAMs are used, connect this pin to both SDRAMs.

- **$\overline{\text{CAS}}$ (O)**

Outputs column address strobe signal for SDRAM.
When two 16 bit SDRAMs are used, connect this pin to both SDRAMs.

- **$\overline{\text{WE}}$ (O)**

Outputs write strobe signal for SDRAM.
When two SDRAMs are used, connect this pin to both SDRAMs.

- **DQM3-0 (O)**

Outputs data mask signal for SDRAM. DQM3, DQM2, DQM1 and DQM0 are mask control signals for SDQ31-24, SDQ23-16, SDQ15-8 and SDQ7-0 respectively. When masking the data, corresponding DQM pin outputs high level signal.
When one 16 bit SDRAM is used, DQM3-2 pins are not used, thus they are to be kept open.

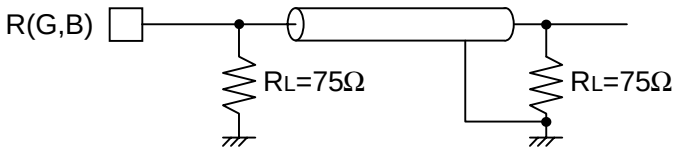
- **SDCLK (I/O)**

Outputs CLK for SDRAM. SDCLK inputs the clock once outputted from this pin to use it as fetch clock to obtain setup time at SDQ input.

< Display monitor interface >

- **R, G, B (O: analog output)**

Outputs linear RGB signal. Termination resistor of 37.5Ω is connected to this pin to make the resolution of output voltage amplitude 8 bits. Monitor with impedance of 75Ω can be driven directly through this interface as shown below.



- **REXT (I: analog input)**

A resistor is connected between this pin and GND(AVSS4) for adjusting the amplitude of signal outputted from DAC for RGB. The standard amplitude of signal outputted from DAC is 0.7 V (rREXT=470 Ω). The amplitude of the output can be adjusted finely within around ±100Ω by using the following formula.

$$Vp\_p = 470 \times 0.7 / rREXT$$

- **$\overline{\text{CSYNC}}$ (O)**

Outputs composite sync signal for external monitor. In interlaced scanning mode, equalizing pulses are added to this signal. This pin can output $\overline{\text{VSYNC}}$ by using internal register setting.

- **$\overline{\text{HSYNC}}$ (O)**

Outputs horizontal sync signal for external monitor.

- **$\overline{\text{BLANK}}$ (O)**

Outputs a signal that indicates effective display period when LCD panel is connected to the device.

- **AT1-0 (O)**

AT1-0 bits of display data are outputted from these pins.

- **FSC (O)**

Outputs subcarrier clock for video encoder. The subcarrier clock is created by dividing the clock inputted to DCKIN pin by 1, 2, 4, or 8, which is determined by register setting. For example, inputting 14.318 MHz to DCKIN pin and dividing it by “4” give subcarrier clock of 3.58 MHz.

● **DRO5-0, DGO5-0, DBO5-0 (O)**

Outputs digital image signal. The output data format can be set to 18 bit RGB, 16 bit YCbCr(ITU601) or ITU656(8bit) by using R_YRT[1:0] and R_DOF[1:0].

16 bit YCbCr and image data for ITU656 are outputted as described below.

18bit RGB	16 bit YCbCr	ITU656(8bit)
DRO[5]	n.c.	α [6]
DRO[4]	n.c.	α [5]
DRO[3]	CO[7]	α [4]
DRO[2]	CO[6]	α [3]
DRO[1]	CO[5]	α [2]
DRO[0]	CO[4]	α [1]
DGO[5]	CO[3]	α [0]
DGO[4]	CO[2]	n.c.
DGO[3]	CO[1]	n.c.
DGO[2]	CO[0]	n.c.
DGO[1]	YO[7]	DO[7]
DGO[0]	YO[6]	DO[6]
DBO[5]	YO[5]	DO[5]
DBO[4]	YO[4]	DO[4]
DBO[3]	YO[3]	DO[3]
DBO[2]	YO[2]	DO[2]
DBO[1]	YO[1]	DO[1]
DBO[0]	YO[0]	DO[0]

n.c.: Stands for “no connection”.

● **GCKOUT (O)**

Outputs clock for digital image signal output. The state of the digital image signal changes synchronizing with this clock. Maximum frequency of the clock is 80 MHz

< External video input >

- **$\overline{\text{VSIN}}$ (I: Pull Up)**

Resets vertical timing function of AVDP6. When this input signal is sampled at intervals equivalent to the width of horizontal sync pulse signal and low level is detected three times consecutively, this pin resets the internal V counters at HTL (time where horizontal sync signal starts). This function makes it possible to reset internal V counter synchronizing with vertical sync signal when composite sync signal is inputted to this pin. At the same time, this function automatically identifies fields in interlaced scanning mode.

- **$\overline{\text{HSIN}}$ (I: Pull Up)**

Resets horizontal timing function of AVDP6. AVDP6 samples the input signal synchronizing with the main clock and sets horizontal scanning time to the horizontal sync start position at the moment the signal falls from high level to low level, and at the same time, adjust the phase of division clock to $\overline{\text{HSIN}}$.

- **DRI5-0, DGI5-0, DBI5-0 (I: Pull Up)**

Digital image signal input pin. This pin becomes valid when internal register R_EIE is "1". The input data format can be set to 18 bit RGB, 16 bit YCbCr(ITU601) or ITU656(8bit) depending on the value of internal register R_EIF[1:0].

Input a signal to individual pins as shown below in accordance with the input data format.

18 bit RGB	16 bit YCbCr	ITU656(8bit)	
DRI[5]	not use	SDI[7]	Data for capture
DRI[4]	not use	SDI[6]	
DRI[3]	CI[7]	SDI[5]	
DRI[2]	CI[6]	SDI[4]	
DRI[1]	CI[5]	SDI[3]	
DRI[0]	CI[4]	SDI[2]	
DGI[5]	CI[3]	SDI[1]	
DGI[4]	CI[2]	SDI[0]	
DGI[3]	CI[1]	$\overline{\text{SHSIN}}$	HSIN for capture
DGI[2]	CI[0]	$\overline{\text{SVSIN}}$	VSIN for capture
DGI[1]	YI[7]	BDI[7]	Data for BG
DGI[0]	YI[6]	BDI[6]	
DBI[5]	YI[5]	BDI[5]	
DBI[4]	YI[4]	BDI[4]	
DBI[3]	YI[3]	BDI[3]	
DBI[2]	YI[2]	BDI[2]	
DBI[1]	YI[1]	BDI[1]	
DBI[0]	YI[0]	BDI[0]	
$\overline{\text{HSIN}}$	$\overline{\text{HSIN}}$	$\overline{\text{HSIN}}$	HSIN for BG
$\overline{\text{VSIN}}$	$\overline{\text{VSIN}}$	$\overline{\text{VSIN}}$	VSIN for BG

- **GCKIN (I)**

Clock for external video input is inputted to this pin.

This pin is valid only when $\overline{\text{GCKS}}$ pin is low. Maximum frequency of this signal is 80 MHz.

- **$\overline{\text{GCKS}}$ (I: Pull Up)**

When external image input signal is present, low level signal is inputted to $\overline{\text{GCKS}}$ pin so that the GCKIN pin input is used as the video capture clock. When data are displayed on the back drop plane, this signal can be used as dot clock by using register setting.

When no external image signal is not present, the clock inputted through DCKIN and DCKOUT pins can be used as GCK by making $\overline{\text{GCKS}}$ open state or high level. In this case, be sure to input a fixed signal to GCKIN pin.

< PLL >

- **DCKIN (I), DCKOUT (O)**

XTAL connection pins for generating dot clock. The dot clock is used by sync control, display control and screen composition blocks. By using the built-in PLL, dot clock with various frequencies that synchronizes with the clock of DCKIN pin can be generated. When $\overline{\text{SYCKS}}$ pin is brought to high level, system clock is generated together with dot clock from input clock of DCKIN pin.

Dot clock can be generated from input clock of DCKIN pin in accordance with the setting of the built-in registers, however, it is necessary to input some clock to DCKIN pin. (DCKIN pin is used to input initialization clock.)

- **SYCKIN (I), SYCKOUT (O)**

XTAL connection pins for generating system clock. This clock is supplied to SDRAM interface, CPU interface, drawing processor, and video capture blocks individually. When making $\overline{\text{SYCKS}}$ pin open or high level, input a fixed signal to SYCKIN pin. SYCKOUT pin can be left open.

Externally oscillated clock, if used, should be inputted to SYCKIN.

< Power supply >

- **AVDD1 (I), AVSS1 (I)**

Supplies power to PLL (PLLDCK) for dot clock. Connect 3.3 V to AVDD1 and GND level to AVSS1.

When designing the circuit board, take care so that the noise from the lines that supply power to other power supply pins of AVDP6 does not enter these pins.

- **AVDD2 (I), AVSS2 (I)**

These pins supply power to PLL (PLLVCK) for system clock. Connect 3.3 V to AVDD2 and GND level to AVSS2. When designing the circuit board, take care so that the noise from the lines that supply power to other power supply pins of AVDP6 does not enter these pins.

- **AVDD3 (I), AVSS3 (I)**

Use these pins to supply power to the digital circuit of the build-in 8 bit DAC. Connect 3.3 V to AVDD3 and GND level to AVSS3. When designing the circuit board, take care so that the noise from the lines that supply power to other power supply pins of AVDP6 does not enter these pins.

- **AVDD4 (I), AVSS4 (I)**

Use these pins to supply power to the analog circuit of the build-in 8 bit DAC. Connect 3.3 V to AVDD4 and GND level to AVSS4. When designing the circuit board, take care so that the noise from the lines that supply power to other power supply pins of AVDP6 does not enter these pins.

- **VDD (I), VSS (I)**

These pins supply power to digital circuits and I/O section. Connect 3.3 V to VDD and GND level to VSS. When designing the circuit board, take care so that the noise from the lines that supply power to other power supply pins of AVDP6 does not enter these pins.

< Others >

- **$\overline{\text{TEST2-0}}$, $\overline{\text{TCKS}}$, TCK80 (I)**

Input pins for testing. Input high level signal for regular operations of the device.

■ Electrical Characteristics

Note!
The values of electrical characteristics shown in this section are target data, and do not guarantee the specifications at the shipment of this product. The specification data may be changed without prior notice. Therefore, please confirm the newest data when using this product.

● Absolute maximum ratings

Items	Symbol	Ratings	Unit
Supply Voltage	V_{DD}[*1]	–0.5 to +4.6	V
Input Voltage[*2]	V_I[*1]	–0.5 to V_{DD}+ 0.5	V
Input Voltage[*3]	V_I[*1]	–0.5 to 5.5	V
Output Voltage[*2]	V_O[*1]	–0.5 to V_{DD}+ 0.5	V
Output Current	I_O	–20 to +20	mA
Storage temperature	T_{stg}	–50 to +125	°C

[*1]: Value with respect to V_{SS} (GND) = 0V
[*2]: for no-tolerant pins
[*3]: for tolerant pins

● Recommended operating conditions

Items	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}[*1]	3.0	3.3	3.6	V
Low Level Input Voltage[*2]	V_{IL}[*1]	–0.3		0.8	V
High Level Input Voltage[*2]	V_{IH}[*1]	2.0		V_{DD}+ 0.3	V
Low Level Input Voltage[*3]	V_{IL}[*1]	–0.3		0.3V_{DD}	V
High Level Input Voltage[*3]	V_{IH}[*1]	0.7V_{DD}		V_{DD}+ 0.3	V
Low Level Input Voltage[*4]	V_{IL}[*1]	–0.3		0.8	V
High Level Input Voltage[*4]	V_{IH}[*1]	2.0		5.5	V
Ambient operating temperature	T_{OP}	–45		+85	°C

[*1]: Value with respect to V_{SS} (GND) = 0V
[*2]: when signal is inputted to I/O pins except DCIKN, SYCKIN and tolerant
[*3]: DCIKN, SYCKIN pins
[*4]: for tolerant pins

● Electrical characteristics under recommended operating conditions

● DC characteristics

Items	Symbol	Min.	Typ.	Max.	Unit
Low level output voltage (CMOS)	V_{OL}[*1]			0.4	V
High level output voltage (CMOS)	V_{OH}[*2]	2.4			V
Input leakage current	I_{LI}			10	µA
Output leakage current	I_{LO}			25	µA
Current consumption	I_{DD}				mA

[*1]: Measurement condition I_{OL}=100µA
[*2]: Measurement condition I_{OH}=-100µA

● Pin Capacitance

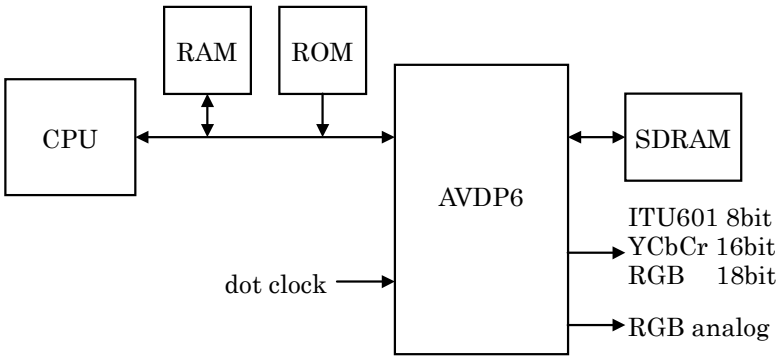
Items	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	C_I			8	pF
Output Pin Capacitance	C_O			10	pF
I/O Pin Capacitance	C_{IO}			12	pF

■ Example of System Configuration

AVDP6 is a display control device that operates as 16 bit or 32 bit I/O device on the external general purpose bus of CPU on the system in which the device is built-in. Because CPU I/F of AVDP6 uses asynchronous I/F, it can be controlled with general purpose SRAM I/F. SDRAM is connected on the local bus of AVDP6 to be used as video memory. The timing for this SDRAM is made by AVDP6 independently. In the SDRAM, bit map image and palette data that are displayed by AVDP6 are stored, and in addition, memory domain of SDRAM can be mapped directly on the bus of CPU so that the vacant space is utilized as the work domain of CPU. The memory space of SDRAM is controlled with general purpose SDRAM I/F.

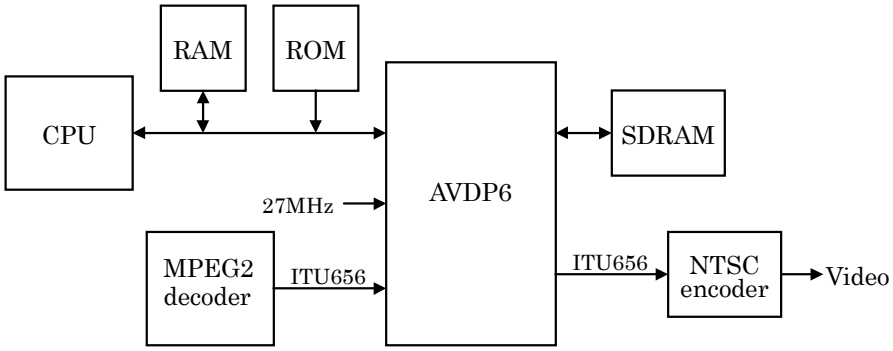
Examples of system configuration are shown below by application.

Independent (free running) system



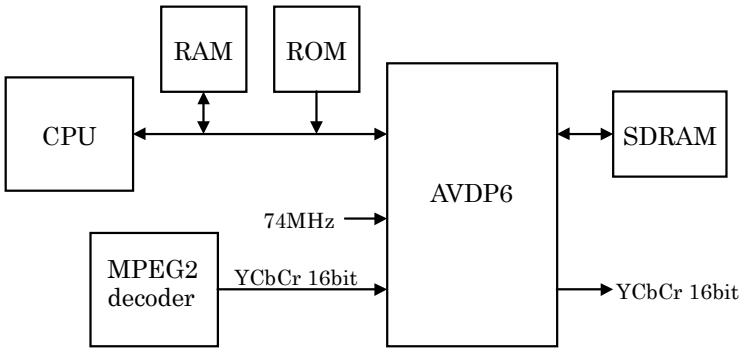
When displaying bit map image stored in the video memory independently, it is possible to output sync signal and display data that are compatible with various scan timing functions by supplying dot clock that is suited to the display device and by writing timing parameter into the registers for internal scan timing. Since the display data are outputted as analog and digital data, an LCD panel can be connected directly to the device and video signal can be created by Video Encoder device.

OSD of NTSC digital images



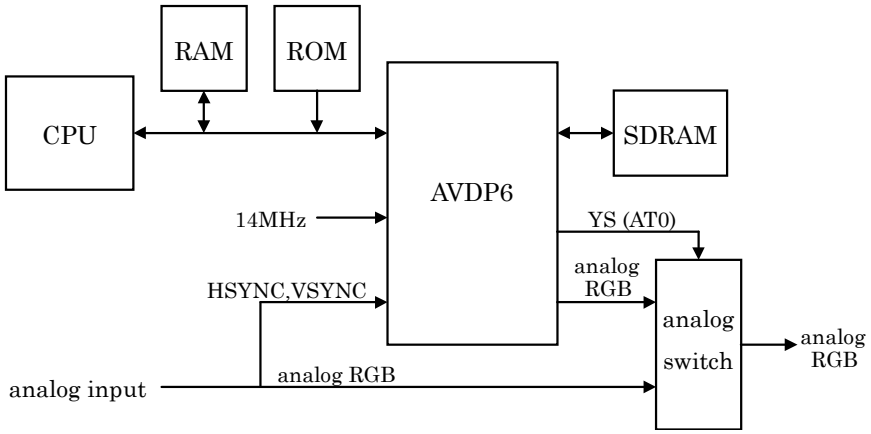
This is an example of system configuration that uses AVDP6 to display OSD images of digital video equipment conforming to NTSC (SDTV) such as DVD. Since AVDP6 is equipped with input / output pins for digital images, the digital video signal can be inputted without converting it to analog signal, processed with OSD and α blending without deteriorating the quality of images, and then outputted. When displaying bitmap image of AVDP6 for external video with OSD, it is necessary to synchronize the external video signal with scanning of AVDP6. At this time, OSD image can be synchronized with external video by inputting sync signal of the external video into scan control circuit of AVDP6. (As the dot clock, use the clock that is synchronized with external video signal.)
The digital image I/F of AVDP6 is compatible with digital I/F that conforms to CCIR-Rec601/656 (ITU656).

OSD of HDTV digital image



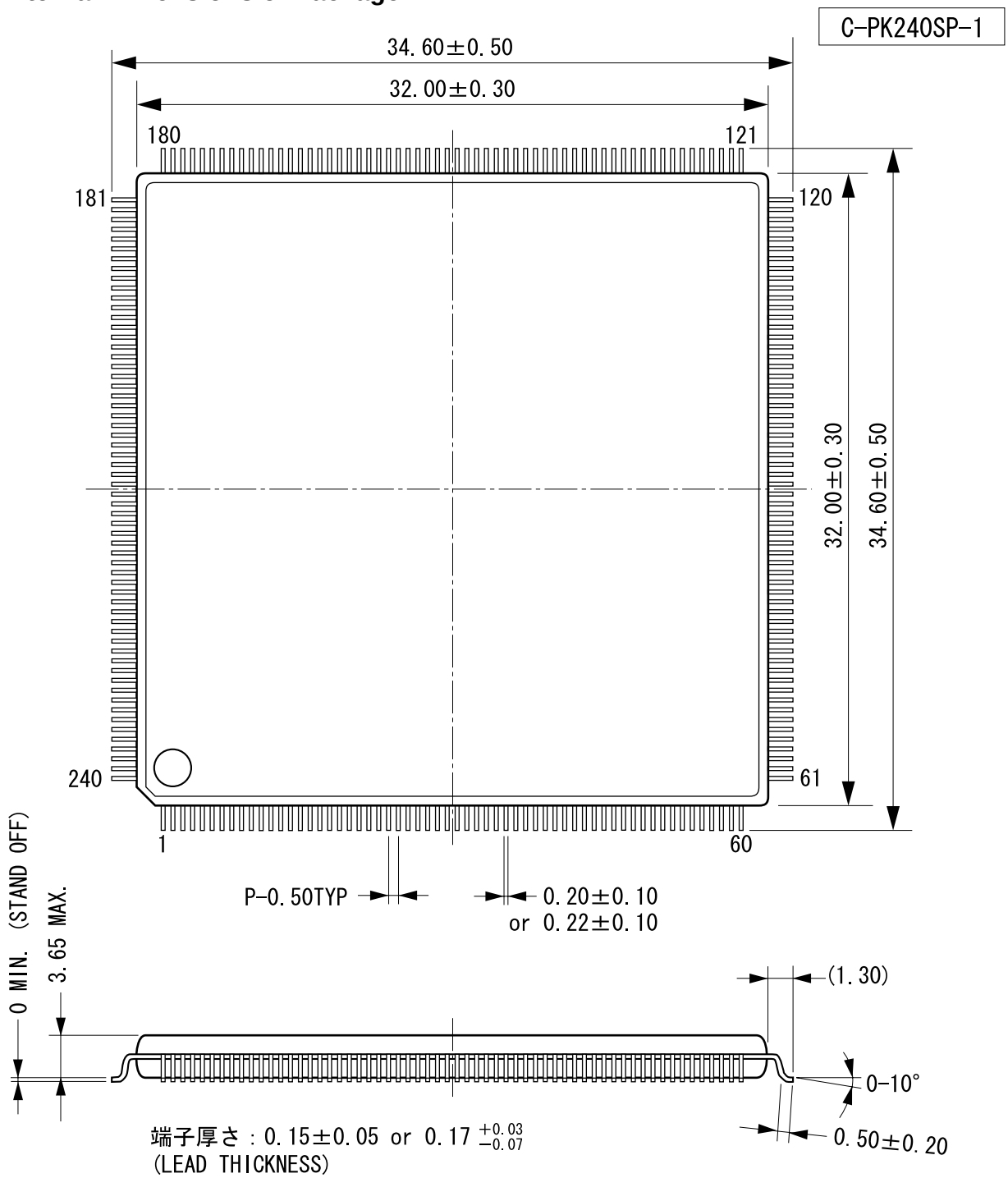
This is an example of the system configuration that uses AVDP6 as OSD image display device in HDTV. Since the device is able to input / output YCbCr422 data at the frequency up to 80 MHz, it is possible to control OSD for video signal of HDTV (1125i). In this case, The frequency of dot clock of OSD image becomes up to 40 MHz (the resolution equivalent to color difference data).
(As the 74 MHz dot clock, it is necessary to input clock that synchronizes with external video signal.)

OSD of NTSC analog image



When the external video is analog signal, switching signal for analog switch can be outputted together with OSD display data. Since the dot clock that synchronizes with sync signal of external video can be regenerated by using the built-in PLL, the superimposing function can be realized easily also for analog image signal.

■ External Dimensions of Package



モールドコーナー形状は、この図面と若干異なるタイプのものもあります。
カッコ内の寸法値は参考値とする。
モールド外形寸法はバリを含まない。
単位(UNIT)：mm(millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.
The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

注） 表面実装LSIは保管条件及び、半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせ下さい。

Note: The LSIs for surface mount need special consideration on storage and soldering conditions.
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