YAMAHA

YGV628B

AVDP7

Advanced Video Display Processor 7

■ Outline

YGV628B (hereafter called AVDP7) is the latest version of YAMAHA AVDP series which has many past successful records in various visual equipments, vehicle equipment, etc.

Three bit-map planes are equipped, and it can be displayed in piles to an external image; furthermore, AVDP7 has many functions as OSD (On Screen Display), such as α-blending, change of a display priority, etc. In addition, it has a digital image Input/Output function to allow an external image to be expanded or reduced.

Moreover, AVDP7 is supports to the resolution up to SVGA, and it is possible to apply to the various digital equipments only by connecting one SDRAM to an external memory as a frame memory.

■ Feature

□ OSD Function

- The OSD images which is composed of plains in case of a digital image input is overlaid. Simultaneous use of three plains is possible in AVDP7 at its maximum.
- The natural picture display of 65536 colors by R5bit, G6bit, and B5bit. It is the palette color of 256 colors in 16777216 colors.
- Supports 16bit YCrCb422
- 16 gray-levels of α-blending in dot units
- Conversion of display priority is possible

□ Display Resolution

- Creation of the Display Timing of NTSC, PAL, QVGA, Wide QVGA, VGA, Wide VGA, and SVGA is possible.
- Examples of Correspondence Resolution : 320×240, 400×240, 720×240, 640×480, 800×480, 800×600, etc..
- Resolution Converting Function : Horizontal direction → 1/2 times to 8192 times display
  Vertical direction → 1/4 times to 8192 times display.

YAMAHA CORPORATION

YGV628B CATALOG
CATALOG No.: LSI-4GV628B20
2005.7

□ Digital Image Input/Output Function

- Corresponding to 18bit RGB, 16bit YCrCb422, and ITU656.
- By YS bit output, Mixing with an image signal are possible externally.

□ Analog Image Output Function

- Analog RGB output which has 8 bits DAC for each R,G,B
- By YS bit output, super-impose of image data is available from an outside.

□ Capture Function

- The depiction from the external image input of 18bit RGB, 16bit YCrCb422, and ITU656 to frame memory is possible in real time.
- When the digital image input is ITU656, it is possible to select from two systems of asynchronous input.
- Pixel Skipping Functions of Horizontal direction and Vertical direction.
- Interlace → Progressive Conversion Function

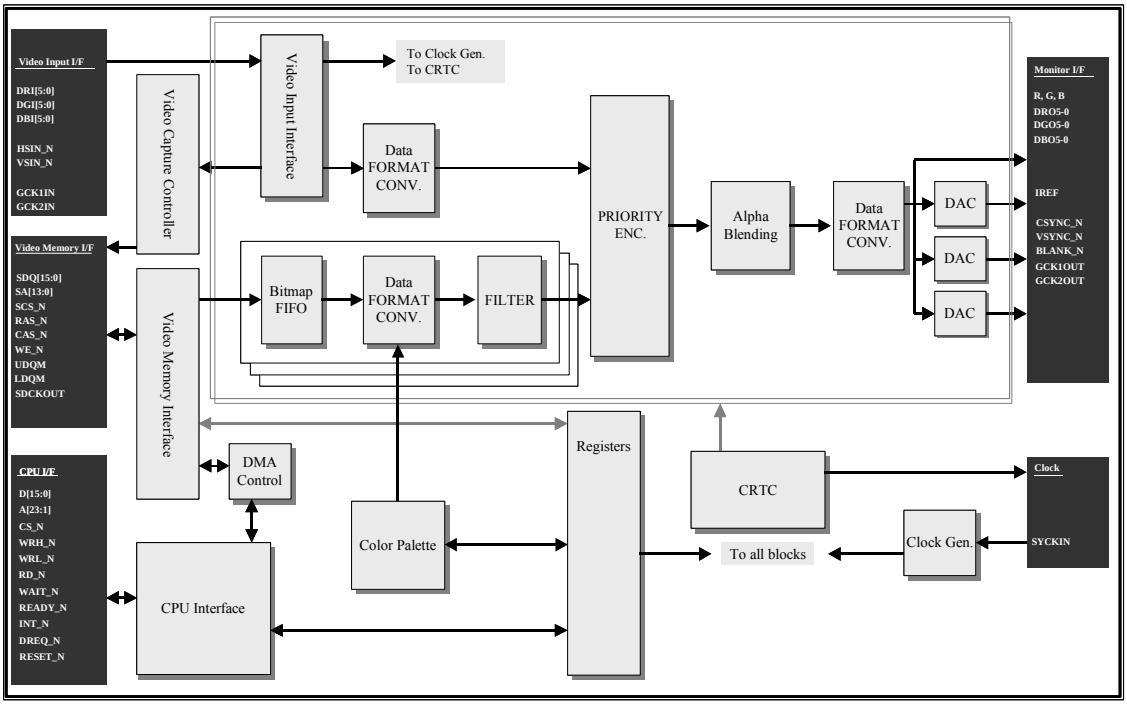
□ External Memory

- Video Memory
  - 16Mbit, 64Mbit, 128Mbit, and 256Mbit(x16) of SDRAM are connectable. However, only a half domain is possible to use at the time of 256Mbits of SDRAM is in use.
  - WRITE/READ access by the memory transfer function
  - The maximum operating frequency of SDRAM clock is 81MHz.

□ Others

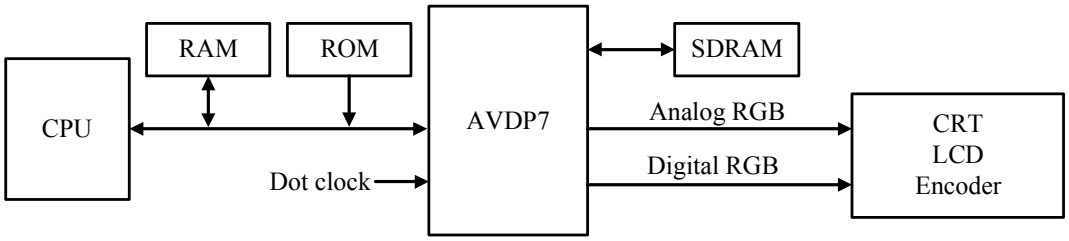
- High flexibility CPU I/F with 16bit CPU bus width and endian control are adopted.
- Built-in register is directly mapped to the 256 Bytes of CPU memory space.
- 176 pin plastic LQFP Pin lead coating is Pb free. (YGV628B-VZ)
- Operating temperature: -40 degree to +85 degree.
- CMOS, 3.3V unity voltage(5V tolerant)

■ Block Diagram

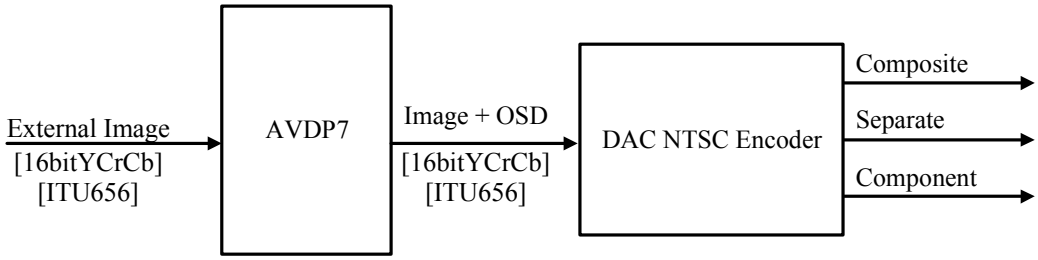


■ Examples of System Composition

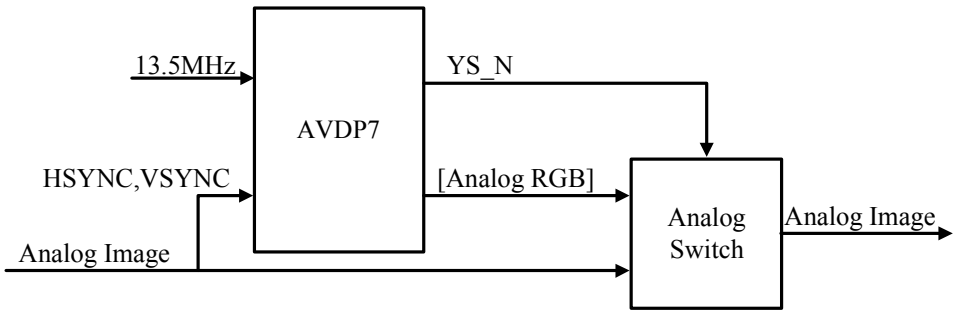
- Independent (self-propelled) system



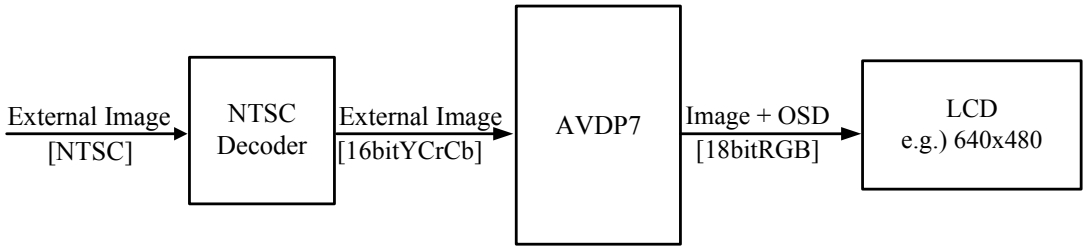
- Example of OSD to Digital Image (CPU, SDRAM, etc. are omitted)



- Example of OSD to Analog Image (CPU, SDRAM, etc. are omitted)



- Example of application to liquid crystal television (CPU, SDRAM, etc. are omitted)



Capture + Interlace Progressive Conversion

- Example of application to on-board multi-vision (CPU, SDRAM, etc. are omitted)

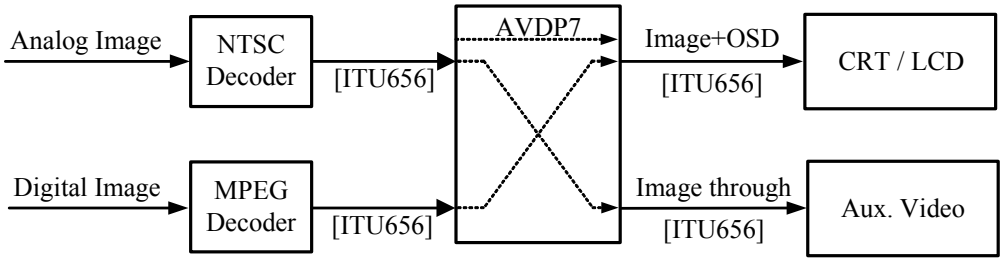
Capture + Resolution Conversion

e.g.)

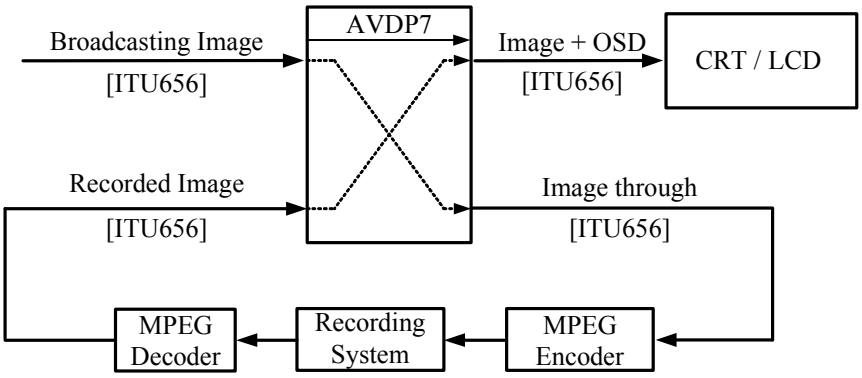
- 720x480/2 [4:3]
- 720x360/2 [16:9] → 800x480
- 720x346/2 [1.85:1]
- 720x270/2 [2.35:1]

[ ]= aspect ratio

- Example of application to digital image equipment (CPU, SDRAM, etc. are omitted)



- Example of application to digital recording equipment (CPU, SDRAM, etc. are omitted)



■ Pin Table

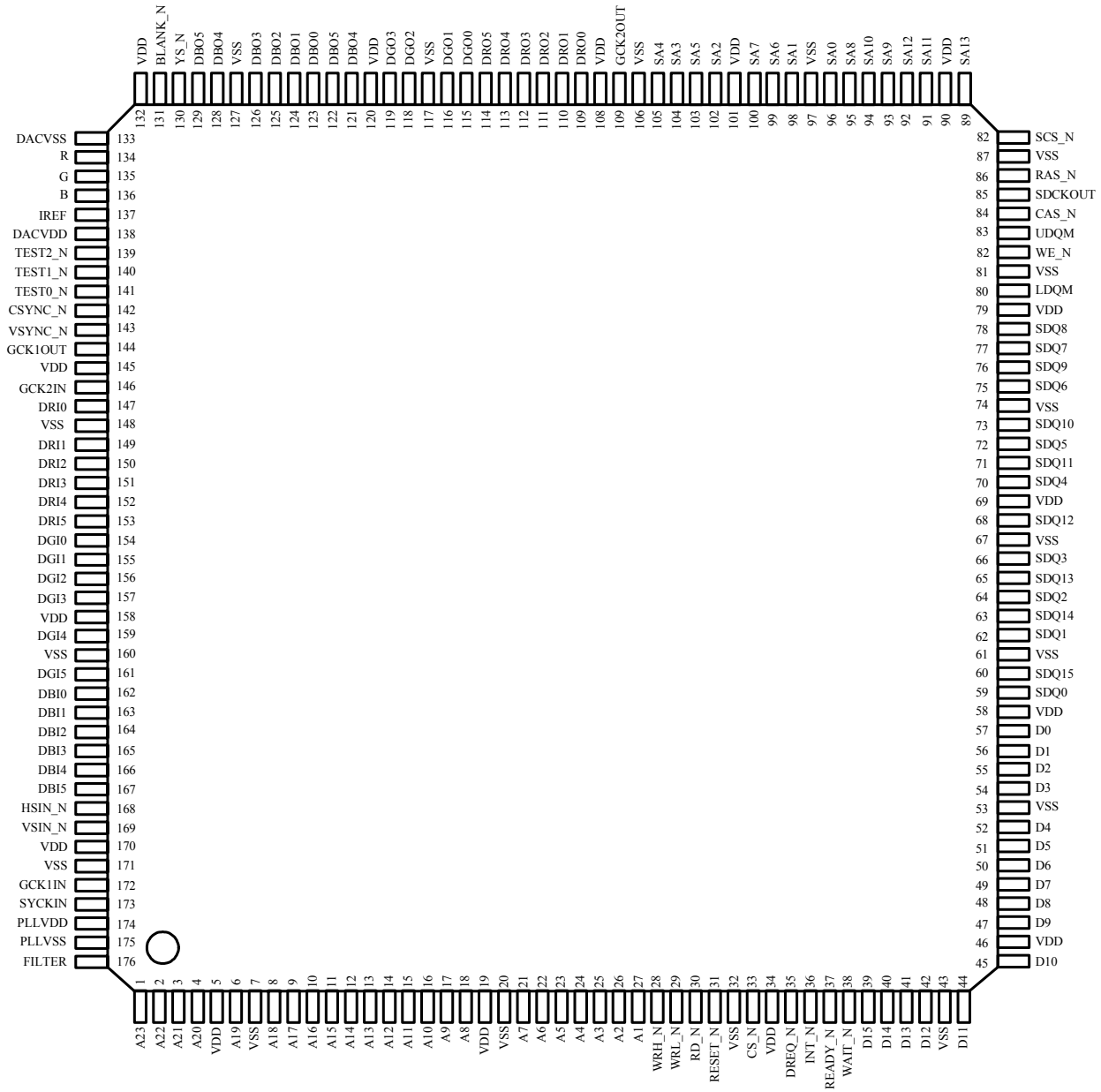
Pins Name	Numbers	I/O	Functions	Level	5Tr	Drive
CUP Interface						
D15-0	16	I/O	CPU Data Bus	LVTTL	○	4mA
A23-1	23	I	CPU Address Bus	LVTTL	○	
CS_N	1	I	Chip Select	LVTTL	○	
RD_N	1	I	READ Pulse Input	LVTTL	○	
WRH_N	1	I	WRITE Strobe Input/D15-8	LVTTL	○	
WRL_N	1	I	WRITE Strobe Input/D7-0	LVTTL	○	
WAIT_N	1	O	CPU Bus WAIT (3-State Output)	LVTTL	○	4mA
READY_N	1	O	CPU Bus Ready (3-State Output)	LVTTL	○	4mA
INT_N	1	O	Interrupt	LVTTL	×	4mA
DREQ_N	1	O	Direct Memory Access	LVTTL	×	4mA
RESET_N	1	I	Reset Input	LVCMOS	○	
Video Memory Interface						
SDQ15-0	16	I/O	Video Memory Data Bus	LVTTL	○	4mA
SA13-0	14	O	Video Memory Address Bus	LVTTL	×	4mA
SCS_N	1	O	Video Memory Chip Enable	LVTTL	×	4mA
RAS_N	1	O	Video Memory Low Address Strobe Output	LVTTL	×	4mA
CAS_N	1	O	Video Memory Column Address Strobe Output	LVTTL	×	4mA
WE_N	1	O	Video Memory WRITE Enable	LVTTL	×	4mA
UDQM	1	O	Video Memory Data Mask Output/ SDQ15-8	LVTTL	×	4mA
LDQM	1	O	Video Memory Data Mask Output/ SDQ7-0	LVTTL	×	4mA
SDCKOUT	1	O	Video Memory Clock Output	LVTTL	×	8mA
Monitor Interface						
R,G,B	3	O	Analog R, G, B, Signals Output	Analog	×	
IREF	1	-	DAC Reference Electric-current Input	Analog	×	
DRI5-0	6	I	Digital R Signal Input	LVTTL	○	
DGI5-0	6	I	Digital G Signal Input	LVTTL	○	
DBI5-0	6	I	Digital B Signal Input	LVTTL	○	
HSIN_N	1	I	Horizontal Synchronized Signal Input	LVTTL	○	
VSIN_N	1	I	Vertical Synchronized Signal Input	LVTTL	○	
YS_N	1	O	YS Signal Output	LVTTL	×	4mA
DRO5-0	6	O	Digital R Signal Output	LVTTL	×	4mA
DGO5-0	6	O	Digital G Signal Output	LVTTL	×	4mA
DBO5-0	6	O	Digital B Signal Output	LVTTL	×	4mA
VSYNC_N	1	O	Vertical Synchronized Signal Output	LVTTL	×	4mA
CSYNC_N	1	O	Horizontal Synchronized Signal / Compound Synchronized Signal Output	LVTTL	×	4mA
BLANK_N	1	O	Non-display Interval Output	LVTTL	×	4mA
GCK1OUT	1	O	Dot Clock Output 1	LVTTL	×	4mA
GCK2OUT	1	O	Dot Clock Output 2	LVTTL	×	4mA

5Tr : 5V supply Yes/No Yes → ○ / No → ×　　Drive：Driving Capability

Pins Name	Numbers	I/O	Functions	Level	5Tr	Drive
Clock						
GCK1IN	1	I	Dot Clock Input1	LVTTL	○	
GCK2IN	1	I	Dot Clock Input 2	LVTTL	○	
SYNCKIN	1	I	System Clock Input	LVTTL	○	
FILTER	1	-	Filter Connect Pin for PLL	Analog	×	
Power Supply						
VDD	15	-	Power Supply for Digital Circuit Part		×	
VSS	17	-	Ground for Digital Circuit Part		×	
PLLVDD	1	-	Analog Power Supply for built-in PLL		×	
PLLVSS	1	-	Ground for built-in PLL		×	
DACVDD	1	-	Analog Power Supply for built-in DAC		×	
DACVSS	1	-	Analog Ground for built-in DAC		×	
TEST Pin						
TEST2-0_N	3	I	Test Pin: Input H Level	LVTTL	○	

5Tr : 5V supply Yes/No Yes → ○ / No → × Drive：Driving Capability

■ Pin Assignment



<Top View>

■ Pin Assignment Table

No.	Terminal name	I/O	No.	Terminal name	I/O	No.	Terminal name	I/O	No.	Terminal name	I/O
1	A23	I	45	D10	I/O	89	SA13	O	133	DACVSS	
2	A22	I	46	VDD		90	VDD		134	R	O
3	A21	I	47	D9	I/O	91	SA11	O	135	G	O
4	A20	I	48	D8	I/O	92	SA12	O	136	B	O
5	VDD		49	D7	I/O	93	SA9	O	137	IREF	
6	A19	I	50	D6	I/O	94	SA10	O	138	DACVDD	
7	VSS		51	D5	I/O	95	SA8	O	139	TEST2_N	I
8	A18	I	52	D4	I/O	96	SA0	O	140	TEST1_N	I
9	A17	I	53	VSS		97	VSS		141	TEST0_N	I
10	A16	I	54	D3	I/O	98	SA1	O	142	CSYNC_N	O
11	A15	I	55	D2	I/O	99	SA6	O	143	VSYNC_N	O
12	A14	I	56	D1	I/O	100	SA7	O	144	GCK1OUT	O
13	A13	I	57	D0	I/O	101	VDD		145	VDD	
14	A12	I	58	VDD		102	SA2	O	146	GCK2IN	I
15	A11	I	59	SDQ0	I/O	103	SA5	O	147	DRI0	I
16	A10	I	60	SDQ15	I/O	104	SA3	O	148	VSS	
17	A9	I	61	VSS		105	SA4	O	149	DRI1	I
18	A8	I	62	SDQ1	I/O	106	VSS		150	DRI2	I
19	VDD		63	SDQ14	I/O	107	GCK2OUT	O	151	DRI3	I
20	VSS		64	SDQ2	I/O	108	VDD		152	DRI4	I
21	A7	I	65	SDQ13	I/O	109	DRO0	O	153	DRI5	I
22	A6	I	66	SDQ3	I/O	110	DRO1	O	154	DGI0	I
23	A5	I	67	VSS		111	DRO2	O	155	DGI1	I
24	A4	I	68	SDQ12	I/O	112	DRO3	O	156	DGI2	I
25	A3	I	69	VDD		113	DRO4	O	157	DGI3	I
26	A2	I	70	SDQ4	I/O	114	DRO5	O	158	VDD	
27	A1	I	71	SDQ11	I/O	115	DGO0	O	159	DGI4	I
28	WRH_N	I	72	SDQ5	I/O	116	DGO1	O	160	VSS	
29	WRL_N	I	73	SDQ10	I/O	117	VSS		161	DGI5	I
30	RD_N	I	74	VSS		118	DGO2	O	162	DBI0	I
31	RESET_N	Ist	75	SDQ6	I/O	119	DGO3	O	163	DBI1	I
32	VSS		76	SDQ9	I/O	120	VDD		164	DBI2	I
33	CS_N	I	77	SDQ7	I/O	121	DGO4	O	165	DBI3	I
34	VDD		78	SDQ8	I/O	122	DGO5	O	166	DBI4	I
35	DREQ_N	O	79	VDD		123	DBO0	O	167	DBI5	I
36	INT_N	O	80	LDQM	O	124	DBO1	O	168	HSIN_N	I
37	READY_N	OT	81	VSS		125	DBO2	O	169	VSIN_N	I
38	WAIT_N	OT	82	WE_N	O	126	DBO3	O	170	VDD	
39	D15	I/O	83	UDQM	O	127	VSS		171	VSS	
40	D14	I/O	84	CAS_N	O	128	DBO4	O	172	GCK1IN	I
41	D13	I/O	85	SDCKOUT	O	129	DBO5	O	173	SYCKIN	I
42	D12	I/O	86	RAS_N	O	130	YS_N	O	174	PLLVDD	
43	VSS		87	VSS		131	BLANK_N	O	175	PLLVSS	
44	D11	I/O	88	SCS_N	O	132	VDD		176	FILTER	

I : Input, 1_{st} : schmitt trigger input, O : Output, Od : Open drain output, OT : 3-state output,
I/O : Input/Output

■ Pins Functions

AVDP7 operates with a 3.3V power supply. Therefore, input and output of the interface to the peripheral circuits operates at LVTTL (3.3v)except RESET_N pin. However, the tolerant voltage to Input/Output signals are guaranteed up to 5V, therefore, connection to a 5V TLL level compatible device is also possible.

Please use a register separately for each pin when making pull-up or pull-down of I/O pins outside of the device. However, when an input signal is fixed by pull-up or pull-down resistor, a common resistor can be used for these input pins.

1) Power Supply

AVDP7 is the 3.3V single power supply specification. In addition, exclusive analog power supply pins are prepared for the built-in PLL and the built-in DAC respectively.

Be sure to observe the following instructions when performing power-on and power-off.

- Simultaneous power-on and power-off is the rule.
- When a time difference occurs due to the design, please follow the following order of power-on and power-off.
- Please perform power-on and power-off so that PLLVDD does not become higher than VDD.

The order of power-on and power-off.

- At the time of power-on.

VDD(Digital power supply)→**PLLVDD**(Analog power supply for PLL)→**DACVDD**(Analog power supply for DAC) →**Signals**.

- At the time of power-off

Signals→**DACVDD**(Analog power supply for DAC)→**PLLVDD**(Analog power supply for PLL)→**VDD**(Digital power supply).

When power-on and power-off are performed in reverse order against a recommended procedure in two kinds of power supplies in any of the power supplies mentioned above, a problem might be occurred to have an influence on the reliability of LSI. For the reason, please avoid such operations.

- **VDD** (Power Supply Pin No.5, 19, 34,46, 58, 69, 79, 90, 101, 108, 120, 132, 145, 158, 170)
- **VSS** (Power Supply Pin No.7, 20, 32, 43, 53, 61, 67, 74, 81, 87, 97, 106, 117, 127, 148, 160, 171)
  - Power Supply Pin for Internal Digital Circuit.
  - Please supply 3.3V to VDD pins, and supply a ground level to VSS pin.

- **PLLVDD** (Power Supply Pin No.174)
- **PLLVSS** (Power Supply Pin No.175)
  - It is an analog power supply pin for built-in PLL.
  - Please supply a ground level to PLLVSS pins, and supply 3.3V to PLLVDD.
  - Be sure to perform power supply power-on and power-off, so that PLLVDD may not become higher than VDD.

- **DACVDD** (Power Supply Pin No.138)
- **DACVSS** (Power Supply Pin No.133)
  - It is an analog power supply pin for built-in DAC.
  - Please supply 3.3V to DACVDD pin, and supply a ground level to DACVSS pin. Be sure to supply separately to other power supplies.

2) Clock

To AVDP7, a clock (dot clock) for a scan timing of monitor display, and for passing a display data, a clock (capture clock) for capturing a digital image input, and a clock (system clock) which is used for other process are supplied separately.

Please input a dot clock and a capture clock into GCK1IN pin and GCK2IN pin, and input a system clock into SYCKIN pin.
Since there is no function of XTAL oscillation, be sure to input the clock which carried out the external oscillation.

- **GCK1IN** (Input Pin No.172)
- **GCK2IN** (Input Pin No.146)
  - These are input pins of a dot clock and a capture clock.
  - Be sure to input the 5MHz to 40MHz clock oscillated externally into these pins.

- **SYCKIN** (Input Pin No. 173)
  - It is a system clock input pin. The reference clock for the built-in PLL is input.
  - Be sure to input the 5MHz to 40MHz clock into SYCKIN.

- **FILTER** (Analog Pin No.176)
  - It is the filter connection pin for built-in PLL used for a system clock oscillation.
  - Please connect a resistor and a capacitor externally between PLLVSS pin and FILTER pin.

3) CPU Interface

- **D15-0** (Input/Output Pin No. 39-42, 44, 45, 47-52, 54-57)
  - It is a CPU data bus pin. It connects with an external data bus of CPU.
  - Since these pins do not internally have a pull-up resistor, please make the pull-up outside of the device.

- **A23-1**(Input Pin No. 1-4, 6, 8-18, 21-27)
  - It is a CPU address bus pin. It connects with an external address bus of CPU.
  - Since these pins do not internally have a pull-up resistor, please make the pull-up outside of the device if necessary.

- **CS_N** (Input Pin No.33)
  - It is a chip select input pin.
  - The chip select signals from CPU to register space or video memory space are input.
  - Since this pin does not internally have a pull-up resistor, please make the pull-up outside of the device if necessary.
  - This signal is low active.

- **RD_N** (Input Pin No.30)
  - It is a READ pulse input pin.
  - The strobe signal for data read-out from CPU is input.
  - Since this pin does not internally have a pull-up resistor, please make the pull-up outside of the device if necessary.
  - This signal is low active.

- **WRH_N** (Input Pin No.28)
- **WRL_N** (Input Pin No. 29)
  - It is a WRITE pulse input pin. The strobe signal for data writing from CPU is input.
  - Since these pins do not internally have a pull-up resistor, please make the pull-up outside of the device if necessary.

- These signals are low active.

- **WAIT_N** (3-state Output Pin No.38)
  - It is a CPU bus WAIT pin.
  - The bus WAIT demand signal to CPU is output.
  - Since this pin does not internally have a pull-up resistor, please make the pull-up outside of the device.
  - This signal is low active.

- **READY_N** (3-state Output Pin No.37)
  - It is a CPU bus READY pin.
  - The bus READY signal to CPU is output.
  - Since this pin does not internally have a pull-up resistor, please make the pull-up outside of the device.
  - This signal is low active.

- **INT_N** (Output Pin No.36)
  - It is an interrupt signal output pin.
  - The interrupt request signal to CPU is output.
  - This signal is low active.

- **DREQ_N** (Output Pin No.35)
  - It is a DMA request signal output pin.
  - The DMA request signal to CPU is output.
  - This signal is low active.

4) Video Memory Interface

- **SDQ15-0** (Input/Output Pin No. 59, 60, 62-66, 68, 70-73, 75-78)
  - It is a data input/output bus pin for video memories.
  - It connects with the data bus of a video memory.
  - Since these pins do not internally have a pull-up resistor, please make the pull-up outside of the device.

- **SA13-0** (Output Pin No. 89, 91-96, 98-100, 102-105)
  - It is an address bus output pin for video memories.
  - It connects with the address bus of a video memory.
  - The signal attribute output from SA13-0 pin differs according to the kind of external SDRAM.

- **SCS_N** (Output Pin No.88)
  - It is a tip select output pin for video memories.
  - The tip select signal to a video memory is output.
  - This signal is low active.

- **RAS_N** (Output Pin No.86)
  - It is a low address strobe output pin for video memories.
  - The low address strobe signal to a video memory is output.
  - This signal is low active.

- **CAS_N** (Output Pin No.84)
  - It is a column address strobe output pin for video memories.
  - The column address strobe signal to a video memory is output.
  - This signal is low active.

- **WE_N** (Output Pin No.82)
  - It is a WRITE strobe output pin for video memories.
  - The WRITE strobe signal to a video memory is output.
  - This signal is low active.

- **UDQM** (Output Pin No.83)
- **LDQM** (Output Pin No.80)
  - It is a data mask signal output pin for video memories.
  - The data mask signal to a video memory is output.
  - UDQM pin is a data mask signal SDQ15-8 pin, and LDQM pin is a data make signal to SDQ7-0.
  - These signals are high active.

- **SDCKOUT** (Output Pin No.85)
  - It is a clock output pin for video memories.
  - The clock to a video memory is output.
  - The clock frequency output from this pin is 75MHz to 81MHz.

5) Monitor Interface

- **R** (Analog Output Pin No.134)
- **G** (Analog Output Pin No.135)
- **B** (Analog Output Pin No.136)
  - It is an analog RGB output pin.
  - Linear R, G, and B signal are output.
  - When the analog RGB output is not used, please connect nothing.

- **IREF** (Analog Pin No.137)
  - It is a standard current input pin for RGB DAC.
  - When an analog RGB output is not used, please connect nothing.

- **DRO5-0** (Output Pin No.109-114)
- **DGO5-0** (Output Pin No.115, 116, 118, 119, 121, 122)
- **DBO5-0** (Output Pin No.123-126, 128, 129)
  - It is a digital RGB output pin.
  - When a digital RGB output is not used, please connect nothing.

- **DRI5-0** (Input Pin No.147, 149-153)
- **DGI5-0** (Input Pin No.154-157, 159, 161)
- **DBI5-0** (Input Pin No.162-167)
  - It is a digital RGB input pin.
  - Since these pins do not internally have a pull-up resistor, please make the pull-up outside of the device if necessary.

- **VSYNC_N** (Output Pin No.143)
  - It is a vertical synchronized signal output pin.
  - Vertical synchronized signal is output.
  - This signal is low active.

- **CSYNC_N** (Output Pin No.142)
  - It is a horizontal / composite synchronized signal output pin.
  - Horizontal synchronized signal or Composite synchronized signal are output.
  - This signal is low active.

- **HSIN_N** (Input Pin No.168)
  - It is a horizontal synchronized signal input pin.
  - The external horizontal synchronized signal for resetting an internal horizontal counter is input.
  - When not used, please make the pull-up outside of the device if necessary because this pin does not internally have a pull-up resistor.

- This signal is low active.

- **VSIN_N** (Input Pin No.169)
  - It is a vertical synchronized signal input pin.
  - The external vertical synchronized signal for resetting an internal vertical counter is input.
  - When not used, please make the pull-up outside of the device if necessary because this pin does not internally have a pull-up resistor.
  - This signal is low active.

- **BLANK_N** (Output Pin No.131)
  - It is a display timing output pin.
  - The signal which shows a no-display period is output.
  - This signal is low active.

- **YS_N** (Output Pin No.130)
  - It is YS signal output pin.
  - YS signal at the time of superimpose is output.
  - This signal is low active.

- **GCK1OUT** (Output Pin No.144)
- **GCK2OUT** (Output Pin No.107)
  - It is a dot clock output pin.
  - A dot clock is output.

6) System Reset

- **RESET_N** (Schmitt trigger type input Pin No.31)
  - It is a reset pin.
  - Please input a power-on reset signal.
  - The reset signal input having predetermined period is surely required at the power-on.
  - Since this pin does not internally have a pull-up resistor, please make the pull-up outside of the device if necessary.
  - This signal is low active. This pin uses the schmitt trigger type buffer.

7) LSI Test

- **TEST2-0_N** (Input Pin No. 139, 140, 141)
  - It is a test mode setting pin for a device test.
  - Since these pins do not internally have a pull-up resistor, please make the pull-up outside of the device.

■ Electrical Characteristics

- Absolute Maximum Ratings

Items	Symbol	Rating	Unit	Note
Power Supply Voltage (VDD Pin)	V_{DD}	-0.5 to +4.6	V	1
DAC Power Supply Voltage (DACVDD pin)	V_{DAC}	-0.5 to +4.6	V	1
PLL Power Supply Voltage(PLLVDD pin)	V_{PLL}	-0.5 to +4.6	V	1
Input Pin Voltage	V_I	-0.5 to +5.5	V	1
Output Pin Voltage (5V tolerant Pin)	V_O	-0.5 to +5.5	V	1
Output Pin Voltage (Other than Above)	V_O	-0.5 to V_{DD}+0.5	V	1
Output Pin Electric Current	I_O	-20 to +20	mA	
Storage Temperature	T_{stg}	-50 to +125	°C	

Note 1) Value based on Vss(GND) =0V

- Recommended Operating Condition

Items	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	3.0	3.3	3.6	V	1
DAC Power Supply Voltage (DACVDD pin)	V_{DAC}	3.0	3.3	3.6	V	1
PLL Power Supply Voltage (PLLVDD pin)	V_{PLL}	3.0	3.3	3.6	V	1
Ambient Operation Temperature	T_{OP}	-40		+85	°C	2

Note 1) Value based on Vss(GND) =0V

Note 2) The board wiring density is estimated to be 260% or over.

- DC Characteristics

Items	Symbol	Min	Typ	Max	Unit	Note
Low Level Input Voltage (RESET_N pin, TEST2-0_N pin)	V_{IL}	-0.3		V_{DD}×0.2	V	1
Low Level Input Voltage (except RESET_N pin, TEST2-0_N pin)	V_{IL}	-0.3		0.8	V	1
High Level Input Voltage (RESET_N pin, TEST2-0_N Pin)	V_{IH}	V_{DD}×0.8		5.5	V	1
High Level Input Voltage (except RESET_N pin, TEST2-0_N pin)	V_{IH}	2.0		5.5	V	1
Built-in DAC Recommended Operation Condition						
Reference Current (IREF Pin)			-9.38		mA	
Output Load (R,G,B)			37.5		Ω	

Note 1) Value based on Vss(GND) =0V

Items	Condition	Symbol	Min	Typ	Max	Unit	Note
Low Level Output Voltage	I_{OL}=100μA	V_{OL}	0		0.4	V	
High Level Output Voltage	I_{OH}= -100μA	V_{OH}	2.4		V_{DD}	V	
Input Leakage Current		I_{LI}	-10		+10	μA	2
Output Leakage Current		I_{LO}	-25		+25	μA	
Total Power Consumption	C_L=20pF	P_D			1.2	W	3
Consumption Current Items							
VDD	C_L=20pF	I_{VDD}			230	mA	3
DACVDD	When 0V output	I_{DAC}			80	mA	3
PLLVDD	When 81MHz	I_{PLL}			2.5	mA	3

Note 2) Be sure to use the resistance less than 7kΩwhen connecting an external pull-up resistance. The minimum and the maximum of input leak current are a value when having not connected external resistance.

Note 3) V_{IL} = GND, V_{IH} = V_{DD} for consumption current and power consumption value.

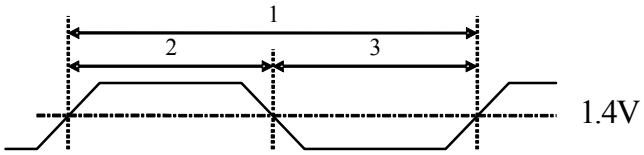
Items	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_I			10	pF
Output Pin Capacitance	C_O			10	pF
Input/Output Pin Capacitance	C_{IO}			10	pF

- AC Characteristics

NOTE : A timing measurement level is 1.4V and input signal transient time is 1ns.

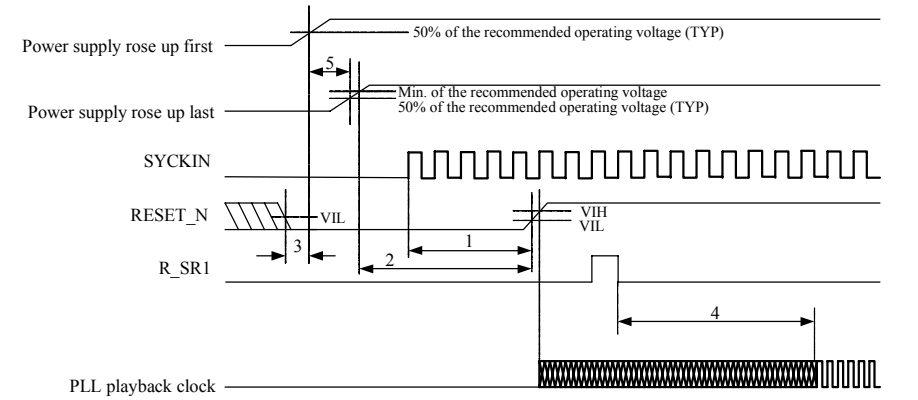
- Clock Input

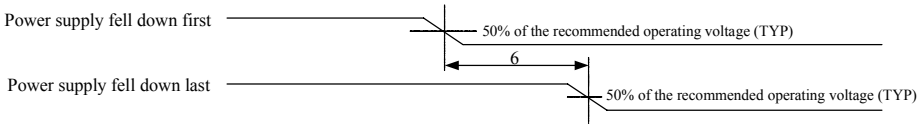
No.	Item	Symbol	Min	Typ	Max	Unit
1	SYCKIN Input Clock Frequency	f_{SYCK}	5		40	MHz
	SYCKIN Clock Cycle Time	t_{cSYCK}	25		200	ns
2	SYCKIN Clock High Level Pulse Width	t_{whSYCK}	7.5			ns
3	SYCKIN Clock Low Level Pulse Width	t_{wlSYCK}	7.5			ns
4	MCLK(PLL Out) Clock Frequency	f_{MCLK}	75		81	MHz
	MCLK(PLL Out) Clock Cycle Time	t_{cMCLK}	13.3		12.3	ns



- Reset Input and Power Supply

No.	Item	Symbol	Min	Typ	Max	Unit
1	RESET_N Pin Input Time (respect to SYCKIN)	t_{wRES1}	1			µs
2	RESET_N Pin Input Time (respect to VDD)	t_{wRES2}	1			µs
3	VDD-RESET_N Pin Setup Time	t_{sRES}	0			s
4	PLL Lock up Time	t_{wPLU}	10			ms
5	Time Difference in Power-on	t_{VSKWR}			1	s
6	Time Difference in Power-off	t_{VSKWF}			1	s





- CPU Interface (Measurement Condition : CL=20pF)

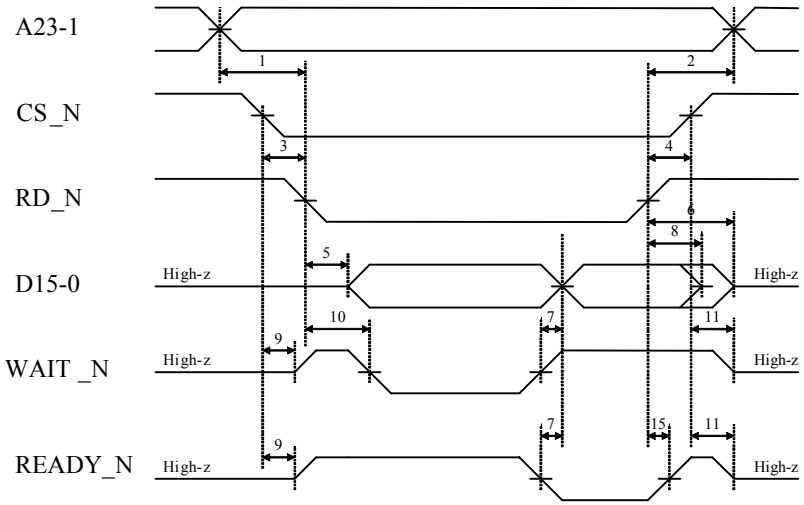
No.	Item	Symbol	Min	Typ	Max	Unit	Note
1	A23-1 : setup time	tsA	1			ns	1
2	A23-1 : hold time	thA	0				1
3	CS_N: setup time	tsCS	1				2
4	CS_N: hold time	thCS	0				2
5	D15-0 : output data turn on time	tonD	0				
6	D15-0 : output data turn off time	toffD			10		
7	D15-0 : output data valid delay time	tdD			0		
8	D15-0 : output data hold time	thD	0				
9	WAIT_N, READY_N: turn on time	tonWAIT	0				
10	WAIT_N, READY_N: valid delay time	tdWAIT			15		
11	WAIT_N,READY_N: turn off time	toffWAIT			15		
12	D15-0 : input data setup time	tsD	tcMCLK+10				3
13	D15-0 : input data hold time	thD	0				3
14	WRx_N: hold time	thWR	0				
15	READY_N: hold time from WRx_N, RD_N inactive	thREADY	0		12		

Note 1) This is a regulation for WRH_N, WRL_N, and RD_N signals. However, in case of CS_N control, it is a rule for CS_N.

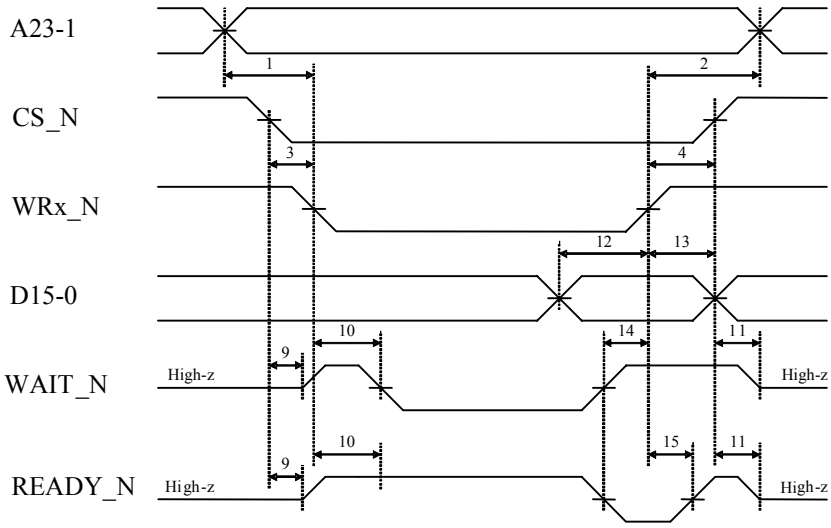
Note 2) They are the conditions of being WRH_N, WRL_N, and RD_N control. It becomes CS_N control when not filling this regulation.

Note 3) D15-8 is the regulation to WRH_N. D7-0 is the regulation to WRL_N.

● CPU READ Cycle



- CPU WRITE Cycle

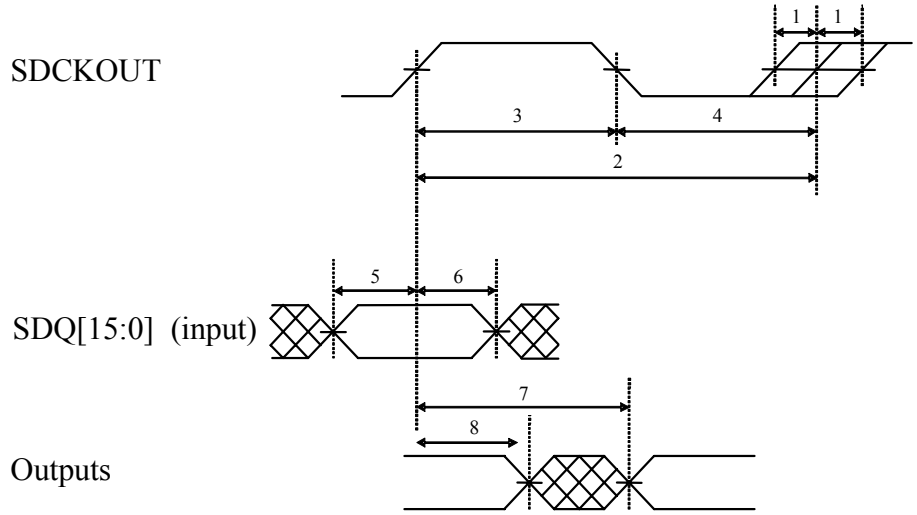


- SDRAM Interface (Measurement Condition: CL=15pF)

No.	Item	Symbol	Min	Typ	Max	Unit	Note
1	SDCKOUT: jitter	t_{jSDCK}	-1		1	ns	1
2	SDCKOUT: frequency	f_{SDCK}	75		81	MHz	1,2
	SDCKOUT: cycle time	t_{cSDCK}	12.35		13.33		1,3
3	SDCKOUT: clock high level width	t_{whSDCK}	3.5				1
4	SDCKOUT: clock low level width	t_{wlSDCK}	3.5				1
5	SDQ15-0 : input data setup time	t_{sSDQ}	4				1
6	SDQ15-0 : input data hold time	t_{hSDQ}	1			ns	1
7	SCS_N, RAS_N, CAS_N, WE_N, SA13-0, SDQ15-0, UDQM, LDQM : output delay time	t_{dSDO}			9		1
8	SCS_N, RAS_N, CAS_N, WE_N, SA13-0, SDQ15-0, UDQM, LDQM : output hold time	t_{hSDO}	1.5				1

Contents of Mode Register			
Read/Write Mode		Burst Read and Burst Write	
CAS Latency		2	
Wrap Type		Sequential	
Burst Length		2	
Command Interval			4
Clock Cycle Time (C_L=2)	t_{CK2}	Less than 10 ns	
Ref/Active – Ref/Active Command Interval	t_{RC}	Six or less cycle (in case of SDCKOUT frequency 81 MHz, less than 74ns)	5
Pre-charge – Active Command Interval	t_{RP}	Two or less cycle (in case of SDCKOUT frequency 81 MHz, less than 24ns)	
WRITE Recovery Time	t_{WR}	Two or less cycle (in case of SDCKOUT frequency 81 MHz, less than 24ns)	
Data in – Command Interval	t_{DAL}	Four or less cycle (in case of SDCKOUT frequency 81 MHz, less than 49ns)	
Active – Pre-charge Command Interval	t_{RAS}	Five or less cycle (in case of SDCKOUT frequency 81 MHz, less than 61ns)	
Active – Read / Write Command Delay Time	t_{RCD}	Two or less cycle (in case of SDCKOUT frequency 81 MHz, less than 24ns)	
Mode Register Set Cycle Time	t_{RSC}	Four or less cycle (in case of SDCKOUT frequency 81 MHz, less than 49ns)	

Note 1) PLL must be in stable state.
Note 2) Fulfill a condition → $f_{SDCK} \geqq f_{GCK1O} \times 2$
Note 3) Fulfill a condition → $t_{cSDCK} \times 2 \leqq t_{cGCK1O}$
Note 4) Conditions of SDRAM to be chosen.
Note 5) Although some SDRAM makers may have divided and specified the interval from the auto-refresh to the following command (t_{RRC}), it is necessary to be lower than t_{RC}.



＃Outputs：SCS_N, RAS_N, CAS_N, WE_N, SA13-0, SDQ15-0(output), UDQM, LDQM

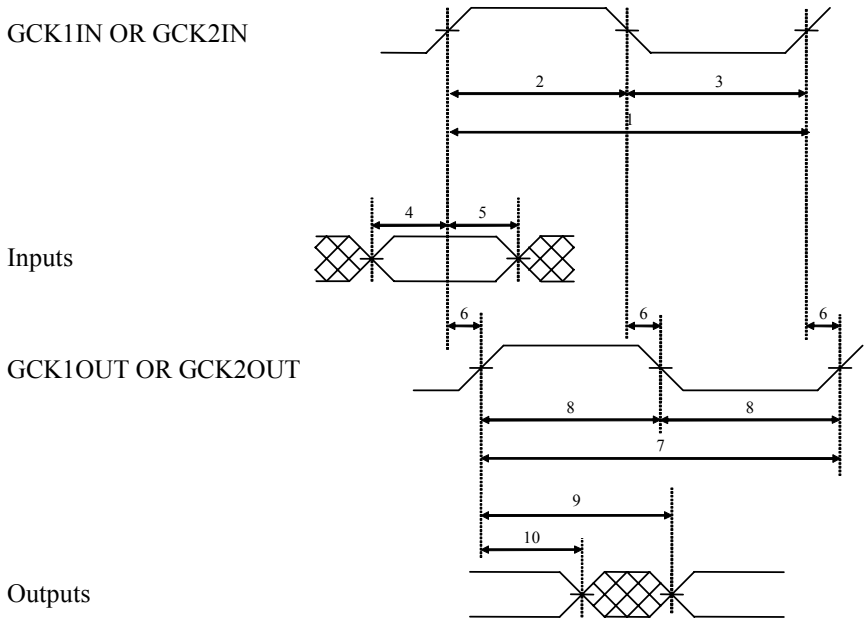
- Display Timing Signals (Measurement Condition : CL=20pF)

No.	Item	Symbol	Min	Typ	Max	Unit	Note
1	GCK1IN, GCK2IN : frequency	f_{GCKI}	5		40	MHz	1
	GCK1IN, GCK2IN : cycle time	t_{cGCKI}	25		200	ns	2
2	GCK1IN, GCK2IN : clock high level width	t_{whGCKI}	8			ns	
3	GCK1IN, GCK2IN : clock low level width	t_{wlGCKI}	8			ns	
4	HSIN_N, VSIN_N, DRI5-0, DGI5-0, DBI5-0: input data setup time	t_{sDI}	3			ns	
5	HSIN_N,VSIN_N,DRI5-0, DGI5-0, DBI5-0: input data hold time	t_{hDI}	1			ns	
6	GCK1OUT: delay time	t_{dGCK1O}	0		20	ns	
	GCK2OUT: delay time	t_{dGCK2O}	0		20	ns	
7	GCK1OUT : frequency	f_{GCK1O}	5		40	MHz	
	GCK1OUT : cycle time	t_{cGCK1O}	25		200	ns	
	GCK2OUT : frequency	f_{GCK2O}	5		40	MHz	
	GCK2OUT : cycle time	t_{cGCK2O}	25		200	ns	
8	GCK1OUT, GCK2OUT : clock duty	t_{duGCKO}	45		55	%	3
9	YS_N, CSYNC_N, VSYNC_N, BLANK_N, DRO5-0, DGO5-0, DBO5-0: output delay time	t_{dDISP1}			9	ns	
10	YS_N, CSYNC_N, VSYNC_N, BLANK_N, DRO5-0, DGO5-0,DBO5-0: output hold time	t_{hDISP1}	0			ns	

Note 1) Fulfill a condition → $f_{SDCK} \geqq f_{GCK1O} \times 2$

Note 2) Fulfill a condition → $t_{cSDCK} \times 2 \leqq t_{cGCK1O}$

Note 3) In the cases of other than Analog synchronization



Inputs：HSIN_N, VSIN_N, DRI5-0, DGI5-0, DBI5-0
Outputs：YS_N, CSYNC_N, VSYNC_N, BLANK_N, DRO5-0, DGO5-0, DBO5-0

- Analog Characteristics

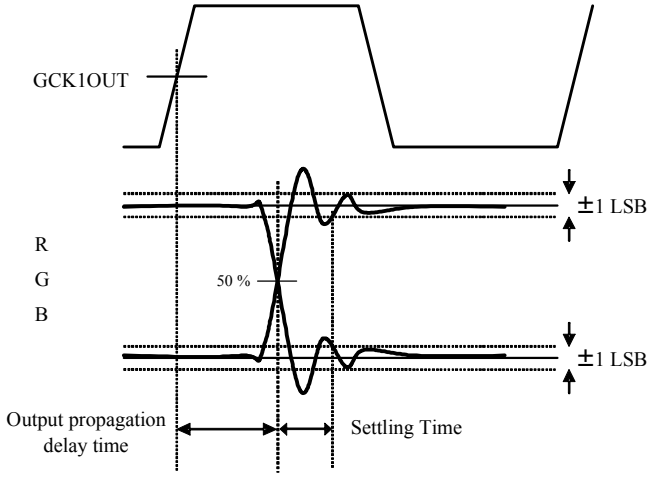
In AVDP7, R, G, and B pin is an output pin for an Analog signal.

RGB Pin Output Characteristics

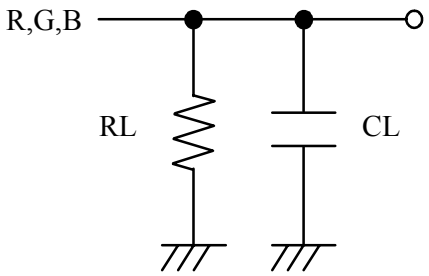
Item	Condition	Min	Type	Max	Unit
Resolution	R_L = 37.5Ω C_L = 30 pF IREF = -9.38mA Additional capacity of GCK1OUT = 20pF			8	bit
Settling Time			20		ns
Output Propagation Delay Time		-5		3	ns
Output Voltage Amplitude (Vp-p)			0.7		V
Max Output Voltage (VWHITE)			0.7		V
Min Output Voltage (VBLACK)			0		V
Vp-p Deviation of R, G, B				3	%

Settling time is defined as the interval between the point at which DAC output level comes up to 50% and the point at which the output level reaches and stays within ±1 LSB centered on the resulting output level.

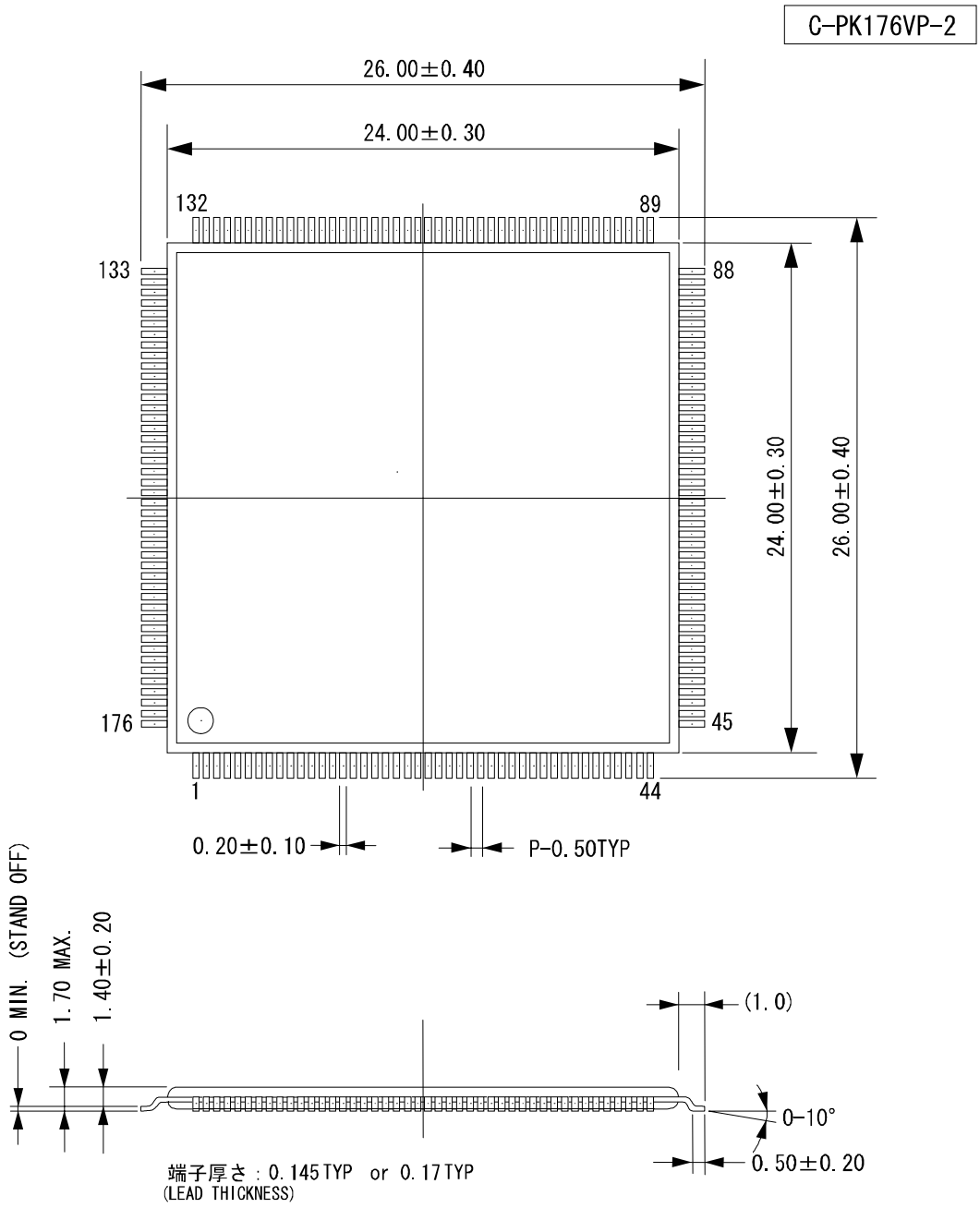
Output Propagation Delay Time is defined as the interval between the rising edge of GCK1OUT and the point at which DAC output level comes up to 50%.



Measurement Circuit



■ Package Outline Drawing



モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位：mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

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