YAMAHA

CONFIDENTIAL

PRELIMINARY

YGV630

AVDP8

Advanced Video Display Processor 8

■ Overview

YGV630 (AVDP8) is an in-car image control device, which has video decoder function, video image correction function, scaler function, multiscreen control function, etc., as well as the inherited features as AVDP series high-performance OSD (On Screen Display) controller.

■ Features

□ CPU Interface

- 16 bits or 32 bits Data Bus width selection
- Byte-write operation with WR3-0_N pin
- Supports data access in both big-endian and little–endian formats
- Direct rendering to the entire video memory space from CPU
- Prepares interrupt pin
- Controllable Bus Wait and Bus Ready signals

□ Clock

- Built-in PLL for system clock generation
- Built-in PLL for dot clock generation

□ Analog Video Input

- 12-channel analog video inputs
- Supports Composite Video, S Video, Component Video input
  - — supports NTSC-M, NTSC-JAPAN, PAL-I,B,G,H,D,N, combination N
- Supports analog RGB input (supports only progressive scan)
- Up to 4-line analog RGB connection

□ Digital Video Input

- Supports ITU-R BT.656
- Supports Digital RGB (6-bit each)
  - — Supports both interlace scan and progressive scan
  - — Dot clock of 75MHz or lower
- Digital RGB (6-bit each) input up to 1 channel or ITU-R BT.656 input up to 2 channels

The contents of this booklet are target specifications and they might be changed without notice. Please confirm the finalized specifications again before the use of this LSI.

YAMAHA CORPORATION

YGV630 CATALOG
CATALOG No.: LSI-4GV630A00
2006.5

□ Decoder Function
- Three 10-bit ADCs
- Two video decoders
- Analog video input simultaneous decoding up to 2 channels
  - Decodable combinations:
    Composite Video × 2
    Composite Video + S video
    Composite Video + Component Video
- Multiple analog video sources switching function
- Brightness correction function
- Tone correction function

□ Video Memory Interface
- Selectable video memory (64Mbit, 128Mbit, or 256Mbit)
- Video inputs that can be captured:
  - Composite Video, S Video, Component Video, Analog RGB, ITU-R BT.656, and Digital RGB
    (However, as for Digital RGB, dot clock must be lower than 30MHz and the size must be smaller than 720×480 with the progressive scan performed.)
- Capture (only Y component) for recognizing images
- Area designation for capturing video
- Captured video error control function
- Interlace function
- Automatic frame period conversion function

□ Rendering Function
- Rendering function with rendering commands
- Three types of commands: LINE, FILL, and COPY
- Built-in Command FIFO (next rendering command can be issued before the end of the previous command.)
- Format conversion function
- α-blending function at the rendering (α value can be designated in dot.)
- Color Mask function
- Antialias function at LINE command

□ Display Function
- Simultaneous display up to 5 planes: Backdrop plane, two OSD planes, and two capture planes
- Display priority control function
- Window function (only capture plane)
- Transparent dot designation
- α-blending function
- Flicker cancel function
- Captured video correction function: Scaling, distortion correction, inclination correction (only capture plane)
- Resolution conversion function (only capture plane)
- PAL → NTSC conversion function
- NTSC → PAL conversion function
- Interlace → progressive conversion function

□ CRT Control Function
- Supports both interlace scan and progressive scan
- Supports both NTSC and PAL
- Supports QVGA to XGA
- Display timing setting in dots and lines

- Equivalent pulse insertion function for Composite Sync signal
- Dot clock inversion function
- Sync signal inversion function
- External Sync function
- External Sync video error control function

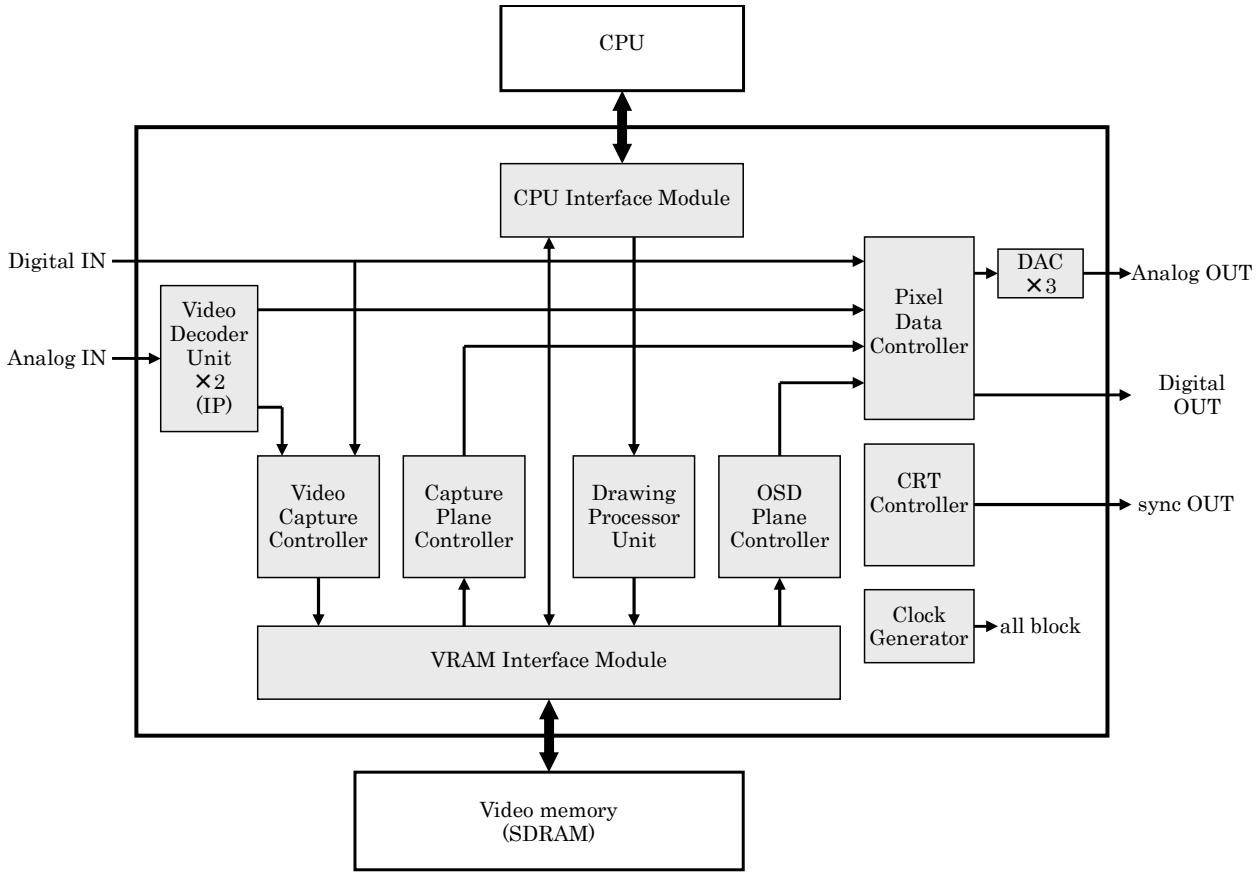
□ Video Output

- Analog RGB output (Resolution: 8bit each; Maximum operating frequency: 40MHz)
- Digital RGB output (Resolution: 6bit each; Maximum operating frequency: 75MHz)
- ITU-R BT.656 output (Unavailable when analog RGB video or digital RGB video is displayed on the backdrop plane.)
- Gamma correction function

□ Others

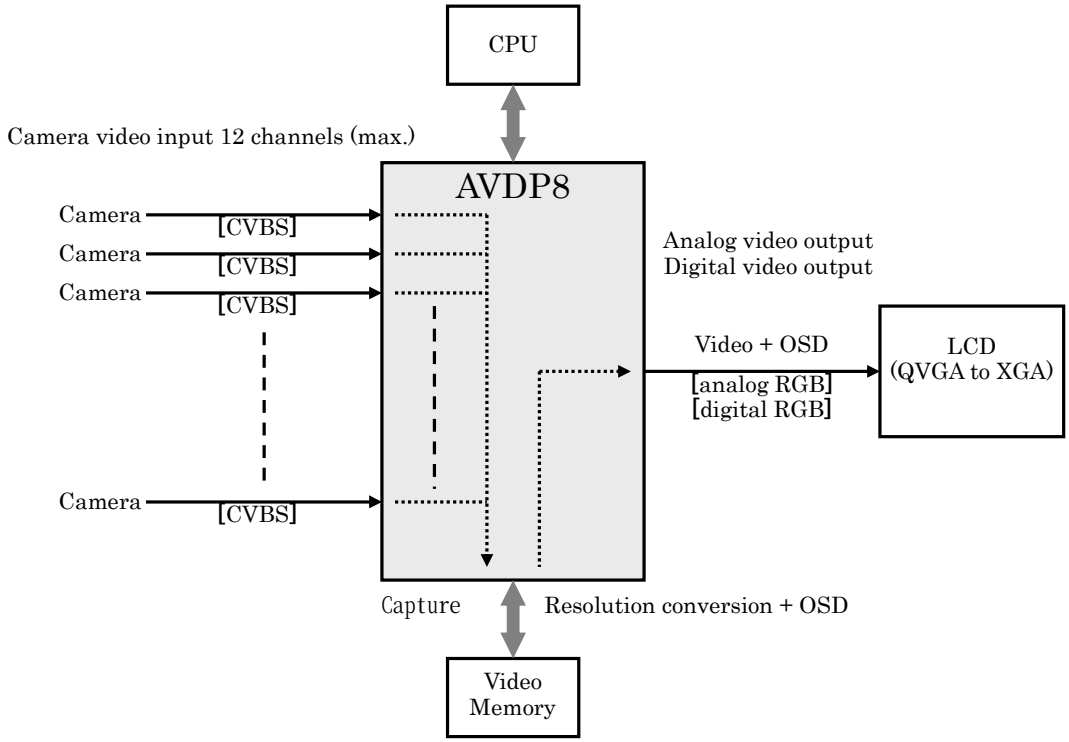
- Supply Voltage 3.3V and 1.8V
- Package Lead-free 329-pin BGA
- Operating Ambient Temp. -40°C to 85°C

■ Block Diagram

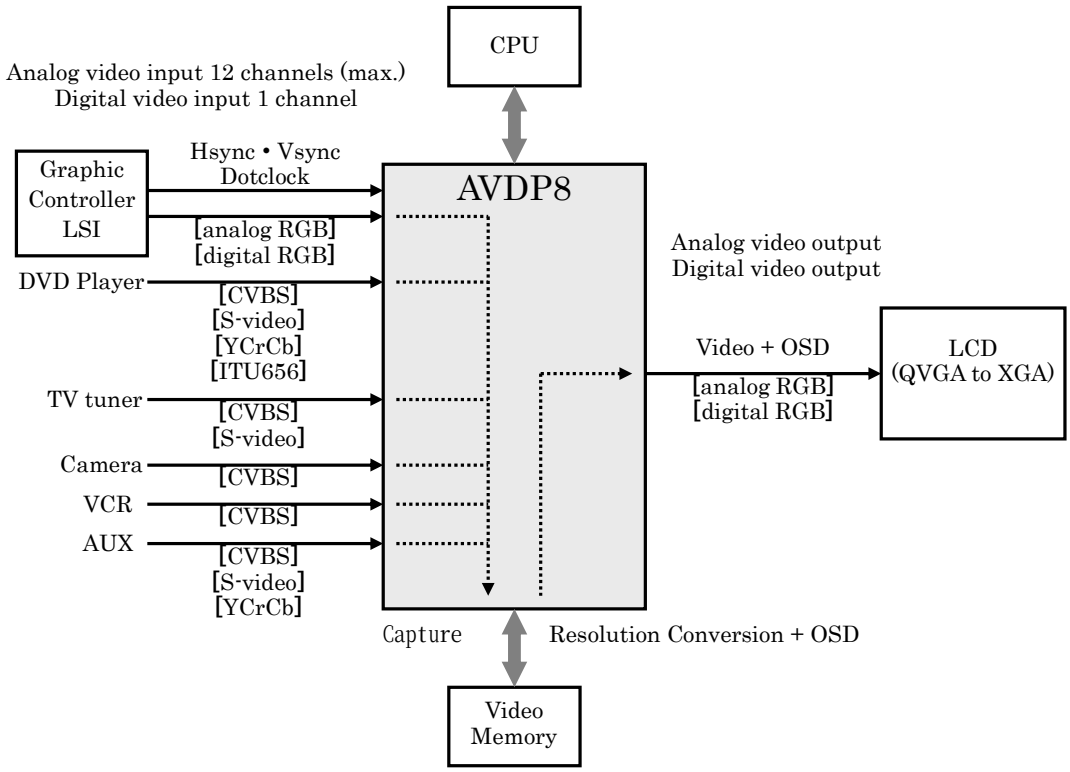


■ Example of System Configuration

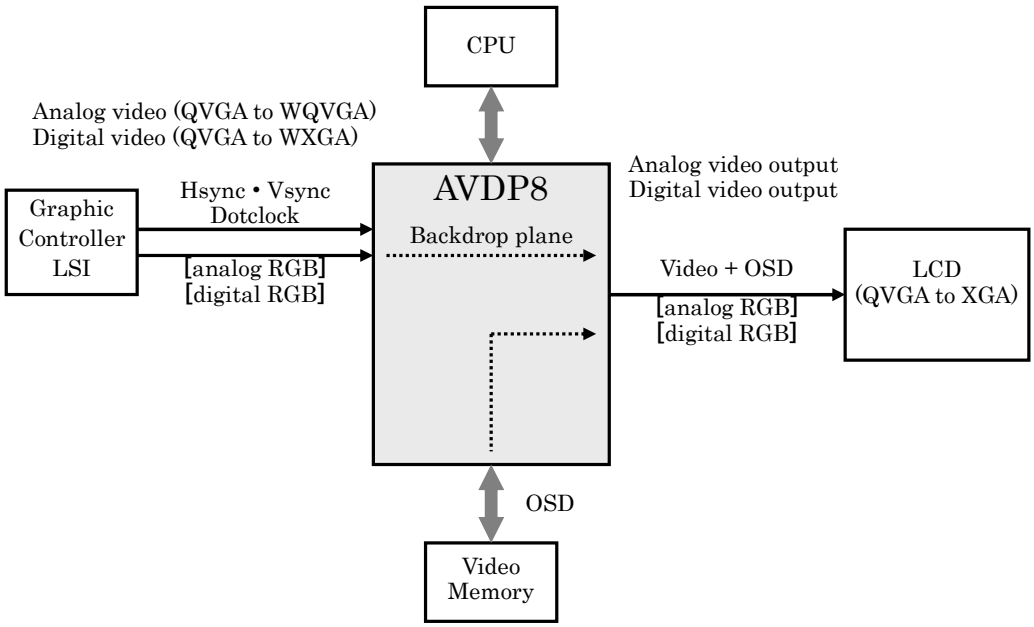
・Camera monitoring system



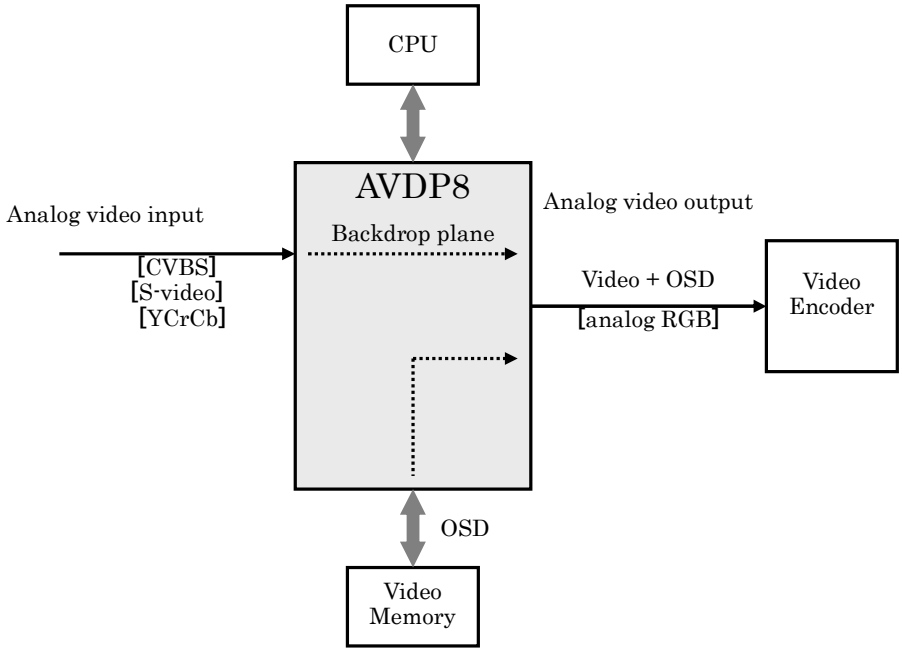
・In-car Rear Seat Entertainment system (RSE)



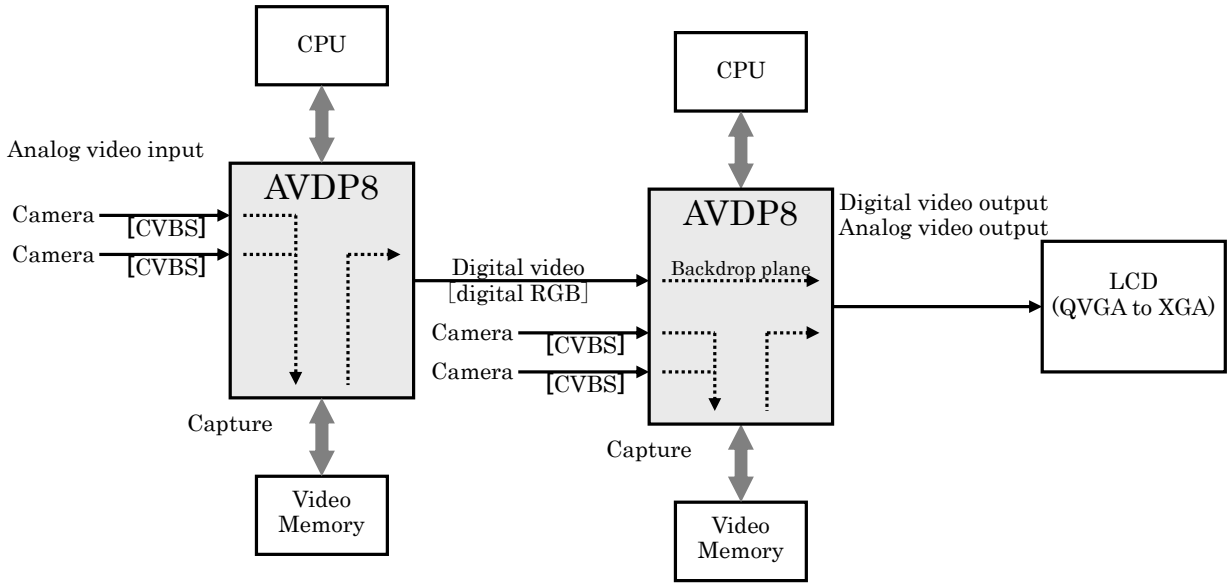
・OSD for panel resolution to video input



・OSD for analog video input



・4-plane simultaneous capture



■ Pin Function

Name	Qty	I/O	Function	Attribute	Drive
Power supply (111)					
VDD33	18	—	Digital power supply for PAD	—	—
VDD18	19	—	Digital power supply for internal circuit	—	—
VSS	33	—	Digital VSS (I/O, internal circuit)	—	—
PLLVDD	6	—	Power supply for PLL (1.8V) (2 PLLs × 3)	—	—
PLLVSS	6	—	VSS for PLL (2 PLLs ×3)	—	—
DACVDD	7	—	Power supply for DAC (1.8V)	—	—
DACVSS	7	—	VSS for DAC	—	—
AFEVDD	3	—	Power supply for AFE (3.3V)	—	—
AFEVSS	4	—	VSS for AFE	—	—
System Reset (1)					
RESET_N	1	IS	Reset input	5VT	—
Clock (6)					
XIN1	1	I	Clock input 1	—	—
XOUT1	1	O	Clock 1 Xtal connection pin	—	—
XIN2	1	I	Clock input 2	—	—
XOUT2	1	O	Clock 2 Xtal connection pin	—	—
REFCKS1-0	2	I	Reference Clock selection pin	5VT	—
CPU Interface (48)					
D15-0	16	I/O	CPU data bus	5VT	8mA
A22-2	21	I	CPU address bus	5VT	—
CSREG_N	1	I	Chip Select for register access	5VT	—
CSMEM_N	1	I	Chip Select for video memory access	5VT	—
RD_N	1	I	Read Pulse	5VT	—
WR3_N/A1	1	I	Write Pulse/CPU address	5VT	—
WR2_N/LEND_N	1	I	Write Pulse/Endian control	5VT	—
WR1-0_N	2	I	Write Pulse	5VT	—
WAIT_N	1	OT	Bus Wait	5VT	8mA
READY_N	1	OT	Bus Ready	5VT	8mA
INT_N	1	OD	Interrupt output	5VT	8mA
C32_N	1	I	CPU bus width selection	5VT	—
Video Memory Interface (91)					
SDQ63-0	64	I/O	Video memory data bus	—	8mA
SA11-0	12	O	Video memory address bus	—	8mA
SBA1-0	2	O	Video memory bank address bus	—	8mA
SRAS_N	1	O	Video memory row address strobe	—	8mA
SCAS_N	1	O	Video memory column address strobe	—	8mA
SWE_N	1	O	Video memory write enable	—	8mA
SDQM7-0	8	O	Video memory data mask	—	8mA
SDCLKO	1	O	Clock output for video memory	—	12mA
SDCLKI	1	I	Clock input for video memory	—	—
Video Input Interface (48)					
GI23-8/D31-16	16	I/O	Video input/CPU data bus	5VT	8mA
GI7-0	8	I	Video input	5VT	—
AVSIN0_N	1	I	Analog video channel 0 Vertical sync input	5VT	—
AHSIN0_N	1	I	Analog video channel 0 Horizontal sync input	5VT	—

AGCKIN0	1	I	Analog video channel 0 Sync clock input	5VT	—
DGCKIN0	1	I	Digital video channel 0 Sync clock input	5VT	—
AIN11-0	12	I	Analog video input	AN	—
VCM_0	1	I	ADC_0 reference input	AN	—
VCM_1	1	I	ADC_1 reference input	AN	—
VCM_2	1	I	ADC_2 reference input	AN	—
VCM	1	O	Common mode voltage output	AN	—
VREFP	1	O	Positive reference voltage pin for ADC	AN	—
VREFN	1	O	Negative reference voltage pin for ADC	AN	—
VBG	1	O	Band gap voltage pin	AN	—
IBEXT	1	O	Bias voltage monitor pin	AN	—
Monitor Interface (29)					
R,G,B	3	O	Analog video output	AN	—
COMP	1	O	Correction pin for DAC	AN	—
VREFIN	1	I	Reference voltage input for DAC	AN	—
VREFOUT	1	O	Reference voltage output for DAC	AN	—
RSET	1	I/O	Amplitude control resistor connection pin	AN	—
DRO5-0	6	O	Digital video R output	—	8mA
DGO5-0	6	O	Digital video G output	—	8mA
DBO5-0	6	O	Digital video B output	—	8mA
VSYNC_N	1	O	Vertical sync signal output	—	8mA
HCSYNC_N	1	O	Horizontal sync/composite sync signal output	—	8mA
BLANK_N	1	O	Display timing output	—	8mA
DOTCLK	1	O	Dot clock output	—	8mA
Test pin (3)					
XTEST2-0	3	I	Test pin	5VT	—

I: Input pin IS: Input pin with Schmitt trigger
O: Output pin OT: 3-state output pin OD: Open Drain
I/O: Input/Output pin
5VT: 5V Tolerant pin
AN: ANalog pin

■ Pin Arrangement Diagram

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	
23	A13	A12	A10	A7	A3	WR2_N/ LEND_N	CS MEM_N	DOT CLK	DBO5	DBO2	DGO4	DGO0	DRO3	XOUT2	PLL VDD	PLL VSS	DAC VSS	VREFIN	DAC VDD	G	B	DAC VDD	DAC VSS	23
22	A14	A11	A9	A6	A2	WR1_N	CS REG_N	BLA NK_N	VSS	DBO1	DGO3	DRO5	DRO2	XIN2	PLL VSS	PLL VDD	DAC VSS	RSET	R	DAC VSS	DAC VSS	VDD33	VSS	22
21	A16	A15	A8	A5	WR3_N/ A1	WRO_N	VSS	HCS YNC_N	DBO4	DBO0	DGO2	VSS	DRO1	VSS	PLL VSS	DAC VDD	DAC VDD	COMP	DAC VSS	DAC VDD	SDQ52	SDQ55	SDQ54	21
20	A19	A18	A17	A4	VDD18	RD_N	VDD33	VSY NC_N	DBO3	DGO5	DGO1	DRO4	DRO0	VDD33	PLL VDD	DAC VDD	VREF OUT	DAC VSS	DAC VDD	VSS	SDQ51	SDQ53	SDQ56	20
19	VDD33	A22	A21	A20																VDD18	SDQ50	SDQ57	SDQ58	19
18	INT_N	READY_ N	WAIT_N	VSS																SDQ49	VDD33	SDQ59	SDQ60	18
17	D3	D2	D1	D0						TOP VIEW										VDD18	SDQ48	SDQ61	SDQ62	17
16	D6	D5	D4	VSS																SDQM6	SDQM4	VSS	SDQ63	16
15	D9	VDD33	D8	D7																VSS	SDQ39	SDQM7	SDQM5	15
14	D12	D11	VSS	D10						VDD33	VSS	VDD18	VSS	VDD33						SDQ37	SDQ38	SDQ40	VDD33	14
13	GI8/ D16	D15	D14	D13						VSS	VDD18	VDD18	VDD18	VSS						SDQ36	VSS	SDQ41	SDQ42	13
12	GI12/ D20	GI11/ D19	GI10/ D18	GI9/ D17						VDD18	VDD18	VDD18	VDD18	VDD18						SDQ34	SDQ35	SDQ43	SDQ44	12
11	GI16/ D24	GI15/ D23	GI14/ D22	GI13/ D21						VSS	VDD18	VDD18	VDD18	VSS						SDQ32	SDQ33	SDQ45	VSS	11
10	GI19/ D27	GI18/ D26	GI17/ D25	VSS						VDD33	VSS	VDD18	VSS	VDD33						SA1	SA2	SDQ46	SDQ47	10
9	GI23/ D31	GI22/ D30	GI21/ D29	GI20/ D28																VSS	SA0	SA3	SA4	9
8	VSS	VDD33	C32_N	VDD18																SA10	SBA1	SA5	VDD33	8
7	REF CKS1	XTEST0	XTEST1	XTEST2																SBA0	VSS	SA6	SA7	7
6	REF CKSO	VSS	VDD33	VDD18																VDD18	SA11	SA8	SA9	6
5	GI2	GI1	GI0	RESET_ N																VDD33	SDCLKI	VSS	SD CLKO	5
4	GI6	GI5	GI4	GI3	PLL VDD	AFE VDD	AIN9	AIN5	AIN1	VCM_2	AFE VSS	AFE VDD	SDQ0	VSS	SDQ3	SDQ5	SDQ7	SDQM2	SDQ17	SDQ19	SRAS_N	SWE_N	SCAS_N	4
3	AHSINO _N	AVSINO _N	GI7	PLL VSS	PLL VSS	AFE VSS	AIN8	AIN4	AIN0	VREFP	IBEXT	VSS	SDQ1	SDQ2	SDQ4	SDQ6	SDQM0	SDQ16	SDQ18	SDQ20	SDQ21	SDQ22	SDQ23	3
2	DG CKINO	AG CKINO	VSS	PLL VDD	AFE VSS	AIN11	AIN7	AIN3	VCM_0	VREFN	VBG	VDD33	SDQ14	SDQ12	VDD33	SDQ10	SDQ8	SDQM3	SDQ30	SDQ29	VDD33	SDQ27	SDQ24	2
1	XIN1	XOUT1	PLL VDD	PLL VSS	VCM	AIN10	AIN6	AIN2	VCM_1	AFE VDD	AFE VSS	SDQ15	SDQ13	SDQ11	VSS	SDQ9	SDQM1	SDQ31	VSS	SDQ28	VSS	SDQ26	SDQ25	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	

■ **Pin Assignment Table**

No.	Pin Number	Pin Name	IO
1	A1	XIN1	I
2	A2	DGCKIN0	I
3	A3	AHSIN0_N	I
4	A4	GI6	I
5	A5	GI2	I
6	A6	REFCKS0	I
7	A7	REFCKS1	I
8	A8	VSS	
9	A9	GI23/D31	IO
10	A10	GI19/D27	IO
11	A11	GI16/D24	IO
12	A12	GI12/D20	IO
13	A13	GI8/D16	IO
14	A14	D12	IO
15	A15	D9	IO
16	A16	D6	IO
17	A17	D3	IO
18	A18	INT_N	OT
19	A19	VDD33	
20	A20	A19	I
21	A21	A16	I
22	A22	A14	I
23	A23	A13	I
24	B1	XOUT1	O
25	B2	AGCKIN0	I
26	B3	AVSIN0_N	I
27	B4	GI5	I
28	B5	GI1	I
29	B6	VSS	
30	B7	XTEST0	I
31	B8	VDD33	
32	B9	GI22/D30	IO
33	B10	GI18/D26	IO
34	B11	GI15/D23	IO
35	B12	GI11/D19	IO
36	B13	D15	IO
37	B14	D11	IO
38	B15	VDD33	
39	B16	D5	IO
40	B17	D2	IO
41	B18	READY_N	OT
42	B19	A22	I
43	B20	A18	I
44	B21	A15	I
45	B22	A11	I
46	B23	A12	I
47	C1	PLLVDD	
48	C2	VSS	
49	C3	GI7	I
50	C4	GI4	I
51	C5	GI0	I
52	C6	VDD33	
53	C7	XTEST1	I
54	C8	C32_N	I
55	C9	GI21/D29	IO
56	C10	GI17/D25	IO
57	C11	GI14/D22	IO
58	C12	GI10/D18	IO
59	C13	D14	IO
60	C14	VSS	
61	C15	D8	IO
62	C16	D4	IO
63	C17	D1	IO
64	C18	WAIT_N	OT
65	C19	A21	I
66	C20	A17	I
67	C21	A8	I
68	C22	A9	I
69	C23	A10	I
70	D1	PLLVSS	
71	D2	PLLVDD	
72	D3	PLLVSS	
73	D4	GI3	I
74	D5	RESET_N	I$
75	D6	VDD18	
76	D7	XTEST2	I
77	D8	VDD18	
78	D9	GI20/D28	IO
79	D10	VSS	
80	D11	GI13/D21	IO
81	D12	GI9/D17	IO
82	D13	D13	IO
83	D14	D10	IO
84	D15	D7	IO
85	D16	VSS	
86	D17	D0	IO
87	D18	VSS	
88	D19	A20	I
89	D20	A4	I
90	D21	A5	I
91	D22	A6	I
92	D23	A7	I
93	E1	VCM	AO
94	E2	AFEVSS	

No.	Pin Number	Pin Name	IO
95	E3	PLLVSS	
96	E4	PLLVDD	
97	E20	VDD18	
98	E21	WR3_N/A1	I
99	E22	A2	I
100	E23	A3	I
101	F1	AIN10	AI
102	F2	AIN11	AI
103	F3	AFEVSS	
104	F4	AFEVDD	
105	F20	RD_N	I
106	F21	WR0_N	I
107	F22	WR1_N	I
108	F23	WR2_N/LEND_N	I
109	G1	AIN6	AI
110	G2	AIN7	AI
111	G3	AIN8	AI
112	G4	AIN9	AI
113	G20	VDD33	
114	G21	VSS	
115	G22	CSREG_N	I
116	G23	CSMEM_N	I
117	H1	AIN2	AI
118	H2	AIN3	AI
119	H3	AIN4	AI
120	H4	AIN5	AI
121	H20	VSYNC_N	O
122	H21	HCSYNC_N	O
123	H22	BLANK_N	O
124	H23	DOTCLK	O
125	J1	VCM_1	AI
126	J2	VCM_0	AI
127	J3	AIN0	AI
128	J4	AIN1	AI
129	J20	DBO3	O
130	J21	DBO4	O
131	J22	VSS	
132	J23	DBO5	O
133	K1	AFEVDD	
134	K2	VREFN	AO
135	K3	VREFP	AO
136	K4	VCM_2	AI
137	K10	VDD33	
138	K11	VSS	
139	K12	VDD18	
140	K13	VSS	
141	K14	VDD33	

No.	Pin Number	Pin Name	IO
142	K20	DGO5	O
143	K21	DBO0	O
144	K22	DBO1	O
145	K23	DBO2	O
146	L1	AFEVSS	
147	L2	VBG	AO
148	L3	IBEXT	AO
149	L4	AFEVSS	
150	L10	VSS	
151	L11	VDD18	
152	L12	VDD18	
153	L13	VDD18	
154	L14	VSS	
155	L20	DGO1	O
156	L21	DGO2	O
157	L22	DGO3	O
158	L23	DGO4	O
159	M1	SDQ15	IO
160	M2	VDD33	
161	M3	VSS	
162	M4	AFEVDD	
163	M10	VDD18	
164	M11	VDD18	
165	M12	VDD18	
166	M13	VDD18	
167	M14	VDD18	
168	M20	DRO4	O
169	M21	VSS	
170	M22	DRO5	O
171	M23	DGO0	O
172	N1	SDQ13	IO
173	N2	SDQ14	IO
174	N3	SDQ1	IO
175	N4	SDQ0	IO
176	N10	VSS	
177	N11	VDD18	
178	N12	VDD18	
179	N13	VDD18	
180	N14	VSS	
181	N20	DRO0	O
182	N21	DRO1	O
183	N22	DRO2	O
184	N23	DRO3	O
185	P1	SDQ11	IO
186	P2	SDQ12	IO
187	P3	SDQ2	IO
188	P4	VSS	

No.	Pin Number	Pin Name	IO
189	P10	VDD33	
190	P11	VSS	
191	P12	VDD18	
192	P13	VSS	
193	P14	VDD33	
194	P20	VDD33	
195	P21	VSS	
196	P22	XIN2	I
197	P23	XOUT2	O
198	R1	VSS	
199	R2	VDD33	
200	R3	SDQ4	IO
201	R4	SDQ3	IO
202	R20	PLLVDD	
203	R21	PLLVSS	
204	R22	PLLVSS	
205	R23	PLLVDD	
206	T1	SDQ9	IO
207	T2	SDQ10	IO
208	T3	SDQ6	IO
209	T4	SDQ5	IO
210	T20	DACVDD	
211	T21	DACVDD	
212	T22	PLLVDD	
213	T23	PLLVSS	
214	U1	SDQM1	O
215	U2	SDQ8	IO
216	U3	SDQM0	O
217	U4	SDQ7	IO
218	U20	VREFOUT	AO
219	U21	DACVDD	
220	U22	DACVSS	
221	U23	DACVSS	
222	V1	SDQ31	IO
223	V2	SDQM3	O
224	V3	SDQ16	IO
225	V4	SDQM2	O
226	V20	DACVSS	
227	V21	COMP	AO
228	V22	RSET	AIO
229	V23	VREFIN	AI
230	W1	VSS	
231	W2	SDQ30	IO
232	W3	SDQ18	IO
233	W4	SDQ17	IO
234	W20	DACVDD	
235	W21	DACVSS	

No.	Pin Number	Pin Name	IO
236	W22	R	AO
237	W23	DACVDD	
238	Y1	SDQ28	IO
239	Y2	SDQ29	IO
240	Y3	SDQ20	IO
241	Y4	SDQ19	IO
242	Y5	VDD33	
243	Y6	VDD18	
244	Y7	SBA0	O
245	Y8	SA10	O
246	Y9	VSS	
247	Y10	SA1	O
248	Y11	SDQ32	IO
249	Y12	SDQ34	IO
250	Y13	SDQ36	IO
251	Y14	SDQ37	IO
252	Y15	VSS	
253	Y16	SDQM6	O
254	Y17	VDD18	
255	Y18	SDQ49	IO
256	Y19	VDD18	
257	Y20	VSS	
258	Y21	DACVDD	
259	Y22	DACVSS	
260	Y23	G	AO
261	AA1	VSS	
262	AA2	VDD33	
263	AA3	SDQ21	IO
264	AA4	SRAS_N	O
265	AA5	SDCLKI	I
266	AA6	SA11	O
267	AA7	VSS	
268	AA8	SBA1	O
269	AA9	SA0	O
270	AA10	SA2	O
271	AA11	SDQ33	IO
272	AA12	SDQ35	IO
273	AA13	VSS	
274	AA14	SDQ38	IO
275	AA15	SDQ39	IO
276	AA16	SDQM4	O
277	AA17	SDQ48	IO
278	AA18	VDD33	
279	AA19	SDQ50	IO
280	AA20	SDQ51	IO
281	AA21	SDQ52	IO
282	AA22	DACVSS	

No.	Pin Number	Pin Name	IO
283	AA23	B	AO
284	AB1	SDQ26	IO
285	AB2	SDQ27	IO
286	AB3	SDQ22	IO
287	AB4	SWE_N	O
288	AB5	VSS	
289	AB6	SA8	O
290	AB7	SA6	O
291	AB8	SA5	O
292	AB9	SA3	O
293	AB10	SDQ46	IO
294	AB11	SDQ45	IO
295	AB12	SDQ43	IO
296	AB13	SDQ41	IO
297	AB14	SDQ40	IO
298	AB15	SDQM7	O
299	AB16	VSS	
300	AB17	SDQ61	IO
301	AB18	SDQ59	IO
302	AB19	SDQ57	IO
303	AB20	SDQ53	IO
304	AB21	SDQ55	IO
305	AB22	VDD33	
306	AB23	DACVDD	
307	AC1	SDQ25	IO
308	AC2	SDQ24	IO
309	AC3	SDQ23	IO
310	AC4	SCAS_N	O
311	AC5	SDCLKO	O
312	AC6	SA9	O
313	AC7	SA7	O
314	AC8	VDD33	
315	AC9	SA4	O
316	AC10	SDQ47	IO
317	AC11	VSS	
318	AC12	SDQ44	IO
319	AC13	SDQ42	IO
320	AC14	VDD33	
321	AC15	SDQM5	O
322	AC16	SDQ63	IO
323	AC17	SDQ62	IO
324	AC18	SDQ60	IO
325	AC19	SDQ58	IO
326	AC20	SDQ56	IO
327	AC21	SDQ54	IO
328	AC22	VSS	
329	AC23	DACVSS	

The meaning of the symbol shown in IO is as follows.

I: Input
I$: Schmitt trigger input
IO: Input/Output
O: Output
OD: Open Drain output
OT: 3-state output
AI: Analog Input
AO: Analog Output
AIO: Analog Input/Output

■ Pin Function

3.3 V is used for I/O pin power supply in this LSI; therefore, it interfaces with peripheral circuits at 3.3 V. However, since tolerant voltage up to 5V is guaranteed for Input/Output pins specified as 5VT, these pins can be connected to 5V TTL level-compatible devices.

・How to pull-up or pull-down:
- ―This LSI has neither pull-up resistor nor pull-down resistor in it, so please use external pull-up or pull-down resistor.
- ―Use a separate resistor for each input/output pin to pull it up or pull it down externally.
- ―A common pull-up or pull-down resistor can be used to fix input pins to a potential.
- ―Use a resistor lower than 7kΩ to pull down the Tolerant pin to GND level.

1) Power Supply

The kinds of power supplies and its supply voltages are as follows.

Kinds of Power Supplies	Name	Standard Voltage
Power Supply for I/O pins	VDD33	3.3V
Power Supply for Internal Circuits	VDD18	1.8V
Power Supply for analog front-end	AFEVDD	3.3V
Power Supply for PLL	PLLVDD	1.8V
Power Supply for DAC	DACVDD	1.8V

・Power-on Procedure

－Power on the 1.8V power supplies and then power on the 3.3V power supplies. The power-on procedure between the power supplies with the same standard voltage is arbitrary.

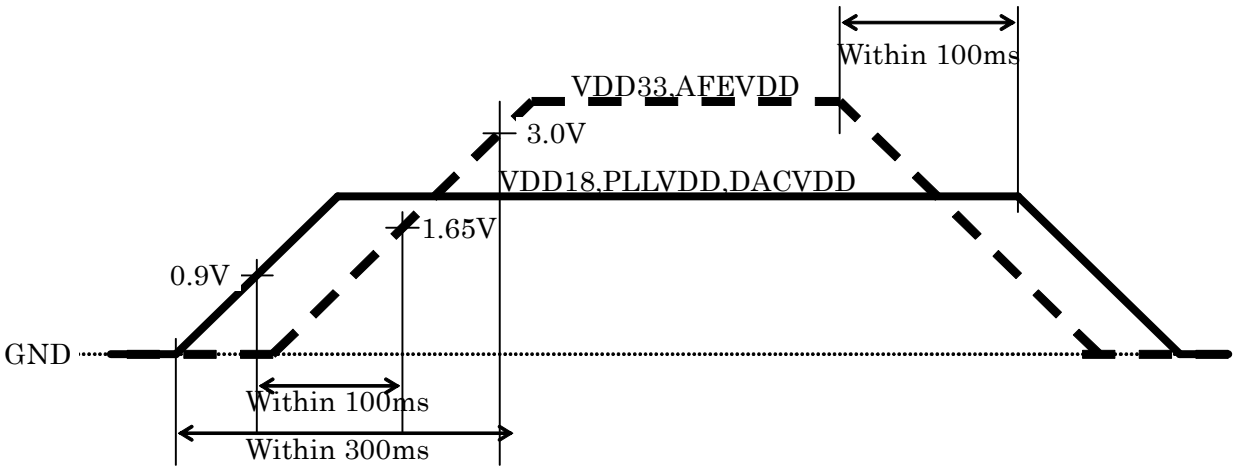
－The time from when any of 1.8V power supplies is powered on till when all the power supplies reach at the lower limit of the recommended operating voltage should be within 300ms.

－The time from when any of 1.8V power supplies reaches at 0.9V till when all the 3.3V power supplies reach at 1.65V should be within 100ms.

・Power-off Procedure

－Power off the 3.3V power supplies and then power off the 1.8V power supplies. The power-off procedure between the power supplies with the same standard voltage is arbitrary.

－The time from when any of 1.8V power supplies is powered off till when all the 3.3V power supplies are powered off should be within 100ms.



- **VDD33**
- **VDD18**
- **VSS**

VDD33 is power supply pin for I/O pins. Connect 3.3V to the VDD33 pin.
VDD18 is power supply pin for internal circuits. Connect 1.8V to VDD18 pin.
VSS is Ground pin common to both I/O pins and internal circuits. Connect the Ground level to VSS pin.

- **AFEVDD**
- **AFEVSS**

  These are power supply pins for AFE.
  Connect 3.3V to AFEVDD pin and connect the Ground level to AFEVSS pin.

- **PLLVDD**
- **PLLVSS**

  These are power supply pins for PLL.
  Connect 1.8V to PLLVDD pin and connect the Ground level to PLLVSS pin.

- **DACVDD**
- **DACVSS**

  These are analog power supply pins for the built-in DAC.
  Connect 1.8V to DACVDD pin and connect the Ground level to DACVSS pin.

2) System Reset

This LSI must be initialized at power-on.

- **RESET_N**
  This is Reset pin. The reset signal for a given time must be input after the power-on.
  This is an active low signal.
  RESET_N pin uses a schmitt trigger buffer.

3) Clock

- **XIN1**
- **XOUT1**

These are Xtal oscillation input pins. Connect a Xtal resonator between XIIN1 and XOUT1 pins to generate a clock.
When an external clock is used, connect it to XIN1 pin.
The frequency that can be input to XIN1 pin is 27MHz.
A clock that inputs to XIN1 pin is used as an operation clock of built-in video decoder and as a reference clock of a PLL for system clock.
The operation clock of built-in video decoder and the reference clock of a PLL for system clock can be generated from a clock that is input to DGCKIN0 pin. In that case, no clock is necessary to input to XIN1 pin. And, at this time, tie XIN1 pin to “L” level externally. No-connection is required for XOUT1.

- **XIN2**
- **XOUT2**

These are Xtal oscillation input pins. Connect a Xtal resonator between XIIN2 and XOUT2 pins to generate a clock.
When an external clock is used, connect it to XIN2 pin.
The frequency that can be generated with XIN2 and XOUT2 pins is in the range of 5MHz to 30MHz.
The frequency that can be input to XIN2 pin is in the range of 5MHz to 75MHz.
Please input a source clock to XIN2 pin for generating the internal dot clock.
When the dot clock is generated from a clock other than the clock from XIN2 pin, it is necessary to input a clock to XIN2 pin. In that case, tie XIN2 pin to “L” level externally. No-connection is required for XOUT2 pin.

- **REFCKS1-0**

These are pins for selecting a reference clock of a PLL for system clock.
Please do settle the input level of REFCKS1-0 pin during RESET_N= "L" at power-on, and during operation, do not change the input level.

4) CPU Interface

- **C32_N**

  This pin selects a data bus width of the CPU interface.

  Since this LSI shares pins between CPU interface pin and Video input pin, the pin function varies depending on a data bus width (32bit or 16bit) of CPU interface.

  Please do settle the input level of C32_N pin during RESET_N= "L" at power-on, and during operation, do not change the input level.

- **D31-0**

  These are CPU data bus pins, connecting to the external data bus of CPU.

  When a CPU data bus width of 16bit is used (C32_N=H), use only D15-0 pins.

  These pins become output pins when RD_N pin is asserted at the time either of CSREG_N or CSMEM_N pins is in active state, and with the other cases, they become input pins.

  D31-0 pin does not have any pull-up resistor inside, so please pull it up externally.

- **A22-1**

  These are CPU address bus pins, connecting to CPU external address bus.

  When a CPU data bus width of 32bit is used (C32_N=L), use only A22-2 pins.

  Address input to A22-14 pins is ignored when accessing to the register area.

- **CSREG_N**
- **CSMEM_N**

  CSREG_N pin is a chip select pin for the register space. When CSREG_N pin is in the active state, input to WR3-0_N and RD_N pins becomes valid and this enables access to the register space.

  CSMEM_N pin is a chip select pin for video memory space. When CSMEM_N pin is in the active state, input to WR3-0_N and RD_N pins becomes valid and this enables access to the video memory space.

  Connect both CSREG_N pin and CSMEM_N pin to the chip select signals for external device of CPU.

  When sharing the same external space between this LSI and other device, connect the CPU chip select signals to CSREG_N pin and CSMEM_N pin after gating the chip select signals with the address decode signal.

  Both CSREG_N and CSMEM_N pins are low active signal.

- **RD_N**

  This pin is used to input a data read strobe signal from CPU.

  Asserting RD_N pin when CSREG_N pin is in the active state can read data from the register space.

  Asserting RD_N pin when CSMEM_N pin is in the active state can read data from the video memory space.

  This is an active low signal.

- **WR3-0_N**

  This pin is used to input a data write strobe signal from CPU.

  Asserting WR3-0_N pin when CSREG_N pin is in the active state can write data into the register space.

  Asserting WR3-0_N pin when CSMEM_N pin is in the active state can write data into the video memory space.

  When data bus width of 16bit is used (C32_N=H), only WR1_N and WR0_N pin is used.

  This is an active low signal.

- **WAIT_N**

  This pin outputs a bus wait request signal to CPU.

  When either of CSREG_N or CSMEM_N pins is in the active state, WAIT_N pin drives to "H" or "L" level. In other conditions, WAIT_N pin becomes Hi-Z state.

  WAIT_N pin does not have a pull-up resistor inside, so pull it up externally.

  This is an active low signal.

- **READY_N**

  This pin is used to output Bus Ready signal to CPU.

  When READY_N mode is Hi-z mode, READY_N pin drives logic “H” or “L” at a time when either of CSREG_N pin or CSMEM_N pin is in the active state, and in other states, READY_N pin becomes Hi-z state.

  When READY_N mode is Lo-z mode, it always drives logic “H” or “L.”

  READY_N pin does not have a pull-up resistor inside, so pull it up externally.

  This is an active low signal.

- **INT_N**

  This pin outputs an interrupt signal to CPU.

  INT_N signal is asserted when the flag, which indicates that Interrupt Enable bit is set to "1", is set in the internal register.

  INT_N signal is negated and turned into Hi-z state when the flag bit is reset by writing to the bit or when “0” is set to the Interrupt Enable bit.

  INT_N pin does not have a pull-up resistor inside, so pull it up externally.

  This is an active low signal.

- **LEND_N**

  This pin selects a type of CPU data alignment when 16bit of CPU interface data bus width is used (C32_N=H).

  This pin is not used when 32bit of CPU interface data bus width is used (C32_N=L).

  Please do settle the input level of LEND_N pin during RESET_N= “L” at power-on, and during operation, do not change the input level.

5) Video Memory Interface

- **SDCLKO**
  This is a clock output of the video memory.

- **SDCLKI**
  This is a clock input of the video memory.
  Connect this pin to SDCLKO pin.

- **SDQ63-0**
  These are data input/output bus pins for the video memory.
  SDQ63-0 pins are used as output pins only when performing write access to the video memory and are used as input pins in other cases.
  When 32bit of data bus width is set for the video memory, SDQ63-32 pins are always used as input pins. In this case, pull up SDQ63-32 pins externally.
  SDQ63-0 pins do not have a pull-up resistor inside, so pull it up externally.

- **SA11-0**
  These are address bus output pins for the video memory.
  SA11 pin is not used when video memory size is 64Mbit and bus width is 32bit or the memory size is 128Mbit and bus width is 64bit. At this time, no-connection is required for SA11 pin.

- **SBA1-0**
  These are bank address output pins for the video memory.

- **SRAS_N**
  This is a row address strobe output pin for the video memory.
  This is an active low signal.

- **SCAS_N**
  This is a column address strobe output pin for the video memory.
  This is an active low signal.

- **SWE_N**
  This is a write strobe output pin for the video memory.
  This is an active low signal.

- **SDQM7-0**
  These are write mask enable output pins for the video memory.
  SDQM7 pin is a data mask signal for SDQ63-56 pins; likewise, SDQM6 pin is for SDQ55-48 pins, SDQM5 pin is for SDQ47-40 pins, SDQM4 pin is for SDQ39-32 pins, SDQM3 pin is for SDQ31-24 pins, SDQM2 pin is for SDQ23-16 pins, SDQM1 pin is for SDQ15-8 pins, SDQM0 pin is for SDQ7-0 pins.
  When video memory bus width of 32bit is used, SDQM7-4 pins are not used. At this time, no-connection is required for SDQM7-4 pins.
  This is an active high signal.

6) Video Input Interface

- **DGCKIN0**

  This pin is used to input a dot clock synchronizing with digital video when inputting digital video in RGB666 format.

  And, this pin is used to input a dot clock synchronizing with channel 0 digital video when inputting digital video in ITU-R BT.656 format.

  When DGCKIN0 pin is not used, tie this pin to "L" level externally.

- **DGCKIN1**

  This pin is used to input a dot clock synchronizing with channel 1 digital video when inputting digital video in RGB666 format.

  When DGCKIN1 pin is not used, tie this pin to "L" level externally.

- **DRI5-0**
- **DGI5-0**
- **DBI5-0**

  These are RGB format digital RGB input pins.

  DRI5-0, DGI5-0, and DBI5-0 pins are enabled by setting CPU interface data bus width and digital video input format.

  When DRI5-0, DGI5-0, and DBI5-0 pins are not used, tie there pins to "H" or "L" level externally.

- **D0IN7-0**

  This pin is used to input the channel 0 digital video when inputting digital video in ITU-R BT.656 format.

  D0IN7-0 pins are enabled by setting CPU interface data bus width and digital video input format.

  When these pins are not used, tie there pins to "H" or "L" level externally.

- **D1IN7-0**

  This pin is used to input the channel 1 digital video when inputting digital video in ITU-R BT.656 format.

  D1IN7-0 pins are enabled by setting CPU interface data bus width and digital video input format.

  When these pins are not used, tie there pins to "H" or "L" level externally.

- **DVSIN_N**

  This pin is used to input the vertical sync signal of digital video when inputting digital video in RGB666 format.

  DVSIN_N pin is enabled by setting CPU interface data bus width and digital video input format.

  When this pin is not used, tie it to "H" level externally.

  This is an active low signal.

- **DHSIN_N**

  This pin is used to input the horizontal sync signal of digital video when inputting digital video in RGB666 format.

  DHSIN_N pin is enabled by setting CPU interface data bus width and digital video input format.

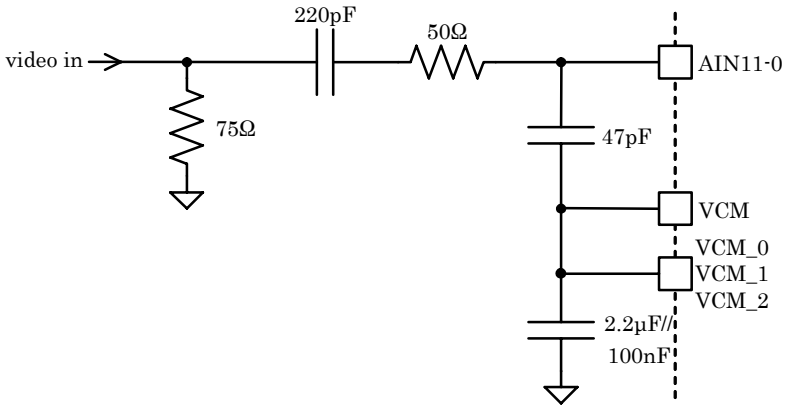
  When this pin is not used, tie it to "H" level externally.

  This is an active low signal.

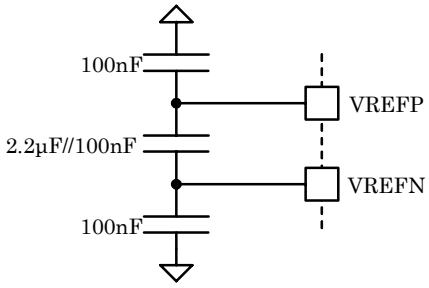
- **AIN11-0**
  This pin is used to input analog video.
  When analog video is not input, tie this pin to “L” externally.

- **VCM_0**
- **VCM_1**
- **VCM_2**
  There pins are used to input a common mode voltage of ADC_0, ADC_1, and ADC_2.
  When AFE is not used, tie VCM_0, VCM_1, and VCM_2 pins to “L” externally.

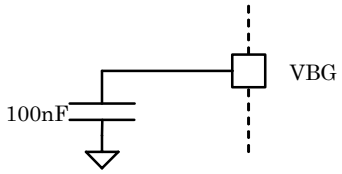
- **VCM**
  This is the common mode voltage output pin.
  Connect decoupling capacitors to VCM pins.
  When AFE is not used, no-connection is required for VCM pin.



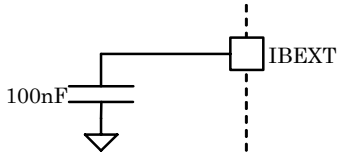
- **VREFP**
- **VREFN**
  These are ADC reference voltage pins.
  Connect decoupling capacitors to VREFP pin and VREFN pin.
  When AFE is not used, no-connection is required for VREFP pin and VREFN pin.



- **VBG**
  This is the band gap voltage pin.
  Connect a decoupling capacitor to VBG pin.
  When AFE is not used, no-connection is required for VBG pin.



- **IBEXT**
  This is the bias current pin.
  Connect a decoupling capacitor to IBEXT pin.
  When AFE is not used, no-connection is required for IBEXT pin.



- **AGCKIN0**
  This pin is used to input a dot clock of channel 0 analog RGB.
  When AGCKIN0 pin is not used, tie this pin to “L” externally.

- **AGCKIN1**
  This pin is used to input a dot clock of channel 1 analog RGB.
  AGCKIN1 pin is enabled by setting CPU interface data bus width and digital video input format.
  When AGCKIN1 pin is not used, tie this pin to “L” externally.

- **AGCKIN2**
  This pin is used to input a dot clock of channel 2 analog RGB.
  AGCKIN2 pin is enabled by setting CPU interface data bus width and digital video input format.
  When AGCKIN2 pin is not used, tie this pin to “L” externally.

- **AGCKIN3**
  This pin is used to input a dot clock of channel 3 analog RGB.
  AGCKIN3 pin is enabled by setting CPU interface data bus width and digital video input format.
  When AGCKIN3 pin is not used, tie this pin to “L” externally.

- **AVSIN0_N**
  This pin is used to input a vertical sync signal of channel 0 analog RGB.
  When AVSIN0_N pin is not used, tie this pin to “H” externally.
  This is an active low signal.

- **AVSIN1_N**
  This pin is used to input a vertical sync signal of channel 1 analog RGB.
  AVSIN1_N pin is enabled by setting CPU interface data bus width and digital video input format.
  When AVSIN1_N pin is not used, tie this pin to “H” externally.
  This is an active low signal.

- **AVSIN2_N**
  This pin is used to input a vertical sync signal of channel 2 analog RGB.
  AVSIN2_N pin is enabled by setting CPU interface data bus width and digital video input format.
  When AVSIN2_N pin is not used, tie this pin to “H” externally.
  This is an active low signal.

- **AVSIN3_N**
  This pin is used to input a vertical sync signal of channel 3 analog RGB.
  AVSIN3_N pin is enabled by setting CPU interface data bus width and digital video input format.
  When AVSIN3_N pin is not used, tie this pin to “H” externally.
  This is an active low signal.

- **AHSIN0_N**
  This pin is used to input a horizontal sync signal of channel 0 analog RGB.
  When AHSIN0_N pin is not used, tie this pin to “H” externally.
  This is an active low signal.

- **AHSIN1_N**
  This pin is used to input a horizontal sync signal of channel 1 analog RGB.
  AHSIN1_N pin is enabled by setting CPU interface data bus width and digital video input format.
  When AHSIN1_N pin is not used, tie this pin to “H” externally.
  This is an active low signal.

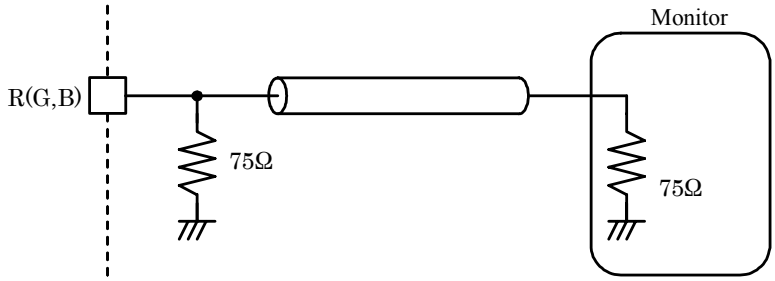
- **AHSIN2_N**
  This pin is used to input a horizontal sync signal of channel 2 analog RGB.
  AHSIN2_N pin is enabled by setting CPU interface data bus width and digital video input format.
  When AHSIN2_N pin is not used, tie this pin to “H” externally.
  This is an active low signal.

- **AHSIN3_N**
  This pin is used to input a horizontal sync signal of channel 3 analog RGB.
  AHSIN3_N pin is enabled by setting CPU interface data bus width and digital video input format.
  When AHSIN3_N pin is not used, tie this pin to “H” externally.
  This is an active low signal.
  This is an active low signal.

7) Monitor Interface

- **R**
- **G**
- **B**

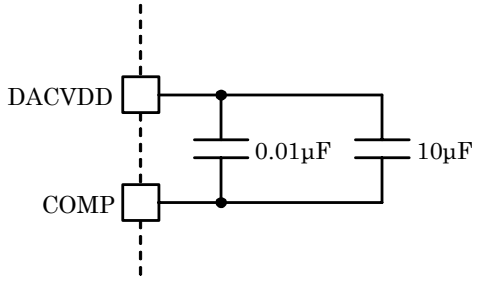
These are analog RGB output pins.
AVDP8 can directly drive a display monitor with an impedance of 75Ω.



When the analog RGB output is not used, no-connection is required for R, G, and B pin.

- **COMP**

This is a correction pin for RGB DAC.
Connect a ceramic capacitor of 0.01µF in parallel with a tantalum capacitor of 10µF between COMP pin and DACVDD pin.



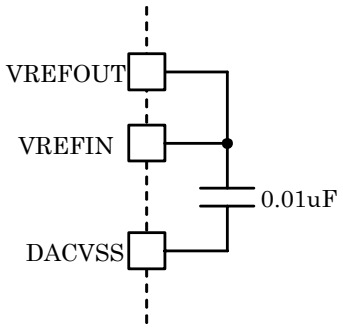
When the analog RGB output is not used, no-connection is required for COMP pin.

- **VREFIN**

This is the reference voltage input pin for RGB DAC.

- **VREFOUT**

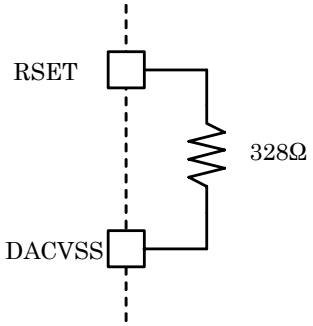
This is the reference voltage output pin for RGB DAC.
The reference voltage of 1.201V is output from this pin.
Connect VREFOUT pin to VREFIN pin. In addition, connect a ceramic capacitor of 0.01µF between this pin and DACVSS pin.



Also when the analog RGB output is not used, connect VREFOUT pin to VREFIN pin. At this time, no capacitor is required between VREFIN and DACVSS.

- **RSET**

  This pin is used to connect a resistor that adjusts RGB DAC amplitude.
  Connecting a resistor of 328Ω between RSET pin and DACVSS pin gives 0.7Vp-p output amplitude.



  The value for the amplitude adjustment resistor can be found by the following formula.

  R = VREFIN × 5.096 / IOFS

  VREFIN: a reference voltage that inputs to VREFIN pin (1.201V (standard))
  IOFS : Output current at the maximum amplitude (Max. amplitude/load resistance)

  When the analog RGB output is not used, no-connection is required for RSET pin.

- **DRO5-0**
- **DGO5-0**
- **DBO5-0**

  These pins output digital video signal.

- **VSYNC_N**

  This pin outputs vertical sync signal.
  This output can be inverted by the control of register setting.
  This is an active low signal.

- **HCSYNC_N**

  This pin outputs horizontal sync signal or composite sync signal.
  Setting the register selects horizontal sync signal or composite sync signal.
  This output can be inverted by the control of register setting.
  This is an active low signal.

- **BLANK_N**

  This pin outputs a signal that indicates a non-display period.
  This signal can be used to request a signal (DE) that indicates a display period with LCD panel etc.
  This is an active low signal.

- **DOTCLK**

  This pin outputs a dot clock.
  This output can be inverted by the control of register setting.

8) LSI Test

- **XTEST2–0**
  This is the test mode setting pin for device test.
  XTEST2-0 pin does not have a pull-up resistor, so pull it up externally.

■ Electrical Characteristics

- **Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit	Note
Supply Voltage (VDD33 pin)	V_{DD33}	-0.5 to +4.6	V	1
Supply Voltage（VDD18 pin）	V_{DD18}	-0.5 to +2.5	V	1
AFE Supply Voltage（AFEVDD pin）	V_{AFE}	-0.5 to +4.6	V	1
PLL Supply Voltage（PLLVDD pin）	V_{PLL}	-0.5 to +2.5	V	1
DAC Supply Voltage（DACVDD pin）	V_{DAC}	-0.5 to +2.5	V	1
Input pin voltage (5V tolerant pin)	V_I	-0.5 to +5.5	V	1
Input pin voltage (except the above)	V_I	-0.5 to VDD+0.5(≤4.6 Max.)	V	1
Output pin voltage (5V tolerant pin, Including input output pins)	V_O	-0.5 to +5.5	V	1
Output pin voltage (except the above)	V_O	-0.5 to VDD+0.5(≤4.6 Max.)	V	1
Input pin current	I_I	-20 to +20	mA	
Output pin current	I_O	-20 to +20	mA	
Storage Temperature	T_{stg}	-50 to +125	℃	

Note 1) This is the value on the basis of V_{SS}(GND)=0V.

- **Recommended Operating Conditions**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage (VDD33 pin)	V_{DD33}	3.0	3.3	3.6	V	1
Supply Voltage (VDD18 pin)	V_{DD18}	1.65	1.8	1.95	V	1
AFE Supply Voltage (AFEVDD pin)	V_{AFE}	3.0	3.3	3.6		1
PLL Supply Voltage (PLLVDD pin)	V_{PLL}	1.65	1.8	1.95	V	1
DAC Supply Voltage (DACVDD pin)	V_{DAC}	1.65	1.8	1.95	V	1
Operating Ambient Temperature	T_{OP}	-40		85	℃	

Note 1) This is the value on the basis of V_{SS}(GND)=0V.

• **DC Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Low level input voltage (XIN1,XIN2)	V_{IL}	-0.3		$0.3\times V_{DD33}$	V	1
Low level input voltage (except the above)	V_{IL}	-0.3		0.8	V	1
High level input voltage (XIN1,XIN2)	V_{IH}	$0.7\times V_{DD33}$		$V_{DD33}+0.3$	V	1
High level input voltage (5V tolerant pin)	V_{IH}	2.0		5.5	V	1
High level input voltage (except the above)	V_{IH}	2.0		$V_{DD33}+0.3$	V	1

Note 1) This is the value on the basis of V_{SS}(GND)=0V.

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit	Note
Low level output voltage (except XOUT1, XOUT2)	I_{OL}=100µA	V_{OL}	0		0.2	V	1
	I_{OL}=2mA	V_{OL}	0		0.4	V	1
High level output voltage (except XOUT1, XOUT2)	I_{OH}= -100µA	V_{OH}	V_{DD33}-0.2		V_{DD33}	V	1
	I_{OH}= -2mA	V_{OH}	2.4		V_{DD33}	V	1
Input leak current		I_{LI}	-10		+10	µA	
Output leak current		I_{LO}	-10		+10	µA	

Note 1) This is the value on the basis of V_{SS}(GND)=0V.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C_I			10	pF
Output pin capacitance	C_O			10	pF
Input/output pin capacitance	C_{IO}			10	pF

・**AC Characteristics**

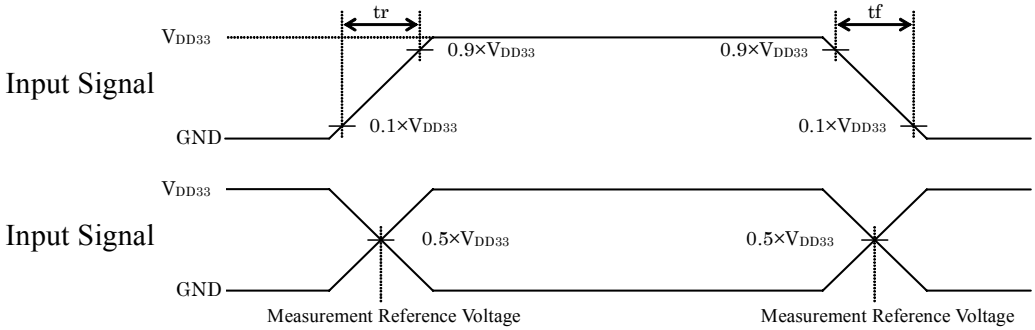
・ Unless otherwise specified, the characteristics of AVDP8 are measured under the following conditions.

■ Input Signal Measurement Condition

Input voltage : 0V/V_{DD33}

Input transient time (tr,tf): 1ns (Transient time is defined between $0.1\times V_{DD33}$ and $0.9\times V_{DD33}$.)

Input measurement reference voltage: $0.5\times V_{DD33}$

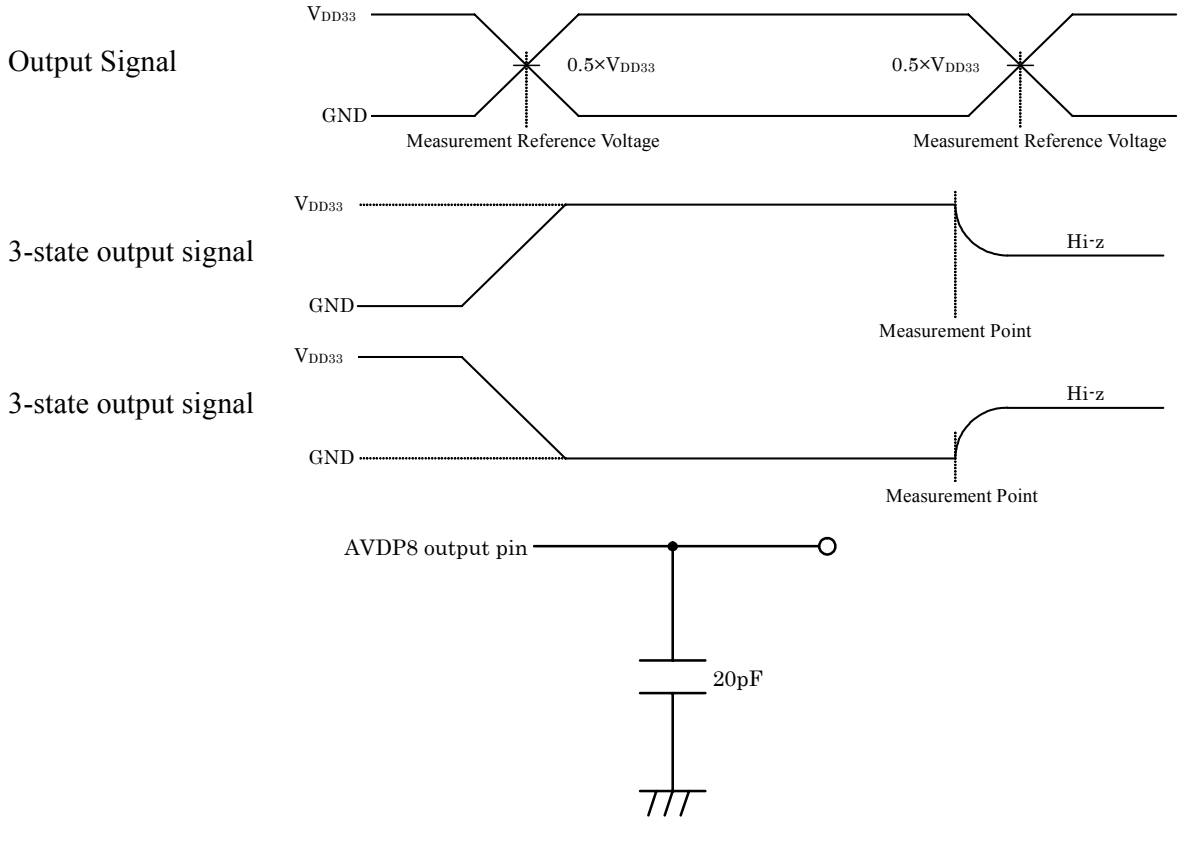


■Output Signal Measurement Condition

Output measurement reference voltage: $0.5\times V_{DD33}$

(At 3-state output pin and input/output pin, the output waveform does not change even when it goes to Hi-z state; therefore, for AVDP8, transient time to Hi-z state is defined by the time I/O cell is disabled.)

Output load capacitance: 20pF



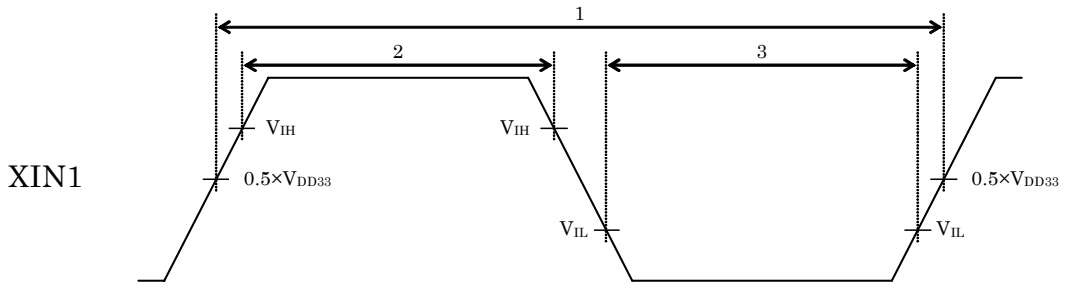
・Clock Input

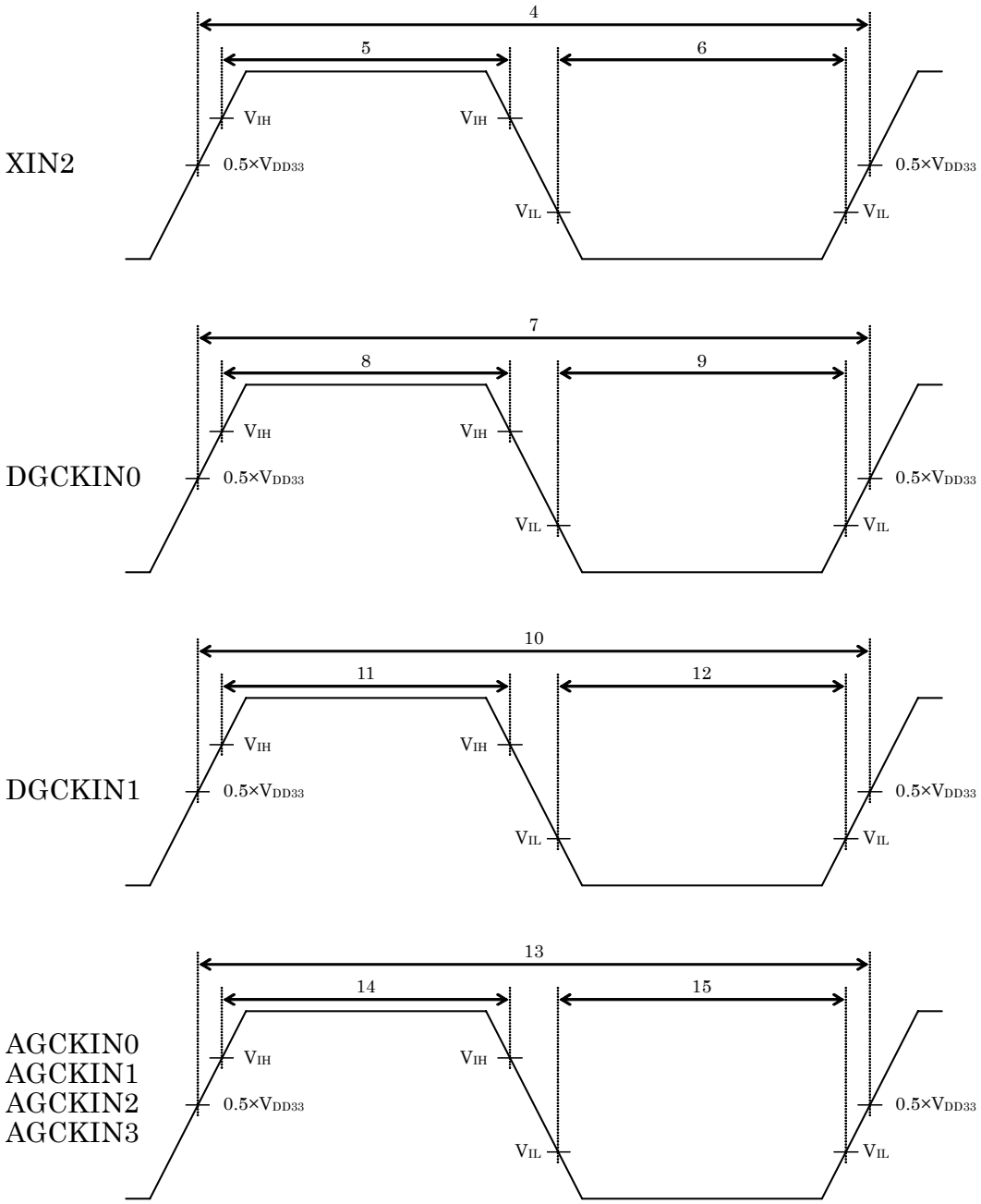
No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
1	XIN1: frequency	f_{XIN1}		27		MHz	
	XIN1: cycle time	t_{cXIN1}		37		ns	
2	XIN1: high level time	t_{whXIN1}	15			ns	
3	XIN1: low level time	t_{wlXIN1}	15			ns	
4	XIN2: frequency	f_{XIN2}	5		75	MHz	
	XIN2: cycle time	t_{cXIN2}	13.3		200	ns	
5	XIN2: high level time	t_{whXIN2}	5			ns	
6	XIN2: low level time	t_{wlXIN2}	5			ns	
7	DGCKIN0: frequency	$f_{DGCKIN0}$	5	(27)	75	MHz	
	DGCKIN0: cycle time	$t_{cDGCKIN0}$	13.3	(37)	200	ns	
8	DGCKIN0: high level time	$t_{whDGCKIN0}$	5(15)			ns	1
9	DGCKIN0: low level time	$t_{wlDGCKIN0}$	5(15)			ns	1
10	DGCKIN1: frequency	$f_{DGCKIN1}$		27		MHz	
	DGCKIN1: cycle time	$t_{cDGCKIN1}$		37		ns	
11	DGCKIN1: high level time	$t_{whDGCKIN1}$	15			ns	
12	DGCKIN1: low level time	$t_{wlDGCKIN1}$	15			ns	
13	AGCKIN0, AGCKIN1, AGCKIN2, AGCKIN3: frequency	f_{AGCKIN}	5		10	MHz	
	AGCKIN0, AGCKIN1, AGCKIN2, AGCKIN3 : cycle time	$t_{cAGCKIN}$	100		200	ns	
14	AGCKIN0, AGCKIN1, AGCKIN2, AGCKIN3 : high level time	$t_{whAGCKIN}$	40			ns	
15	AGCKIN0, AGCKIN1, AGCKIN2, AGCKIN3 : low level time	$t_{wlAGCKIN}$	40			ns	
16	SYCLK: frequency	f_{SYCLK}	115		126	MHz	2
	SYCLK: cycle time	t_{cSYCLK}	7.93		8.69	ns	2
17	DCLK: frequency	f_{DCLK}	5		75	MHz	2
			5		40		2,3
	DCLK: cycle time	t_{cDCLK}	13.3		200	ns	2
			25		200		2,3

Note 1) When DGCKIN0 is selected as AFECLK (frequency of 27MHz), the high level time and low level time should be 15 ns or over.

Note 2) Both SYCLK and DCLK are internal clocks.

Note 3) This is the rating when DAC is used.



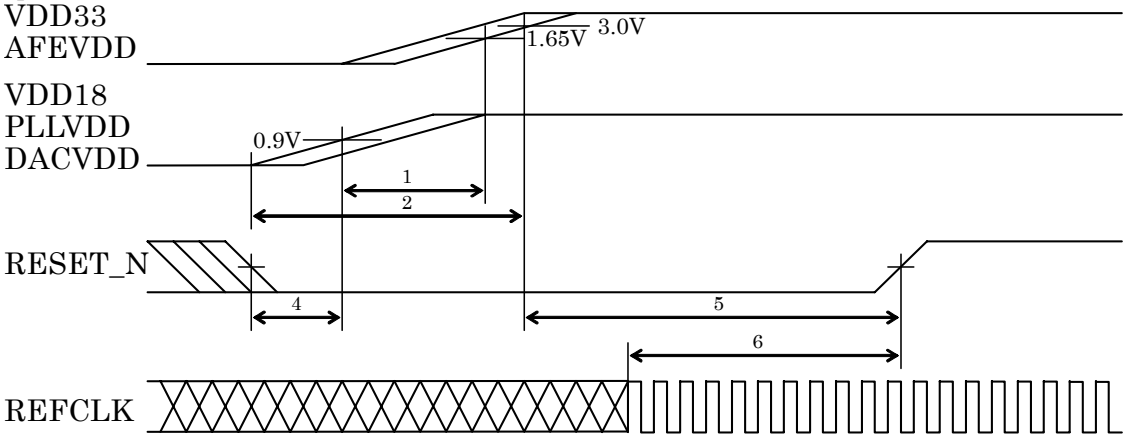

XIN2
4
5
6
VIH
VIH
0.5×VDD33
0.5×VDD33
VIL
VIL
DGCKIN0
7
8
9
VIH
VIH
0.5×VDD33
0.5×VDD33
VIL
VIL
DGCKIN1
10
11
12
VIH
VIH
0.5×VDD33
0.5×VDD33
VIL
VIL
AGCKIN0
AGCKIN1
AGCKIN2
AGCKIN3
13
14
15
VIH
VIH
0.5×VDD33
0.5×VDD33
VIL
VIL

・Power-on and Reset input

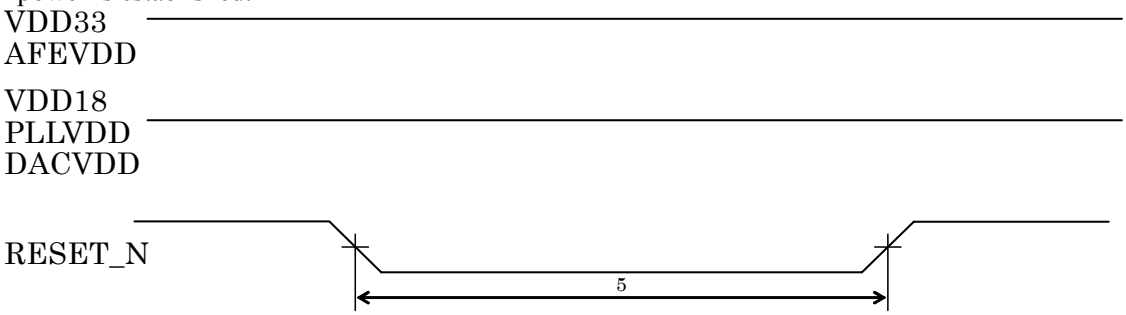
No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
1	Power-on time interval 1	t_{VSKWU1}			100	ms	1
2	Power-on time interval 2	t_{VSKWU2}			300	ms	2
3	Power-off time difference	t_{VSKWD}			100	ms	3
4	RESET_N setup time	t_{sRES}	0			µs	4
5	RESET_N pin input time (to VDD)	t_{wRES}	30			µs	5
6	RESET_N pin input time (to CLK)	t_{SCLK}	1			µs	

Note 1) This is the time from when a power supply that reaches at 0.9V first out of VDD18, PLLVDD, and DACVDD till when a power supply that reaches at 1.65V last out of VDD33 or AFEVDD.
Note 2) This is the time from when a power supply that is first powered on out of VDD18, PLLVDD, and DACVDD till when a power supply in all the power supplies that reaches at the minimum value of the recommended operating voltage last.
Note 3) This is the time from when a power supply that is first powered off out of VDD18, PLLVDD, and DACVDD till when a power supply that is powered off last out of VDD33 or AFEVDD.
Note 4) This is the rating for a power supply that reaches at 1.65V first out of VDD18, PLLVDD, and DACVDD.
Note 5) This is the rating for a VDD that reaches at 3.3V last out of VDD33 and AFEVDD.

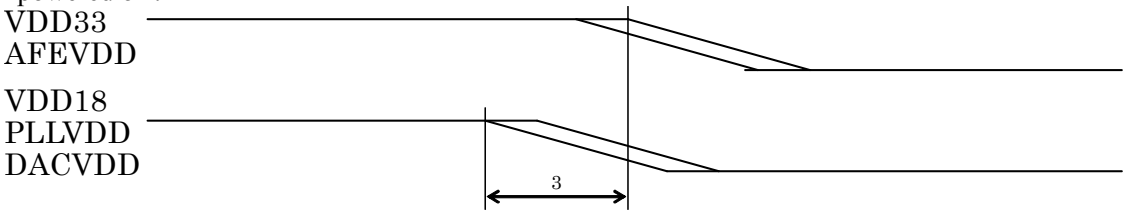
■When powered on:



■When power is established:



■When powered off:



・CPU Interface

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
1	A22-1: input setup time	t_{sA}	1			ns	1,2
2	A22-1: input hold time	t_{hA}	0				1,3
3	CSREG_N,CSMEM_N : setup time	t_{sCS}	0				4
4	CSREG_N,CSMEM_N : hold time	t_{hCS}	0				4
5	D31-0: output turn-on time	t_{onD}	0				5
6	D31-0: output turn-off time	t_{offD}			10		5
7	D31-0: output delay time	t_{dD}			0		5
8	D31-0: output hold time	t_{hD}	0				5
9	WAIT_N,READY_N : output turn-on time	t_{onWAIT}	0				
10	WAIT_N: output delay time	t_{dWAIT}			10		
11	WAIT_N,READY_N : output turn-off time	$t_{offWAIT}$			10		
12	D31-0: input setup time	t_{sD}	t_{SYCLK}+10				5,6,8
13	D31-0: input hold time	t_{hD}	0				5,7
14	WR3-0_N: input hold time	t_{hWR}	0				
15	READY_N: output delay time	t_{dREADY}	0		10		
16	CSREG_N,CSMEM_N,WR3-0_N, RD_N: high level time	t_{whCMD}	t_{SYCLK}+2				8

Note 1) This is the rating for the falling edge transient characteristics of WR3-0_N, RD_N. However, this value is applied to CSREG_N and CSMEM_N when CS_N control is used.

Note 2) In write access operation, this is the rating for the first falling edge out of WR3-0_N.

Note 3) In write access operation, this is the rating for the last falling edge out of WR3-0_N.

Note 4) This is a condition of being in WR3-0_N, RD_N control. When it does not meet this rating, CS_N control is used.

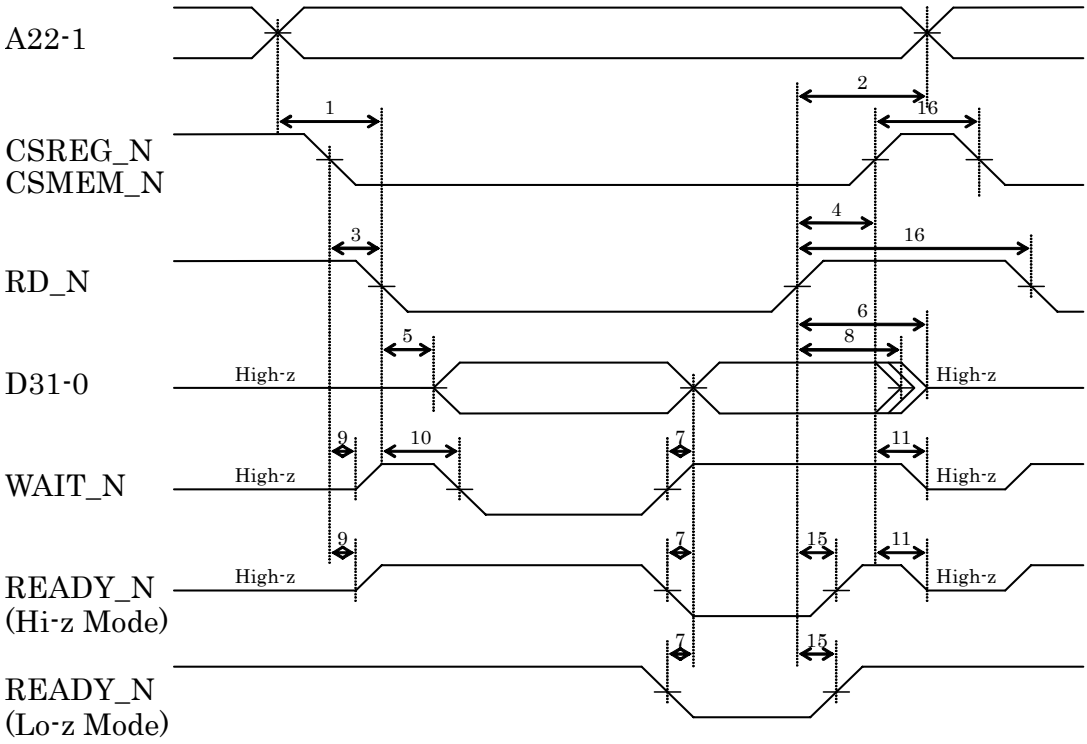
Note 5) When data bus width of 16bit is used for CPU interface, this is the rating for D15-0.

Note 6) This is the rating for the first rising edge out of WR3-0_N.

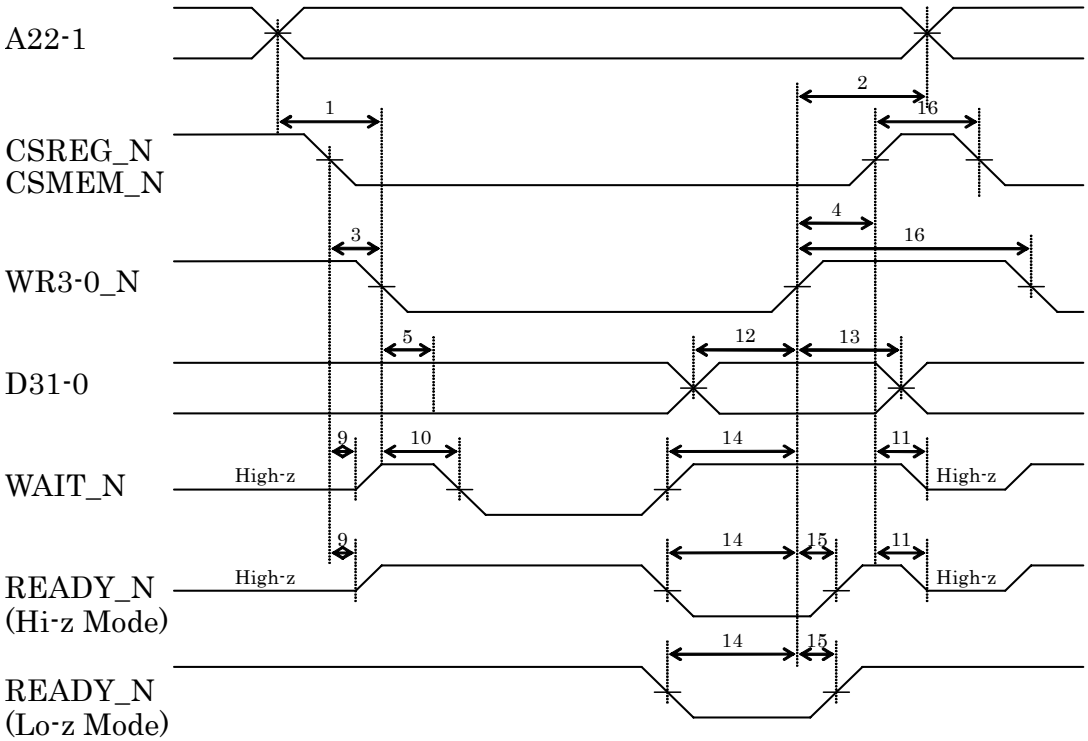
Note 7) This is the rating for the last rising edge out of WR3-0_N.

Note 8) A PLL for the system clock needs to be in the lock state. t_{SYCLK} is the period of the reference clock until SR is executed after power-on.

- CPU Read Cycle



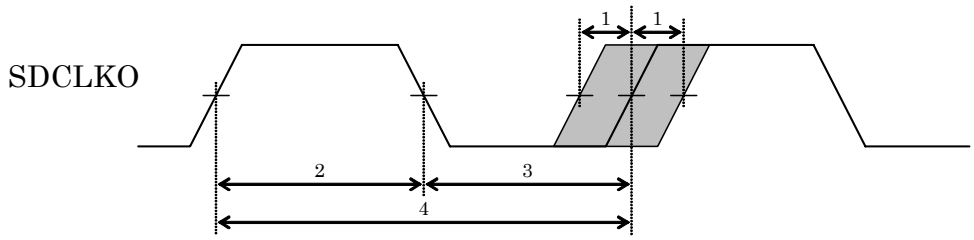
- CPU Write Cycle

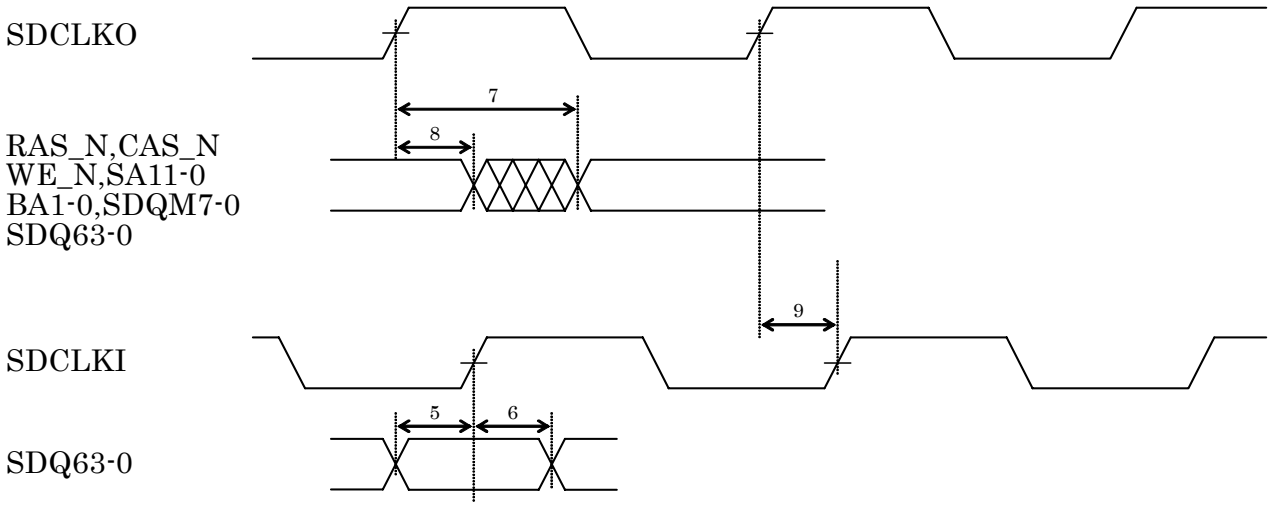


・SDRAM Interface (Measurement Condition: CL=15pF)

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
1	SDCLKO: jitter	t_{jSDCLK}	-0.4		0.4	ns	1
2	SDCLKO: frequency	f_{SDCLK}	115		126	MHz	1
	SDCLKO: cycle time	t_{cSDCLK}	7.9		8.7	ns	1
3	SDCLKO: high level time	$t_{whSDCLK}$	2.5				1
4	SDCLKO: low level time	$t_{wlSDCLK}$	2.5				1
5	SDQ63-0: input setup time	t_{sSDQ}	2				1
6	SDQ63-0: input hold time	t_{hSDQ}	1				1
7	RAS_N,CAS_N,WE_N,SA11-0,BA1-0, SDQM7-0,SDQ63-0: output delay time	t_{dSDO}			5.5		1
8	RAS_N,CAS_N,WE_N,SA11-0,BA1-0, SDQM7-0,SDQ63-0: output hold time	t_{hSDO}	1				1
9	SDCLKI: input delay time	t_{SDCLKI}			1		1

Note 1) A PLL for the system clock needs to be in the lock state.





・Display Timing Signal

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
1	DOTCLK: frequency	f_{DOTCLK}	5		75	MHz	
	DOTCLK: cycle time	$t_{cDOTCLK}$	13.3		200		
2	DOTCLK: high level time	$t_{whDOTCLK}$	$0.45 \times t_{cDOTCLK}$				1
3	DOTCLK: low level time	$t_{wlDOTCLK}$	$0.45 \times t_{cDOTCLK}$				1
4	DRI5-0,BGI5-0,DBI5-0, DVSIN_N,DHSIN_N, D0IN7-0,D1IN7-0, AVSIN0_N,AHSIN0_N, AVSIN1_N,AHSIN1_N, AVSIN2_N,AHSIN2_N, AVSIN3_N,AHSIN3_N : input setup time	t_{sDI}	3				2
5	DRI5-0,BGI5-0,DBI5-0, DVSIN_N,DHSIN_N, D0IN7-0,D1IN7-0, AVSIN0_N,AHSIN0_N, AVSIN1_N,AHSIN1_N, AVSIN2_N,AHSIN2_N, AVSIN3_N,AHSIN3_N : input hold time	t_{hDI}	1			ns	2
6	DR5O-0,DGO5-0,DBO5-0, VSYNC_N,HCSYNC_N, BLANK_N: output delay time	t_{dDISP}			5		
7	DRO5-0,DGO5-0,DBO5-0, VSYNC_N,HCSYNC_N, BLANK_N: output hold time	t_{hDISP}	0				

Note 1) This is the rating for the use of the dot clock PLL.

Note 2) The time of DRI5-0, DGI5-0, DBI5-0, DVSIN_N, DHSIN_N, and D0IN7-0 is the ratings to DGCKIN0.

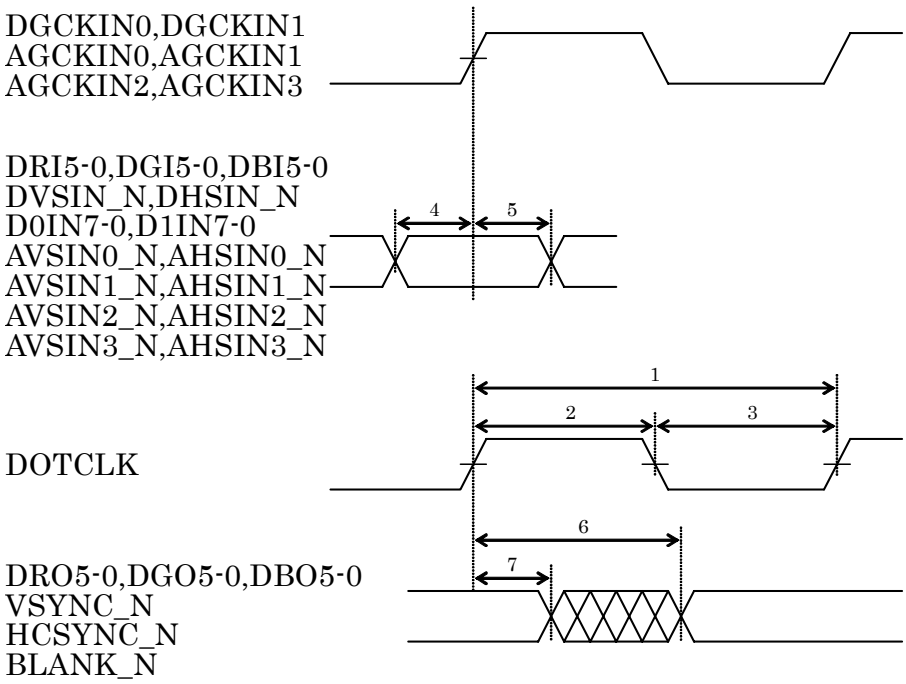
The time of D1IN7-0 is the rating to DGCKIN1.

The time of AVSIN0_N and AHSIN0_N is the rating to AGCKIN0.

The time of AVSIN1_N and AHSIN1_N is the rating to AGCKIN1.

The time of AVSIN2_N and AHSIN2_N is the rating to AGCKIN2.

The time of AVSIN3_N and AHSIN3_N is the rating to AGCKIN3.


DGCKIN0,DGCKIN1
AGCKIN0,AGCKIN1
AGCKIN2,AGCKIN3
DRI5-0,DGI5-0,DBI5-0
DVSIN_N,DHSIN_N
D0IN7-0,D1IN7-0
AVSIN0_N,AHSIN0_N
AVSIN1_N,AHSIN1_N
AVSIN2_N,AHSIN2_N
AVSIN3_N,AHSIN3_N
4
5
1
2
3
DOTCLK
6
7
DRO5-0,DGO5-0,DBO5-0
VSYNC_N
HCSYNC_N
BLANK_N

・ADC characteristics (this specification is tentative.)

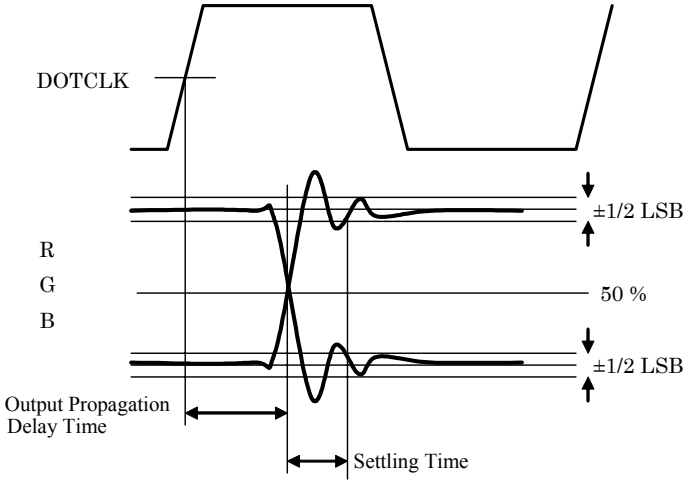
Parameter	Condition	Min.	Typ.	Max.	Unit	Note
Analog Video Input Range		0.375		3	V_{pp}	
Input Signal Band		6			MHz	
Resolution	AFEVDD=3.3V			10	Bit	
Differential Non-Linearity(DNL)	Temp=25°C		0.5		LSB	
Integral Non-Linearity (INL)	Input signal=1.5V_{pp}		1		LSB	
Signal-to-Noise Ratio(SNR)		50			dB	
Crosstalk		66			dB	
Differential Gain (DG)				1	%	
Differential Phase (DP)				1	degrees	

・RGB Output Characteristics (This specification is tentative.)

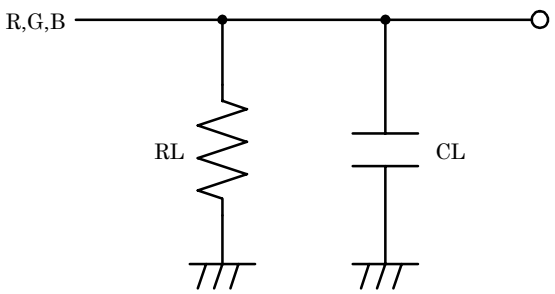
Parameter	Condition	Min.	Typ.	Max.	Unit	Note
Resolution	DACVDD=1.8V			8	bit	
Settling Time	Temp=25°C			20	ns	1
Output Propagation Delay Time	R_L = 37.5Ω		0		ns	2
Output Voltage Amplitude(V_{p-p})	C_L = 30 pF		0.7		V	
Max. Output Voltage (V_{WHITE})	RSET = 328Ω		0.7		V	
Min. Output Voltage (V_{BLACK})			0		V	
Deviation of V_{p-p} between R,G, and B				3	%	

Note 1) The settling time is defined as the time from when DAC output level reaches at 50% till when the level settles within ±1 LSB as shown below.

Note 2) The Output Propagation Delay is defined as the time from the rising edge of DOTCLK to 50% of a DAC output level, as shown below.

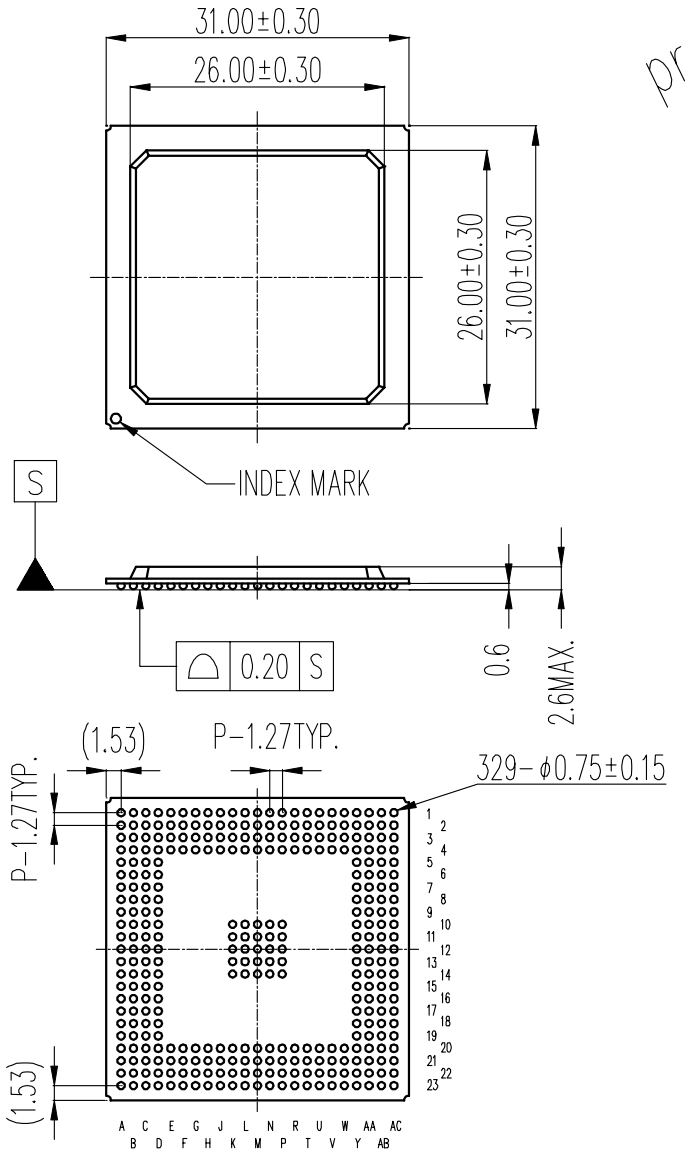


Measurement Circuit



■ Package Dimensions

C-PK329BP-0



モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位： mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせください。

Note: The storage and soldering of LSIs for surface mounting need special consideration.
For detailed information, please contact your local Yamaha agent.

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Notice The specification given here are provisional and subject to change without prior notice. Please confirm the latest documentation before using this product.

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