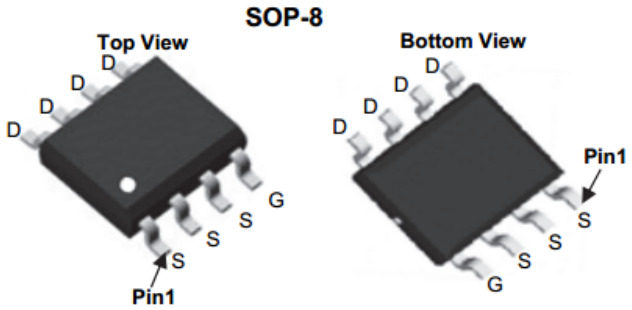
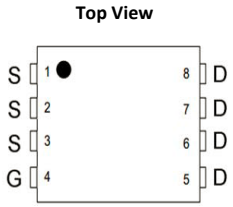
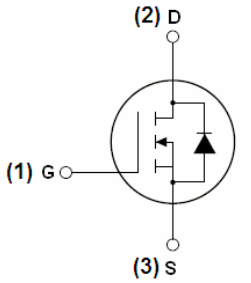
N-Channel Enhancement Mode Field Effect Transistor







Product Summary

- V_{DS} 60V
- I_D(at V_{GS}=10V) 12A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜9.0mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜13.0mΩ
- 100% UIS Tested
  100% Rg Tested
  100% ▽VDS Tested

General Description

- Split Gate Trench Power MV MOSFET technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- Optimized for fast-switching applications

Applications

- Synchronus Rectification in DC/DC and AC/DC Converters
- Industrial and Motor Drive application

■Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current [G]	T_C=25℃	I_D	12	A
	T_C=100℃		9	
Pulsed Drain Current [C]		I_{DM}	48	A
Avalanche energy L=0.5mH [C]		E_{AS}	195	mJ
Power Dissipation [A]	T_C=25℃	P_{DSM}	3.1	W
	T_C=100℃		2.0	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

Thermal Characteristics

Parameter		Symbol	Typ.	Max.	Unit
Junction-to-Ambient [A]	T≤10s	$R_{\theta JA}$	30	40	℃/ W
Junction-to-Ambient [A D]	Steady-State		58	75	℃/ W
Junction-to-Case	Steady-State	$R_{\theta JC}$	15	24	℃/ W

■Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJS12G06A			4000			Tape & reel

■Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	60	65		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V			1	μA
		V_{DS}=60V,V_{GS}=0V,T_J=55℃			5	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.1	1.7	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=12A		8.2	9.0	mΩ
		V_{GS}= 4.5V, I_D=12A		10.5	13.0	
Diode Forward Voltage	g_{FS}	V_{DS}=5V,I_D=12A	30			S
Diode Forward Voltage	V_{SD}	I_S=12A,V_{GS}=0V		0.83	0.99	V
Maximum Body-Diode Continuous Current [G]	I_S				12	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=30V,V_{GS}=0V,f=1MHZ		1988		pF
Output Capacitance	C_{oss}			470		
Reverse Transfer Capacitance	C_{rss}			14		
Gate Resistance	R_g	V_{DS}=0V,V_{GS}=0V,f=1MHZ		1.6		Ω
Switching Parameters						
Total Gate Charge	Q_g(10V)	V_{GS}=10V,V_{DS}=30V,I_D=12A		31		nC
Total Gate Charge	Q_g(4.5V)			16		
Gate Source Charge	Q_{gs}			6		
Gate Drain Charge	Q_{gd}			5		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=15V,R_L=2.5Ω, R_{GEN}=3Ω		10.5		ns
Turn-on Rise Time	t_r			4.5		
Turn-off Delay Time	$t_{D(off)}$			29.5		
Turn-off Fall Time	t_f			8		
Body Diode Reverse Recovery Time	t_{rr}	I_F=12A,di/dt=500A/us		17		
Body Diode Reverse Recovery Charge	Q_{rr}	I_F=12A,di/dt=500A/us		58		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.

■ Typical Performance Characteristics

Fig 1: Output Characteristics

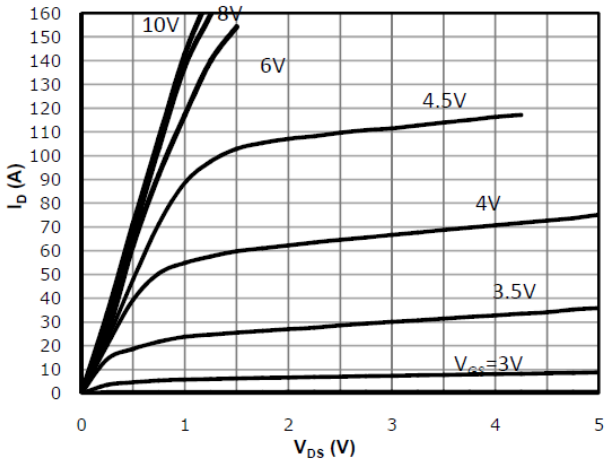


Fig 2: Transfer Characteristics

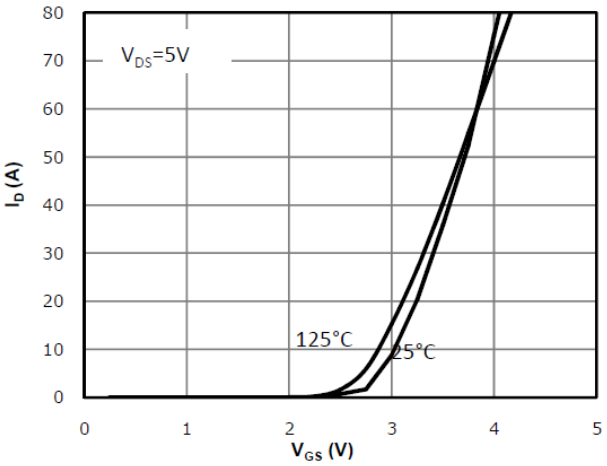


Fig 3: Rds(on) vs Drain Current and Gate Voltage

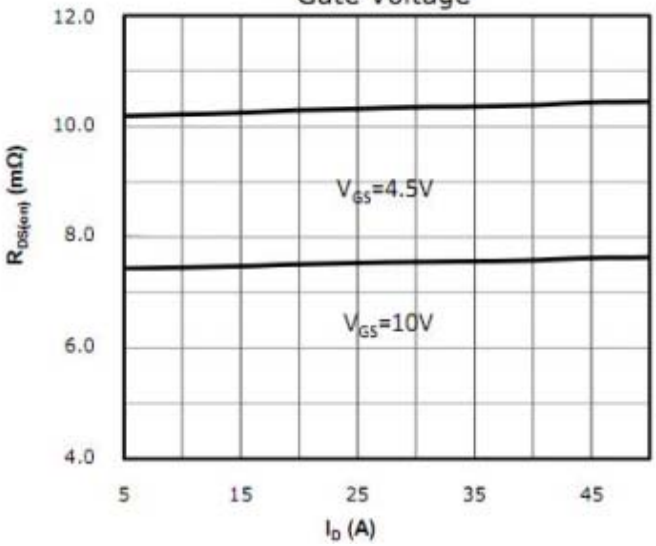


Fig 4: Rds(on) vs Gate Voltage

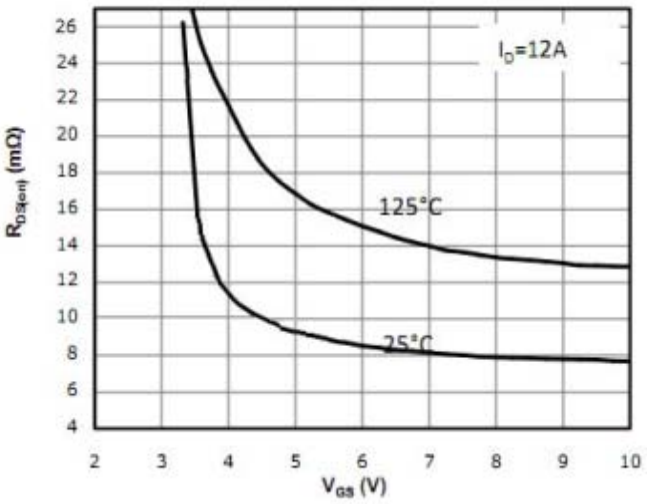


Fig 5: Rds(on) vs. Temperature

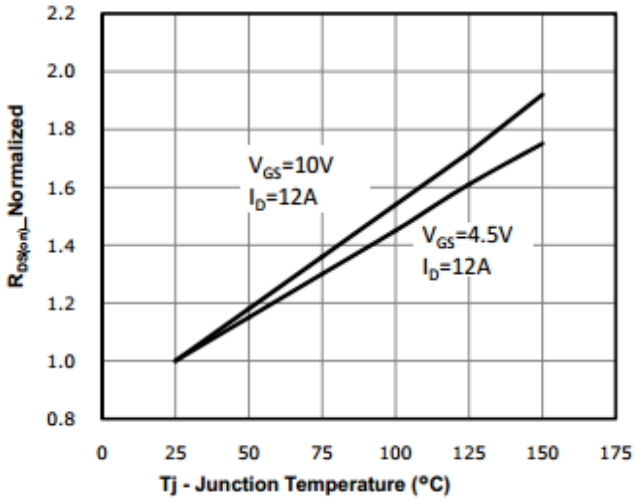


Fig 6: Capacitance Characteristics

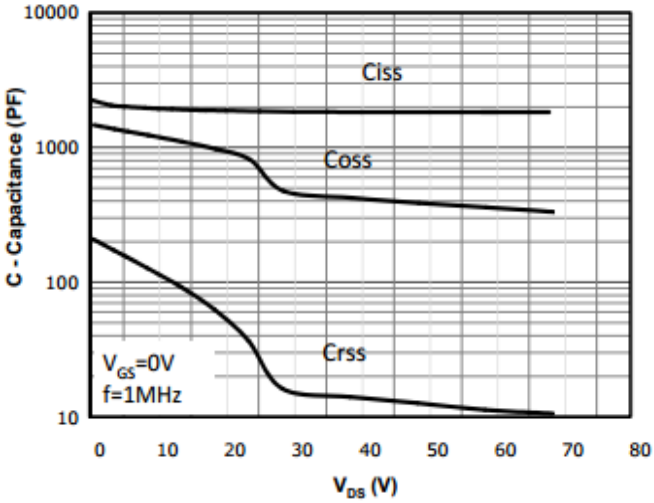


Fig 7: Gate Charge Characteristics

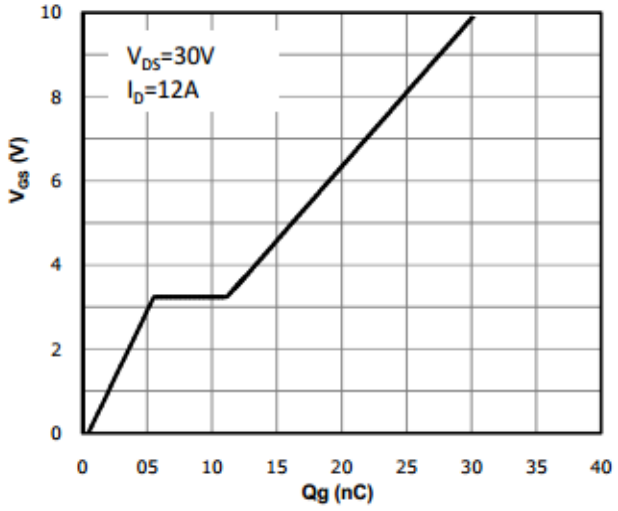


Fig 8: Body-diode Forward Characteristics

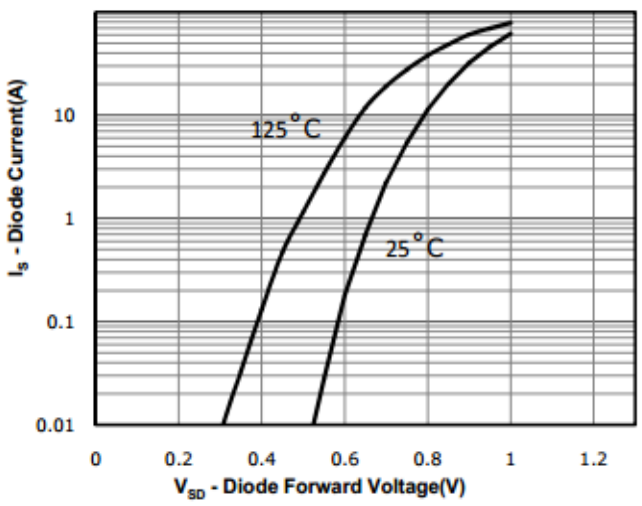


Fig 9: Power Dissipation

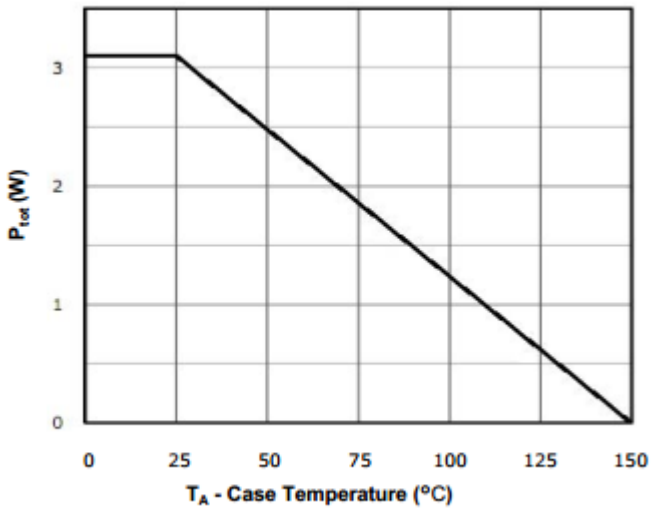


Fig 10: Drain Current Derating

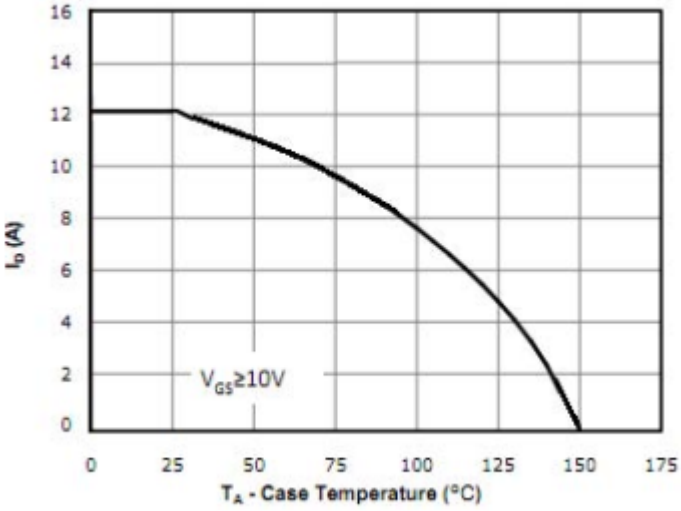


Figure A: Gate Charge Test Circuit & Waveforms

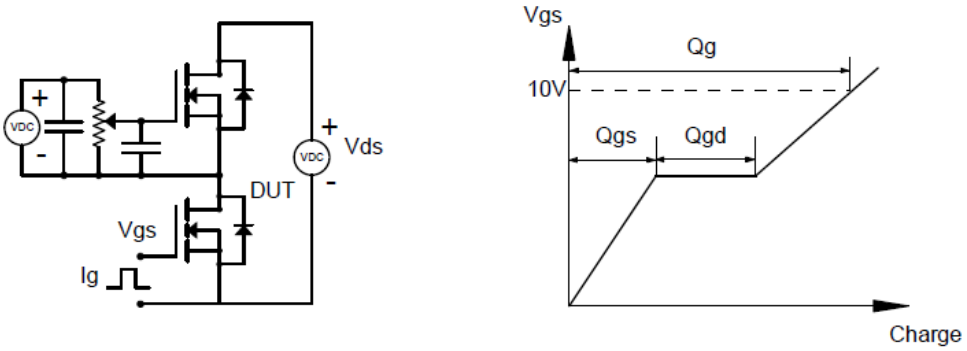


Figure B: Resistive Switching Test Circuit & Waveforms

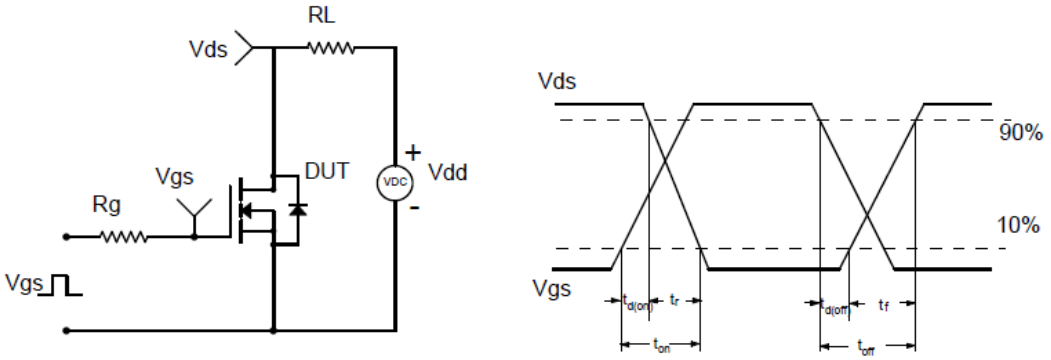


Figure C: Unclamped Inductive Switching (UIS) Test

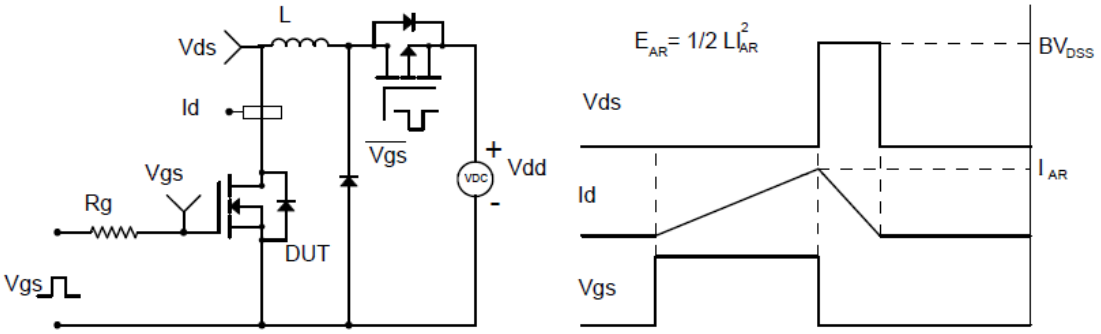
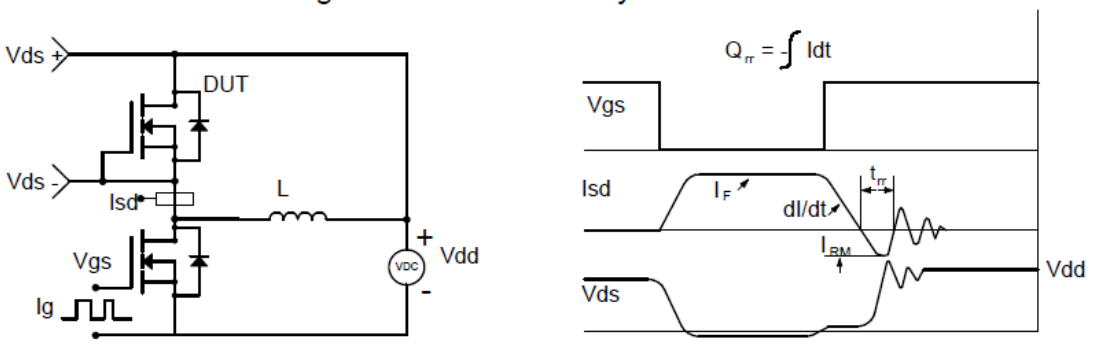
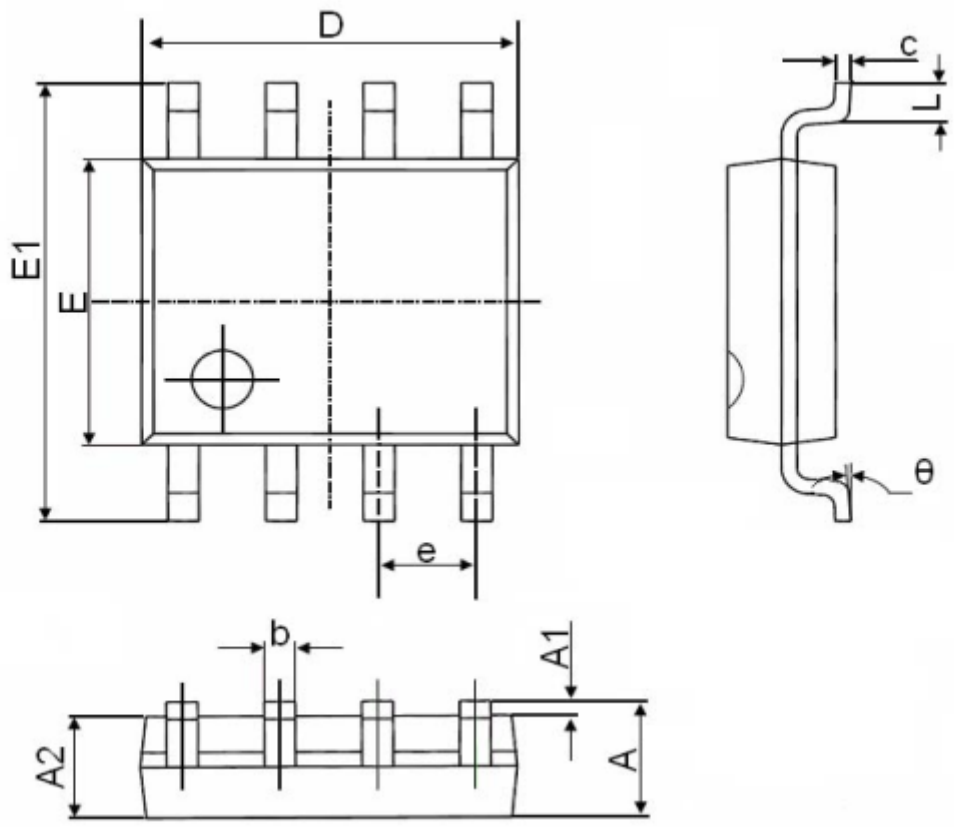


Figure D: Diode Recovery Test Circuit & Waveforms



■SOP-8 Package information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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