1.4MHz, 1.3A Synchronous Step-Down Converter

FEATURES

- High Efficiency: Up to 96%
- 1.4MHz Constant Frequency Operation
- 1.3A Output Current
- No Schottky Diode Required
- 2.4V to 5.5V Input Voltage Range
- Output Voltages from 0.6V to V_{IN}
- 100% Duty Cycle in Dropout
- Low Quiescent Current: 35μA
- Slope Compensated Current Mode Control for Excellent Line and Load Transient Response
- Short Circuit Protection
- Thermal Fault Protection
- Inrush Current Limit and Soft Start
- <1μA Shutdown Current
- Available IN DFN22-6
- -40°C to +85°C Temperature Range

APPLICATIONS

- Cellular and Smart Phones
- Wireless and DSL Modems

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GENERAL DESCRIPTION

The YK3412 is a constant frequency, current mode PWM step-down converter. The device integrates a main switch and a synchronous rectifier for high efficiency without an external Schottky diode. It is ideal for portable equipment requiring very high current up to 1.3A from single-cell Lithium-ion batteries while still achieving over 96% efficiency during peak load conditions. The YK3412 also can run at 100% duty cycle for low dropout operation, extending battery life in portable systems while light load operation provides very low output ripple for noise sensitive applications. This device offers two operation modes, PWM control and PFM Mode switching control, which allows a high efficiency over the wider range of the load

Typical Application

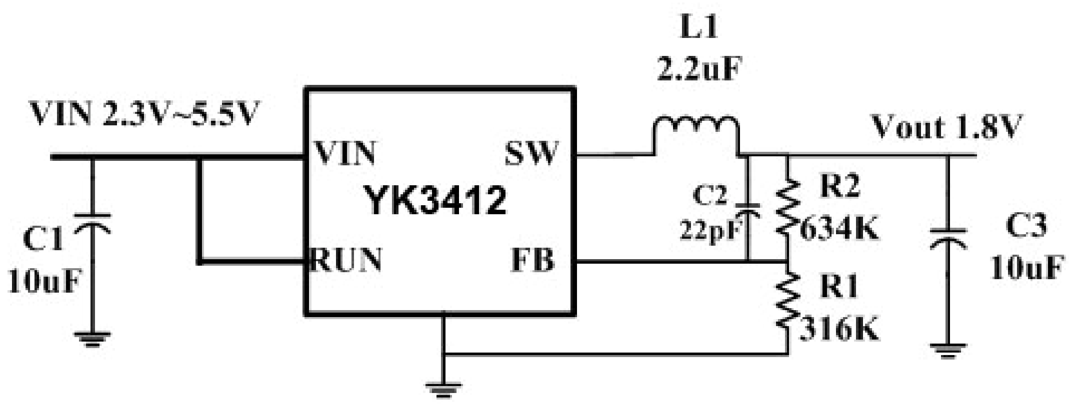


Figure 1. Basic Application Circuit

Absolute Maximum Ratings (Note 1)

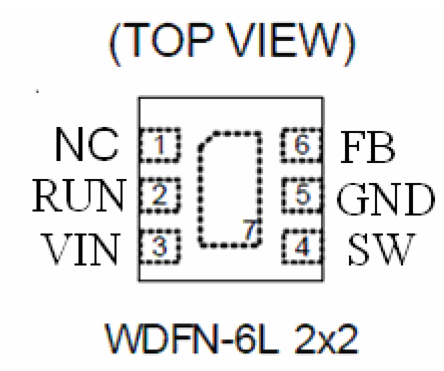
Input Supply Voltage ……… -0.3V to 6V
EN,VFB Voltages…….-0.3 to (Vin+0.3V)
LX Voltage …………-0.3V to (Vin+0.3V)

Operating Temperature Range … -40°C to +85°C
Lead Temperature(Soldering,10s) ……...+300°C
Storage Temperature Range ..…-65°C to 150°C

Pin Description

PIN	NAME	FUNCTION
1	NC	No connect.
2	RUN	Chip Enable Pin. Drive RUN above 1.5V to turn on the part. Drive RUN below 0.3V to turn it off. Do not leave RUN floating.
3	VIN	Supply input pin.
4	SW	Power Switch Output. It is the switch node connection to Inductor. This pin connects to the drains of the internal P-ch and N-ch MOSFET switches.
5	GND	Ground pin
6	FB	Adjustable version feedback input. Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.6V.
	EP	Power Ground exposed pad, Must be connected to bare copper ground plane

Pin Configuration



Electrical Characteristics (Note 3)

(V_{IN}=V_{RUN}=3.6V, V_{OUT}=1.8V, T_A = 25°C, unless otherwise noted.)

Parameter	Conditions	MIN	TYP	MAX	unit
Input Voltage Range		2.4		5.5	V
UVLO Threshold		1.7	1.9	2.1	V
Input DC Supply Current	(Note 4)				µA
PWM Mode	Vout = 90%, Iload=0mA		150	300	µA
PFM Mode	Vout = 105%, Iload=0mA		35	75	µA
Shutdown Mode	V_{RUN} = 0V, V_{IN}=4.2V		0.1	1.0	µA
Regulated Feedback Voltage	T_A = 25°C	0.588	0.600	0.612	V
	T_A = 0°C ≤ T_A ≤ 85°C	0.586	0.600	0.613	V
	T_A = -40°C ≤ T_A ≤ 85°C	0.585	0.600	0.615	V
Reference Voltage Line Regulation	Vin=2.5V to 5.5V		0.1		%/V
Output Voltage Accuracy	V_{IN} = 2.5V to 5.5V, Iout=10mA to 2000mA	-3		+3	%Vout
Output Voltage Load Regulation	Iout=10mA to 2000mA		0.2		%/A
Oscillation Frequency	Vout=100%		1.4		MHz
	Vout=0V		300		KHz
On Resistance of PMOS	I_{SW}=100mA		150	200	mΩ
On Resistance of NMOS	I_{SW}=-100mA		120	180	mΩ
Peak Current Limit	V_{IN}= 3V, Vout=90%		2.6		A
EN Threshold		0.30	1.0	1.50	V
EN Leakage Current			±0.01	±1.0	µA
SW Leakage Current	V_{RUN}=0V,V_{IN}=Vsw=5V		±0.01	±1.0	µA

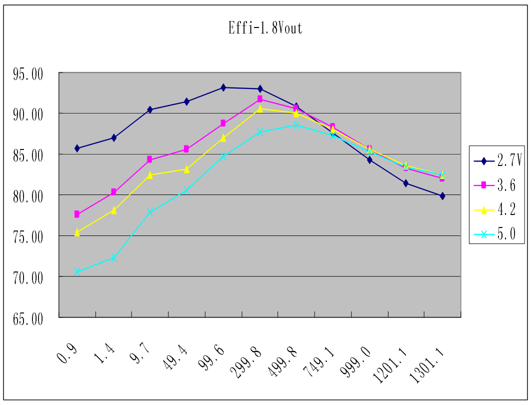
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

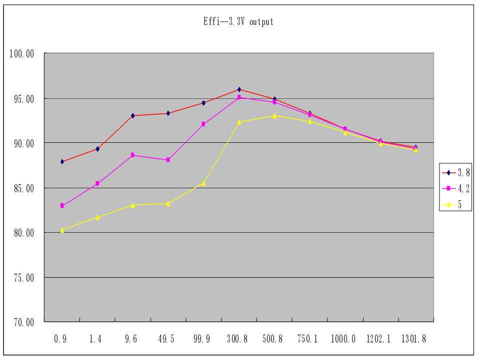
Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D) \times (250°C/W)$.

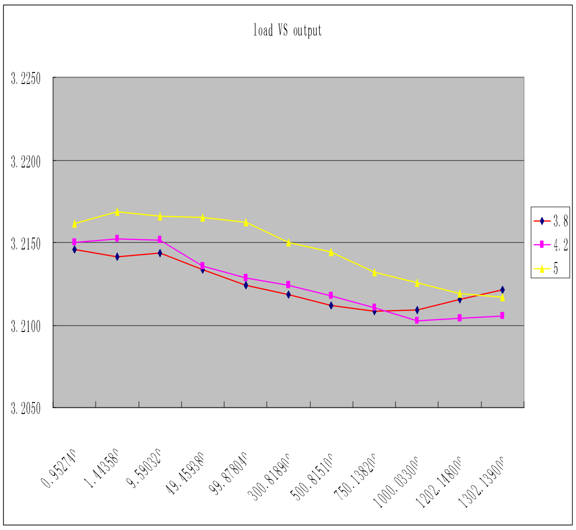
Note3: 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

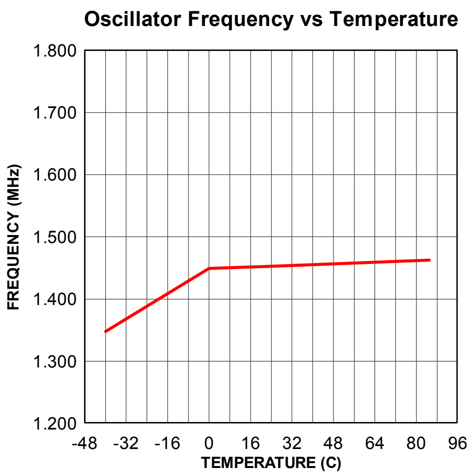
Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency

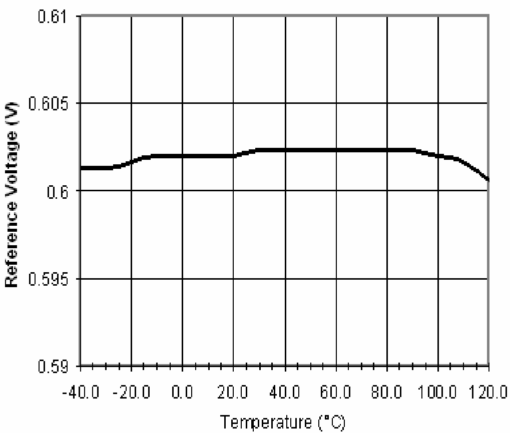
Typical Performance Characteristics

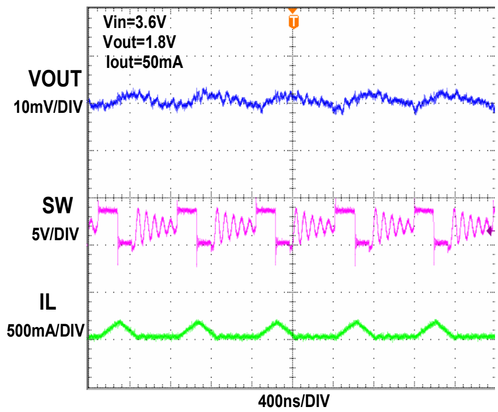




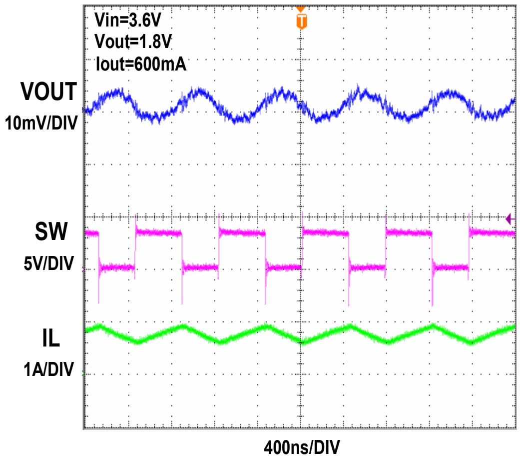




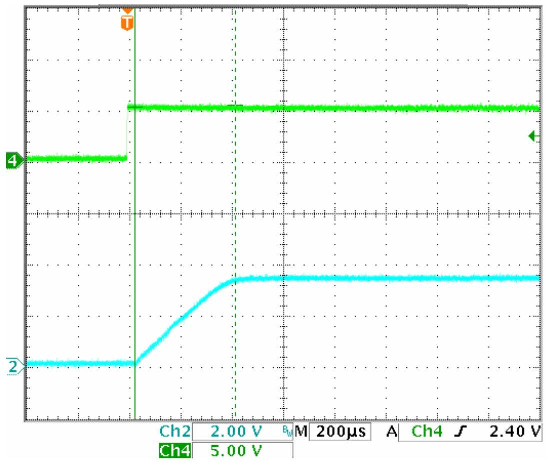




PFM MODE



PWM MODE



Start up

Functional Block Diagram

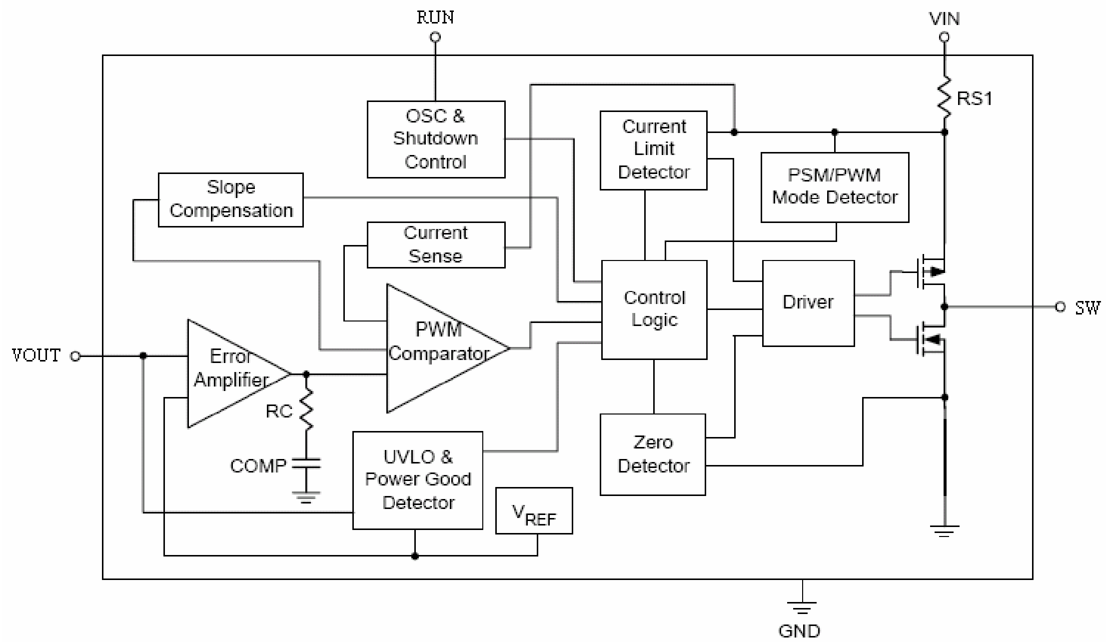


Figure 2. YK3412 Block Diagram

Functional Description

The YK3412 is a high output current monolithic switch mode step-down DC-DC converter. The device operates at a fixed 1.4MHz switching frequency, and uses a slope compensated current mode architecture. This step-down DC-DC converter can supply up to 1.3A output current at VIN = 3V and has an input voltage range from 2.4V to 5.5V. It minimizes external component size and optimizes efficiency at the heavy load range. The slope compensation allows the device to remain stable over a wider range of inductor values so that smaller values (1μH to 4.7μH) with lower DCR can be used to achieve higher efficiency. Apart from the small bypass input capacitor, only a small L-C filter is required at the output. The fixed output version requires only three external power components (CIN, COUT, and L). The adjustable version can be programmed with external feedback to any voltage, ranging from 0.6V to near the input voltage. It uses internal MOSFETs to achieve high efficiency and can generate very low output voltages by using an internal reference of 0.6V. At dropout, the converter duty cycle increases to 100% and the output voltage tracks the input voltage minus the low RDS(ON) drop of the P-channel high-side MOSFET and the inductor DCR. The internal error amplifier and compensation provides excellent transient response, load and line regulation. Internal soft start eliminates any output voltage overshoot when the enable or the input voltage is applied.

APPLICATIONS INFORMATION

Inductor Selection

For most designs, the YK3412 operates with inductors of 1μH to 4.7μH. Low inductance values are physically smaller but require faster switching, which results in some efficiency loss. The inductor value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is inductor Ripple Current. Large value inductors result in lower ripple current and small value inductors result in high ripple current. For optimum voltage-positioning load transients, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range.

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency should be less than input source impedance to prevent high frequency switching current passing to the input. A low ESR input capacitor sized for maximum RMS current must be used. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 10μF ceramic capacitor for most applications is sufficient. A large value may be used for improved input voltage filtering.

Output Capacitor Selection

The output capacitor is required to keep the output voltage ripple small and to ensure regulation loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and high ripple current ratings. The output ripple V_{OUT} is determined by:

$$\Delta V_{OUT} \le \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{OSC} \times L} \times \left(ESR + \frac{1}{8 \times f_{osc} \times C3} \right)$$

A 10μF ceramic can satisfy most applications.

PC Board Layout Checklist

When laying out the PC board, the following layout guideline should be followed to ensure proper operation of the YK3412:

1. The exposed pad (EP) must be reliably soldered to the GND plane. A PGND pad below EP is strongly recommended.
2. The power traces, including the GND trace, the LX trace and the IN trace should be kept short, direct and wide to allow large current flow. The L1 connection to the LX pins should be as short as possible. Use several VIA pads when routing between layers.
3. The input capacitor (C1) should connect as closely as possible to IN and AGND to get good power filtering.
4. Keep the switching node, LX away from the sensitive FB/OUT node.
5. The feedback trace or OUT pin should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation. If external feedback resistors are used, they should be placed as closely as possible to the FB pin

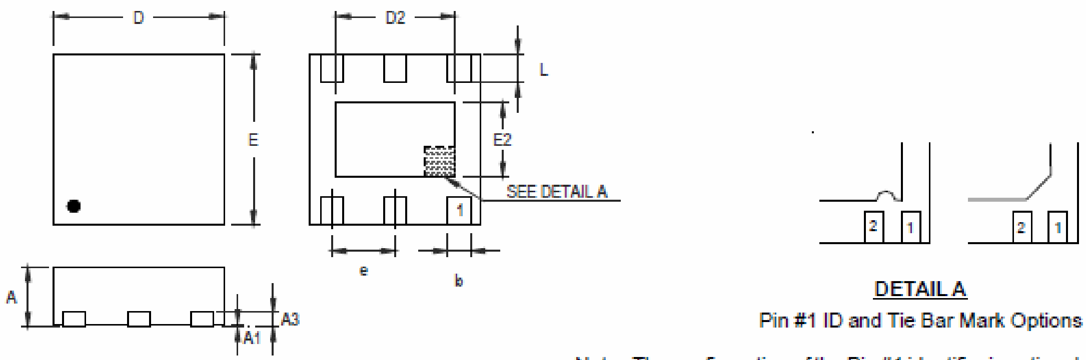
to minimize the length of the high impedance feedback trace.

6. The output capacitor C2 and L1 should be connected as closely as possible. The connection of L1 to the LX pin should be as short as possible and there should not be any signal lines under the inductor.

7. The resistance of the trace from the load return to PGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.

Package Description

Outline Dimension



Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.350	0.008	0.014
D	1.950	2.050	0.077	0.081
D2	1.000	1.450	0.039	0.057
E	1.950	2.050	0.077	0.081
E2	0.500	0.850	0.020	0.033
e	0.650		0.026	
L	0.300	0.400	0.012	0.016

W-Type 6L DFN 2x2 Package