NO. 85-03 3

YM3015

2-Channel Serial & Binary input Floating D/A Converter(DAC-GS)

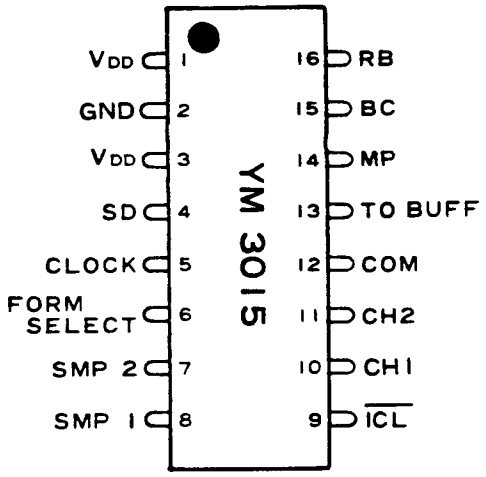
■ OUTLINE

The YM 3015: DAC-GS is a floating D/A converter (referred to as DAC hereafter) with the 2-channel serial and 16-bit binary input or 2's complement input. It can produce analog output (16-bit dynamic range) which has 10-bit mantissa and 7-step exponent characteristic for the input digital signal.

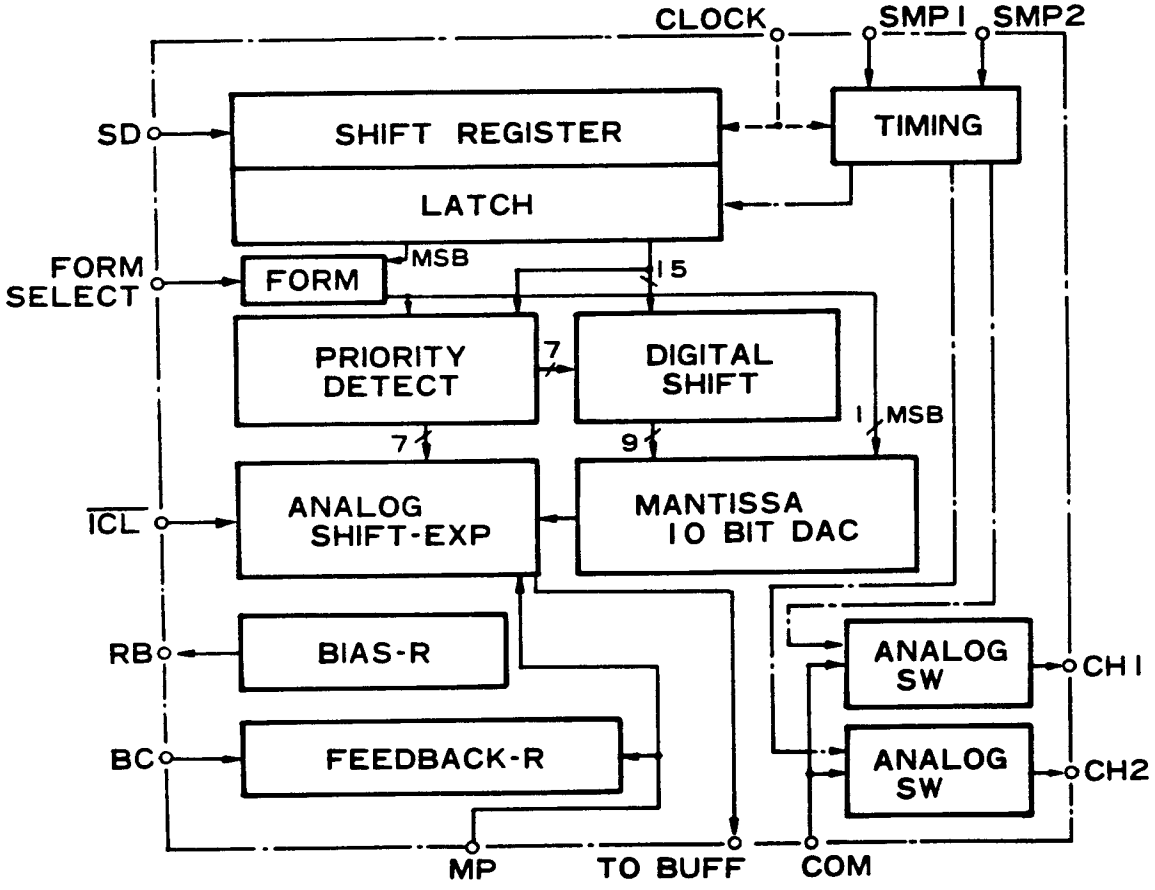
■ FEATURES

- 16-bit input format can select either binary or 2's complement (equipped with a built-in floating converter logic).
- Externally equipped with buffer operational amplifier it allows easy analog output.
- 16-bit wide dynamic range.
- Capable of processing PCM sound source up to 2 channels.
- Equipped with a built-in analog switch for sample hold.
- Lower noise and less harmonic distortion and outstanding temperature characteristics.
- Made by the monolithic process of highly accurate thin film resistor and CMOS and enclosed in the 16-pin plastic flat package.

■ Pin assignment



■ Block diagram



■ Pin function

Pin No.	Signature	Description
1	V_{DD}	High electric potential side standard power source
2	V_{SS}	Low electric potential side power source (GND)
3	V_{DD}	High electric potential side standard power source
4	SD	Serial input of digital signal to be converted
5	CLOCK	Clock to operate shift register and timing generator (Ø4)
6	FORM SELECT	Capable of processing binary input format at "1" and 2's complement input format at "0"
7	SMP2	Interval "1" becomes sampling time for CH2.
8	SMP1	Interval "1" becomes sampling time for CH1. The internal signal for latching serial data is produced by using SMP 1 and SMP 2 fall.
9	$\overline{ICL}$	"1" - normal operation, "0" - output under −36dB regardless of the signal SD.
10	V_{OUT} CH1	Sample hold analog switch output for CH1.
11	V_{OUT} CH2	Sample hold analog switch output for CH2.
12	COM	Common input to analog switches for CH1 and CH2.
13	To BUFF	DAC analog output, input to the buffer operational amplifier.
14	MP	Exponential analog shift is carried out with the electric potential applied to the MP as a standard. Normally it is biased to the 1/2 V_{DD}.
15	BC	Included between this terminal and 14 pin is a resistor which cancels an error caused by the input bias current of the buffer operational amplifier. It is recommended to add phase compensation capacity Cc externally. As shown in the standard circuit example, it can be used with or without being connected with 14 pin.
16	R_B	Internally generated highly accurate 1/2 V_{DD} voltage comes out through this pin and it is applied to 14 pin by way of the buffer operational amplifier.

■ Description of Operation

1. Operation

The serial digital input data is synchronized with the clock fall and taken into the shift register through the SD pin. The latch signal is produced in the timing circuit by making use of the fall of SMP1 and SMP2 and it latches $I_{15} - I_0$ serial data.

After being latched, the 16-bit binary or 2's complemant input data or I_{15} to I_0 are logic converted into the data for the floating DAC by means of the priority detecting circuit and digital shift circuit. Then they become 10-bit mantissa DAC data and 7-step exponential characteristic DAC (analog shift) data and determine the DA conversion output value.

The data conversion truth table is given below.

	Analog shift						
N	0	1	2	3	4	5	6
⌜1⌟	S_0	S_1	S_2	S_3	S_4	S_5	S_6
I_{14}	$\overline{I}_{15}$	I_{15}	I_{15}	I_{15}	I_{15}	I_{15}	I_{15}
I_{13}	—	$\overline{I}_{15}$	I_{15}	I_{15}	I_{15}	I_{15}	I_{15}
I_{12}	—	—	$\overline{I}_{15}$	I_{15}	I_{15}	I_{15}	I_{15}
I_{11}	—	—	—	$\overline{I}_{15}$	I_{15}	I_{15}	I_{15}
I_{10}	—	—	—	—	$\overline{I}_{15}$	I_{15}	I_{15}
I_9	—	—	—	—	—	$\overline{I}_{15}$	I_{15}

Mantissa 10-bit data	Analog shift						
⌜1⌟	S_0	S_1	S_2	S_3	S_4	S_5	S_6
D_9	$\overline{I}_{15}$	$\overline{I}_{15}$	$\overline{I}_{15}$	$\overline{I}_{15}$	$\overline{I}_{15}$	$\overline{I}_{15}$	$\overline{I}_{15}$
D_8	I_{14}	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8
D_7	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7
D_6	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6
D_5	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5
D_4	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4
D_3	I_9	I_8	I_7	I_6	I_5	I_4	I_3
D_2	I_8	I_7	I_6	I_5	I_4	I_3	I_2
D_1	I_7	I_6	I_5	I_4	I_3	I_2	I_1
D_0	I_6	I_5	I_4	I_3	I_2	I_1	I_0

This is the case of 2's complement input.
With binary input, positive and negative of I_{15} are reversed.

The DA converted analog output voltage is, for example with the standard circuit, as follows.

$$V_{OUT} = \frac{1}{2}V_{DD} + \frac{1}{4}V_{DD}(-1 + D_9 + D_8 2^{-1} + \cdots\cdots + D_0 2^{-9} + 2^{-10})\, 2^{-N}$$

It has 1/2 V_{DD} maximum amplitude and 1/2 $V_{DD} \cdot 2^{-16}$ minimum amplitude with the 1/2 V_{DD} electric potential as the center.

The analog output comes out to the TO BUFF pin. When this is input through an appropriate buffer operational amplifier and resistor into the COM pin, it is output to the CH1 and CH2 pins in the interval

"1" of the SMP1 and SMP2, and the analog output of each channel is retained to the proper electrostatic capacity in the interval "0".

2. Tips on Operation

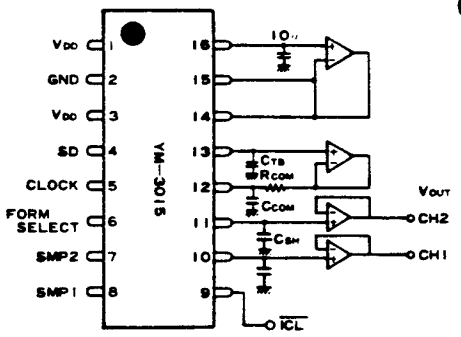
- As shown in the timing diagram Fig. 3, be sure to synchronize the fall of SMP1 and SMP2 with the rear end timing of the MSB (I_{15}) signal.
- The sampling time of the SMP1 and SMP2 can be set to other than 8-bit time which is shown in Fig. 3.
- When using the CH1 only, be sure to synchronize the rear end timing of the MSB (I_{15}) signal and the SMP1 fall timing, for example, by setting the SMP2 to V_{SS}.
- When executing the conversion cycle at a different bit time, an adjustment can be made by increasing or decreasing the number of invalid bits.

3. Initial Clear Function

Setting the $\overline{ICL}$ to "0", the mantissa of the output coming out to both channels remains the same and its exponent characteristic is decreased to 2^{-6} regardless of digital input data value.

■ Standard circuit example

NJM4560 equivalent
OFFSET Within ± 2.0mV



External constant example	Recommended	
Example hold capacity	2700PF	C_{SH} 3300PF ~2200PF
Common resistor	33Ω	R_{COM} 0~180

The optimum value varies slightly with the usage conditions of V_{DD} and others.

For the V_{DD} power source, it is desirable to use the one equivalent to the commercially available 3-pin regulator in the output impedance and stability.

*C_{TB}68PF, added, good noise resistance

■ Electrical characteristics

① Absolute maximum ratings

Item	Rating	Unit
Supply voltage	−0.3 ~ +15.0	V
High-level input voltage	V_{DD} +0.3	V
Low-level input voltage	V_{SS} −0.3	V
Operating ambient temperature	0~70	°C
Storing temperature	−50~+125	°C

② Recommended conditions

Item	Signature	Min	Nom	Max	Unit
Supply voltage	V_{DD}	9.0	12.0	12.0	V
	V_{SS}	0	0	0	V
Input signal voltage	CLOCK SD SMP1, 2 $\overline{ICL}$	0	—	V_{DD}	V
Operating ambient temperature	Ta	0	—	70	°C

③ DC characteristics

Item	Signature	Measuring Conditions	Min	Nom	Max	Unit
High-level input voltage	V_{IH}	$V_{DD} \geqq 9.0V$	1/3 V_{DD}	—	—	V
Low-level input voltage	V_{IL}	$V_{DD} \geqq 9.0V$	—	—	1.0	V
Input current	I_{IN}	$V_{DD} = 12.0V$	—	—	10^{-3}	μA
Analog output voltage	V_{OUT}		—	0.50V_{DD}	—	Vp−p
Supply current	I_{DD}	$V_{DD} = 12.0V$	—	—	6	mA

④ AC characteristics

Item	Signature	Conditions	Min	Nom	Max	Unit
• Clock						
Frequency	fc		0.65	4.3	5.0	MHz
High-level time	T_H		100			ns
Rise time	T_r				30	ns
Fall time	T_f				30	ns
• Data		SD				
Setup time	T_{DS}	SMP 1	50			ns
Rise time	T_r	SMP 2			30	ns
Fall time	T_f				30	ns

⑤ Capacity

Item	Signature	Conditions	Min	Nom	Max	Unit
Input capacity	C_{IN}		—	—	5	PF

⑥ DAC characteristics

Item	Signature	Conditions	Min	Nom	Max	Unit
Maximum output amplitude	V_{OUT}			1/2 V_{DD}		V_{PP}
Resolution				16		Bit
Setting time	T_s			1.5	3.5	μsec
Total harmonic distortion	THD 1	V_{DD} = 9V, 1KHz, Level 0dB		0.06	0.10	%
normal: noise contained				0.20		
	THD 6	−40dB			0.35	%
Noise				−92	−80	dBm
Crosstalk		1KHz, 0dB		−74		dB
Temperature characteristics		Output voltage				
		Total harmonic distortion		5		ppm/°C

Recommended constant and Midpoint buffer operational amplifier NJM 4560 (offset voltage within ±2mV) used,
Any other condition such as supply voltage is specified separatedly.

7. Timing diagram

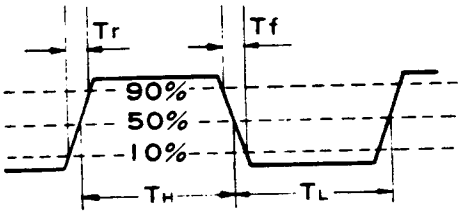


Fig. 1 Data timing

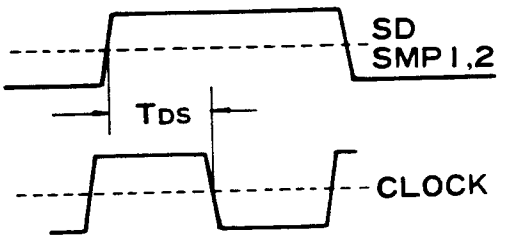


Fig. 2 Input data clock timing

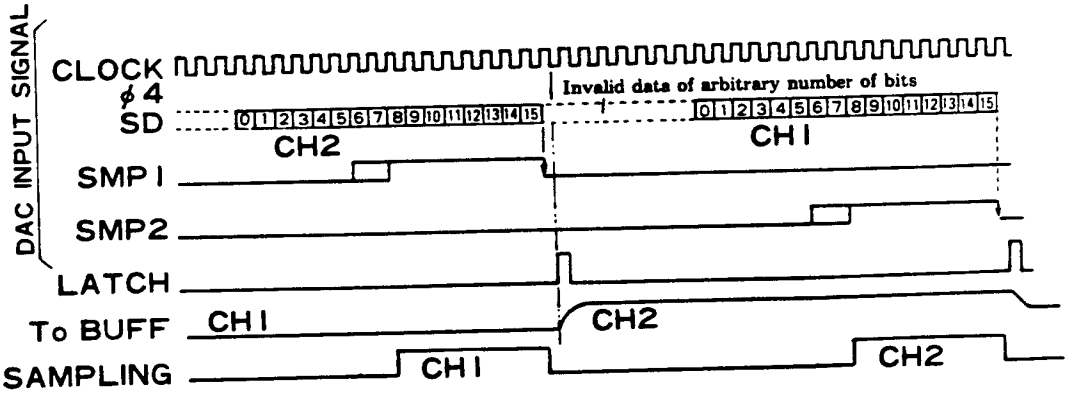
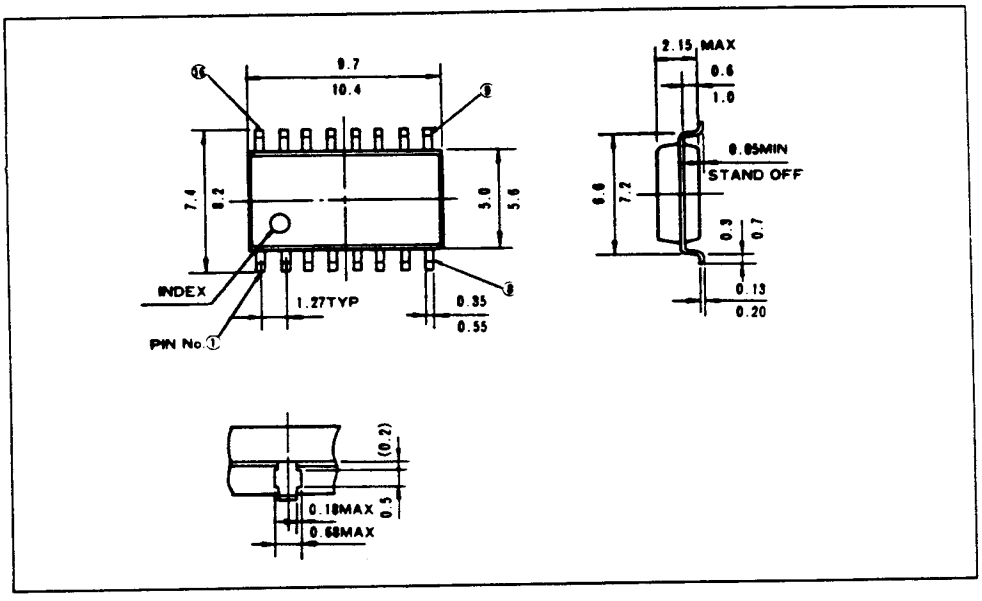
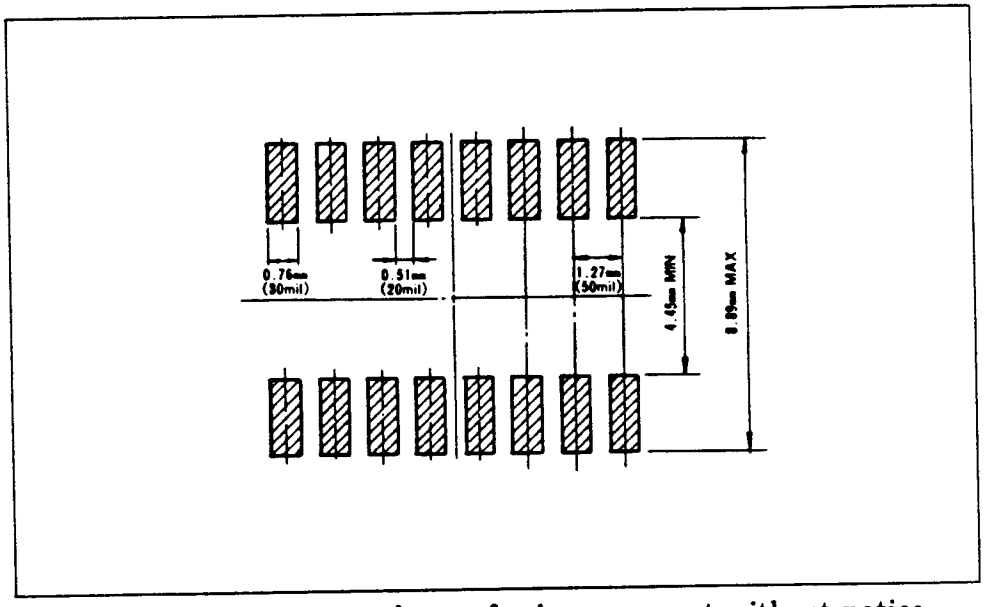


Fig. 3 YM 3015 timing

■ Dimensions





*Specifications subject to change for improvement without notice.

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