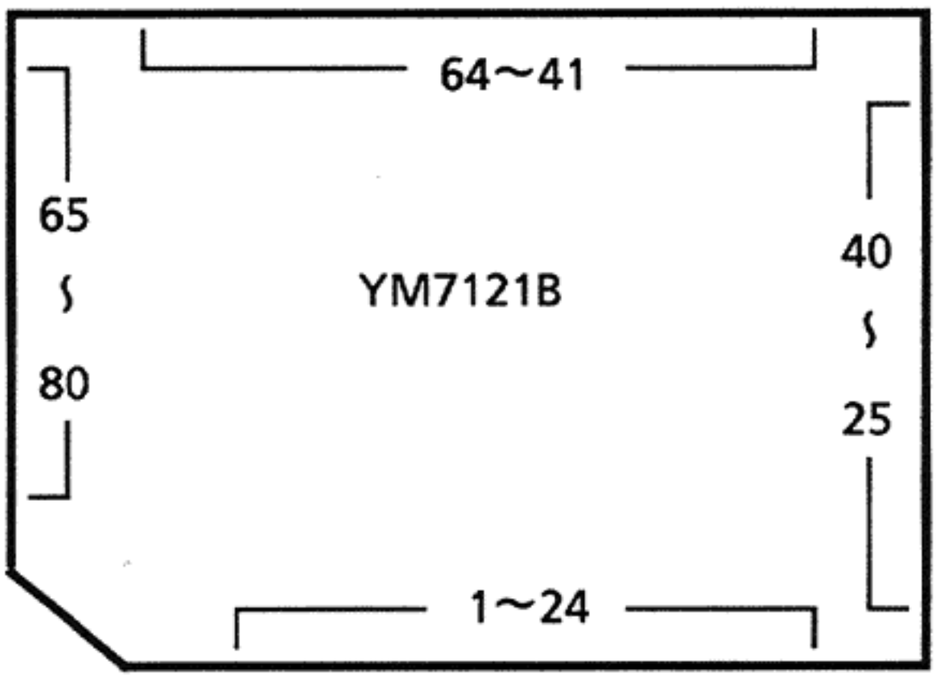
Description of Major LSIs

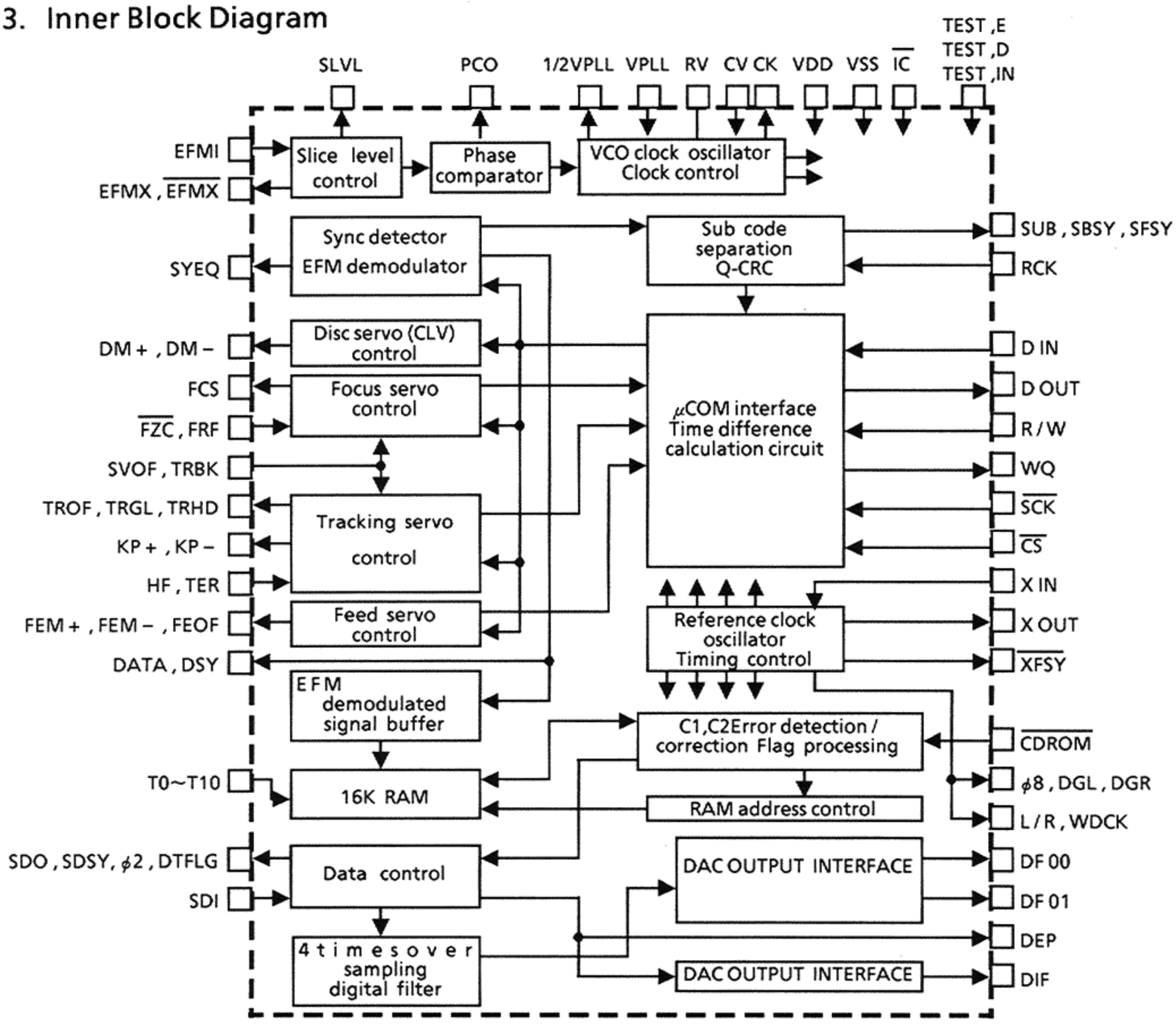
■YM7121B(IC401)

1. Outline

YM7121 is a C-MOS LSI for signal processing and servo control (SVC) in a CD player. It is used for the demodulation of the EFM signal from the laser pick up , detection / correction of the error signal , signal processing in digital filtering , etc. and for various servo controls (focusing , disc , tracking and feed servos).
And it contains digital interface which output the audio digital signals in S-RAM and CD-player. This digital interface matches EIAJ standards.



3. Inner Block Diagram



4. Terminal Function

Pin No.	Symbol	I/O	Function and Operation
1	CV	I	Adequate time constant is added to this terminal and input the PCO output. This makes the structure of clock reproduce circuit by inner VCO circuit.
2	RV	–	RV terminal is standard voltage terminal of inner VCO. And capacity for stabilizing is added to this terminal.
3 32 72	VDD	–	These are +5V power supply terminals.
4 5 70	TEST. IN TEST. E TEST. D	I I I	These terminals are for test.
6	SYEQ	O	This is the check output terminal, it becomes high when flame synchronizing signal detected from EFM pattern coincides frame synchronizing signal from internal counter.
7	DSY	O	DSY is synchronizing signal which becomes high when first signal of data output comes in. This terminal is the check terminal.
8	DATA	O	This terminal is for checks. The DATA is a serial signal of CK bit rate and it contains 8 bit EFM demodulation signal and 5 bit data control signal in 17 bit.
9	CK	O	CK has 4.3218 MHz clock.
10~19	T0~T9	I	This terminal is internal RAM test terminal, and connected GND.
22	DEP	O	De-emphasis is necessary when this terminal is high.
23	DIF	O	DIF is digital audio interface format output matched EIAJ standards.
24	SDO	O	SDO is a serial signal output of $\phi 2$ bit rate. (The MSB puts in at first.)
25	SDI	I	SDI is the input terminal of 4 times over sampling digital filter. It is usually connected with SDO.
26	SDSY	O	This terminal changes the Lch/Rch by LSB of the SDO.
27	DTFLG	O	Not used.
28	$\phi 2$	O	$\phi 2$ is 2.1168 MHz crystal clock.
29, 52, 77	VSS	–	GND
30	XOUT	O	Not used.
31	XIN	I	Input from crystal clock.
33 34 35 36 37 38 39 40 41 42 43 44 45	$\overline{\text{XFSY}}$ SUB SBSY RCK SFSY $\overline{\text{CDROM}}$ $\Phi 8$ WDCK L/R DGL DGR DF01 DF00	O O O I O O O O O O O O O	Not used.
46	$\overline{\text{SCK}}$	I	This terminal is connected to μCOM. It is an input terminal that carries the clock signal for data transfers.
47	R/W	I	This connects with microcomputer and it is an output terminal for switching data transmission mode. it enables to transmit data from SVC to microcomputer when R/M is "L" and from microcomputer to SVC when R/W is "H".
48	$\overline{\text{CS}}$	I	This is a chip select terminal for YM7121.
49	DOUT	O	This terminal is the data output terminal connected to μCOM. When R/W is low, data is transferred from YM7121 to μCOM, according to theSCK clock input.

Pin No.	Symbol	I/O	Function and Operation
50	WQ	O	This terminal is connected to μCOM. It is a request signal which demands to μCOM inputting the data transfer (YM7121 to μCOM).
51	DIN	I	This is a data input terminal connected to μCOM. When R/W is high, the data is transferred from μCOM to YM7121 according to the SCK clock input.
53 54	DM+ DM−	O O	These terminals output the PWM to control the speed of spindle motor. The speed of the motor goes up when DM+ is high, and slows down when DM− is high: both terminals can not become high simultaneously.
55 56 60 61 62 63 64	HF TER TRHD TRGL TROF KP− KP+	I I O O O O O	When tracks are being crossed during serches, the amplitude variation of the generated HF signal is sampled at the zero − cross point of the tracking error signal TER and the TROF signal is output. The level variations of this signal turn the servo on and off, greatly facilitaing track acquisition. KP+ or KP− is output to conduct tracking, and TRHD is output during tracking to cause generation of the tracking error signal. The TRGL signal is for increasing the tracking gain after tracking is completed.
57 58 59	FEM+ FEM− FEOF	O O O	The FEM+ and FEM− are output as high speed feed signals, and FEOF signal is output for cutting the feed servo during high speed feed.
65	TRBK	I	TRBK is input to apply tracking brake from outside. TRGL becomes low with high input and inner control signal TBKE becomes high.
66	SVOF	I	When the signal inputs to SVOF, tracking and feed servo set to OFF. TROF and FEOF become "H" with high input, and TRHD, KP+, KP− become low.
67 58 59	$\overline{\text{FZC}}$ FCS FRF	I O I	These terminals are used for controlling the focus servo. The FCS is for a leading signal of Focusing; the signal, generated when the focus point is achieved, terminate the focusing operation; and FCO flag is dropped internally by FRF signal generated when reflected light is detected.
71	$\overline{\text{IC}}$	I	YM7121 needs initializing when power supply turn on. IC will be low more than 400μs since XIN is input clock with VDD standard.
73 74 75	SLVL EFMX $\overline{\text{EFMX}}$	O O O	Amplitude limited, mutually anti-phased signals are output from EFMX and EMFX. Slice level is controlled by these signals and external amplifier. SLVL is output amplitude alteration component of both terminals. When integral circuit is connected to external. YM7121 easily can control slice level.
76	EFMI	I	This terminal is input EFM signal. (1~2 Vpp)
78	PCO	O	This terminal outputs the phase difference when the polarity of the clock and the EFM pattern changes.
79	VPLL	I	This terminal is input D.C. voltage matched VCO free run frequency. (17.2872 MHz)
80	1/2 VPLL	O	This terminal outputs a half of VPLL input, and capacity for stabilizing is added to this terminal.