YAMAHA LSI

T-77-21

YM7121C

Signal Processor & Controller (& RAM) for Compact Disc Player (SPC V)

■ OUTLINE

YM7121C is one-chip CMOS LSI to provide various servo control and signal processing capabilities needed in compact disc players.

It has a built-in slice level control for EFM signals from optical pickup and a clock reproduction circuit; it performs EFM demodulation, error detection and correction, jitter absorption by internal RAM, and operation of various intelligent servo controls for focusing, tracking, feeding, and disc motor.

This LSI also has digital audio interface output capability conforming to EIAJ format and four-times oversampling digital filter adaptable to either 1DAC or 2DAC of MSB first output, to realize various applications.

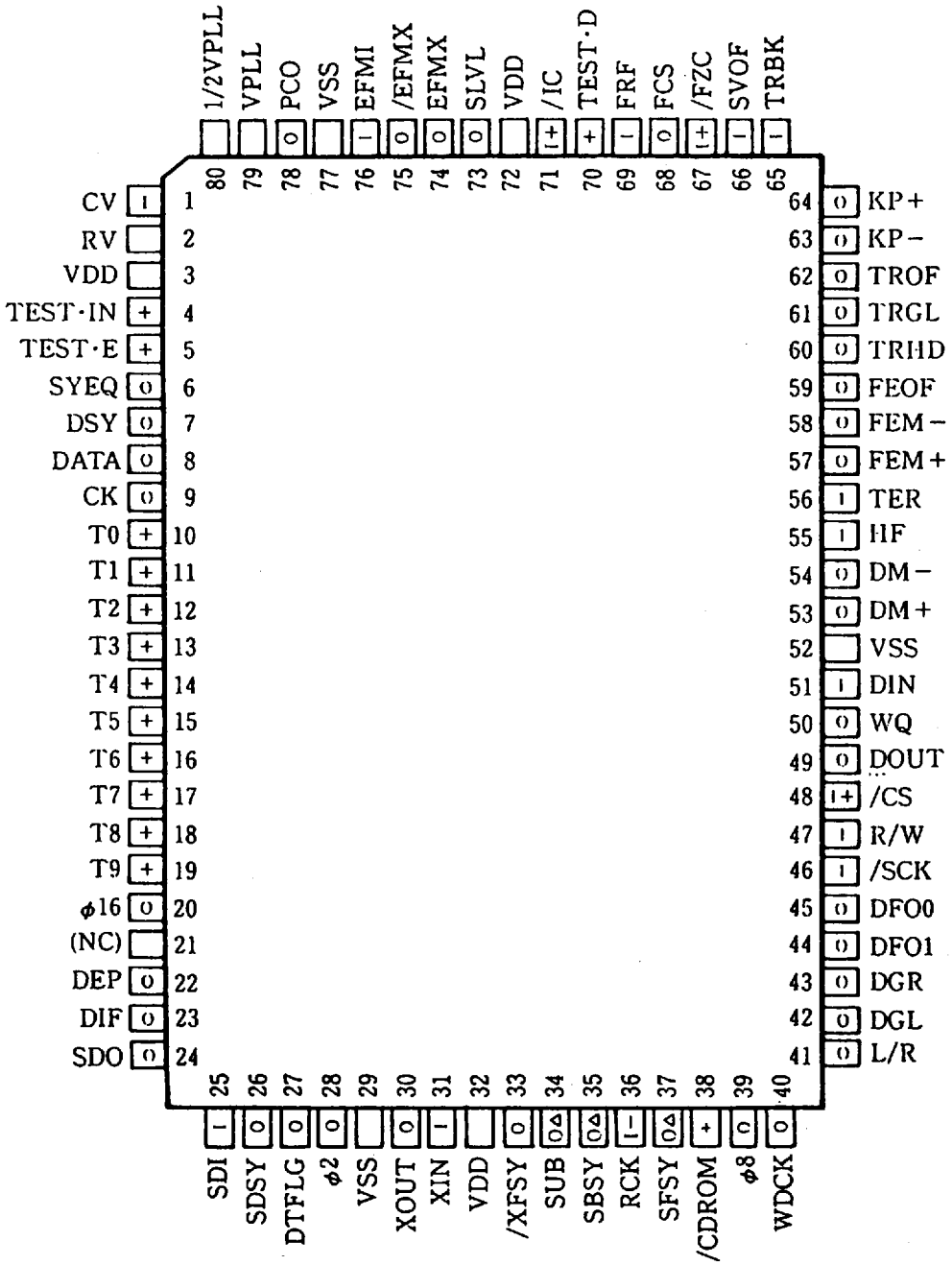
■ FEATURES

- X'tal (16.9344 MHz) is connected to generate standard clock oscillation and necessary timing signals.
- The built-in VCO oscillation and slice level control circuit perform clock reproduction, sync. signal separation, and EFM demodulation.
- In addition to sub code separation and output following to EIAJ format, Q sub codes are CRC checked for output to a microprocessor.
- Phase difference between reproduced and standard clock signals is detected to control the disc motor with PWM.
- Command input on a microprocessor administrates various servo controls for focusing search as well as tracking feed for quick access and skipping.
- In addition to automatic searching capability for quick access, track counter for high-speed searching is built in.
- The built-in RAM buffers the EFM demodulation signals to absorb wow and flutter of the disc. (Jitter absorption range: ±4 frames)
- EFM demodulation signals are unscrambled and de-interleaved.
- Error detection and correction as well as flag processing for digital audio signals (Double error correction for both C1 and C2)
- Linear interpolation is used to replace the uncorrectable error data (up to a maximum if 8 consecutive errors). And preceding data hold is applied for errors over eight.
- The data output is in MSB first format and four-times oversampling digital filter is built in.

YM7121C CATALOG
CATALOG No. : LSI-2171214
1991.12

- Output of digital audio interface signals conforming to EIAJ for interface with other audio equipments.
- Error flag output ,for CD-ROM.
- 80-pin flat package, silicone gate CMOS LSI, operated by 5V power supply.

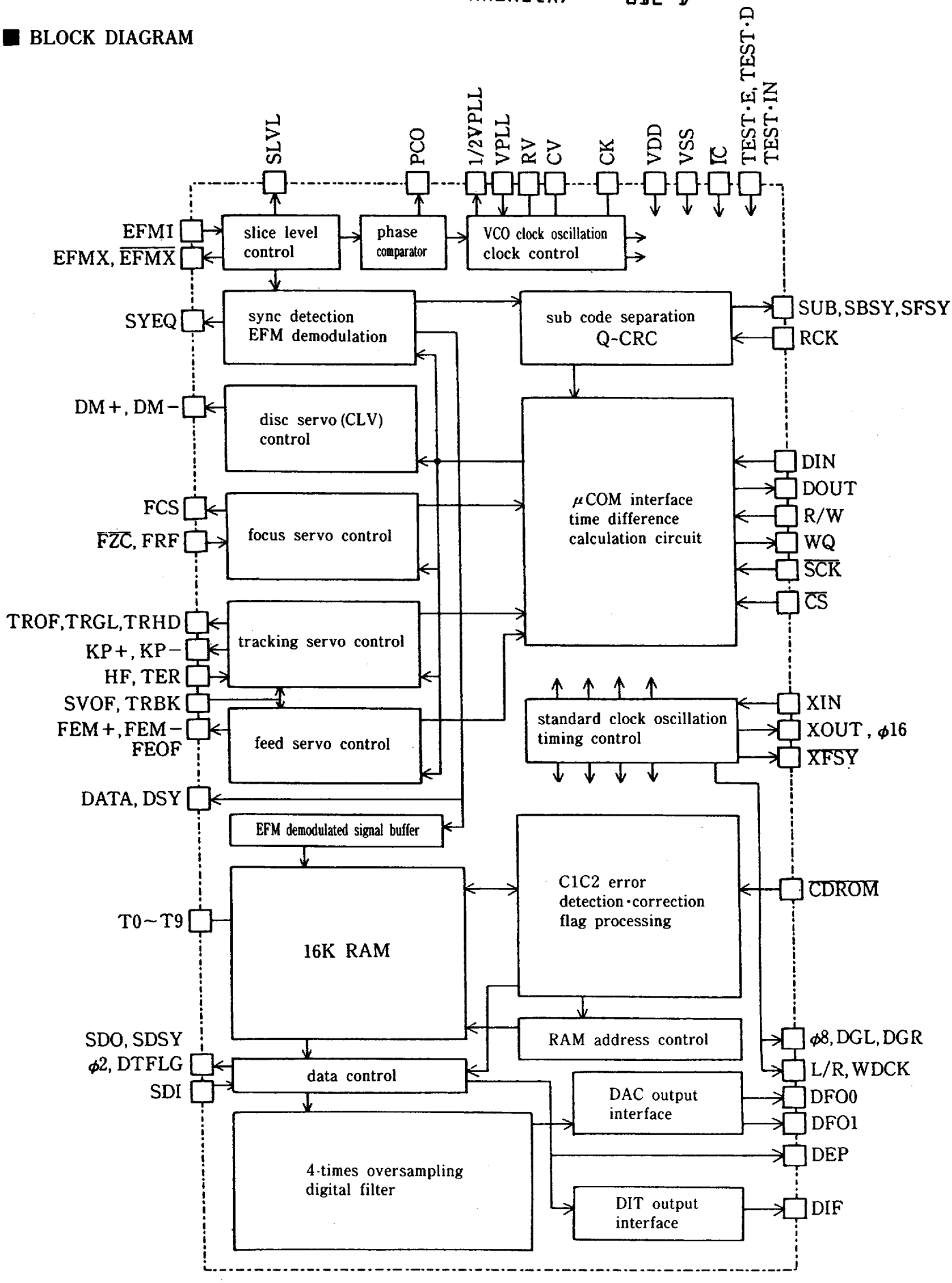
■ PIN CONFIGURATION



TOP VIEW

I : Input terminal
O : Output terminal
+ : Pull-up, − : Pull-down
△ : Open-drain

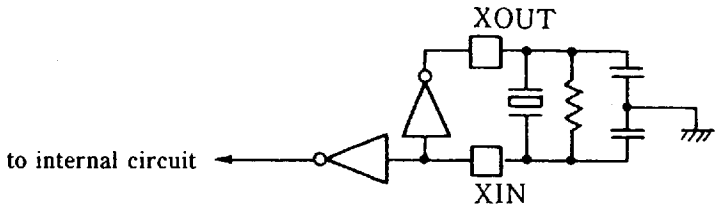
BLOCK DIAGRAM



■ PIN DESCRIPTION

1. Clock Oscillation XIN, XOUT, ϕ16

When X'tal oscillators (16.9344 MHz) are connected to both terminals and capacitors are connected between each terminal and the ground, oscillation is generated. Clock is output from the ϕ16 terminal.



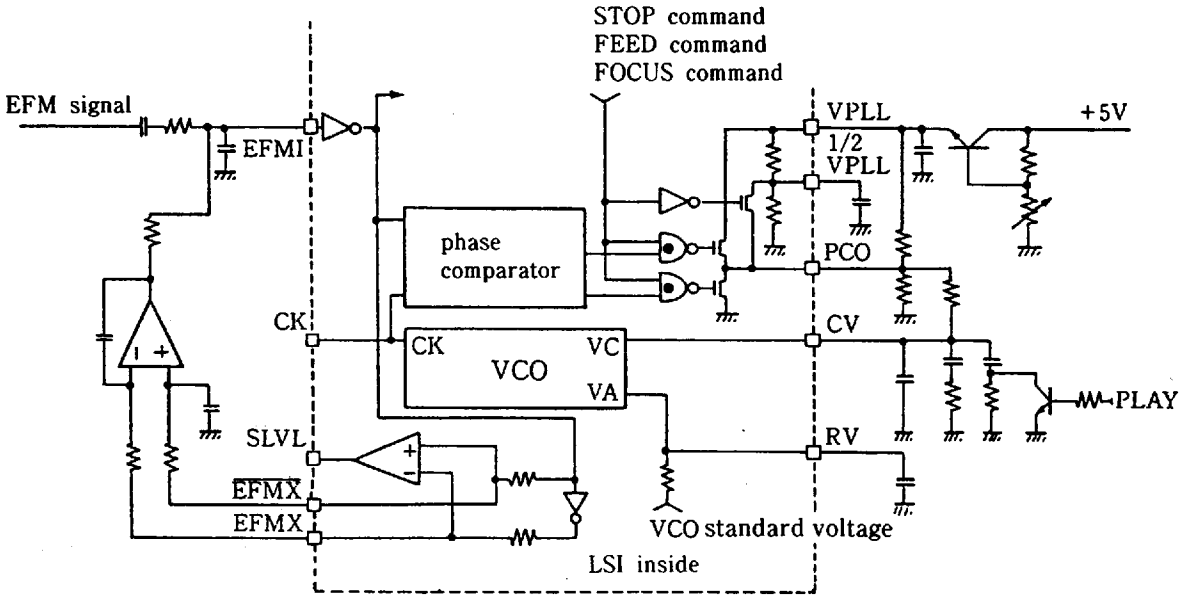
2. Slice Level Control Circuit EFMI, $\overline{\text{EFMX}}$, EFMX, SLVL

To EFMI terminal, signals from optical pickup at an adequate level (1~2 Vpp) are input. From $\overline{\text{EFMX}}$ and EFMX, signals antiphased each other are output with amplitude limiting. Slice level control is performed with these signals and external amplifier. At SLVL, amplitude change component for both terminals are output, and by adding an adequate external integral circuit, simple slice level control can be performed.

3. Clock reproduction circuit PCO, CK, CV, RV, VPLL, 1/2 VPLL

Output at PCO terminal is phase difference output at the time of polarity change of clock and EFM pattern, and clock reproduction circuit with internal VCO oscillation circuit can be configured by adding certain time constant from outside for input to CV terminal. VPLL terminal is for input of DC voltage adapted to VCO free run frequency (8.6436 MHz). 1/2 VPLL terminal is for output of half cut VPLL terminal input, and voltage stabilizing capacitor shall be mounted here externally.

RV terminal is the standard voltage terminal of internal VCO, and requires mounting of external stabilizing capacitor. CK is the clock of 4.3218 MHz (average) which is obtained by dividing of VCO frequency into four.

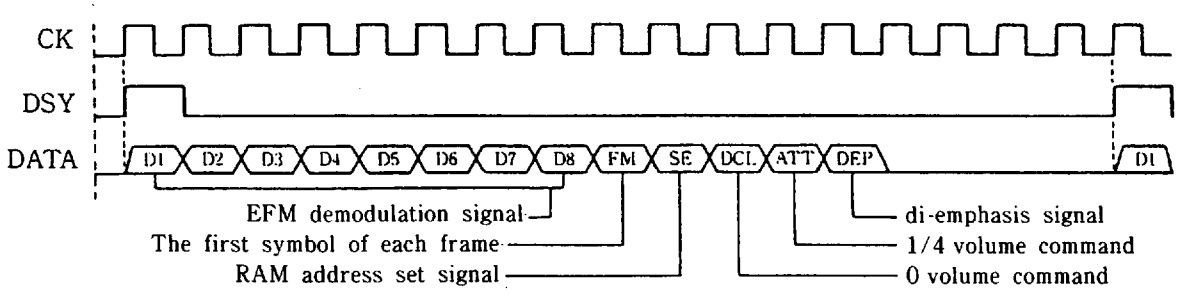


4. Sync. Equal Signal SYEQ

This is a check output terminal which becomes "H" when the frame synchronizing signals detected from input EFM pattern equals the frame synchronizing signals from internal counter.

5. Output of EFM demodulation signal checking DATA, DSY

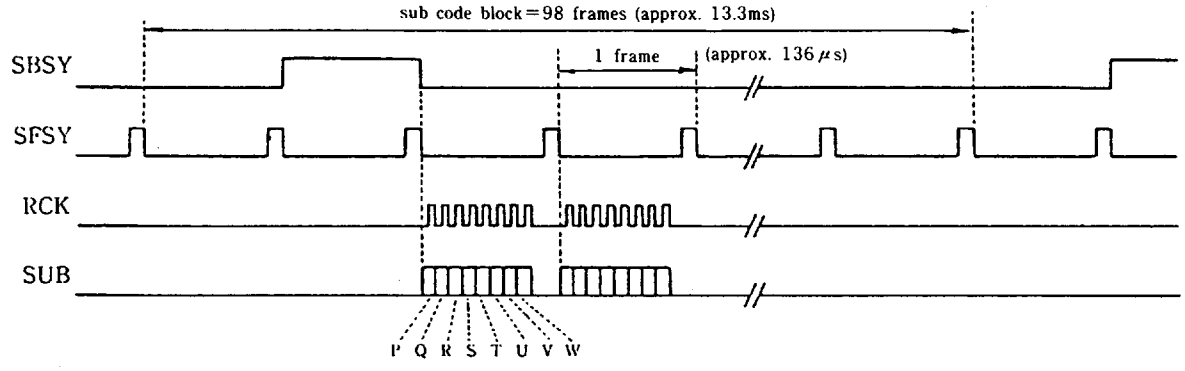
DATA is a serial signal of CK clock bit rate, which consists of 17 bits and includes eight bits of EFM demodulation signal and five bits of data control signal. DSY is the synchroizing signal to turn "H" at the timing which coincides initial of DATA output. These therminals are for checking.

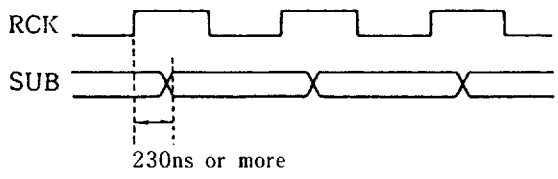


6. Sub code output SUB, SBSY, SFSY, RCK

SBSY is for sub code frame synchronizing signal output, which becomes "H" when it finds sub code frame period (Usually two clocks for every 98 clocks for the frame synchronizing signal SFSY) and keeps "H" for that period.

When the change from "H" to "L" of SFSY is checked from outside and eight clocks are input to RCK terminal, sub codes P to W are serially output from SUB terminal. When SBSY is "H", S0·S1 are output at P code timing. Each of these terminal conform to EIAJ sub code interface standard.





7. Q Code Output WQ, R/W, Dout, $\overline{SCK}$, $\overline{CS}$

These terminals serve as interface to inform the microprocessor of LSI internal status and Q code information.

When WQ turns "H" under the conditions below, the following information for the bytes 1~11 can be read from DOUT by sending clock signals from the microprocessor to the SCK terminal.

byte	DOUT contents
1	internal status
2	CONT ADR
3	TNO
4	X
5	MIN
6	SEC
7	FRAME
8	P-CODE
9	A MIN
10	A SEC
11	A FRAME

contents of the internal status (1st byte)

D7	D6	D5	D4	D3	D2	D1	D0
SIGN	S2	S1	8F	4F	MZ	FCO	NQ

SIGN : search sign
S1,S2 : search mode
4F,8F : search frame error
MZ : disc motor stop ('1'=stop)
FCO : focus out ('1'=out)
NQ : new Q code ('1'=new Q code)
※When track count finishes, D7='1'
D6~D3='0000'
When 1 track kick finishes,
D7~D3='11111'

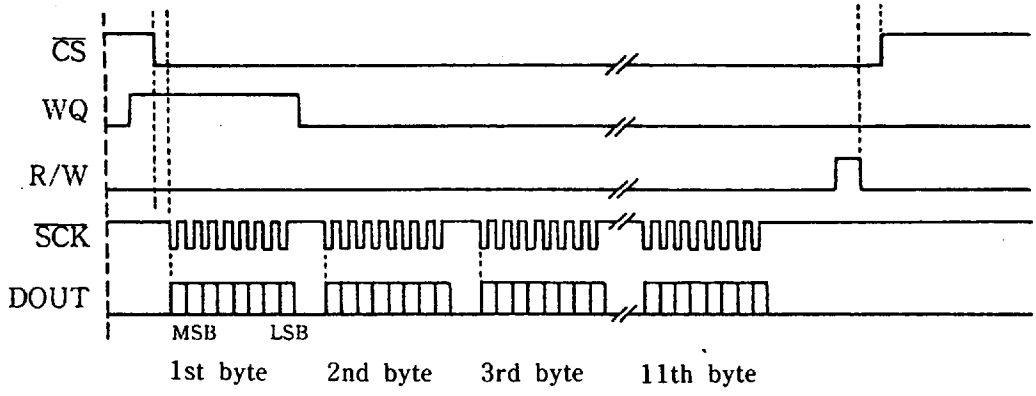
Conditions when WQ becomes "H"

1) When the disc motor starts rotation, or when the disc motor stops.
2) When focus is in operation, or when focus operation stops.
3) When new and correct Q codes are set in the internal register.
4) When the track count is completed.

When WQ is "H", at least 1 byte in the internal status needs to be read out, but reading can be stopped at any arbitrary byte afterward.

In search mode, search completion does not cause WQ to be "H", and the internal status shall be always monitored.

Only when $\overline{CS}$ = "L", DOUT is output.



8. Microprocessor Instructions R/W, DIN, $\overline{SCK}$, $\overline{CS}$

The following instructions are available for control of this LSI from microprocessors.

All the instructions except for search and track count consist of 1byte (8 bits). For search and track count instructions, target value of 3 bytes shall be input after the instruction.

$\overline{CS}$ terminal is for chip select when the serial port of microprocessor is used for other interfaces at the same time, and YM7121B receives commands only when $\overline{CS}$ is "L".

HEX	commands	D7	D6	D5	D4	D3	D2	D1	D0	volume	command bytes
00H	STOP	0	0	0	×	0	0	0	0	0	1
01H	+1 TRACK KICK	0	0	0	0	0	0	0	1	0	1
11H	−1 TRACK KICK	0	0	0	1	0	0	0	1	0	1
20H	FEED FORWARD	0	0	1	0	0	0	0	0	0	1
30H	FEED RETURN	0	0	1	1	0	0	0	0	0	1
40H	FOCUS START	0	1	0	×	0	0	0	0	0	1
60H	DISC START	0	1	1	0	0	0	0	0	0	1
70H	DISC BRAKE *1	0	1	1	1	0	0	0	0	0	1
80H	PLAY	1	0	0	0	0	0	0	0	1	1
90H	PLAY MUTE	1	0	0	1	0	0	0	0	0	1
A0H	FF *2	1	0	1	0	0	0	0	0	1/4	1
B0H	FB *2	1	0	1	1	0	0	0	0	1/4	1
C0H	FFF *2	1	1	0	0	0	0	0	0	1/4	1
D0H	FFB *2	1	1	0	1	0	0	0	0	1/4	1
E0H	SEARCH (PAUSE)	1	1	1	0	0	0	0	0	0	4
F0H	TRACK COUNT	1	1	1	1	0	0	0	0	0	4
08H	INITIAL SET	0	0	0	0	1	0	0	0	0	1

*1 : When stop condition is MZ='1' only, in DISC BRAKE,
01110000 → 01110100

*2 : When 1/4 volume makes 0,
101×0000 → 101×1100
110×0000 → 110×1100

SEARCH COMMAND

COMMAND BYTE	1	2	3	4
COMMAND	SEARCH	MINITES	SECONDS	FRAMES

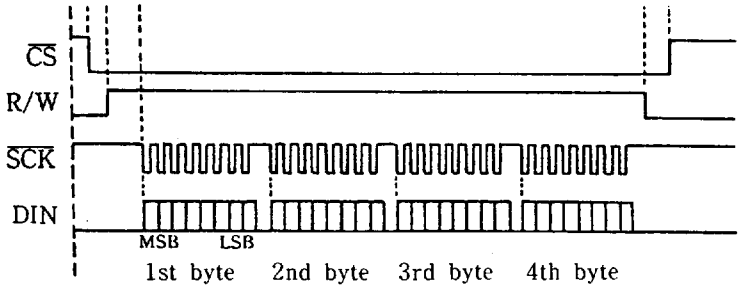
TRACK COUNT COMMAND

COMMAND BYTE	1	2	3	4
COMMAND	TRACK COUNT	TRACK NUMBER		0

D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
S	T7	T6	T5	T4	T3	T2	T1	T0	0	0	0	0	0	0	0

track number = $(1-2S) \times (2^7 \times T7 + 2^6 \times T6 + 2^5 \times T5 + 2^4 \times T4 + 2^3 \times T3 + 2^2 \times T2 + 2^1 \times T1 + T0) \times 128$

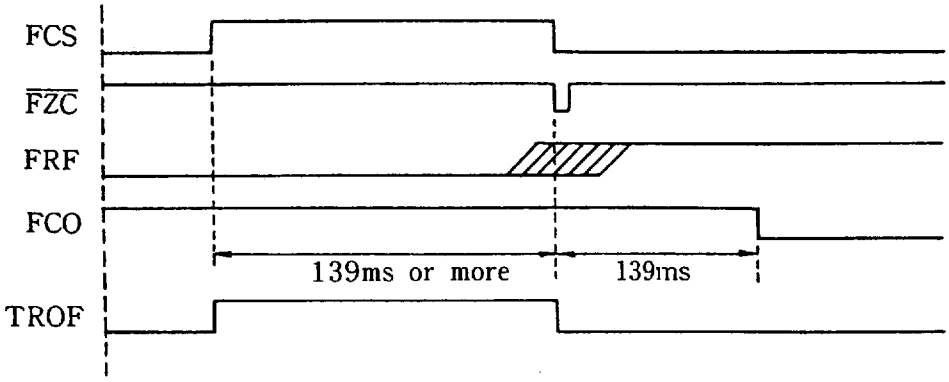
sign bit S = 0 : from inside to outside S = 1 : from outside to inside



9. Focus Servo $\overline{\text{FZC}}$, FRF, FCS, TROF

These terminals are used for focus searching.

FCS (="H") signal is for focus leading. If $\overline{\text{FZC}}$ signal (="L") which is generated at the focus point is detected, leading operation is stopped and FRF signal which detected the mirror level falls FCO flag in the internal status. And during the focus leading, TROF terminal become "H" to keep tracking servo off.



10. Disc Servo DM+ and DM−

DM+ and DM− terminals are provided for speed control of the disc motor. Using PWM output, they output DM+ ="H" when accelerated and DM− ="H" when braking. PWM resolution is 1/144 (945 nS) of one frame (136 μS) and the maximum value is 128/144 (121 μS).

●Combination of command, disc servo internal mode and output

command (HEX)	00", 20", 30"	40"	60"	70"	80", 90", A0", B0", C0", D0", E0", F0"			DM+,DM− (DUTY)	1 frame (136 μs) / 121 μs
internal mode	OFF	HOLD	ACC	BRK	ACC	AFC	PLL		
DM+			O		O	O	O	128/144	
DM+ (PWM)		O					O	1/144~127/144	
no output	O	O	O	O	O	O	O	0	
DM− (PWM)							O	1/144~127/144	
DM−				O		O	O	128/144	

11. Tracking Servo HF, TER, TROF, TRGL, TRHD, KP+, KP−, SVOF, TRBK

HF signal amplitude change caused at the time of track crossing during search is sampled at zero cross point of the tracking error signal TER to output TROF signal. This signal turns on (when TROF="L") and off (TROF="H") the tracking servo, to facilitate the track capturing.

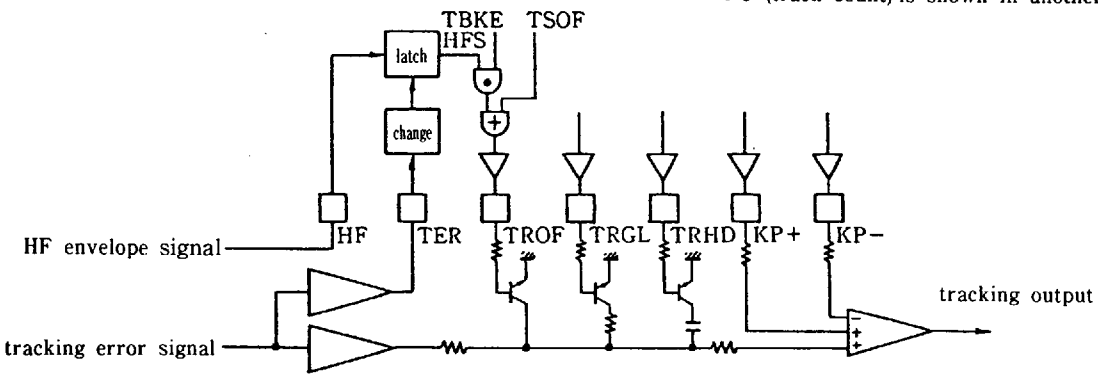
For track kick, KP+ (forward) and KP− (backward) signals are output. At this period, TRHD becomes "H" and have the tracking error signal held. And TRGL is the output to raise the tracking gain after track kick, and TRGL="H" for normal gain.

SVOF is the input to turn off the tracking servo and feed servo from outside. "H" input makes TROF = "H", FEOF="H", TRHD="L", KP+="L", and KP−="L".

TRBK is the input to operate the tracking brake mechanism from outside. Input of "H" to this terminal makes TRGL="L" and the internal control signal TBKE="H".

command	A0"	B0"	C0"	D0"			01"	11"	others *2
repeat cycle (fast forward)	104ms	47.9ms	104ms	104ms			once	once	
TSOF *1									
TBKE *1									
TRGL									
TRHD									
KP+									
KP−									
pattern (ms)	0.272 / 0.544	0.272 / 0.544	0.816 / 1.497	0.816 / 1.497	2.993 / 5.714	2.993 / 5.714	0.136more / 0.181 / 5.6ms TER turn	0.136more / 0.181 / 5.6ms TER turn	
repeat cycle (search)	17.4ms	17.4ms	17.4ms	17.4ms	34.8ms	34.8ms			
search ($E0^H$) (sub mode)	7 · 1	(7 · 4) 7 · 5	7 · 2	7 · 6	7 · 3	7 · 7			7 · 0
time difference (unit : s)	+1/4~+4	(~−1/4) −1/4~+4	−4~+128	−4~−128	+128~	−128~			~+1/4

*1 : TSOF, TBKE indicate LSI's intenal terminals.
*2 : FO^H(track count) is shown in another fig.

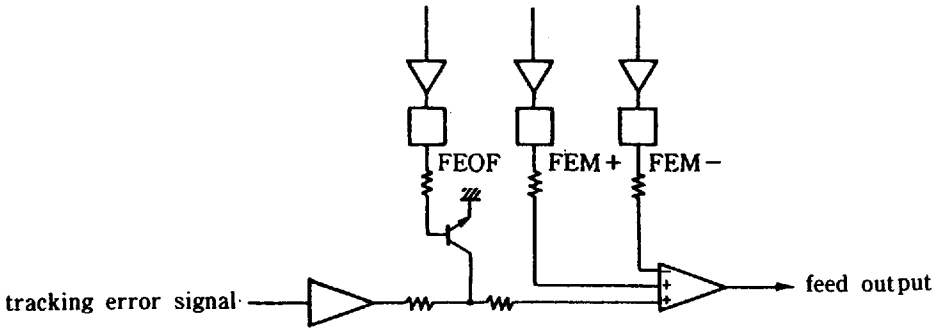


12. Feed Servo Mechanism FEOF, FEM+, FEM−

FEM+ or FEM− signals are output as high-speed feed signals.

During this output, FEOF="H" is also output to cut the feed servo operation.

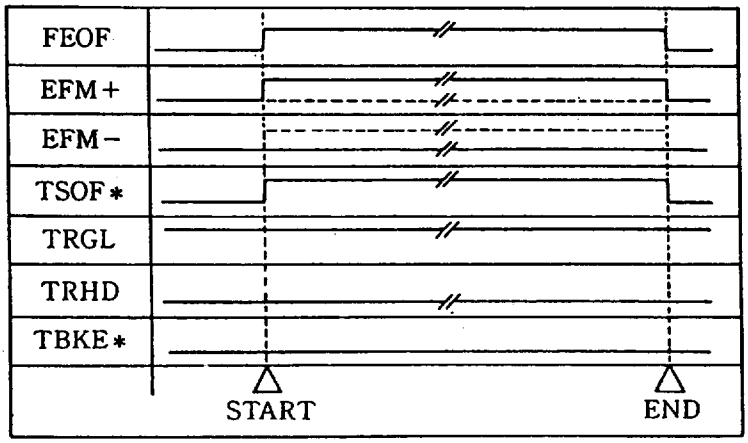
command	00", 40", 60", 70"	20"	30"	80", 90", A0", B0", C0", D0"		
FEOF						
EFM+						
EFM−						
repeat cycle (unit : ms)					34.8ms	34.8ms
sparch (sub mode)				7 · 0, 1, 2 7 · 4, 5, 6	7 · 3	7 · 7



13. Track count commands

When track count commands are implemented, control signals are set at each terminal as shown below. Since TER signals are used for track count, attention is required for TER noise when using track count. Rising of TER signals is differentiated to obtain count pulse. When counted number becomes equal to target value, each control signal will have the same status as that for play mute.

To stop track count, track count command shall be input with the count target value of "0", before necessary command input.

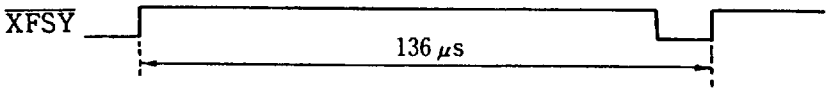


* : TSOF, TBKE are LSI's internal terminals

EFM+, EFM− : — : inside→outside
--- : outside→inside

14. X'tal clock synchronizing signal $\overline{\text{XFSY}}$

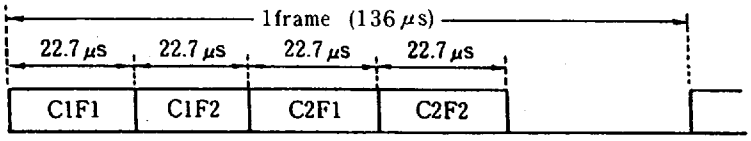
This output is the frame sync. signal of 7.35KHz generated from X'tal clock.



15. Error Correction Check Signals C1 and C2 DTFLG, TEST · IN

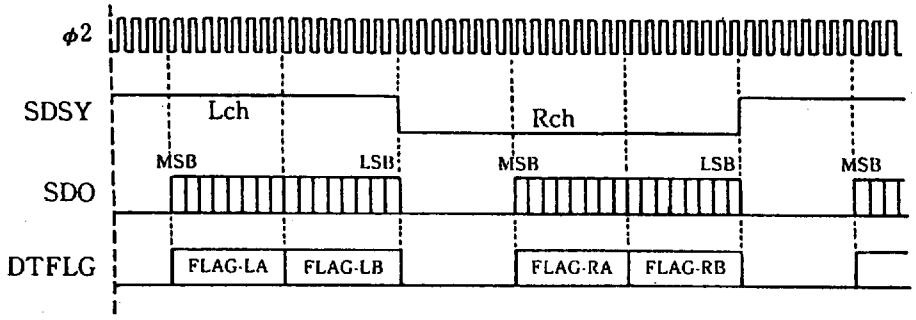
DTFLG terminal is usually used for the flag to show that the SDO output is supplemented by interpolation or preceding data hold. When TESE · IN terminal is set to "L", however, check signal to show the operation of C1 and C2 error correction circuit is output from this terminal.

C1, C2	F1	F2
no error	0	0
single error correction	0	1
double error correction	1	0
uncorrerctable	1	1



16. Data Control and Serial Signal Output ϕ2, SDO, SDSY, DTFLG, $\overline{\text{CDROM}}$

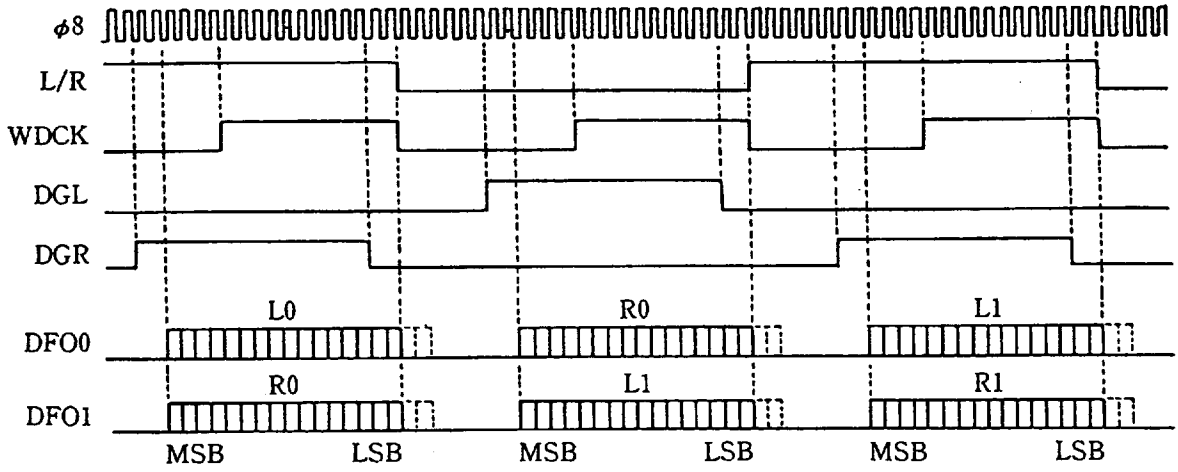
ϕ2 is X'tal clock of 2.1168MHz. SDO is serial signal output with ϕ2 bit rate and is MSB first. DTFLG terminal is used for the error flag to indicate that the SDO output contains interpolation or preceding data hold. This can be used to lighten the burden of software in applications such as CD-ROM. Linear interpolation is used to replace the uncorrectable error data up to eight samples for L/R respectively, and preceding data hold is applied for errors over eight. When $\overline{\text{CDROM}}$ terminal is set to "L", interpolation and preceding data hold can be masked for CD-ROM and other applications.



17. Digital Filter SDI, ϕ8, WDCK, L/R, DFO0, DFO1, DGL, DGR

SDI is an input terminal for four-times oversampling digital filter and usually connected with SDO. DFO0 and DFO1 are serial signals for MSB first DAC ϕ8 bit rate (8.4672MHz). WDCK and L/R are sync. signals.

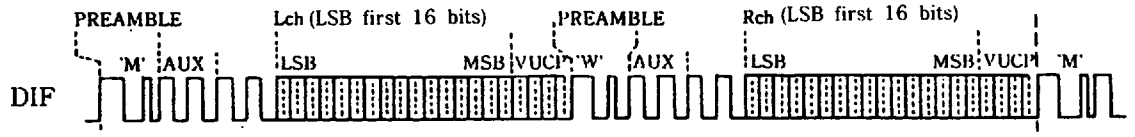
These signals can be used for either of 1DAC or 2DAC system. For 2DAC, Lch output uses DFO0 and Rch output uses DFO1, data latch uses L/R output and deglitcher uses DGL output. For 1DAC, output uses DFO0 and data latch uses WDCK output, and deglitcher uses DGL and DGR outputs.



18. Digital Audio Interface Output DIF

DIF terminal output is digital audio interface format output conforming to EIAJ, and biphase marked with bits C and U.

This output depends on sound volume given in the command. (see the table of p.7) When the volume "0" is commanded, audio data and V flag become "0".



19. Di-emphasis signal DEP

When DEP output is "H", di-emphasis is required.

20. Initial Clear $\overline{IC}$

This LSI needs initial clear operation when turned on.

With VDD at the standard voltage, $\overline{IC}$ shall be kept at "L" for 400 μs or more after clock input to XIN.

21. Test Terminals TEST · IN, TEST · E, TEST · D, T0 to T9

Terminals T0 to T9 are for internal RAM test, and used with non-connected. Other terminals are also for test, but pulled up internally and can be used without connection.

■ ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3～+7.0	V
Input voltage	V_I	−0.3～V_{DD}+0.5	V
Operating temperature	Top	−20～+75	℃
Storage temperature	Tstg	−50～+125	℃

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	Top	0	25	75	℃

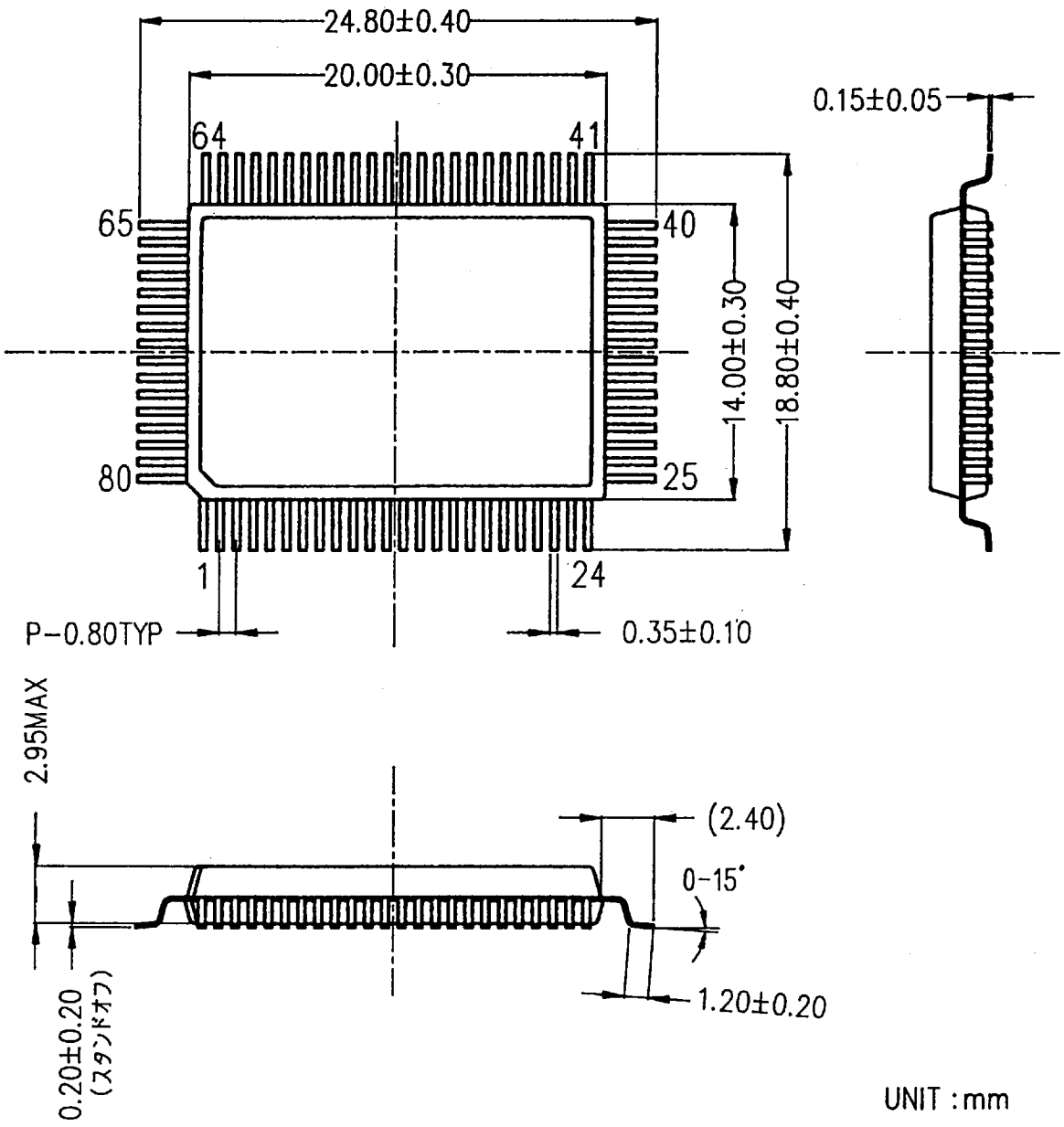
Electrical Characteristics (Condition : Ta=+25℃, VDD = 5.0±0.25V)

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit	Remarks
Power supply current	I_{DD}	V_{DD} =5V		70		mA	
Output voltage H level	V_{OH}	I_{OH} =20μA	4.0			V	
Output voltage L level	V_{OL}	I_{OL} =1mA			0.4	V	
Input voltage H level (1)	V_{IH1}		3.5			V	※1
Input voltage L level (1)	V_{IL1}				1.5	V	※1
Input voltage H level (2)	V_{IH2}		2.0			V	※2
Input voltage L level (2)	V_{IL2}				0.8	V	※2

※1 : Applicable to the terminals EFMI, $\overline{FZC}$, FRF, HF, TER, RCK.

※2 : Applicable to the terminals DIN, $\overline{SCK}$.

■ EXTERNAL DIMENSIONS



UNIT : mm

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