YAMAHA

YMF827B

Application Manual

APL-5

YAMAHA CORPORATION

YMF827B Application Manual
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PRECAUTIONS AND INSTRUCTIONS FOR SAFETY

WARNING

Prohibited	Do not use the device under stresses beyond those listed in Absolute Maximum Ratings.Such stresses may become causes of breakdown, damages, or deterioration, causing explosion or ignition, and this may lead to fire or personal injury.
Prohibited	Do not mount the device reversely or improperly and also do not connect a supply voltage in wrong polarity. Otherwise, this may cause current and/or power-consumption to exceed the absolute maximum ratings, causing personal injury due to explosion or ignition as well as causing breakdown, damages, or deterioration. And, do not use the device again that has been improperly mounted and powered once.
Prohibited	Do not short between pins.In particular, when different power supply pins, such as between high-voltage and low-voltage pins, are shorted, smoke, fire, or explosion may take place.
Instructions	As to devices capable of generating sound from its speaker outputs, please design with safety of your products and system in mind, such as the consequences of unusual speaker output due to a malfunction or failure. A speaker dissipates heat in a voice-coil by air flow accompanying vibration of a diaphragm. When a DC signal (several Hz or less) is input due to device failure, heat dissipation characteristics degrade rapidly, thereby leading to voice-coil burnout, smoking or ignition of the speaker even if it is used within the rated input value.

CAUTION

Prohibited	Do not use Yamaha products in close proximity to burning materials, combustible substances, or inflammable materials, in order to prevent the spread of the fire caused by Yamaha products, and to prevent the smoke or fire of Yamaha products due to peripheral components.
Instructions	Generally, semiconductor products may malfunction and break down due to aging, degradation, etc. It is the responsibility of the designer to take actions such as safety design of products and the entire system and also fail-safe design according to applications, so as not to cause property damage and/or bodily injury due to malfunction and/or failure of semiconductor products.
Instructions	The built-in DSP may output the maximum amplitude waveform suddenly due to malfunction from disturbances etc. and this may cause damage to headphones, external amplifiers, and human body (the ear). Please pay attention to safety measures for device malfunction and failure both in product and system design.
Instructions	As semiconductor devices are not nonflammable, overcurrent or failure may cause smoke or fire. Therefore, products should be designed with safety in mind such as using overcurrent protection circuits to control the amount of current during operation and to shut off on failure.
Instructions	Products should be designed with fail safe in mind in case of malfunction of the built-in protection circuits. Note that the built-in protection circuits such as overcurrent protection circuit and high-temperature protection circuit do not always protect the internal circuits. In some cases, depending on usage or situations, such protection circuit may not work properly or the device itself may break down before the protection circuit kicks in.
Instructions	Use a robust power supply.The use of an unrobust power supply may lead to malfunctions of the protection circuit, causing device breakdown, personal injury due to explosion, or smoke or fire.
Instructions	Product's housing should be designed with the considerations of short-circuiting between pins of the mounted device due to foreign conductive substances (such as metal pins etc.). Moreover, the housing should be designed with spatter prevention etc. due to explosion or burning. Otherwise, the spattered substance may cause bodily injury.
Instructions	The device may be heated to a high temperature due to internal heat generation during operation.Therefore, please take care not to touch an operating device directly.
Instructions	Electrostatic discharges can damage and destroy semiconductor devices.Pay close attention to static build-up when handling devices.

v03

Table of Contents

Introduction

This document describes the functions, applications, and electrical characteristics of YMF827B.

The document structure is summarized as follows:

- 1. Overview
- 2. Features
- 3. Pin Assignment
- 4. Pin Function
- 5. Block Diagram
- 6. Application Information
- 7. Typical Application Circuits
- 8. Electrical Characteristics
- 9. Package Information

Symbols, Marks, and Notations

Icons used in this document

: Indicates noteworthy restrictions and pitfalls often seen in the application.

: Indicates supplementary information and design hints.

Numbers

Numbers are expressed in the form: <size> <base_format> <number>. In this form, <size>, size in bits, and <base_format> elements are optional. Single bits, binary numbers of 1-bit size, are expressed in another form that is described later in this section.

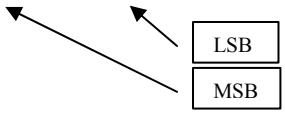
Example: *The value of* ***15*** *(in decimal) expressed in different bases:*

- *Binary:* ***8'b 0000_1111***
- *Decimal:* ***15*** *(of unspecified size and in the default base of 10)*
- *Hexadecimal:* ***8'h0F***

Bit/Digit Order

- The most significant bit or digit appears first in <number>, followed by progressively less significant bits, and the least significant bit or digit at the end.

Example: *8'b 1000_1110*



Binary value is thus converted to its corresponding value using

$(2^n \times Dn) + \cdots (2^1 \times D1) + (2^0 \times D0)$

Example: *If REG_A register is described as:*

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
REG_A							

and when D7 through D0 has the value of 8'b 0001_0101,
REG_A value in decimal is 21. $(21 = 2^4 + 2^2 + 2^0)$

Single Bit Notations

- Logic signal level on input and output pins is represented as "L" or "H".
- Otherwise, it is represented as "0" or "1".

Other Notations

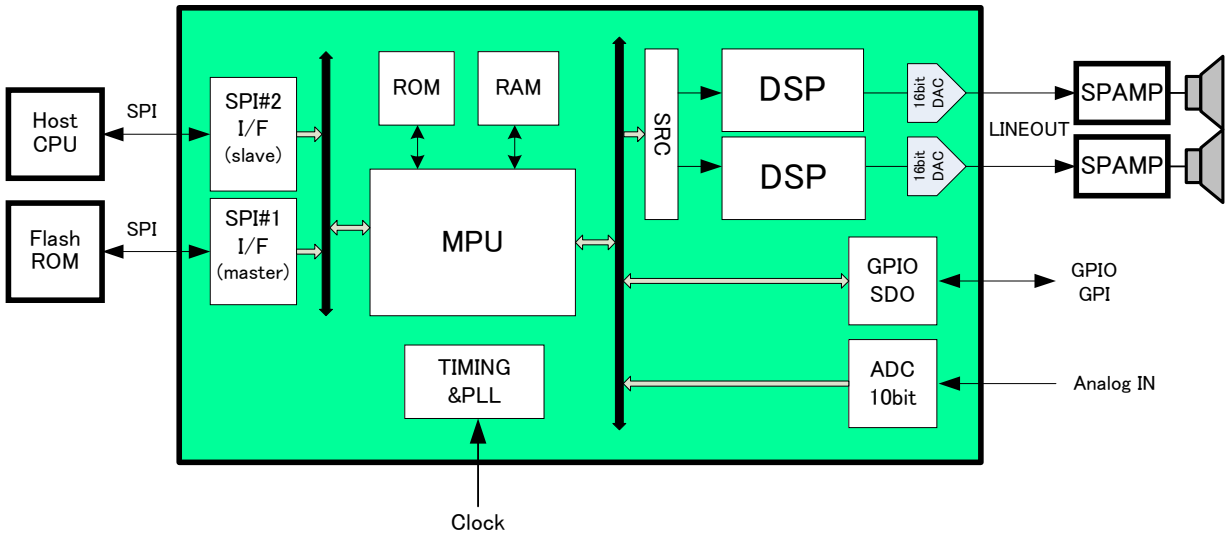
System Sampling Rate

fs, when appears in this document, represents the system sampling rate used in signal processing on this device. ***fs*** is nominally 48 kHz, assuming 24.576 MHz clock input on XI terminal.

fs changes if the clock is changed from the default frequency.

1. Overview

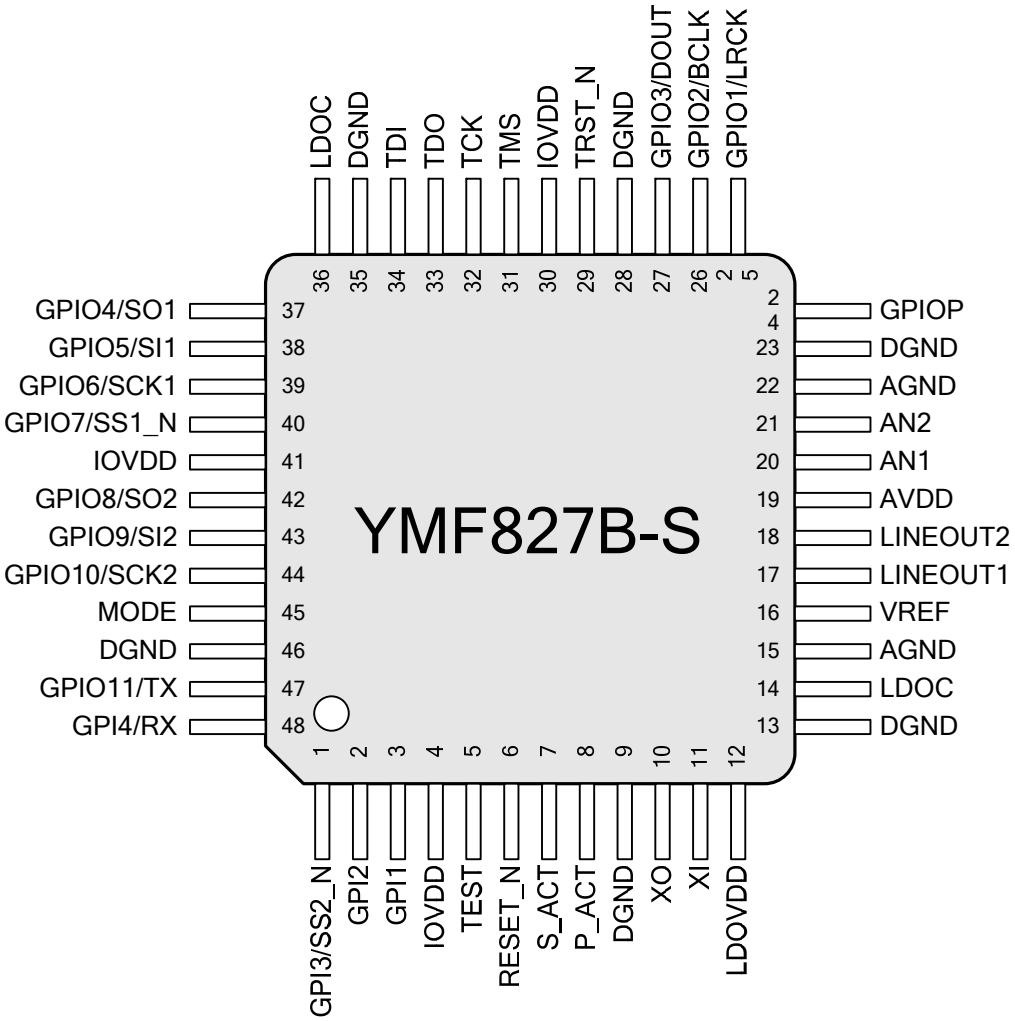
YMF827B is a sound generator device designed for automobile applications.
The integrated DSP is optimized for audio processing and comes with ready-to-use sound conditioning functions like Equalizer, DRC (Dynamic Range Control), and Harmonics Enhancer (audio bandwidth extension) that can be used to optimize reproductions of a given sound material on a wide variety of sound hardware, eliminating the need for offline conditioning of the source materials.
Two sets of DAC allow reproducing two independent set of sounds simultaneously.
When external DACs are connected to the optional two-channel I2S digital audio output on GPIO pins, up to four channels of output are available.
Stand-alone operations playing back contents on the attached flash ROM as well as playing back the contents received from the host controller is supported.



2. Features

- Input and Output Ports
  - Synchronous serial interfaces (SPI compliant)
    Master mode port (SPI#1) and slave mode port (SPI#2)
  - Asynchronous start-stop serial interface (UART compliant)
  - Up to 12 GPIO ports (sharing pins with SPI#1, SPI#2, UART, and I2S ports in mutually exclusive way)
  - Up to 4 GPI ports (sharing pins with SPI#2 and UART ports in mutually exclusive way)
  - Two analog input ports (for 10-bit A/D converter)
- Sound Generator
  - Playing back sound contents sent from the host controller
  - Playing back sound contents on the attached flash ROM
  - DSP and Audio Output
  - DSP processing on 2 of the 4 output channels
    Sound conditioning with 3-band parametric equalizer, Harmonics Enhancer, and DRC processing
  - Integrated 16-bit D/A converters supports two independent sets of sounds from the two LINEOUTs
  - Up to four output channels can be supported with external DACs connected to the optional digital audio output (I2S) port
- Others
  - Clock frequency: 24.576 MHz (quartz crystals assumed)
  - Sleep state reduces standby power consumption
  - Lead-free 48-pin SQFP
  - Supply Voltage: Single 3.3 V power supply (1.8 V generated from 3.3 V with the on-chip LDO regulator)
  - Operating Ambient Temperature: −40 ℃ to + 105 ℃

3. Pin Assignment



<48-pin SQFP Top View>

4. Pin Functions

4.1. Pin List

No.	Pin Name	I/O	Power Supply	Function
1	GPI3/SS2_N	Ish	IOVDD	GPI3 / SPI #2 chip select input
2	GPI2	Ish	IOVDD	GPI2
3	GPI1	Ish	IOVDD	GPI1
4	IOVDD	P	—	Digital power supply (3.3 V typ.)
5	TEST	Ish	IOVDD	Device test signal input (For normal operations, this pin should be connected to DGND.)
6	RESET_N	Ish	IOVDD	Hardware Reset
7	S_ACT	Ish/O	IOVDD	Device startup time adjustments and startup notifications
8	P_ACT	O	IOVDD	Device startup time adjustments and startup notifications
9	DGND	G	—	Digital ground
10	XO	O	IOVDD	Crystal (24.576 MHz) connection
11	XI	Ish	IOVDD	Crystal (24.576 MHz) connection or external 24.576 MHz clock input
12	LDOVDD	P	—	Supply to the on-chip LDO (3.3 V typ.)
13	DGND	G	—	Digital ground
14	LDOC	P_{OUT}	—	LDO output for attaching capacitor
15	AGND	G	—	Analog ground
16	VREF	A	AVDD	Analog reference voltage
17	LINEOUT1	A	AVDD	Line level output #1
18	LINEOUT2	A	AVDD	Line level output #2
19	AVDD	P	—	Analog power supply (3.3 V typ.)
20	AN1	A	AVDD	ADC input 1
21	AN2	A	AVDD	ADC input 2
22	AGND	G	—	Analog ground
23	DGND	G	—	Digital ground
24	GPIOP	Ish/O	IOVDD	Dedicated GPIO port
25	GPIO1/LRCK	Ish/O	IOVDD	GPIO1 / I2S LRCK output
26	GPIO2/BCLK	Ish/O	IOVDD	GPIO2 / I2S BCLK output
27	GPIO3/DOUT	Ish/O	IOVDD	GPIO3 / I2S Data output
28	DGND	G	—	Digital ground
29	TRST_N	Ish	IOVDD	JTAG (TRST_N)
30	IOVDD	P	—	Digital power supply (3.3 V typ.)
31	TMS	Ish	IOVDD	JTAG (TMS)
32	TCK	Ish	IOVDD	JTAG (TCK)
33	TDO	O	IOVDD	JTAG (TDO)
34	TDI	Ish	IOVDD	JTAG (TDI)
35	DGND	G	—	Digital ground

No.	Pin Name	I/O	Power Supply	Function
36	LDOC	P_{OUT}	—	LDO decoupling capacitor
37	GPIO4/SO1	Ish/O	IOVDD	GPIO4 / SPI #1 data output
38	GPIO5/SI1	Ish/O	IOVDD	GPIO5 / SPI #1 data input
39	GPIO6/SCK1	Ish/O	IOVDD	GPIO6 / SPI #1 clock output
40	GPIO7/SS1_N	Ish/O	IOVDD	GPIO7 / SPI #1 chip select output
41	IOVDD	P	—	Digital power supply (3.3 V typ.)
42	GPIO8/SO2	Ish/O	IOVDD	GPIO8 / SPI #2 data output
43	GPIO9/SI2	Ish/O	IOVDD	GPIO9 / SPI #2 data input
44	GPIO10/SCK2	Ish/O	IOVDD	GPIO10 / SPI #2 clock input
45	MODE	Ish	IOVDD	Mode selection
46	DGND	G	—	Digital ground
47	GPIO11/TX	Ish/O	IOVDD	GPIO11 / UART output
48	GPI4/RX	Ish	IOVDD	GPI4 / URAT#1 input

Ish : Digital input (Schmitt trigger input)

O : Digital output

A : Analog port

P : Power Supply

$P_{OUT:}$ Regulator output

G : Ground

See *7.1.1. Resistor and Capacitor in P_ACT and S_ACT* for further information on external component values.

4.2. Pin Descriptions

4.2.1. Power Supply Pins

4.2.1.1. IOVDDs

IOVDD pins supply power to the input and output circuits.
The rated operating voltage range is from 3.0 V to 3.6 V.
Connect 0.1 µF capacitor across IOVDD and DGND.

4.2.1.2. LDOVDD

LDOVDD pin supplies the on-chip regulator.
Connect 0.1 µF capacitor across LDOVDD and DGND.
LDOVDD must be tied to IOVDD on the printed circuit board and powered from the same power supply.

4.2.1.3. AVDD

AVDD pin supplies power to the analog block (DAC, ADC, etc.).
The rated operating voltage range is from 3.0 V to 3.6 V.
Connect 0.1 µF capacitor across AVDD and AGND.

4.2.1.4. DGNDs

DGND pins are the ground returns for both IOVDD and LDOVDD supplies.

4.2.1.5. AGNDs

AGND pins are the ground returns for AVDD supply.

4.2.1.6. LDOCs

The LDOC pins are the on-chip regulator's output pin for capacitor connections.
Put 2.2 µF capacitor from this pins to the ground and place it as close to this pin as possible.

Decoupling (bypass) Capacitor

Connect decoupling capacitors to the ground on the LDOVDD, IOVDD, and AVDD pins.

4.2.2. Clock Pins

4.2.2.1. XI (input)

XI pin is for connecting a crystal or CERALOCK® and also used for external clock inputs.

4.2.2.2. XO (output)

XO pin is for connecting a crystal or CERALOCK®. Do not use this pin in other ways.
This XO pin must be left open if externally generated clocks are fed to XI pin.

4.2.3. Hardware Reset Pin

4.2.3.1. RESET_N (input)

When RESET_N is driven "L", digital core supply is turned off, putting the digital core in Sleep state to reduce power consumption.
When RESET_N is changed from "L" to "H", digital core supply will be turned on and the digital core will be initialized, then resume from the Sleep state.

4.2.4. MODE Selection Pin

4.2.4.1. MODE (Input)

Immediately after the digital core block is turned on, the integrated MPU examines the level of MODE pin to determine the functions of shared pins. The pin functions depend on the logic level of MODE pin as shown in the table below.
(The shared pins function as GPI and GPIO pins until the decision.)
See the pin descriptions described below for the detail.

Pin Name	MODE = "L"	MODE = "H"
GPIO7 / SS1_N	GPIO7	SS1_N (SPI#1)
GPIO6 / SCK1	GPIO6	SCK1 (SPI#1)
GPIO5 / SI1	GPIO5	SI1 (SPI#1)
GPIO4 / SO1	GPIO4	SO1 (SPI#1)
GPI3 / SS2_N	SS2_N (SPI#2)	GPI3
GPIO10 / SCK2	SCK2 (SPI#2)	GPIO10
GPIO9 / SI2	SI2 (SPI#2)	GPIO9
GPIO8 / SO2	SO2 (SPI#2)	GPIO8

4.2.5. UART / GPIO (GPI) Pins

The on-chip firmware does not use UART.

4.2.5.1. GPI4/RX (input)

Use a command from the host controller to switch the function between GPI4 and RX.
This pin functions as GPI4 on reset.

4.2.5.2. GPIO11/TX

Use a command from the host controller to switch the function between GPIO11 and TX.
This pin functions as GPIO11 on reset.

4.2.6. SPI #1 / GPIO (GPI) Pins

When SPI#1 is used, this device operates as a master device to the devices on the SPI bus.

4.2.6.1. GPIO7 / SS1_N

Immediately after the digital core block is turned on, the integrated MPU examines the level of MODE pin to determine this pin's function between GPIO7 and SS1_N.
The pin function can be switched by a command from the host controller as well.
MODE = “L”: GPIO7 pin
MODE = “H”: SS1_N pin (outputs slave select on SPI#1 bus)

4.2.6.2. GPIO6 / SCK1

Immediately after the digital core block is turned on, the integrated MPU examines the level of MODE pin to determine this pin's function between GPIO6 and SCK1.
The pin function can be switched by a command from the host controller as well.
MODE = “L”: GPIO6 pin
MODE = “H”: SCK1 pin (outputs serial data clock for SPI#1 bus)

4.2.6.3. GPIO5 / SI1

Immediately after the digital core block is turned on, the integrated MPU examines the level of MODE pin to determine this pin's function between GPIO5 and SI1.
The pin function can be switched by a command from the host controller as well.
MODE = “L”: GPIO5 pin
MODE = “H”: SI1 (inputs serial data on SPI#1 bus)

4.2.6.4. GPIO4 / SO1

Immediately after the digital core block is turned on, the integrated MPU examines the level of MODE pin to determine this pin's function between GPIO4 and SO1. The pin function can be switched by a command from the host controller as well.
MODE = “L”: GPIO4 pin
MODE = “H”: SO1 (outputs serial data on SPI#1 bus)

When SS1_N = “H”, this pin enters the high-impedance state.
Pull up this pin with an external resistor if necessary.

4.2.7. SPI #2 / GPIO (GPI) Pins

When SPI#2 is used, this device operates as a slave device to the master device on the SPI bus.

4.2.7.1. GPI3 / SS2_N (input)

Immediately after the digital core block is turned on, the integrated MPU examines the level of MODE pin to determine this pin's function between GPI3 and SS2_N. The pin function can be switched by a command from the host controller as well.

MODE = “L”: SS2_N pin (inputs slave select on SPI#2 bus)
MODE = “H”: GPI3 pin

4.2.7.2. GPIO10 / SCK2

Immediately after the digital core block is turned on, the integrated MPU examines the level of MODE pin to determine this pin's function between GPI10 and SCK2. The pin function can be switched by a command from the host controller as well.

MODE = “L”: SCK2 pin (inputs serial data clock for SPI#2 bus)
MODE = “H”: GPIO10 pin

4.2.7.3. GPIO9/SI2

Immediately after the digital core block is turned on, the integrated MPU examines the level of MODE pin to determine this pin's function between GPIO9 and SI2. The pin function can be switched by a command from the host controller as well.

MODE = “L”: SI2 (inputs serial data on SPI#2 bus)
MODE = “H”: GPIO9 pin

4.2.7.4. GPIO8 / SO2

Immediately after the digital core block is turned on, the integrated MPU examines the level of MODE pin to determine this pin's function between GPIO8 and SO2. The pin function can be switched by a command from the host controller as well.

MODE = “L”: SO2 (outputs serial data on SPI#2 bus)
When SS2_N = “H”, this pin enters the high-impedance state.
Pull up this pin with an external resistor if necessary.
MODE = “H”: GPIO8 pin

4.2.8. I2S / GPIO Pins

These pins can switch its function between GPIO and I2S modes by using a command from the host controller.
They function as (input) GPIO ports on reset.

4.2.8.1. GPIO1 / LRCK

GPIO1 (GPIO mode): GPIO1 pin
LRCK (I2S mode): I2S word clock output pin

4.2.8.2. GPIO2 / BCLK

GPIO2 (GPIO mode): GPIO2 pin
BCLK (I2S mode): I2S bit clock output pin

4.2.8.3. GPIO3 / DOUT

GPIO3 (GPIO mode): GPIO3 pin
DOUT (I2S mode): I2S bit data output pin

4.2.9. GPI Pins

4.2.9.1. GPI1, GPI2

These unshared pins work as general purpose input.

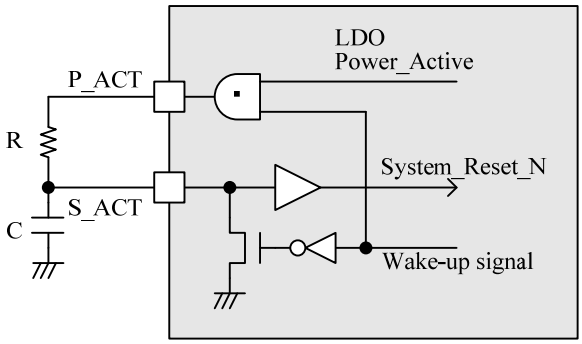
4.2.10. GPIO Pin

4.2.10.1. GPIOP

This unshared pin works as general purpose programmable input and output. This pin is an input on reset.

4.2.11. P_ACT / S_ACT

Connect the resistor R and capacitor C network to P_ACT and S_ACT pins as shown in the diagram below.
The digital core block must be held in its reset state with its power supplied until the crystal (or CERALOCK®) connected to XI and XO pins starts generating stable clocks.
Adjust the RC time constant to provide enough time in the reset state.



4.2.11.1. S_ACT

S_ACT drives "L" when the digital core block is in Sleep state. This pin enter the high-impedance state when the core supply is turned on.
This pin can also be used to reset the digital core block from outside by applying "L".
Notice that this pin can be used as an indication that the digital core block is resumed from Sleep state and in operation.

4.2.11.2. P_ACT

P_ACT drives "L" when the digital core block is in Sleep state and drives "H" when the core supply is turned on.

4.2.12. Analog Pins

4.2.12.1. VREF

Analog reference voltage pin.
Connect 1 μF capacitor from this pin to the ground.

4.2.12.2. LINEOUT1, 2

Line level output pins from the two on-chip DA converters.

4.2.12.3. AN1, AN2

Input pins for the on-chip AD converter.

4.2.13. JTAG Pins

4.2.13.1. TDI, TCK, TMS, TRST_N

JTAG input pins for the integrated MPU.

4.2.13.2. TDO

JTAG output pin for the integrated MPU.

4.2.14. Test Pin

4.2.14.1. TEST

A test mode control pin. During normal operations, connect to DGND.

4.3. Pin States

4.3.1. Digital Signal Pins

4.3.1.1. During Hardware Reset

The table below shows the digital pin states during the hardware reset (RESET_N = "L"):

Pin Name	Description
RESET_N	This pin must remain "L" throughout the hardware reset. (See *8. Electrical Characteristics* for further information on input timing.)
XO	Driving "H"
S_ACT P_ACT	Driving "L"
GPIOP GPIO1/LRCK GPIO2/BCLK GPIO3/DOUT GPIO4/SO1 GPIO5/SI1 GPIO6/SCK1 GPIO7/SS1_N GPIO8/SO2 GPIO9/SI2 GPIO10/SCK2 GPIO11/TX	In the high-impedance state
TDO	In the high-impedance state
GPI1 GPI2 GPI3/SS2_N GPI4/RX MODE TDI TCK TMS TRST_N	These pins must be fixed to either "H" or "L". Intermediate levels are not allowed.
TEST	This pin must be fixed to "L".

4.3.1.2. Immediately After Hardware Reset

The table below shows the digital pin states immediately after the hardware reset (RESET_N = "L"→ "H"):

Pin Name	Description
XI XO	When a crystal (or CERALOCK®) is connected between XI and XO pins: Oscillation will eventually start. When an external clock feeds XI pin: XO pin will output the clocks on XI pin.
S_ACT	In the high-impedance state
P_ACT	This pin is initially "L" and becomes "H" eventually once the digital core power is supplied
GPIOP GPIO1/LRCK GPIO2/BCLK GPIO3/DOUT GPIO4/SO1 GPIO5/SI1 GPIO6/SCK1 GPIO7/SS1_N GPIO8/SO2 GPIO9/SI2 GPIO10/SCK2 GPIO11/TX	These pins will be GPIO inputs until the integrated MPU configures them. These pins must be fixed to either "H" or 'L". Intermediate levels are not allowed.
TDO	This pin will drive either "L" or "H".
GPI1 GPI2 GPI3/SS2_N GPI4/RX MODE TDI TCK TMS TRST_N	These pins must be fixed to either "H" or "L". Intermediate levels are not allowed.
TEST	This pin must be fixed to "L".

4.3.1.3. Digital Core Block Sleep State

The table below shows the digital pin states when the digital core block is in Sleep state (RESET_N = "H"):

Pin Name	Description
XO	Driving "H"
S_ACT P_ACT	Driving "L"
GPIOP GPIO1/LRCK GPIO2/BCLK GPIO3/DOUT GPIO4/SO1 GPIO5/SI1 GPIO6/SCK1 GPIO7/SS1_N GPIO8/SO2 GPIO9/SI2 GPIO10/SCK2 GPIO11/TX	In the high-impedance state
TDO	In the high-impedance state
MODE TDI TCK TMS TRST_N	These pins must be fixed to either "H" or "L". Intermediate levels are not allowed.
GPI3/SS2_N GPI4/RX	These pins must be driven "H" to maintain Sleep state. Intermediate levels are not allowed.
GPI1 GPI2	These pins must be driven "L" to maintain Sleep state. Intermediate levels are not allowed.
TEST	This pin must be fixed to "L".

4.3.1.4. LDOVDD, IOVDD Unpowered

The table below shows the digital pin states when the power is not supplied. (LDOVDD = IOVDD = 0 V)

Pin Name	X: voltage level on the pin		
	X < −0.4 V	−0.4 V ≤ X ≤ 0.4 V	0.4 V < X
S_ACT GPIOP GPIO1/LRCK GPIO2/BCLK GPIO3/DOUT GPIO4/SO1 GPIO5/SI1 GPIO6/SCK1 GPIO7/SS1_N GPIO8/SO2 GPIO9/SI2 GPIO10/SCK2 GPIO11/TX GPI1 GPI2 GPI3/SS2_N GPI4/RX TDI TCK TMS TRSET_N MODE TEST	In the driving state	In the high-impedance state	In the high-impedance state
XI XO P_ACT TDO	In the driving state	In the high-impedance state	In the driving state

* The threshold values of ±0.4 V have some variations. 0.4 V is the typical value.

4.3.2. Analog Pins

State / Pin Name	Sleep State	Operating State				
		AP_VR="1"	AP_VR="0"	AP_VR="0"	AP_VR="0"	AP_VR="0"
		AP_DA1="1"	AP_DA1="1"	AP_DA1="0"	AP_DA1="0"	AP_DA1="0"
		AP_DA2="1"	AP_DA2="1"	AP_DA2="1"	AP_DA2="0"	AP_DA2="0"
		AP_AD="1"	AP_AD="1"	AP_AD="1"	AP_AD="1"	AP_AD="0"
VREF	Z(0 V)	←	Z(1.5 V)	←	←	←
LINEOUT1	F or Z(0 V) (Note 1.)	←	←	D(0.5 V to 2.5 V)	←	←
LINEOUT2	F or Z(0 V) (Note 1.)	←	←	←	D(0.5 V to 2.5 V)	←
AN1, AN2	F	←	←	←	←	F (Note 2.)
LDOC	F	←	D(1.8 V)	←	←	←

F: In the high-impedance state with floating potentials

Z: In the high-impedance state at the specific voltage in parentheses.

D: In the driving state with the voltage in parentheses.

Note 1: "F" when no load is connected to the line level output pins (LINEOUT1, LINEOUT2), "Z(0 V)" otherwise.

Note 2: In the high-impedance state when no AD conversion is in progress, "AVDD/2" in parallel with the input capacitance of 12.8 pF when AD conversion is in progress.

4.3.3. Unused Pins

Unused pins must be wired as follows.
When pulling up to a supply or down to the ground, do so with a 10 kΩ register.

Power supply, ground, clock input (XI), hardware reset (RESET_N), analog reference voltage (VREF), startup timing control (P_ACT and S_ACT) pins are always used, and not included in this table.

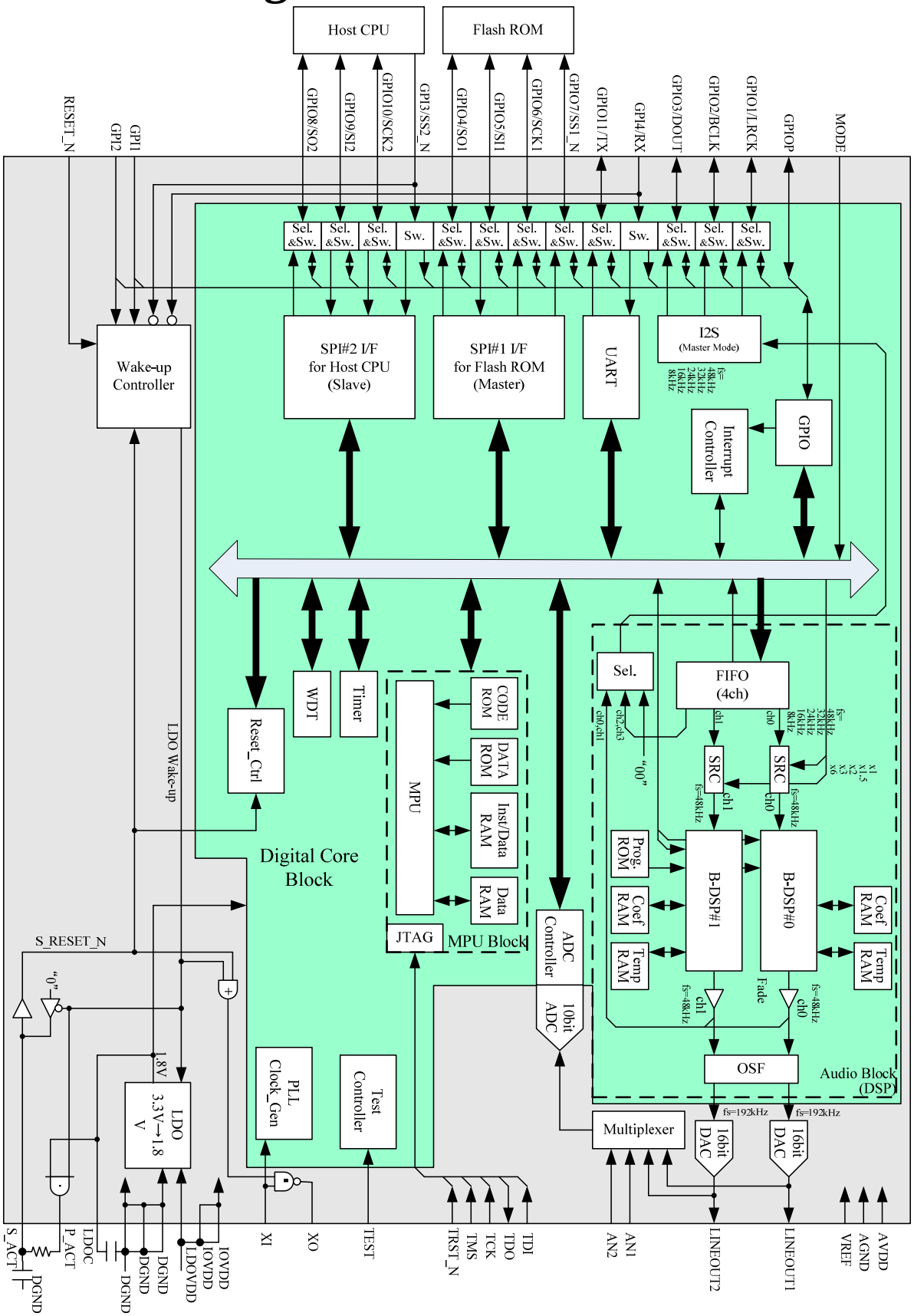
Pin	Wiring when unused
XO	Be left open (unconnected).
GPIOP GPIO1/LRCK GPIO2/BCLK GPIO3/DOUT GPIO4/SO1 GPIO5/SI1 GPIO6/SCK1 GPIO7/SS1_N GPIO8/SO2 GPIO9/SI2 GPIO10/SCK2 GPIO11/TX	Pull up to IOVDD, or down to DGND.
GPI1 GPI2	Tie to or pull down to DGND.
GPI3/SS2_N GPI4/RX	Tie to or pull up to IOVDD.
TDI TCK TMS	Pull up to IOVDD.
TRST_N	Pull down to DGND.
TDO	Be left open (unconnected).
AN1 AN2	Be left open (unconnected), or tie to AGND.
LINEOUT1 LINEOUT2	Be left open (unconnected).
TEST	Must be tied to DGND.

4.3.4. Input Pins

A pin left open in its input state can cause short circuit current through its input stage transistors.
Unconnected pins must be wired as follows.
When pulling up to a supply or down to the ground, do so with a 10 kΩ register.

Pin Name	Unused Pin Connection
XI	Pull up to IOVDD or pull down to DGND with a resistor if the signal source supplying clocks to XI pin sometimes leave the pin open.
RESET_N	Pull down to DGND.
GPIOP GPIO1/LRCK GPIO2/BCLK GPIO3/DOUT GPIO4/SO1 GPIO5/SI1 GPIO6/SCK1 GPIO7/SS1_N GPIO8/SO2 GPIO9/SI2 GPIO10/SCK2 GPIO11/TX	The pins are in input states by default on reset before it can be configured as an output. Pull up to IOVDD or pull down to DGND with a resistor. When connecting to a pin that enters its high impedance state from time to time, pull up to IOVDD or pull down to DGND.
GPI1 GPI2 GPI3/SS2_N GPI4/RX	When connecting to a pin that enters its high impedance state from time to time, pull up to IOVDD or pull down to DGND.
TDI TCK TMS	When connecting to a pin that enters its high impedance state from time to time, pull up to IOVDD.
TRST_N	When connecting to a pin that enters its high impedance state from time to time, pull down to DGND.

5. Block Diagram



[Digital Core Block]

The green part is the digital core block operating from the 1.8 V supply of the integrated regulator.
This block consists of the following sub-blocks:

● Integrated MPU Block

Yamaha's proprietary 32-bit processor. This MPU handles the sound contents playbacks, pitch controls, volume controls, and other controls.

● Serial Interface Block

➢ UART

One UART (Universal Asynchronous Receiver Transmitter) is provided as an auxiliary interface to the host controller.

A command from the host controller (on SPI bus) will switch the shared pin functions between GPIO (GPI) and UART. The on-chip firmware does not support this UART interface. The bit rate of the UART can be selected from the following: 230.4 k, 115.2 k, 57.6 k, 38.4 k, 19.2 k, 10.4 k, 9.6 k, 1.2 k, and 300.

➢ SPI#1 (Master) Interface

One SPI master interface is provided for flash ROM connections. Immediately after the digital core block is turned on, the integrated MPU examines the level of MODE pin to determine the shared pin functions between GPIO (GPI) and SPI#1.

These pin functions can be switched by a command from the host controller as well.

➢ SPI#2 (Slave) Interface

One SPI slave interface is provided for the host controller communications. Immediately after the digital core block is turned on, the integrated MPU examines the level of MODE pin to determine the shared pin functions between GPIO (GPI) and SPI#2. These pin functions can be switched by a command from the host controller as well.

● Integrated MPU Peripherals

➢ GPIO Ports

Up to 12 bidirectional GPIO ports and up to 4 input-only GPI ports can be used.

The list below shows the grouping of these ports:

- Unshared GPIO: 1 pin
- Shared GPIO (default) and digital audio output: 3 pins
- Shared GPIO (default) and UART: 1 pin
- Shared GPIO pins (default) and SPI#1, SPI#2: 7 pins
- Unshared GPI: 2 pins
- Shared GPI (default) and UART: 1 pin
- Shared GPI (default) and SPI#1: 1 pin

➢ Timer

The integrated MPU uses this Timer to measure time.

- Interrupt Controller

  Interrupt Controller provides interrupt controls.

- WDT

  Watch Dog Timer. The WDT will reset the device when the integrated MPU become unresponsive due to some fault condition.

- ADC Controller Block

  The integrated MPU controls the AD converter.

● Audio Block

Audio Block consists of DSP block and I2S block.

- DSP Block
  - FIFO → SRC

    The wave data in sampling frequency (fs = 8 kHz, 16 kHz, 24 kHz, 32 kHz, 48 kHz) on FIFO is converted to the one in fs = 48 kHz and sent to B-DSP.
  - B-DSP#0, #1

    These DSPs provides 3-band parametric equalizer, Harmonics Enhancer, DRC (Dynamic Range Control) processing. Two of the output channel can be processed, and in independent way.
  - Fade

    Fade mute the B-DSP outputs in addition to applying fade-in and fade-out.
  - OSF

    Four-times over sampling filter.

    The signal sampled at fs = 48 kHz is oversampled at fs = 192 kHz and sent to DAC.

- I2S Block

  I2S block outputs the digital audio signals from DSP block in a 2 channel serial format.

● PLL, Clock Generator Block

This block generates clocks required for device operations using a PLL.

[Analog Block]

Analog Block operates from AVDD (3.3 V) supply.

● DAC Block

DAC block converts digital signals (16 bits) from Audio Block into analog signals.

● Line-Level Output Block

Two monaural line level analog outputs from the DAC is provided.

● ADC Block

ADC block is provided for general analog input and also for monitoring the line level output signals.

[Others]

● Wake-up Controller

Wake-up Controller will turn on digital core supply to start the digital core when the core is in Sleep and RESET_N pin is changed from “L” to “H”.

● LDO

Low dropout regulator is integrated to convert 3.3 V on LDOVDD pin into 1.8 V for the digital core.

6. Application Information

6.1. Initializations / Controls and Power Management Settings

6.1.1. Start, Stop, Sleep Controls

6.1.1.1. Power Up

No.	Action	Description
1	Disable the output of circuitry using LINEOUT signals, such as amplifier.	
2	With RESET_N held "L", turn on LDOVDD, IOVDD, and AVDD.	See *8.5.1. Power Supply and Reset Timing* for the minimum time required to keep the RESET_N low.
3	Drive RESET_N "H".	
4	Wait for S_ACT to change from "L" to "H".	The wait time depends on the RC constant on the S_ACT network. It will be about 250 μs when a 0.01 μF capacitor and an 18 kΩ resistor are used.
5	Wait for 10 ms after the step 4.	This wait time allows the PLL to stabilize and the firmware to start execution.
6	Start the on-chip firmware execution.	See *the firmware document* for further information.
7	Enable the output of circuitry using LINEOUT signals.	

6.1.1.2. Entering Sleep State With RESET_N

No.	Action	Description
1	Stop the playback.	Entering Sleep in the middle of a playback results in noise. See *the firmware document* for how to stop playbacks.
2	Disable the output of circuitry using LINEOUT signals.	
3	Drive RESET_N "L".	The digital core power is turned off and the core enters Sleep state.

6.1.1.3. Resuming From Sleep State

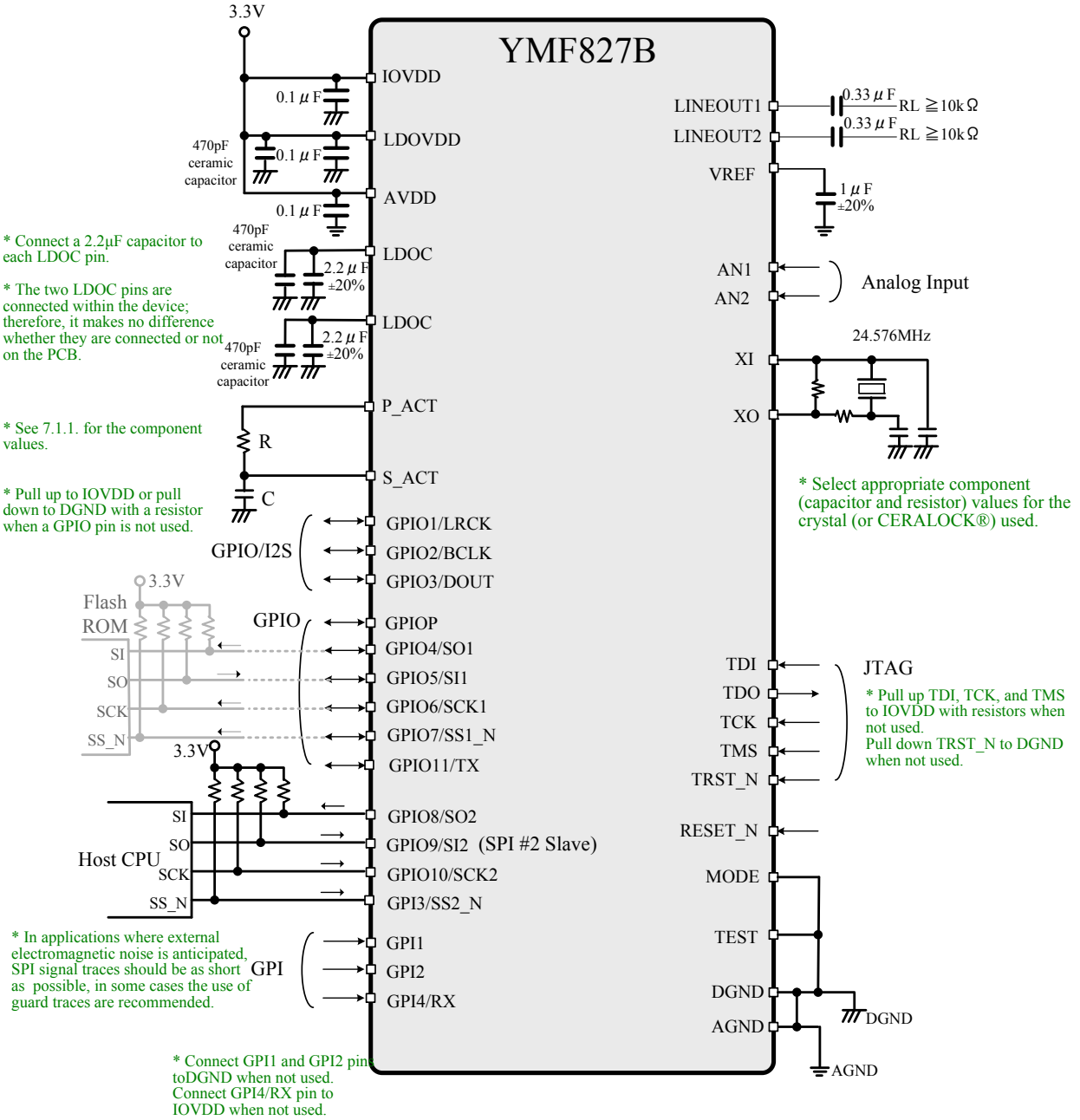
No.	Action	Description
1	Disable the output of circuitry using LINEOUT signals.	
2	Follow the steps 3 through 7 in section *6.1.1.1. Power Up*	

6.1.1.4. Power Down

No.	Action	Description
1	Follow the steps 1, and 2 in section *6.1.1.2. Entering Sleep State With RESET_N.*.	
2	Shutdown the power supplies.	

7. Typical Application Circuits

7.1. Application Circuit Examples

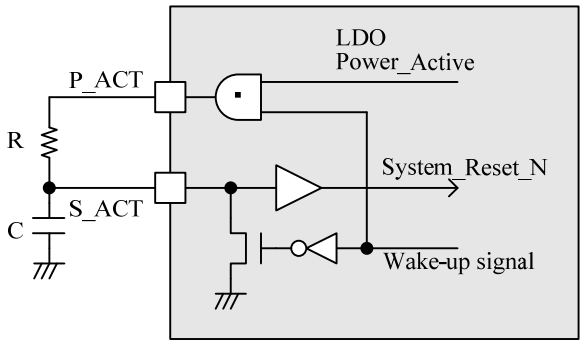


7.1.1. Resistor and Capacitor in P_ACT and S_ACT Network

The digital core block must be held in its reset state with its power supplied until the crystal (or CERALOCK®) connected to XI and XO pins starts generating stable clocks.

Adjust the time constant of the RC network to provide enough time in the reset state.

Select the resistor R and capacitor C as follows:



First, obtain the information about the upper bound of the oscillation stabilization time *t* of the crystal from its vendor.

Put the upper bound figure *t* in the following equation to get the C × R value.

Select some capacitor value and determine the corresponding resistor value from the C × R value.

(Determining the capacitor value for some resistor value also works fine.)

Choose components of such values as they always give a time constant larger than the C × R value when their tolerances are taken into account.

$$C \times R = t \div \ln \{2 \times IOVDD \div (IOVDD - V_{SH})\}$$

IOVDD : IOVDD voltage

V_{SH} : Minimum Schmitt hysteresis voltage IOVDD × 0.1 V

t : Maximum oscillation stabilization time of the crystal (CERALOCK®)
(Ask the resonator vendor.)

<Example> V_{IOVDD} = 3.3 V, t = 100 µs (max.)

$$C \times R = 100[\mu s] \div \ln\{2 \times 3.3\ [V] \div (3.3[V] - 0.33[V])\}$$
$$\approx 125[\mu s]$$

Determine the component values of C and R that give this time constant.

(Choose C and R values whose products come out a little bit larger than the value above.)

If the chosen capacitor value is 0.01 µF, the corresponding resistor can be determined as follows:

If the capacitor's tolerance is ±20 %, C (min.) = 0.01 µF × 0.8 = 0.008 µF.

Then the value R is 15.7 kΩ from the time constant. Assuming the E12 series resistors are used, the next value larger than this is 18 kΩ.

Also the minimum resistance including tolerances must be larger than 15.7 kΩ.

If the resistor's tolerance is ±5 %, R (min.) = 18 kΩ × 0.95 = 17.1 kΩ. This value is larger than 15.7 kΩ; therefore, the 18 kΩ resistor is appropriate in this case.

0.01 µF capacitor and 18 kΩ resistor combination can be used in this example.

7.2. Application Notes

7.2.1. PCB Design Notes

7.2.1.1. Crystals

The performance of the internal oscillator circuit depends on the connected crystal resonator characteristics (oscillation frequency), external components (resistors, capacitors), and the design of the signal traces. When choosing a particular crystal for this device, seek information from the vendor and have them evaluate the crystal and YMF827B combination.

7.2.1.2. Bypass Capacitors

Traces for the bypass capacitors for LDOVDD, IOVDD, AVDD, and LDOC pins must be designed as close to this device as possible.

7.2.1.3. Long Wires on GPIO

When a GPIO port has long wiring and is prone to noise, shield the wiring or place a noise filter network where the wiring goes into this device.

7.2.1.4. High Voltage Traces (Beyond YMF827B Ratings)

When the system uses voltages higher than the YMF827B absolute maximum ratings on the same printed circuit board, YMF827B can be damaged by short circuits with stray solder balls or metal fragments.
PCB traces are to be designed to avoid such damages.

7.2.1.5. Analog Traces Notes

Traces for capacitance on VREF pin must be designed as close to the pin as possible.

7.2.2. Multi-Power Supply Design Notes

When designing Power Traces and Ground Traces for multi-power supply system, study and follow the notes in this section. The separate analog and digital supplies are used as an example of multiple power supply design, in the following description.

Power Traces

Read the notes in *(1) Connection and Traces With Two Power Supplies* when there are two separate power supplies to the analog circuit and the digital circuit (the analog circuitry using this device's output may share the analog supply).

Read the notes in *(2) Connection and Traces With One Power Supply and One Voltage Regulator* when there is one power supply.

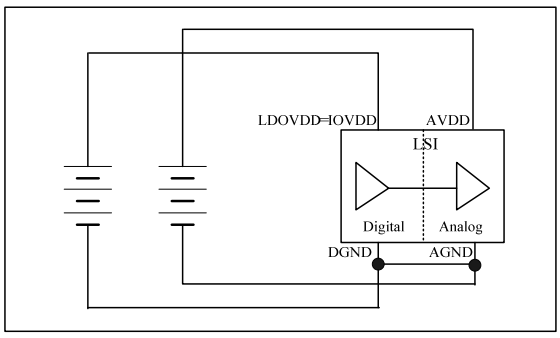
The former system choice, *(1) Connection and Traces With Two Power Supplies*, allow better analog performances although designing the voltage supply sequencing of appropriate timings during power up and down becomes necessary.

Ground Traces

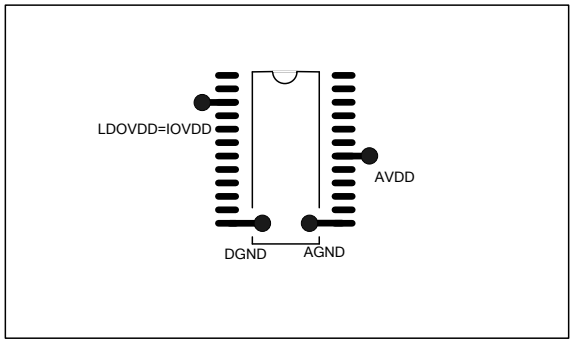
The design consideration to be taken care of for Ground Traces is the same for both system choices, *(1) Connection and Traces With Two Power Supplies*, *(2) Connection and Traces With One Power Supply and One Voltage Regulator*.

In particular, for both choices, the analog and digital Ground Traces must be connected on PCB.

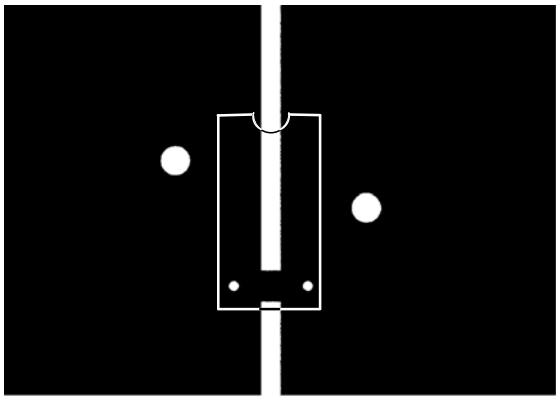
7.2.2.1. (1) Connection and Traces With Two Power Supplies



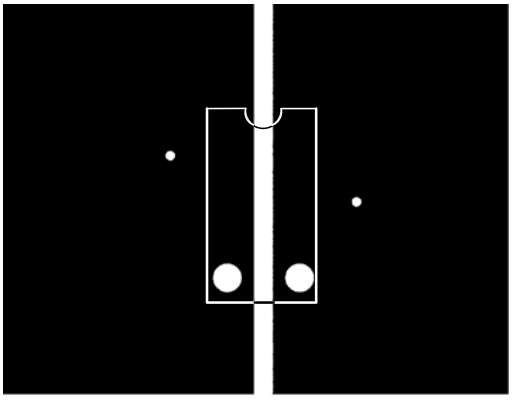
Circuit Diagram



Component Side Traces



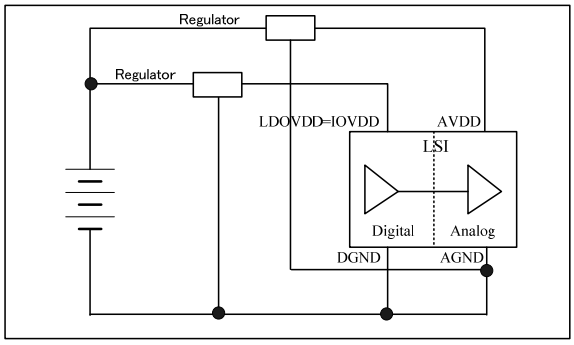
GND Layer Trace



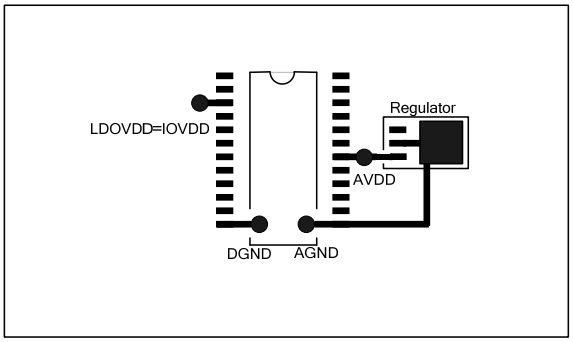
Power Layer Trace

・DGND and AGND traces must be connected in the vicinity of this device. A large inductance between these two grounds makes the system unreliable or results in failures.

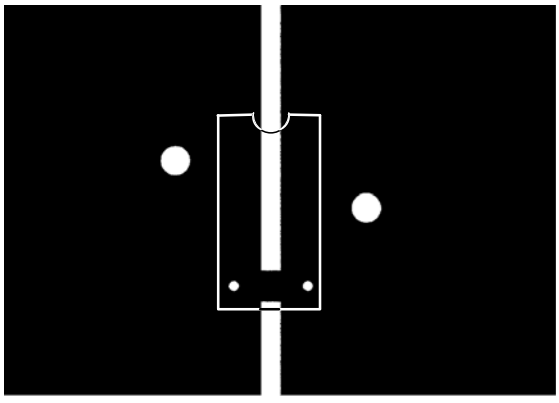
7.2.2.2. (2) Connection and Traces With One Power Supply and One Voltage Regulator



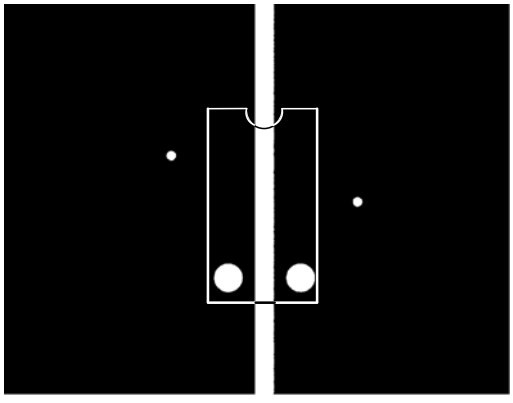
Circuit Diagram



Component Side Traces



GND Layer Trace



Power Layer Trace

・DGND and AGND traces must be connected in the vicinity of this device. A large inductance between these two grounds make the system unreliable or results in failures.

・Design traces to connect the ground pin of the voltage regulator to the analog ground near the AGND pin of this device. This will prevent transient analog current from affecting digital block operations.

・Use AGND as a reference voltage in the analog circuitry on the board that uses this device's outputs

8. Electrical Characteristics

8.1. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
LDOVDD supply voltage	LDOVDD	−0.3	5.2	V
IOVDD supply voltage	IOVDD	−0.3	5.2	V
AVDD supply voltage	AVDD	−0.3	5.2	V
Analog input voltage	V_{INA}	−0.3	AVDD + 0.3	V
Digital input voltage (XI pin)	$V_{IND}1$	−0.3	IOVDD + 0.3	V
Digital input voltage (pins other than XI pin)	$V_{IND}2$	−0.3	5.2	V
Power dissipation (Note 1)	P_D		2386	mW
Storage Temperature	T_{STG}	−50	125	℃

Conditions: DGND = AGND = 0 V

Note 1: Representative value from simulations assuming the following conditions:

Top= 25°C, PCB (136mm×85mm×1.6mm) of glass and epoxy construction, 4-layer board, trace density 379 %

Derate the value with 23.86 mW/°C for the temperature above Top=25 °C.

8.2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
LDOVDD supply voltage	LDOVDD	3.0	3.3	3.6	V
IOVDD supply voltage	IOVDD	3.0	3.3	3.6	V
AVDD supply voltage	AVDD	3.0	3.3	3.6	V
Operating ambient temperature	T_{OP}	−40	25	105	℃

Conditions: DGND = AGND = 0 V

8.3. Power Consumption

Parameter	Conditions	Typ. (Note 1.)	Max. (Note 2.)	Unit
Current drawn from LDOVDD＋IOVDD for normal operation	No signal output	21	25	mA
	Single 1 kHz tone (Note 3)	28	35	mA
	Four 1 kHz tones (Note 3)	29	36	mA
Current drawn from AVDD for normal operation	No signal output	4.4	8	mA
Sleep state	Total current drawn (Note 4)	0.2	5.0	µA

Note 1: LDOVDD=IOVDD=AVDD=3.30 V, Top=25°C, Input pin levels V_{IL}=DGND, V_{IH}=IOVDD

Note 2: LDOVDD=IOVDD=AVDD=3.60 V, Top=−40°C to 105°C, Input pin levels V_{IL}=DGND, V_{IH}=IOVDD

Note 3: DSP processing only 3-band parametric EQ and Harmonics Enhancer.

Note 4: With a crystal or CERALOCK® connected to XI and XO pins

8.4. DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Voltage “H” level (Note 1)	V_{IH}		0.70 × IOVDD		IOVDD + 0.3	V
Input Voltage “L” level (Note 1)	V_{IL}				0.30 × IOVDD	V
Output Voltage “H” level (Note 2)	V_{OH}	I_{OH} = 6 mA	0.80 × IOVDD			V
Output Voltage “L” level (Note 3)	V_{OL}	I_{OL} = 6 mA			0.20 × IOVDD	V
Schmitt hysteresis width (Note 4)	V_{sh}			0.1 × IOVDD		V
Input leakage current	IL		−1		1	µA
Input capacitance	CI				10	pF

Conditions: Top = −40 °C to 105 °C, IOVDD = LDOVDD = 3.0 V to 3.6 V, Capacitive load = 30pF

Note 1: All input and I/O pins supplied from IOVDD

Note 2: All output I/O pins (except S_ACT and XO) supplied from IOVDD

Note 3: All output and I/O pins (except XO) supplied from IOVDD

Note 4: All input and I/O pins (except XI) supplied from IOVDD

8.5. AC Characteristics

8.5.1. Power Supply and Reset Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
RESET_N "L" pulse width (Note 1)	T_{RSTW}	3 (Note 2)			µs
RESET_N (undefined → L) Setup time (Note 1)	T_{RSTS}	0			µs
Supply voltage rise time (Note 3)	T_{VRISE}			10	ms

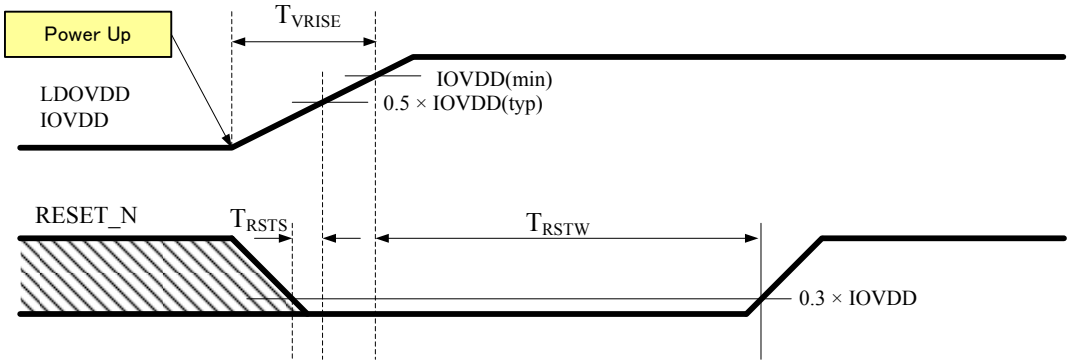
Conditions: the recommended operating conditions

LDOVDD and IOVDD pins must be connected on the printed circuit board and powered from the same power supply.

Note 1: This specifies the pulse width requirement between the time the supply voltage (LDOVDD = IOVDD) reaches at the minimum supply voltage value and the time RESET_N reaches at 0.3× IOVDD.

Note 2: This specifies the minimum value when a 0.022µF capacitor is connected to S_ACT pin.
Use the following equation to find the minimum value for other capacitance values (C).
t [µs] = 136 × C [µF]

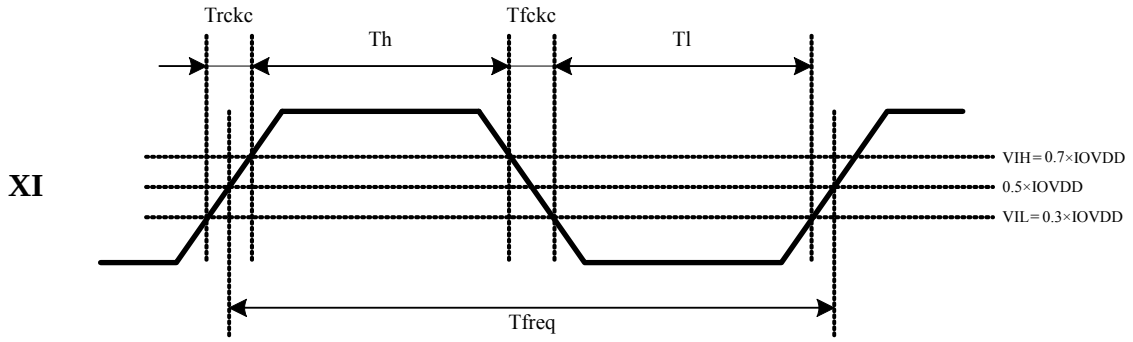
Note 3: This specifies the supply voltage rise time requirement (from the Power Up until the minimum supply voltage of the recommended operating conditions is reached).



8.5.2. Clock Input (XI)

Parameter	Symbol	Min.	Typ.	Max.	Unit
XI Frequency	1 / Tfreq		24.576		MHz
XI Rise time, Fall time	Trckc, Tfckc			10	ns
XI High time	Th	15			ns
XI Low time	Tl	15			ns
Frequency tolerance	–	−5000		+5000	ppm

Conditions: the recommended operating conditions



8.5.3. SPI#1 (Master)

Parameter		Symbol	Min.	Typ.	Max.	Unit
SCK1 Period		T_{SCK}_period		250		ns
SCK1 "L" pulse width		T_{SCK}_low	45			ns
SCK1 "H" pulse width		T_{SCK}_high	45			ns
SS1_N "H" pulse width		T_{SSN}_high	T_{SCK}_period / 2 − 5			ns
SS1_N → SCK1 output delay		T_{SSN}_delay1			T_{SCK}_period + 5	ns
From the last SCK1 edge to SS1_N rise	SCKDV1 ≤ "2" (Note 1)	T_{SSN}_delay2			T_{SCK}_period × 1.5 + 5	ns
	SCKDV1 > "2" (Note 1)				T_{SCK}_period + 5	ns
SI1 Setup time		T_{SI}_setup	45			ns
SI1 Hold time		T_{SI}_hold	5			ns
SO1 output delay	SS1_N → SO1 MSB	T_{SO}_delay1			T_{SCK}_period + 10	ns
	SCK1 → SO1 (other than MSB)	T_{SO}_delay2			10	ns
	SS1_N rise →SO1 drive stop	T_{SO}_delay3			30	ns

Conditions: The recommended operating conditions, capacitive loads = 30 pF

I_{OH} / I_{OL}= 0 mA (SS1_N, SCK1, SO1)

Applied voltage levels: V_{IH} = IOVDD, V_{IL} = 0 V

Reference point voltage levels: V_{IH} = 0.70 × IOVDD, V_{IL} = 0.30 × IOVDD,

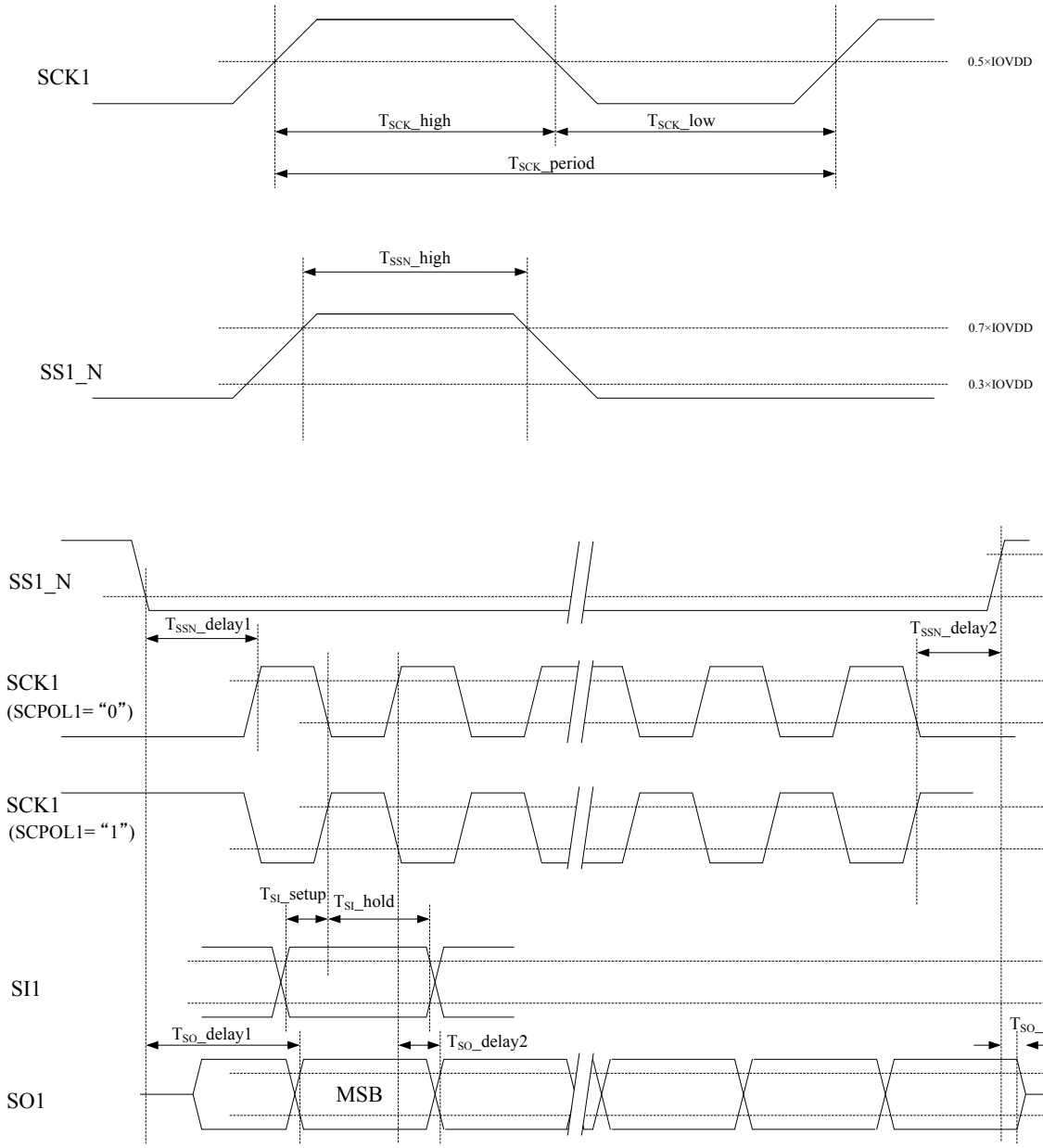
V_{OH}= 0.70 × IOVDD, V_{OL}= 0.30 × IOVDD

Note 1: The divide ratio of SSI clock output on SCK1 pin.

1/ T_{SCK}_period = 36.864 MHz ÷ (2 × SCKDV1): when SCKDV1 ≠ "0"

When SCKDV1 is "0", SSI clock will not be generated.

See *the firmware document* for further information.


SCK1
0.5×IOVDD
TSCK_high
TSCK_low
TSCK_period
TSSN_high
SS1_N
0.7×IOVDD
0.3×IOVDD
SS1_N
TSSN_delay1
TSSN_delay2
SCK1
(SCPOL1= "0")
SCK1
(SCPOL1= "1")
TSI_setup
TSI_hold
SI1
TSO_delay1
TSO_delay2
TSO_delay3
SO1
MSB

8.5.4. SPI#2 (Slave)

Parameter		Symbol	Min.	Typ.	Max.	Unit
SCK2 Period		T_{SCK}_period	(Note 1)			ns
SCK2 “L” pulse width (Note 2)		T_{SCK}_low	(Note 1)			ns
SCK2 “H” pulse width (Note 2)		T_{SCK}_high	95			ns
SCK2 Rise time		T_{SCK}_rise			5	ns
SCK2 Fall time		T_{SCK}_fall			5	ns
SS2_N “H” pulse width		T_{SSN}_high	70			ns
SS2_N Rise time		T_{SSN}_rise			5	ns
SS2_N Setup time		T_{SSN}_setup	35			ns
SS2_N Hold time		T_{SSN}_hold	35			ns
SI2 Setup time		T_{SI}_setup	30			ns
SI2 Hold time		T_{SI}_hold	30			ns
SO2 output delay	SS2_N rise → SO2 “Drive”	T_{SO}_delay1			150	ns
	SCK2 → SO2	T_{SO}_delay2			150	ns
	SS2_N rise → SO2 drive stop	T_{SO}_delay3			160	ns

Conditions: The recommended operating conditions, capacitive loads = 30 pF

I_{OH} / I_{OL} = 0 mA (SO2)

Applied voltage levels: V_{IH} = IOVDD, V_{IL} = 0 V

Reference point voltage levels: V_{IH} = 0.70 × IOVDD, V_{IL} = 0.30 × IOVDD,

V_{OH}= 0.70 × IOVDD, V_{OL}= 0.30 × IOVDD

Note 1: T_{SCK}_low = T_{SO}_delay2 (max.) + T_{HOST}_setup (max.)

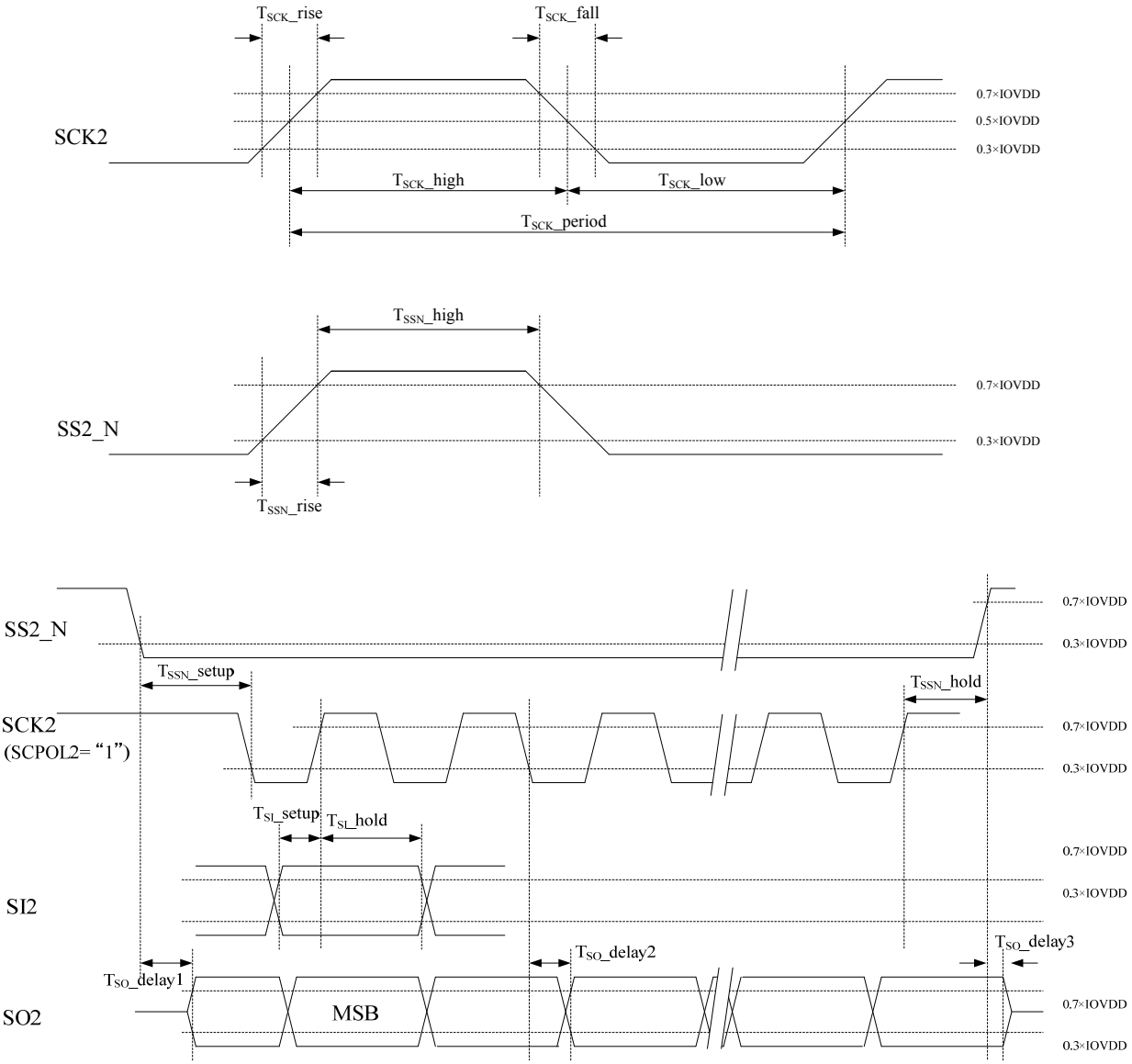
T_{SCK}_period (min.) = T_{SCK}_low + T_{SCK}_high + T_{SCK}_fall

where T_{HOST}_setup is the setup time of SO2 to the rising edge of SCK2 on the receiving device. Check the AC timing specification of the receiver if it allows this timing.

If the duty ratio of SCK2 must be 50 %, use the following expression instead to find this period.

T_{SCK}_period (min.) = T_{SCK}_low × 2

Note 2: Tsck_low + Tsck_high must be more than the minimum value of Tsck_period.


TSCK_rise
TSCK_fall
SCK2
0.7×IOVDD
0.5×IOVDD
0.3×IOVDD
TSCK_high
TSCK_low
TSCK_period
TSSN_high
SS2_N
0.7×IOVDD
0.3×IOVDD
TSSN_rise
SS2_N
TSSN_setup
TSSN_hold
SCK2
(SCPOL2= "1")
TSI_setup
TSI_hold
SI2
TSO_delay1
TSO_delay2
TSO_delay3
SO2
MSB

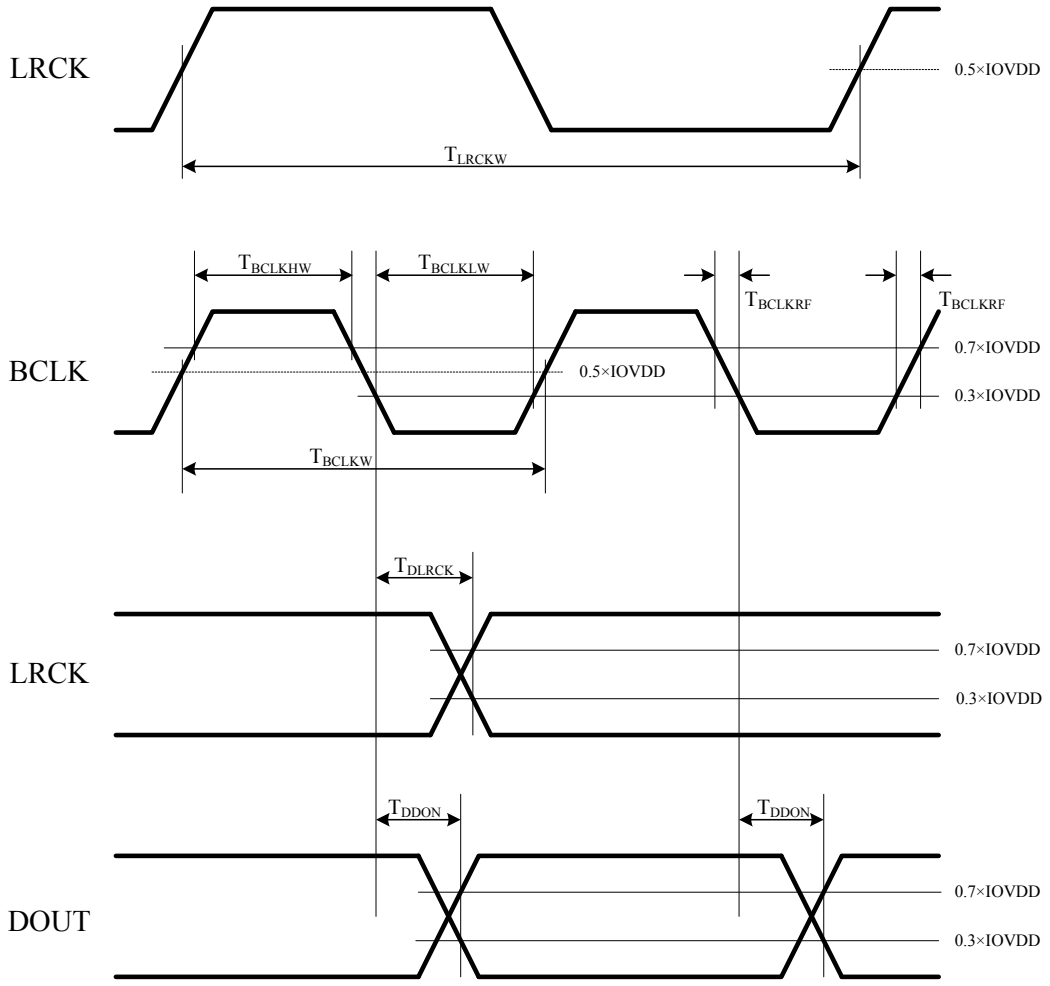
8.5.5. Digital Audio Output

Parameter	Symbol	Min.	Typ.	Max.	Unit
BCLK frequency	$1/T_{BCLKW}$		(Note 1)		ns
BCLK "H" time	T_{BCLKHW}	120			ns
BCLK "L" time	T_{BCLKLW}	120			ns
BCLK Output rising/falling time	T_{BCLKRF}			20	ns
LRCK frequency	$1/T_{LRCKW}$		(Note 2)		ns
DOUT output delay time	T_{DDON}	−20		20	ns
LRCK output delay time	T_{DLRCK}	−20		20	ns

Conditions: The recommended operating conditions, capacitive loads = 30 pF

Note 1: Any of 32 ×, 48 ×, or 64 × fs (sampling frequency)

Note 2: The same as the fs (sampling frequency)



8.6. Analog Characteristics

Conditions: T_{OP} = 25°C, AVDD = LDOVDD = IOVDD = 3.3 V

8.6.1. VREF

Parameter	Min.	Typ.	Max.	Unit
VREF voltage		1.5		V

8.6.2. DAC

Parameter	Min.	Typ.	Max.	Unit
Resolution		16		bit
Full-scale output voltage (Note 1)	1.9	2.0	2.1	Vp-p
THD+N (at 1 kHz)		0.04		%
Residual noise (A-weighted)		−100		dBV
PSRR		78		dB
Pass-band width		0.45 × fs*		kHz
Output resistance		300	600	Ω
Minimum load resistance		10		kΩ
Crosstalk (LINEOUT1-LINEOUT2)		−113		dB

fs* : The sampling frequency (which is supplied from the integrated MPU to the audio block) for wave data.

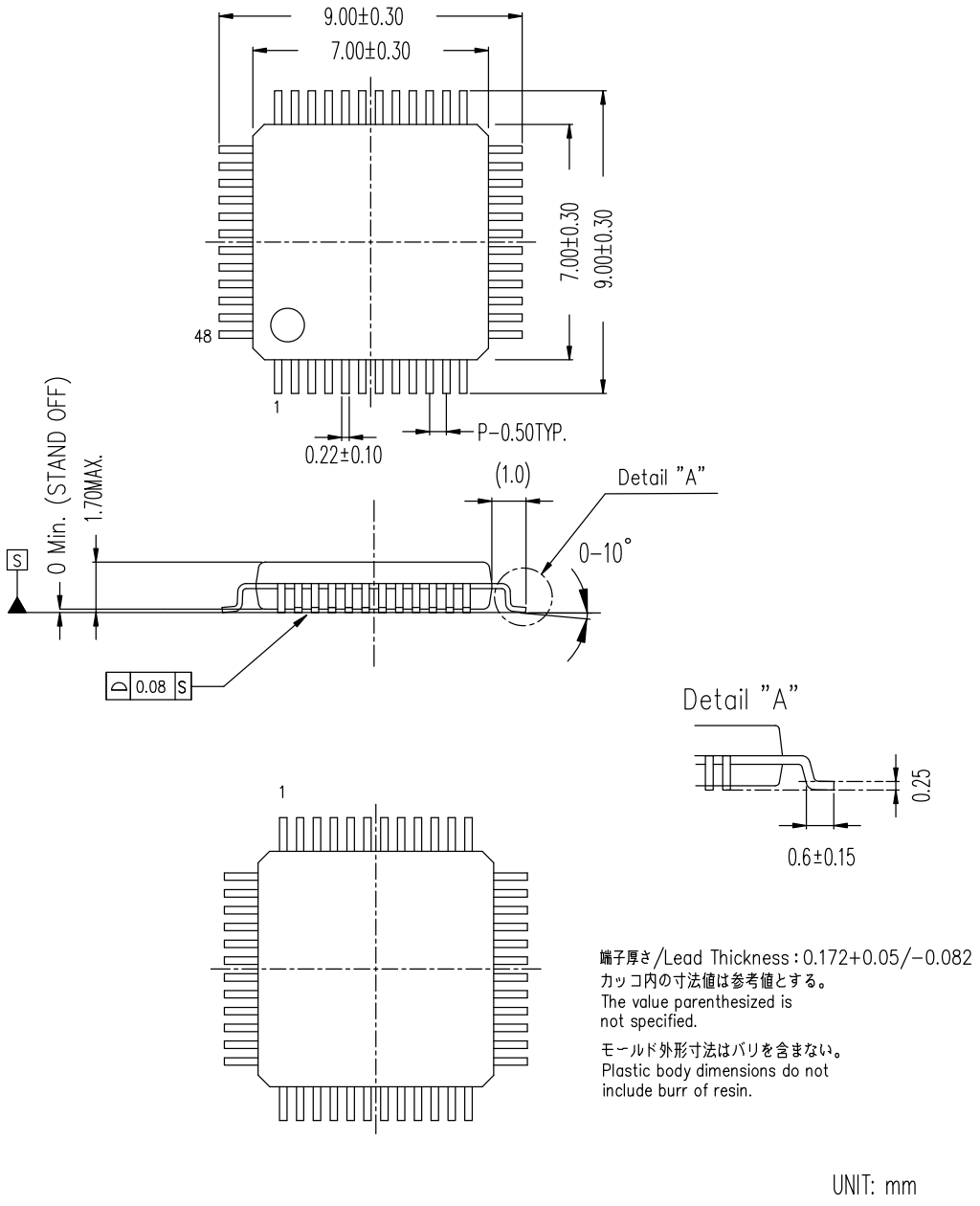
Note 1: These maximum and minimum values assume that the device is operating within the maximum and minimum (supply voltages, operating ambient temperature) values specified in the recommended operating conditions.

8.6.3. ADC

Parameter	Min.	Typ.	Max.	Unit
Resolution		10		bit
Conversion time		16		µs
Analog input voltage range	0		AVDD	V
INL			±2	LSB
DNL			±1	LSB
Offset error			±2	LSB
Gain error			±2	LSB
Input capacitance		12.8		pF

9. Package Information

U-PK48SP1-18-1



UNIT: mm

注） 1. 表面実装LSIは、保管条件、および、半田付けについての特別な配慮が必要です。
2. 組立工場により、寸法や形状などが異なる場合があります。
詳しくはヤマハ代理店までお問い合わせください。

Note: 1. Special attention needs to be paid to the storage conditions and soldering method of the surface mount IC.
2. Dimension, form, etc. may differ depending on assembly plants.
For details, please contact your local Yamaha agent.

Notice The specifications of this product are subject to improvement changes without prior notice.

AGENT

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