

YP6188 1A Iout DC-DC Step-up Converter

General Description

The YP6188 is a high efficiency boost DC-DC converter which combines a current mode, fixed frequency (1.22MHz or 640KHz programmable with FSEL pin) PWM architecture for TFT LCD displays and other portable applications.

YP6188 operates over a wide range of input supply voltage ($2.5V < V_{IN} < 5.5V$) and provides a regulated boost voltage (from V_{IN} up to as high as 15V). The YP6188 also features a skip cycle mode operation for power saving at light loads.

The built-in soft-start circuitry (externally programmable through the CSS pin) provides the freedom for the control of input current ramp rate. Overall current consumption during the power down mode (by pull MPD~pin to logic low) is typically less than 0.1uA. Under-voltage lockout (UVLO), Thermal Shutdown (TSD), Over Current detection/protection (OVL) and other protection features are also incorporated onto the YP6188 to ensure the reliable operation under different operating circumstances.

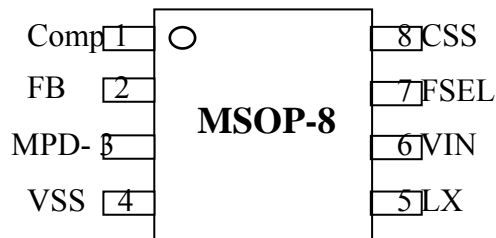
Features

- 90% efficiency
- Built-in 2.4A, 0.18Ω, 20V power NMOS switch
- 640KHz/1.22MHz FSEL pin selectable fixed frequency PWM operation
- Built-in slope compensation circuitry to ensure system stability
- Adjustable output voltage from V_{IN} up to as high as 15V
- Programmable Soft-Start for optimizing control of input current ramp rate.
- Built-in Skip Cycle mode to maintain high power efficiency at light loads.
- Built-in Thermal Shutdown (TSD) and Over-current detection/protection (OVI)
- Built-in maximum duty cycle detection/protection.
- Small 8-pin MSOP Package

Applications

- TFT LCD displays
- Portable Applications
- Handheld Devices

Pin Assignment:



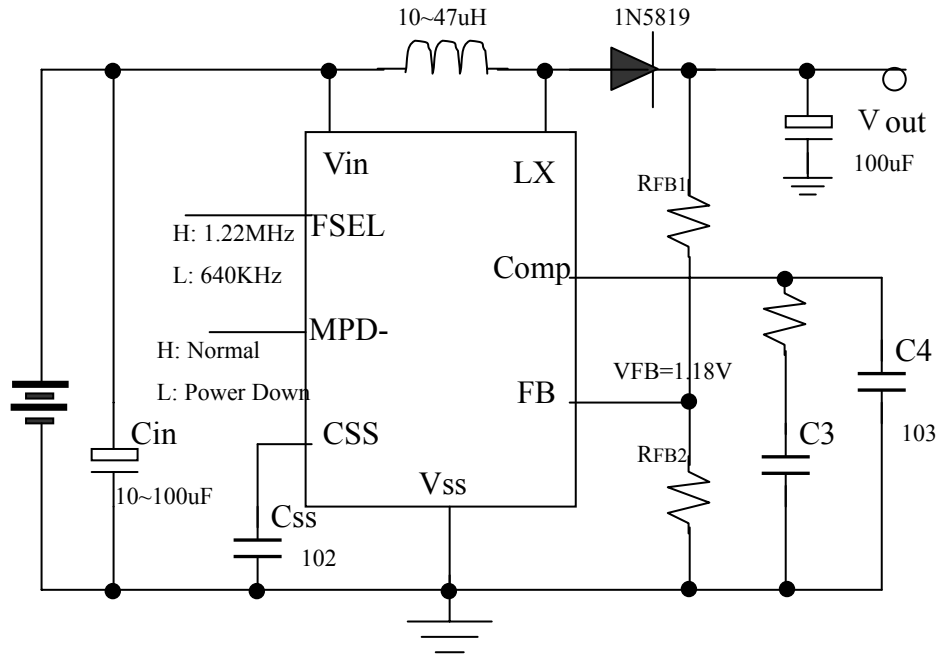
Pin Description

PinNumber	PinName	Pin description
1	COMP	Compensation pin for Error Amplifier Connect RC1 and CC1 in series in-between COMP pin and ground (GND) Optional CC2 between COMP and GND pins will introduce the extra pole to cancel the unwanted zero due to the non-ideal ESR of the output capacitor.
2	FB	Output Voltage Feedback Loop pin. Connect an external precision resistor divider (RFB1 and RFB2) tap to FB pin (reference voltage is 1.18V nominal) Will determine the nominal output voltage. i.e, $V_{OUT} = 1.18 * (1 + R_{FB1}/R_{FB2})$.
3	MPD~	Master power down pin (active low). When MPD~pin goes low, the YP6188 will enter the power down mode.
4	GND	Ground pin
5	LX	Boost converter power switch pin. Connect the inductor (L1) and catch (Schottky) diode (D1) to LX pin with minimum trace area.
6	VIN	Supply voltage input pin (2.5V to 5.5V recommended).
7	FSEL	Frequency selection pin When this pin is low, 640KHz PWM frequency is

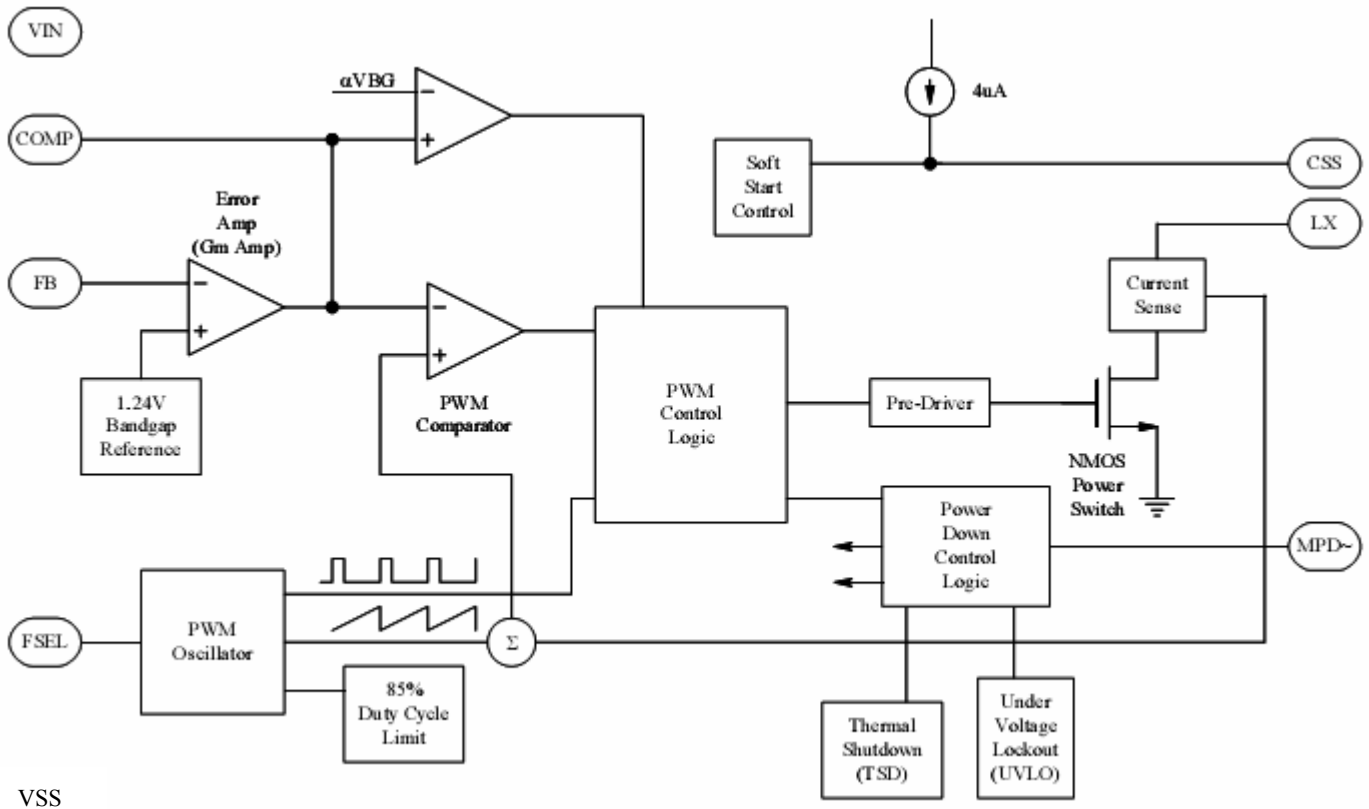
YP6188 1A Iout DC-DC Step-up Converter

		Selected. When this pin is high, the PWM frequency is 1.22MHz. This pin is Default low (640KHz) with internal 5uA pull down device.
8	CSS	Soft-Start current ramp rate control pin. Connect a soft start capacitor (C _{ss}) In-between this pin and ground (GND) to set the proper input current ramp rate.

Typical Application Circuit:



Functional Block Diagram.



Recommended Operating Conditions

VIN Supply Voltage Range	2.5V to 5.5V
--------------------------	--------------

YP6188 1A Iout DC-DC Step-up Converter

Operating Ambient Temperature (T A)	-40°C to 85°C
Output Voltage (VOUT)	VIN to 15V maximum

Absolute Maximum Ratings:

VIN	-0.3V to 5.5V
Lx to GND pin	-0.3V to +20V
MPD~, FSEL, FB to GND pin	-0.3V to (VIN+0.3V)
CSS, COMP to GND pin	-0.3V to(VIN +0.3V)
PMS LX Susceptibility	1.2A
ESD Susceptibility	2KV (Human Body Model) 200V (Machine Model)
Continuous Power Dissipation	Limited by intenal Thermal Shutdown (TSD)
Operating Tem perature Range	-40°C to 85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to 15085°C
Lead Temperature (Soldering, 10s)	+300°C

Electrical Characteristics:

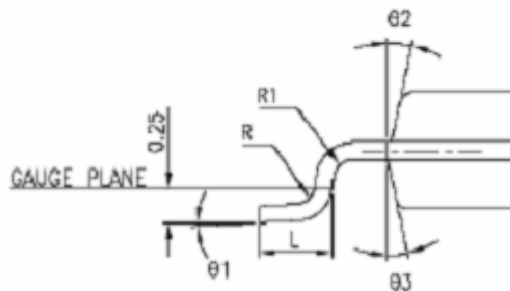
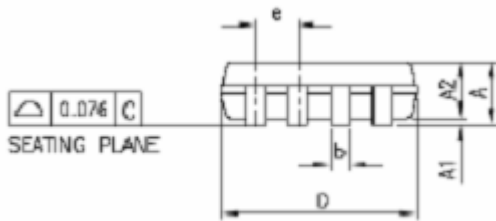
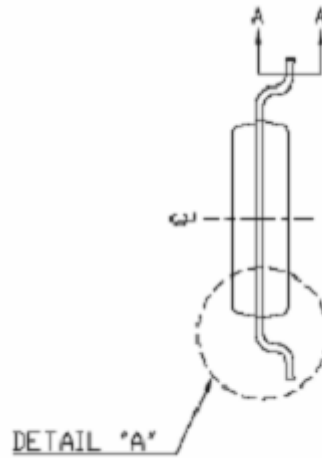
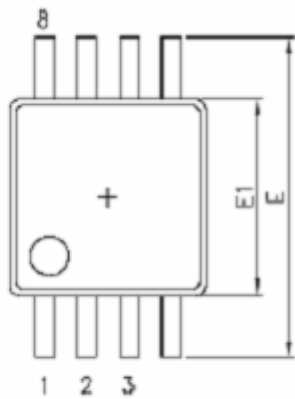
Unless otherwise specified, VIN = MPD~ =3.0V, FSEL = GND, TA= 0°C to 85°C. Typical values are atTA= 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN	Input Supply Voltage		2.5		5.5	V
UVLO_H	Under Voltage Lockout_High	VIN rising edge threshold	2.15	2.28	2.42	V
UVLO_L	Under Voltage Lockout_Low	VIN falling edge threshold	2.11	2.24	2.32	V
IQ1_VIN	Quies eent Current_PWM off	VFB=1.3V (i.e. with PWM switching)		180	350	μA
IQ2_VIN	Quies eent Current_OWM on	VFB=1.0V (i.e. with PWM switching)		2	5	mA
IPD_VIN	Power Down Current	MPD~pin = GND		0.1	10	μA
VFB	Feedback Voltage	VFB Level in order to Priduce VCOMP=1.18V	1.162	1.18	1.198	V
IB_FB	FB pin Bias current	VFB=1.18V		0	40	nA
Gm	Error Amp (E/A) Trans conductance	Δ I=5μA	70	140	240	μmhos
Av	E/A Voltage Gain			700		V/V
Δ VFB/ Δ VIN	Feedback Voltage Line Regulation	Level to produce VCOMP=1.18V (2.5V<VIN<5.5V)		0.05	0.15	%
FOSC_L	Oscillator Frequency_Low	FSEL=GND	540	640	740	KHz
FOSC_H	Oscillator Frequency_High	FSEL=VIN	1.0	1.22	1.5	MHz
D1_Max	Maximum Duty Cycle	FSEL=GND	79	85	92	%
D2_Max	Maximum Duty Cycle	FSEL=VIN		84		%

YP6188 1A Iout DC-DC Step-up Converter

ISW_Max	Switch Current Limit ²	V _{FB} =1V Duty Cycle=65%	1.8	2.4	3.4	A
RDS_On	ON Resistance	ILX=1.2A		0.18	0.35	Ω
ILX_Off	Leakage Current	VLX=12V		0.01	20	μA
RCS	Current Sense Transresistance		0.20	0.30	0.43	Ω
RSS-Reset	Soft Start reset device maximum onresistance				300	Ω
ICH_SS	Soft Start Ramp Up Charge Current	VCSS=1.2V	1.5	4	7	μA
VIL	Digital input low voltage	MPD~ and FSEL 2.5<VIN<5.5V			0.3* VIN	V
VIH	Digital input high voltage	MPD~ and FSEL 2.5<VIN<5.5V	0.7* VIN			V
VHYS	Hysteresis	MPD~ and FSEL		0.1* VIN		V
IFSEL	FSEL pull down current		1.8	5	9	μA
IMPD-	MPD~ input current			0.001	1	μA

Package Information:



DETAIL "A"
SCALE 25:1

YP6188 1A Iout DC-DC Step-up Converter

SYMBOL	DIMENSIGN IN HM			DIMENSON IN INCH		
	MIN	NOM	MAN	MIN	NOM	MAX
A	-		1.10	-		0.043
A1	0.05		0.15	0.002		0.0006
A2	0.81	0.86	0.91	0.032	0.034	0.036
b	0.25		0.40	0.00B		0.012
b1	0.25	0.30	0.35	0.010	0.012	0.014
c	0.13		0.23	0.005		0.009
c1	0.13	0.15	0.18	0.005	0.006	0.007
D	2.90	3.00	3.10	0.114	0.118	0.122
E1	2.90	3.00	3.10	0.114	0.118	0.122
e	0.85 BSC			0.026 BSC		
E	4.90 BSC			0.193 BSC		
L	0.445	0.55	0.648	0.0175	0.0217	0.0255
θ1	0*		B*	0*		B*
θ2	12 REF			12 REF		
θ3	12 REF			12 REF		
R	0.09			0.004		
R1	0.09			0.004		
JEDEC	MO-187AA					