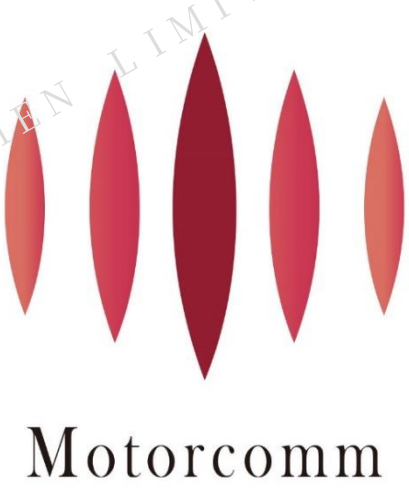



# YT9214NBH Datasheet

## LAYER 2 MANAGED 2+2 PORT 10/100/1000M SWITCH CONTROLLER

**Issue** V1.11

**Date** 2024-12-12

# General Description

YT9214NBH is a QFN88 E-PAD, high-performance 2+2-port Gigabit Ethernet Switch. It integrates 2 PHY support 1000Base-T/100Base-TX/10Base-Te, and 2 extra MAC ports for specific applications that support MII/RMII/RGMII/SGMII/1000Base-X/100Base-FX/2500Base-X. YT9214NBH is also embedded with a RISC-V microprocessor.

The integrated GIGA-PHY complies with 10BASE-Te, 100BASE-TX, and 1000BASE-T IEEE standard 802.3 and also supports Motorcomm's proprietary LRE100-4 feature, which makes the device can auto-negotiate and link up with LRE100-4 compliant link partners. LRE100-4 in extended cable length applications up to 400 meters at 100Mbps over CAT5E cable.

The Extension GMAC1 and Extension GMAC2 of the YT9214NBH support xMII or SerDes interfaces for connecting with an external PHY, MAC, external CPU, or RISC in specific applications, and provide an optical port directly by SerDes. The xMII refers to Reduced Gigabit Media Independent Interface (RGMII), Media Independent Interface (MII), and Reduced Media Independent Interface (RMII). The SerDes supports IEEE SGMII, IEEE 1000Base-X, and IEEE 2500Base-X.

YT9214NBH integrates a 4K look-up table with an efficient hashing algorithm for address searching and learning, each entry can be configured as a static entry.

YT9214NBH supports IEEE 802.1Q VLAN and has a 4K-entry VLAN table. It provides VLAN classification according to port-based, protocol-based, VLAN translation, flow-based capability, and MAC-based. IP-subnet-based VLAN can be supported by configuration. It also supports IVL, SVL, and IVL/SVL for flexible network topology architecture.

YT9214NBH supports standard 802.3x flow control frames for full duplex and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources. YT9214NBH supports storm control.

YT9214NBH supports 384-hardware entry ACL rule check and multiple action options, to support flexible traffic classification. The 384 entries are composed of 48 rows, each row has 8 entries. To support long rule, rule extension is supported by any combination of the 8 entries for each row. Each port can optionally enable or disable the ACL rule check function. The ACL rule key can be based on packet physical port, Layer2, Layer3, and Layer4 information. When an ACL rule matches, the action is configurable to Drop/Permit/Redirect/Mirror, change priority/DSCP value in 802.1q/Q tag, and rate policing.

## Key Features

- High performance, nonblocking, 4 port Ethernet Switch integrating:
  - Two 10/100/1000Mbps PHYs with Advanced Cable Status Diagnostic (CSD)
  - Each PHY supports 10/100/1000M full duplex connectivity (half duplex only supported in 10/100M mode)
  - Full duplex and half duplex operation with IEEE 802.3x flow control and backpressure
- Interface
  - Embedded 2-port 1000Base-T/100Base-TX/10Base-Te PHY
  - Embedded one 3.125Gbps/1.25Gbps SerDes for 2500Base-X/SGMII/1000Base-X/100Base-FX
  - Embedded two RGMII/MII/RMII interface

- Advanced Features
  - Support parallel LED outputs
  - Support SMI/IIC Slave interface
  - Support 1 interrupt output to external CPU for notification
  - Support 64K-byte EEPROM space
  - Link on cable length power saving
  - Link down power-saving
  - Support 9K byte jumbo frames
- Support 2 IEEE 802.3ad Link aggregation port groups
- Security Filtering
  - Disable learning for each port
  - Disable learning-table aging for each port
  - Unknown DA filter mask
  - Support Port Isolation
  - Support Broadcast/Multicast/Unknown DA storm control protects the system from attack by hackers
  - Support DOS attack prevention
- Control, Management, and Statistics
  - Support RFC MIB Counters
  - MIB-II (RFC 1213)
  - Ethernet-Like MIB (RFC 3635)
  - Interface Group MIB (RFC 2863)
  - RMON (RFC 2819)
  - Bridge MIB (RFC 1493)
  - Bridge MIB Extension (RFC 2674)
  - Support OAM and EEE LLDP (Energy Efficient Ethernet Link Layer Discovery Protocol)
  - Support Loop Detection
- Packet Process Engine
  - Support 802.1Q VLANs
  - Support 4K VLANs
  - Support untagged definition in each VLAN
  - Support VLAN policing and VLAN forwarding decision
  - Support port-based, tag-based, and protocol-based VLAN
  - Support per port egress VLAN tagged and untagged
  - Support IEEE 802.1D/s/w Spanning Tree Protocols
  - Support Multicast VLAN (MVR)
  - Support IVL, SVL, and IVL/SVL
  - Support IEEE 802.1ad Stacking VLAN

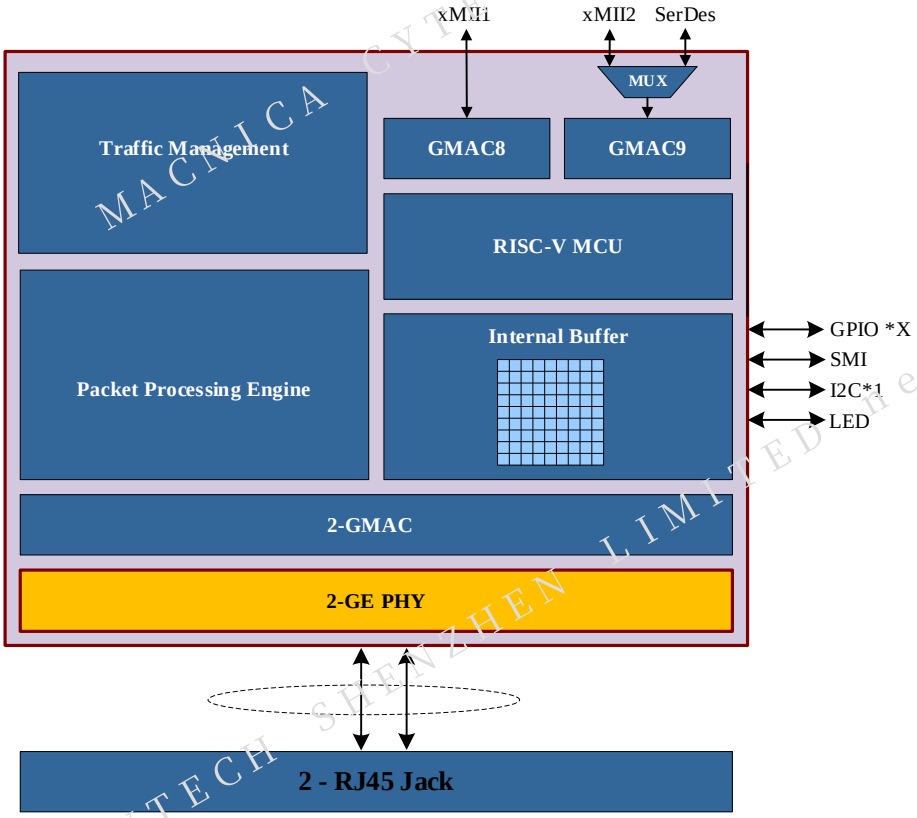
- Support VLAN translation (1:1/2:1/2:2/N:1))
- Support IEEE 802.1x Access Control Protocol
  - Port-Based Access Control
  - MAC-Based Access Control
  - Guest VLAN
- Support ACL Rules
- Support Hardware/Software IGMP/MLD Snooping
  - Support Fast Leave
  - Support IGMP v1/v2/v3
  - Static/Dynamic Router port
- Mirror
  - Port-based mirror
  - Flow-based mirror
- Support reserved multicast control
- Support WOL

- Quality of Service (QoS)
  - Support queue-based DWRR/SP, packet/byte modes are both supported for DWRR
  - Support min-max queue-based shaping, packet/byte modes are both supported
  - Support single token bucket for port-based shaping, packet/byte modes are both supported
  - Support per port input bandwidth control, packet/byte modes are both supported
  - trTCM color aware/blind packet/byte modes
  - Traffic classification based on multiple source type
  - Support 8 unicast queues and 4 multicast queues for each port
  - Tail drop is supported for UQ/MQ, WRED is supported for UQ
- Microprocessor
  - Integrated RISC-V microprocessor
  - Support Flash Interface (Dual mode/Single mode)
- 25MHz crystal or 3.3V OSC input
- QFN 88-pin E-PAD package

# Block Diagram

**Figure 1 Block Diagram**




# System Applications

- 2-Port 1000Base-T+1-Port RGMII+1-Port 2500Base-X Switch
- 2-Port 1000Base-T+2-Port RGMII
- 2-Port 1000Base-T Router with Dual MII/RGMII
- 2-Port 1000Base-T Router with Single SGMII
- 2-Port 1000Base-T NVR
- 2-Port 1000Base-T ONU

# Revision History

| Revision | Release Date | Description |
|---|---|---|
| V1.11 | 2024-12-12 | Update TskewR value, Data Input Hold Time min value, and AC Coupling Capacitor max value, See 7.4 AC Characteristics. |
| V1.1 | 2024-11-26 | • Update electrical characteristics.<br>• Update management interfaces.<br>• Update document style and description. |
| V1.0 | 2024-10-10 | First version. |

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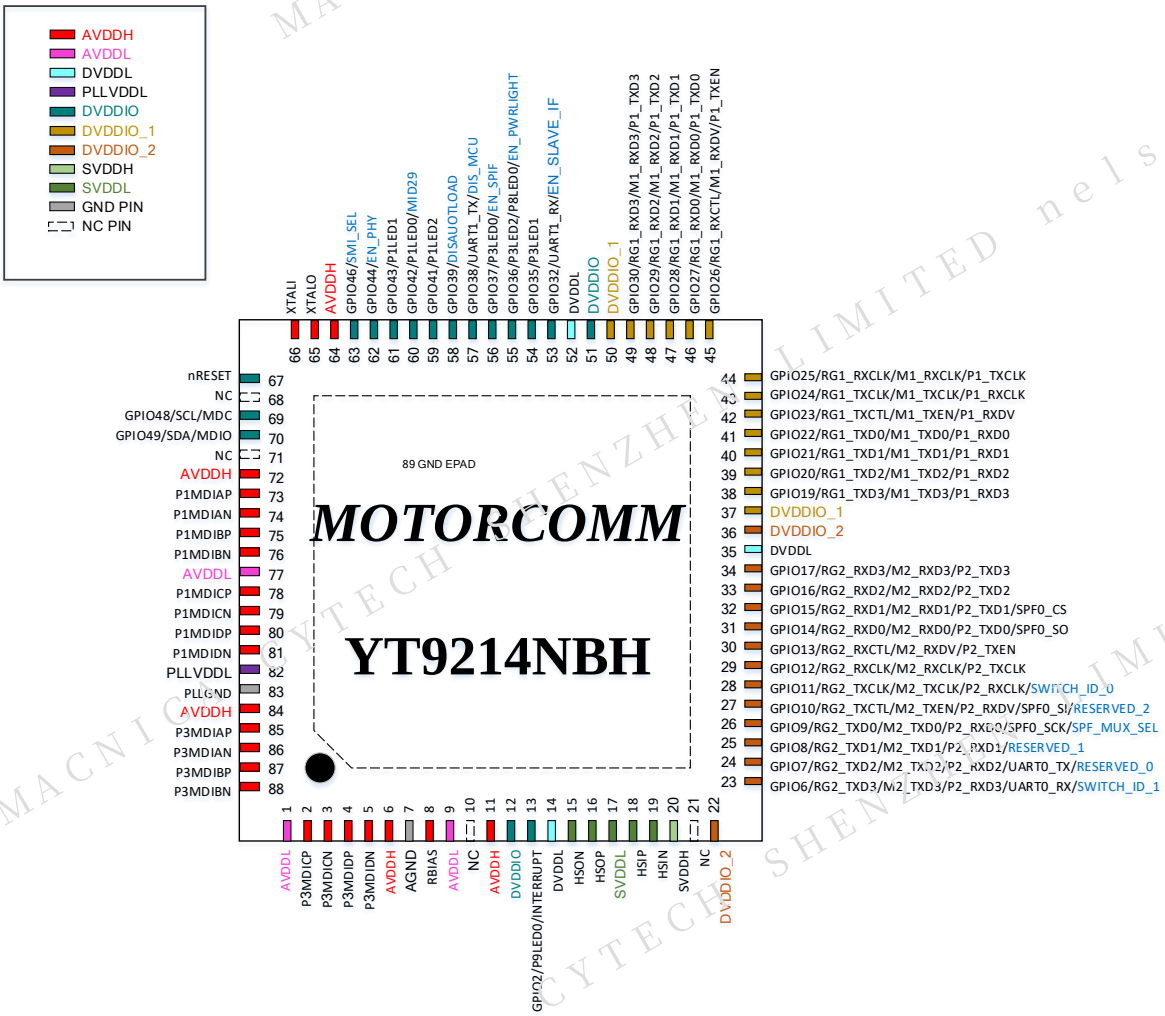
# 1 Pin Assignment

## 1.1 Pin Assignment

The pin map is shown in the following figure.

**Figure 2 Pin Assignment**




## 1.2 Pin Assignment Table

Some pins have multiple functions.

Refer to the Pin Assignment figures for a graphical representation.

- I: Input
- O: Output
- IO: Bidirectional Input and Output
- P: Digital Power Pin
- G: Digital Ground Pin
- PU: Internal Pull Up
- LI: Latched Input During Power Up
- OD: Open Drain

- AI: Analog Input
- AO: Analog Output
- AIO: Analog Bidirectional Input and Output
- AP: Analog Power Pin
- AG: Analog Ground Pin
- PD: Internal Pull Down
- XT: Crystal Related

**Table 1 Pin Assignment**

| No. | Pin Name | Type |
|---|---|---|
| 1 | AVDDL | AP |
| 2 | P3MDICP | AIO |
| 3 | P3MDICN | AIO |
| 4 | P3MDIDP | AIO |
| 5 | P3MDIDN | AIO |
| 6 | AVDDH | AP |
| 7 | AGND | AG |
| 8 | RBIAS | AO |
| 9 | AVDDL | AP |
| 10 | NC | - |
| 11 | AVDDH | AP |
| 12 | DVDDIO | P |
| 13 | GPIO2/P9LED0/INTERRUPT | IO/PU/OD |
| 14 | DVDDL | P |
| 15 | HSON | AO |
| 16 | HSOP | AO |
| 17 | SVDDL | AP |
| 18 | HSIP | AI |
| 19 | HSIN | AI |
| 20 | SVDDH | AP |
| 21 | NC | - |
| 22 | DVDDIO_2 | P |
| 23 | GPIO6/RG2_TXD3/M2_TXD3/P2_RXD3/UART0_RX/SWITCH_ID_1 | IO/LI/PD |
| 24 | GPIO7/RG2_TXD2/M2_TXD2/P2_RXD2/UART0_TX/RESERVED_0 | IO/LI/PU |
| 25 | GPIO8/RG2_TXD1/M2_TXD1/P2_RXD1/RESERVED_1 | IO/LI/PU |
| 26 | GPIO9/RG2_TXD0/M2_TXD0/P2_RXD0/SPF0_SCK/SPF_MUX_SEL | IO/LI/PD |
| 27 | GPIO10/RG2_TXCTL/M2_TXEN/P2_RXDV/SPF0_SI/RESERVED_2 | IO/LI/PD |
| 28 | GPIO11/RG2_TXCLK/M2_TXCLK/P2_RXCLK/SWITCH_ID_0 | IO/LI/PD |
| 29 | GPIO12/RG2_RXCLK/M2_RXCLK/P2_TXCLK | IO/PU |
| 30 | GPIO13/RG2_RXCTL/M2_RXDV/P2_TXEN | IO/PU |
| 31 | GPIO14/RG2_RXD0/M2_RXD0/P2_TXD0/SPF0_SO | IO/PU |
| 32 | GPIO15/RG2_RXD1/M2_RXD1/P2_TXD1/SPF0_CS | IO/PU |
| 33 | GPIO16/RG2_RXD2/M2_RXD2/P2_TXD2 | IO/PU |
| 34 | GPIO17/RG2_RXD3/M2_RXD3/P2_TXD3 | IO/PU |
| 35 | DVDDL | P |
| 36 | DVDDIO_2 | P |
| 37 | DVDDIO_1 | P |
| 38 | GPIO19/RG1_TXD3/M1_TXD3/P1_RXD3 | IO/PU |
| 39 | GPIO20/RG1_TXD2/M1_TXD2/P1_RXD2 | IO/PU |
| 40 | GPIO21/RG1_TXD1/M1_TXD1/P1_RXD1 | IO/PU |
| 41 | GPIO22/RG1_TXD0/M1_TXD0/P1_RXD0 | IO/PU |
| 42 | GPIO23/RG1_TXCTL/M1_TXEN/P1_RXDV | IO/PD |
| 43 | GPIO24/RG1_TXCLK/M1_TXCLK/P1_RXCLK | IO/PU |
| 44 | GPIO25/RG1_RXCLK/M1_RXCLK/P1_TXCLK | IO/PU |
| 45 | GPIO26/RG1_RXCTL/M1_RXDV/P1_TXEN | IO/PU |
| 46 | GPIO27/RG1_RXD0/M1_RXD0/P1_TXD0 | IO/PU |
| 47 | GPIO28/RG1_RXD1/M1_RXD1/P1_TXD1 | IO/LI/PU |
| 48 | GPIO29/RG1_RXD2/M1_RXD2/P1_TXD2 | IO/PU |
| 49 | GPIO30/RG1_RXD3/M1_RXD3/P1_TXD3 | IO/PU |
| 50 | DVDDIO_1 | P |
| 51 | DVDDIO | P |

| No. | Pin Name | Type |
|---|---|---|
| 52 | DVDDL | P |
| 53 | GPIO32/UART1_RX/EN_SLAVE_IF | IO/LI/PU |
| 54 | GPIO35/P3LED1 | IO/PU/OD |
| 55 | GPIO36/P3LED2/P8LED0/EN_PWRLIGHT | IO/LI/PU |
| 56 | GPIO37/P3LED0/EN_SPIF | IO/LI/PU |
| 57 | GPIO38/UART1_TX/DIS_MCU | IO/LI/PU |
| 58 | GPIO39/DISAUOTLOAD | IO/LI/PU |
| 59 | GPIO41/P1LED2 | IO/PU |
| 60 | GPIO42/P1LED0/MID29 | IO/LI/PU |
| 61 | GPIO43/P1LED1 | IO/PU/OD |
| 62 | GPIO44/EN_PHY | IO/LI/PU |
| 63 | GPIO46/SMI_SEL | IO/LI/PU |
| 64 | AVDDH | AP |
| 65 | XTALO | XT |
| 66 | XTALI | XT |
| 67 | nRESET | I/PU |
| 68 | NC | - |
| 69 | GPIO48/SCL/MDC | IO/PU/OD |

| No. | Pin Name | Type |
|---|---|---|
| 70 | GPIO49/SDA/MDIO | IO/PU/OD |
| 71 | NC | - |
| 72 | AVDDH | AP |
| 73 | P1MDIAP | AIO |
| 74 | P1MDIAN | AIO |
| 75 | P1MDIBP | AIO |
| 76 | P1MDIBN | AIO |
| 77 | AVDDL | AP |
| 78 | P1MDICP | AIO |
| 79 | P1MDICN | AIO |
| 80 | P1MDIDP | AIO |
| 81 | P1MDIDN | AIO |
| 82 | PLLVDDL | AP |
| 83 | PLLGND | AG |
| 84 | AVDDH | AP |
| 85 | P3MDIAP | AIO |
| 86 | P3MDIAN | AIO |
| 87 | P3MDIBP | AIO |
| 88 | P3MDIBN | AIO |
| 89 | GND EPAD | G |

# 2 Pin Description

## 2.1 MDI Interface Pins

**Table 2 Transceiver Interface**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 73 | P1MDIAP | AIO | Port 1 Media-dependent interface, differential pairs A, with100Ω termination resistor. |
| 74 | P1MDIAN | AIO | |
| 75 | P1MDIBP | AIO | Port 1 Media-dependent interface, differential pairs B, with 100Ω termination resistor. |
| 76 | P1MDIBN | AIO | |
| 78 | P1MDICP | AIO | Port 1 Media-dependent interface, differential pairs C, with 100Ω termination resistor. |
| 79 | P1MDICN | AIO | |
| 80 | P1MDIDP | AIO | Port 1 Media-dependent interface, differential pairs D, with 100Ω termination resistor. |
| 81 | P1MDIDN | AIO | |
| 85 | P3MDIAP | AIO | Port 3 Media-dependent interface, differential pairs A, with 100Ω termination resistor. |
| 86 | P3MDIAN | AIO | |
| 87 | P3MDIBP | AIO | Port 3 Media-dependent interface, differential pairs B, with 100Ω termination resistor. |
| 88 | P3MDIBN | AIO | |
| 2 | P3MDICP | AIO | Port 3 Media-dependent interface, differential pairs C, with 100Ω termination resistor. |
| 3 | P3MDICN | AIO | |
| 4 | P3MDIDP | AIO | Port 3 Media-dependent interface, differential pairs D, with 100Ω termination resistor. |
| 5 | P3MDIDN | AIO | |

## 2.2 RGMII Interface Pins

**Table 3 RGMII 1 Interface Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 43 | RG1_TXCLK | O/PU | RGMII 1 transmit reference clock will be 125MHz, 25MHz, or 2.5MHz depending on speed.<br>● For Gigabit operation, the clocks will operate at 125MHz.<br>● For 10/100Mbps operation, the clocks will operate at 2.5MHz or 25MHz respectively.<br>TXCLK is an output pin in RGMII mode. |
| 42 | RG1_TXCTL | O/PD | RGMII 1 Transmit Control Signal from the MAC.<br>TXCTL is an output pin in RGMII mode. |
| 38 | RG1_TXD3 | O/PU | RGMII 1 transmit Data.<br>Data is transmitted from MAC to PHY via TXD[3:0].<br>TXD[3:0] are output pins in RGMII mode. |
| 39 | RG1_TXD2 | O/PU | |
| 40 | RG1_TXD1 | O/PU | |
| 41 | RG1_TXD0 | O/PU | |
| 44 | RG1_RXCLK | I/PU | RGMII 1 continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, derived from the received data stream.<br>RXCLK is an input pin in RGMII mode. |

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 45 | RG1_RXCTL | I/PU | RGMII 1 receives the Control Signal to the MAC.<br>RXCTL is an input pin in RGMII mode. |
| 49 | RG1_RXD3 | I/PU | RGMII 1 receives Data.<br>Data is transmitted from PHY to MAC via RXD[3:0].<br>RXD[3:0] are input pins in RGMII mode. |
| 48 | RG1_RXD2 | I/PU | |
| 47 | RG1_RXD1 | I/PU | |
| 46 | RG1_RXD0 | I/PU | |

**Table 4 RGMII 2 Interface Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 28 | RG2_TXCLK | O/LI/PD | RGMII 2 transmit reference clock will be 125MHz, 25MHz, or 2.5MHz depending on speed.<br>● For Gigabit operation, the clocks will operate at 125MHz.<br>● For 10/100Mbps operation, the clocks will operate at 2.5MHz or 25MHz respectively.<br>TXCLK is an output pin in RGMII mode. |
| 27 | RG2_TXCTL | O/PD | RGMII 2 Transmit Control Signal from the MAC.<br>TXCTL is an output pin in RGMII mode. |
| 23 | RG2_TXD3 | O/LI/PD | RGMII 2 transmit Data.<br>Data is transmitted from MAC to PHY via TXD[3:0].<br>TXD[3:0] are output pins in RGMII mode. |
| 24 | RG2_TXD2 | O/PU | |
| 25 | RG2_TXD1 | O/PU | |
| 26 | RG2_TXD0 | O/LI/PD | |
| 29 | RG2_RXCLK | I/PU | RGMII 2 continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, derived from the received data stream.<br>RXCLK is an input pin in RGMII mode. |
| 30 | RG2_RXCTL | I/PU | RGMII 2 receives the Control Signal to the MAC.<br>RXCTL is an input pin in RGMII mode. |
| 34 | RG2_RXD3 | I/PU | RGMII 2 receives Data.<br>Data is transmitted from PHY to MAC via RXD[3:0].<br>RXD[3:0] are input pins in RGMII mode. |
| 33 | RG2_RXD2 | I/PU | |
| 32 | RG2_RXD1 | I/PU | |
| 31 | RG2_RXD0 | I/PU | |

## 2.3 MII Interface Pins

**Table 5 MII 1 Interface Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 43 | M1_TXCLK/<br>P1_RXCLK | IO/PU | ● M_TXCLK Pin in MII MAC Mode.<br>MII Transmit Clock (input). Used to synchronize M_TXD[3:0], and M_TXEN. M_TXCLK is an input pin in MII MAC mode.<br>● P_RXCLK Pin in MII PHY Mode. |

| No. | Pin Name | Type | Description |
|---|---|---|---|
| | | | MII Receive Clock (output). Used to synchronize P_RXD[3:0], and P_RXDV. P_RXCLK is an output pin in MII PHY mode.<br>The frequency depends on the link speed, that is 25MHz at 100Base-TX, and 2.5MHz at 10Base-Te. |
| 42 | M1_TXEN/<br>P1_RXDV | O/PD | ● M_TXEN Pin in MII MAC Mode.<br>MII Transmit Enable. The synchronous output indicates that valid data is being driven on the M_TXD bus. M_TXEN is synchronous to M_TXCLK.<br>● P_RXDV Pin in MII PHY Mode.<br>MII Receive Data Valid. This synchronous output is asserted when valid data is driven on the P_RXD bus. P_RXDV is synchronous to P_RXCLK.<br>M_TXEN/P_RXDV is an output pin in MII MAC mode/MII PHY mode. |
| 38 | M1_TXD3/<br>P1_RXD3 | O/PU | ● M_TXD[3:0] Pin in MII MAC Mode.<br>MII Transmit Data Bus. M_TXD[3:0] is synchronous to M_TXCLK.<br>● P_RXD[3:0] Pin in MII PHY Mode.<br>MII Receive Data Bus. P_RXD[3:0] is synchronous to P_RXCLK.<br>M_TXD[3:0]/P_RXD[3:0] are output pins in MII MAC mode/MII PHY mode. |
| 39 | M1_TXD2/<br>P1_RXD2 | O/PU | |
| 40 | M1_TXD1/<br>P1_RXD1 | O/PU | |
| 41 | M1_TXD0/<br>P1_RXD0 | O/PU | |
| 44 | M1_RXCLK/<br>P1_TXCLK | IO/PU | ● M_RXCLK Pin in MII 1 MAC Mode.<br>MII Receive Clock(input). Used to synchronize M_RXD[3:0], and M_RXDV. M_RXCLK is an input pin in MII MAC mode.<br>● P_TXCLK Pin in MII PHY Mode.<br>MII Transmit Clock (output). Used to synchronize P_TXD[3:0], and P_TXEN. P_TXCLK is an output pin in MII PHY mode.<br>The frequency depends on the link speed, that is 25MHz at 100Base-TX, and 2.5MHz at 10Base-Te. |
| 45 | M1_RXDV/<br>P1_TXEN | I/PU | ● M_RXDV Pin in MII MAC Mode.<br>MII Receive Data Valid. This synchronous input is asserted when valid data is driven on the M_RXD bus. M_RXDV is synchronous to M_RXCLK.<br>● P_TXEN Pin in MII PHY Mode.<br>MII Transmit Enable. The synchronous input indicates that valid data is being driven on the P_TXD bus. P_TXEN is synchronous to P_TXCLK.<br>M_RXDV/P_TXEN is an input pin in MII MAC mode/MII PHY mode. |
| 49 | M1_RXD3/<br>P1_TXD3 | I/PU | ● M_RXD[3:0] Pin in MII MAC Mode. |

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 48 | M1_RXD2/<br>P1_TXD2 | I/PU | MII Receive Data Bus. M_RXD[3:0] is synchronous to M_RXCLK.<br>● P_TXD[3:0] Pin in MII 1 PHY Mode.<br>MII Transmit Data Bus. P_TXD[3:0] is synchronous to P_TXCLK.<br>M_RXD[3:0]/P_TXD[3:0] are input pins in MII MAC mode/MII PHY mode. |
| 47 | M1_RXD1/<br>P1_TXD1 | I/PU | |
| 46 | M1_RXD0/<br>P1_TXD0 | I/PU | |

**Table 6 MII 2 Interface Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 28 | M2_TXCLK/<br>P2_RXCLK | IO/LI/PD | ● M_TXCLK Pin in MII MAC Mode.<br>MII Transmit Clock (input). Used to synchronize M_TXD[3:0], and M_TXEN. M_TXCLK is an input pin in MII MAC mode.<br>● P_RXCLK Pin in MII PHY Mode.<br>MII Receive Clock (output). Used to synchronize P_RXD[3:0], and P_RXDV. P_RXCLK is an output pin in MII PHY mode.<br>The frequency depends on the link speed, that is 25MHz at 100Base-TX, and 2.5MHz at 10Base-Te. |
| 27 | M2_TXEN/<br>P2_RXDV | O/PD | ● M_TXEN Pin in MII MAC Mode.<br>MII Transmit Enable. The synchronous output indicates that valid data is being driven on the M_TXD bus. M_TXEN is synchronous to M_TXCLK.<br>● P_RXDV Pin in MII PHY Mode.<br>MII Receive Data Valid. This synchronous output is asserted when valid data is driven on the P_RXD bus. P_RXDV is synchronous to P_RXCLK.<br>M_TXEN/P_RXDV is an output pin in MII MAC mode/MII PHY mode. |
| 23 | M2_TXD3/<br>P2_RXD3 | O/LI/PD | ● M_TXD[3:0] Pin in MII MAC Mode.<br>MII Transmit Data Bus. M_TXD[3:0] is synchronous to M_TXCLK.<br>● P_RXD[3:0] Pin in MII PHY Mode.<br>MII Receive Data Bus. P_RXD[3:0] is synchronous to P_RXCLK.<br>M_TXD[3:0]/P_RXD[3:0] are output pins in MII MAC mode/MII PHY mode. |
| 24 | M2_TXD2/<br>P2_RXD2 | O/PU | |
| 25 | M2_TXD1/<br>P2_RXD1 | O/PU | |
| 26 | M2_TXD0/<br>P2_RXD0 | O/LI/PD | |
| 29 | M2_RXCLK/<br>P2_TXCLK | IO/PU | ● M_RXCLK Pin in MII MAC Mode.<br>MII Receive Clock(input). Used to synchronize M_RXD[3:0], and M_RXDV. M_RXCLK is an input pin in MII MAC mode.<br>● P_TXCLK Pin in MII PHY Mode. |

| No. | Pin Name | Type | Description |
|---|---|---|---|
| | | | MII Transmit Clock (output). Used to synchronize P_TXD[3:0], and P_TXEN. P_TXCLK is an output pin in MII PHY mode.<br>The frequency depends on the link speed, that is 25MHz at 100Base-TX, and 2.5MHz at 10Base-Te. |
| 30 | M2_RXDV/<br>P2_TXEN | I/PU | ● M_RXDV Pin in MII MAC Mode.<br>MII Receive Data Valid. This synchronous input is asserted when valid data is driven on the M_RXD bus. M_RXDV is synchronous to M_RXCLK.<br>● P_TXEN Pin in MII PHY Mode.<br>MII Transmit Enable. The synchronous input indicates that valid data is being driven on the P_TXD bus. P_TXEN is synchronous to P_TXCLK.<br>M_RXDV/P_TXEN is an input pin in MII MAC mode/MII PHY mode. |
| 34 | M2_RXD3/<br>P2_TXD3 | I/PU | ● M_RXD[3:0] Pin in MII MAC Mode.<br>MII Receive Data Bus. M_RXD[3:0] is synchronous to M_RXCLK.<br>● P_TXD[3:0] Pin in MII PHY Mode.<br>MII Transmit Data Bus. P_TXD[3:0] is synchronous to P_TXCLK.<br>M_RXD[3:0]/P_TXD[3:0] are input pins in MII MAC mode/MII PHY mode. |
| 33 | M2_RXD2/<br>P2_TXD2 | I/PU | |
| 32 | M2_RXD1/<br>P2_TXD1 | I/PU | |
| 31 | M2_RXD0/<br>P2_TXD0 | I/PU | |

## 2.4 RMII Interface Pins

**Table 7 RMII 1 Interface Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 43 | M1_TXCLK/<br>P1_RXCLK | IO/PU | REFCLK pin in RMII Mode.<br>● In RMII MAC Mode, REFCLK is an input pin.<br>● In RMII PHY Mode, REFCLK is an output pin.<br>REF_CLK is a 50MHz clock that provides the timing reference for CRSDV, RXD[1:0], TXEN, and TXD[1:0]. |
| 42 | M1_TXEN/<br>P1_RXDV | O/PD | ● TXEN Pin in RMII MAC Mode.<br>The synchronous output indicates that valid data is being driven on the TXD bus. TXEN is synchronous with REFCLK.<br>● CRSDV Pin in RMII PHY Mode.<br>Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receiving medium is non-idle synchronized with REFCLK. |
| 40 | M1_TXD1/<br>P1_RXD1 | O/PU | |

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 41 | M1_TXD0/<br>P1_RXD0 | O/PU | • TXD[1:0] Pin in RMII MAC Mode, synchronous to REFCLK.<br>• RXD[1:0] Pin in RMII PHY Mode, synchronous to REFCLK. |
| 45 | M1_RXDV/<br>P1_TXEN | I/PU | • CRSDV Pin in RMII MAC Mode<br>Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receiving medium is non-idle synchronized with REFCLK.<br>• TXEN Pin in RMII PHY Mode<br>The synchronous input indicates that valid data is being driven on the TXD bus. TXEN is synchronous with REFCLK. |
| 47 | M1_RXD1/<br>P1_TXD1 | I/PU | • RXD[1:0] Pin in RMII MAC Mode, is synchronous to RXC.<br>• TXD[1:0] Pin in RMII PHY Mode, is synchronous to TXC. |
| 46 | M1_RXD0/<br>P1_TXD0 | I/PU | |

**Table 8 RMII 2 Interface Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 28 | M2_TXCLK /<br>P2_RXCLK | IO/I/PD | • M_TXCLK Pin in MII MAC Mode<br>MII Transmit Clock (input). Used to synchronize M_TXD [3:0], and M_TXEN. M_TXCLK is an input pin in MII MAC mode.<br>• P_RXCLK Pin in MII PHY Mode<br>MII Receive Clock (output). Used to synchronize P_RXD [3:0], and P_RXDV. P_RXCLK is an output pin in MII PHY mode.<br>The frequency depends on the link speed, that is 25MHz at 100Base-TX, and 2.5MHz at 10Base-Te. |
| 27 | M2_TXEN/<br>P2_RXDV | O/PD | • TXEN Pin in RMII MAC Mode<br>The synchronous output indicates that valid data is being driven on the TXD bus. TXEN is synchronous with REFCLK.<br>• CRSDV Pin in RMII PHY Mode<br>Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receiving medium is non-idle synchronized with REFCLK. |
| 25 | M2_TXD1/<br>P2_RXD1 | O/PU | • TXD[1:0] Pin in RMII MAC Mode, synchronous to REFCLK.<br>• RXD[1:0] Pin in RMII PHY Mode, synchronous to REFCLK. |
| 26 | M2_TXD0/<br>P2_RXD0 | O/PD | |

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 30 | M2_RXDV/<br>P2_TXEN | I/PU | • CRSDV Pin in RMII MAC Mode<br>Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receiving medium is non-idle synchronized with REFCLK.<br>• TXEN Pin in RMII PHY Mode.<br>The synchronous input indicates that valid data is being driven on the TXD bus. TXEN is synchronous with REFCLK. |
| 32 | M2_RXD1/<br>P2_TXD1 | I/PU | • RXD[1:0] Pin in RMII MAC Mode, is synchronous to RXC.<br>• TXD[1:0] Pin in RMII PHY Mode, is synchronous to TXC. |
| 31 | M2_RXD0/<br>P2_TXD0 | I/PU | |

## 2.5 High-Speed Serial Interface Pins

**Table 9 High-Speed Serial Interface Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 15 | HSON | AO | High-Speed Serial Interface Pins: support 3.125Gbps or 1.25Gbps. Differential serial output interface. |
| 16 | HSOP | AO | |
| 18 | HSIP | AI | High-Speed Serial Interface Pins: support 3.125Gbps or 1.25Gbps. Differential serial input interface. |
| 19 | HSIN | AI | |

## 2.6 Parallel LED Pins

**Table 10 Parallel LED Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 13 | P9LED0 | IO/PU/OD | This pin can indicate P9LED0 by software configuration which means extra MAC port 1 LED0. |
| 55 | P3LED2/<br>P8LED0 | IO/LI/PU | Default port 3 Parallel LED LED2 Output Signal or indicates P8LED0 by software configuration which means extra MAC port 0 LED0.<br>The LED indicates information is defined by register or EEPROM |
| 54 | P3LED1 | IO/PU/OD | Default port 3 Parallel LED LED1 Output Signal.<br>The LED indicates information is defined by register or EEPROM |
| 56 | P3LED0 | IO/LI/PU | Default port 3 Parallel LED LED0 Output Signal.<br>The LED indicates information is defined by register or EEPROM |
| 59 | P1LED2 | IO/PU | Default port 1 Parallel LED LED2 Output Signal.<br>The LED indicates information is defined by register or EEPROM |
| 61 | P1LED1 | IO/PU/OD | Default port 1 Parallel LED LED1 Output Signal. |

| No. | Pin Name | Type | Description |
|---|---|---|---|
| | | | The LED indicates information is defined by register or EEPROM |
| 60 | P1LED0 | IO/LI/PU | Default port 1 Parallel LED LED0 Output Signal.<br>The LED indicates information is defined by register or EEPROM |

## 2.7 SPI Flash Pins

**Table 11 SPI Flash Interface Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 32 | SPF0_CS | IO/PU | SPI FLASH chip select signal. |
| 31 | SPF0_SO | IO/PU | • In Serial I/O Mode<br>SPI Serial FLASH Serial Data Output (YT9214NBH input pin)<br>• In Dual I/O Mode<br>SPI FLASH bi-directional pin (this is MSB) |
| 27 | SPF0_SI | IO/PD | • In Serial I/O Mode<br>SPI Serial FLASH Serial Data Input (YT9214NBH output pin)<br>• In Dual I/O Mode<br>SPI FLASH bi-directional pin (this is LSB) |
| 26 | SPF0_SCK | IO/PD | SPI FLASH Clock. |

## 2.8 UART Interface Pins

**Table 12 UART 0 Interface Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 23 | UART0_RX | IO/LI/PD | UART RX pin. |
| 24 | UART0_TX | IO/LI/PU | UART TX pin. |

**Table 13 UART 1 Interface Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 53 | UART1_RX | IO/LI/PU | UART RX pin. |
| 57 | UART1_TX | IO/LI/PU | UART TX pin. |

## 2.9 Management Interface Pins

**Table 14 Management Interface Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 69 | SCL/<br>MDC | IO/PU/OD | • EEPROM auto load mode serial clock output<br>• I2C slave mode serial clock input<br>• SMI slave mode serial clock input |
| 70 | SDA/<br>MDIO | IO/PU/OD | • EEPROM auto load mode serial data input<br>• I2C slave mode serial data<br>• SMI slave mode serial data |

## 2.10 GPIO Pins

**Table 15 GPIO Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 13 | GPIO2 | IO/PU/OD | General Purpose Input/Output Interfaces IO2. |
| 23 | GPIO6 | IO/LI/PD | General Purpose Input/Output Interfaces IO6. |
| 24 | GPIO7 | IO/LI/PU | General Purpose Input/Output Interfaces IO7. |
| 25 | GPIO8 | IO/LI/PU | General Purpose Input/Output Interfaces IO8. |
| 26 | GPIO9 | IO/PD | General Purpose Input/Output Interfaces IO9. |
| 27 | GPIO10 | IO/LI/PD | General Purpose Input/Output Interfaces IO10. |
| 28 | GPIO11 | IO/LI/PD | General Purpose Input/Output Interfaces IO11. |
| 29 | GPIO12 | IO/PU | General Purpose Input/Output Interfaces IO12. |
| 30 | GPIO13 | IO/PU | General Purpose Input/Output Interfaces IO13 |
| 31 | GPIO14 | IO/PU | General Purpose Input/Output Interfaces IO14. |
| 32 | GPIO15 | IO/PU | General Purpose Input/Output Interfaces IO15. |
| 33 | GPIO16 | IO/PU | General Purpose Input/Output Interfaces IO16. |
| 34 | GPIO17 | IO/PU | General Purpose Input/Output Interfaces IO17. |
| 38 | GPIO19 | IO/PU | General Purpose Input/Output Interfaces IO19. |
| 39 | GPIO20 | IO/PU | General Purpose Input/Output Interfaces IO20. |
| 40 | GPIO21 | IO/PU | General Purpose Input/Output Interfaces IO21. |
| 41 | GPIO22 | IO/PU | General Purpose Input/Output Interfaces IO22. |
| 42 | GPIO23 | IO/PD | General Purpose Input/Output Interfaces IO23. |
| 43 | GPIO24 | IO/PU | General Purpose Input/Output Interfaces IO24. |
| 44 | GPIO25 | IO/PU | General Purpose Input/Output Interfaces IO25. |
| 45 | GPIO26 | IO/PU | General Purpose Input/Output Interfaces IO26. |
| 46 | GPIO27 | IO/PU | General Purpose Input/Output Interfaces IO27. |
| 47 | GPIO28 | IO/PU | General Purpose Input/Output Interfaces IO28. |
| 48 | GPIO29 | IO/PU | General Purpose Input/Output Interfaces IO29. |
| 49 | GPIO30 | IO/PU | General Purpose Input/Output Interfaces IO30. |
| 53 | GPIO32 | IO/LI/PU | General Purpose Input/Output Interfaces IO32. |
| 54 | GPIO35 | IO/PU/OD | General Purpose Input/Output Interfaces IO35. |

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 55 | GPIO36 | IO/LI/PU | General Purpose Input/Output Interfaces IO36. |
| 56 | GPIO37 | IO/LI/PU | General Purpose Input/Output Interfaces IO37. |
| 57 | GPIO38 | IO/LI/PU | General Purpose Input/Output Interfaces IO38. |
| 58 | GPIO39 | IO/LI/PU | General Purpose Input/Output Interfaces IO39. |
| 59 | GPIO41 | IO/PU | General Purpose Input/Output Interfaces IO41. |
| 60 | GPIO42 | IO/LI/PU | General Purpose Input/Output Interfaces IO42. |
| 61 | GPIO43 | IO/PU/OD | General Purpose Input/Output Interfaces IO43. |
| 62 | GPIO44 | IO/LI/PU | General Purpose Input/Output Interfaces IO44. |
| 63 | GPIO46 | IO/LI/PU | General Purpose Input/Output Interfaces IO46. |
| 69 | GPIO48 | IO/PU/OD | General Purpose Input/Output Interfaces IO48. |
| 70 | GPIO49 | IO/PU/OD | General Purpose Input/Output Interfaces IO49. |

## 2.11 Configuration Pins

**Table 16 Configuration Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 23 | SWITCH_ID_1 | IO/LI/PD | Switch_ID[1:0] for slave SMI and slave I2C format. |
| 28 | SWITCH_ID_0 | IO/LI/PD | |
| 26 | SPF_MUX_EN | IO/PD | SPI Flash Interface Position Select.<br>Pull Up: Select Spi-Flash-0 pin 26\27\31\32. |
| 53 | EN_SLAVE_IF | IO/LI/PU | Enable slave management interface.<br>● Pull Up: Enable slave management interface and refer to [SMI_SEL]<br>● Pull Down: Disable slave management interface |
| 55 | EN_PWRLIGHT | IO/LI/PU | Disable/Enable the LED function When Powered On.<br>● Pull Up: Enable LED<br>● Pull Down: Disable LED. |
| 56 | EN_SPIF | IO/LI/PU | Enable SPI Flash Interface.<br>● Pull Up: Enable Flash interface<br>● Pull Down: Disable Flash interface |
| 57 | DIS_MCU | IO/LI/PU | Disable Embedded MCU.<br>● Pull Up: Disable embedded MCU upon power on or reset<br>● Pull Down: Enable embedded MCU upon power on or reset |
| 58 | DISAUTOLOAD | IO/LI/PU | Disable EEPROM Autoload.<br>● Pull Up: Disable EEPROM autoload upon power on or reset<br>● Pull Down: Enable EEPROM autoload upon power on or reset |
| 60 | MID29 | IO/LI/PU | Slave SMI (MDC/MDIO) Device Address.<br>● Pull Up: Slave SMI (MDC/MDIO) Device Address is 0x1d |

| No. | Pin Name | Type | Description |
|---|---|---|---|
| | | | ● Pull Down: Slave SMI (MDC/MDIO) Device Address is 0x0 |
| 62 | EN_PHY | IO/LI/PU | Enable Embedded PHY.<br>● Pull Up: Enable embedded PHY<br>● Pull Down: Disable embedded PHY |
| 63 | SMI_SEL | IO/LI/PU | EEPROM SMI/MII Management Interface Selection.<br>● Pull Up: EEPROM SMI interface when EN_SLAVE_IF = 1<br>● Pull Down: MII Management interface when EN_SLAVE_IF = 1 |
| 24 | RESERVED_0 | - | Reserved. This pin must be pulled high via an external 4.7kΩ resistor to DVDDIO_2 upon power on. |
| 25 | RESERVED_1 | - | Reserved. This pin must be pulled high via an external 4.7kΩ resistor to DVDDIO_2 upon power on. |
| 27 | RESERVED_2 | - | Reserved. This pin must be pulled high via an external 4.7kΩ resistor to DVDDIO_2 upon power on. |

## 2.12 Power Related Pins

**Table 17 Power Related Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 12, 51 | DVDDIO | P | Digital power 2.5V/3.3V<br>Note: When DVDDIO uses 2.5V, its external interface must also support the corresponding voltage. |
| 37, 50 | DVDDIO_1 | P | Digital power 1.8V/2.5V/3.3V for Extension Port 1<br>Note: When DVDDIO_1 uses 1.8V/2.5V, its external interface must also support the corresponding voltage. |
| 22, 36 | DVDDIO_2 | P | Digital power 1.8V/2.5V/3.3V for Extension Port 2<br>Note: When DVDDIO_2 uses 1.8V/2.5V, its external interface must also support the corresponding voltage. |
| 14, 35, 52 | DVDDL | P | Digital power 1.1V |
| 6, 11, 64, 72, 84 | AVDDH | AP | Analog power 3.3V |
| 1, 9, 77 | AVDDL | AP | Analog power 1.1V |
| 20 | SVDDH | AP | SerDes power 3.3V |
| 17 | SVDDL | AP | SerDes power 1.1V. |
| 82 | PLLVDDL | AP | PLL Power 1.1V. |
| 7 | AGND | AG | Analog GND. |
| 83 | PLLGND | AG | PLL GND. |
| 89 | GND EPAD | G | GND |

## 2.13 Clock Pins

**Table 18 Clock Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 66 | XTAL_I | XT | 25MHz Crystal Input pin.<br>If use an external oscillator or clock from another device.<br>● When connecting an external 25MHz oscillator or clock from another device to the XTAL_O pin, XTAL_I must be shorted to GND.<br>● When connecting an external 25MHz oscillator or clock from another device to the XTAL_I pin, keep the XTAL_O floating. |
| 65 | XTAL_O | XT | 25MHz Crystal Output pin.<br>If use an external oscillator or clock from another device.<br>● When connecting an external 25MHz oscillator or clock from another device to the XTAL_O pin, XTAL_I must be shorted to GND.<br>● When connecting an external 25MHz oscillator or clock from another device to the XTAL_I pin, keep the XTAL_O floating. |

## 2.14 Reset Pins

**Table 19 Reset Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 67 | nRESET | I/PU | Hardware reset, active low. Requires an external pull-up resistor. |

## 2.15 Miscellaneous Pins

**Table 20 Miscellaneous Pins**

| No. | Pin Name | Type | Description |
|---|---|---|---|
| 8 | RBIAS | AO | Bias Resistor.<br>An external 2.49 kΩ±1% resistor must be connected between the RBIAS pin and GND. |
| 10, 21, 68, 71 | NC | - | Not connect. Must be left floating in normal operation. |

# 3 Integrated PHY Functional

YT9214NBH integrates two 10/100/1000M Giga PHY ports. Each PHY port supports 1000Base-T, 100Base-TX, and 10Base-Te by four signal pairs (MDIAP/N, MDIBP/N, MDICP/N and MDIDP/N). Each signal pair consists of two bi-directional pins that can transmit and receive at the same time.

- For 1000Base-T, all four pairs are used in both directions at the same time.
- For 100Base-TX and 10Base-Te, only MDIAP/N and MDIBP/N are used.

## 3.1 Transmit Encoder Modes

### 3.1.1 1000BASE-T

In 1000BASE-T mode, the PHY port scrambles data bytes to be transmitted from the MAC interfaces to 9-bit symbols and encodes them into 4D five-level PAM signals over the four pairs of CAT5E UTP cable.

### 3.1.2 100BASE-TX

In 100BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA.

### 3.1.3 10BASE-Te

In 10BASE-Te mode, the PHY port transmits Manchester-encoded data.

## 3.2 Receive Decoder Modes

### 3.2.1 1000BASE-T

In 1000BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimiters are translated appropriately, and data is output to the MAC interfaces.

### 3.2.2 100BASE-TX

In 100BASE-TX mode, the received data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded to 4-bit data. This output runs to MAC interfaces after data stream delimiters have been translated.

### 3.2.3 10BASE-Te

In 10BASE-Te mode, the recovered 10BASE-Te signal is decoded from Manchester then aligned.

## 3.3 Echo Canceller

A hybrid circuit is used to transmit and receive simultaneously on each pair. A signal reflects as an echo if the transmitter is not perfectly matched to the line. Other connector or cable imperfections, such as

patch panel discontinuity and variations in cable impedance along the twisted pair cable, also lead to drastic SNR degradation on the received signal. The PHY port implements a digital echo canceller to adjust for echo and is adaptive to compensate for the varied channel conditions.

## 3.4 NEXT Canceller

The 1000BASE-T physical layer uses all four pairs of wires to transmit data. Because the four twisted pairs are bundled, significant high-frequency crosstalk occurs between adjacent pairs in the bundle. The PHY port uses three parallel NEXT cancellers on each receive channel to cancel high-frequency crosstalk. The PHY port cancels NEXT by subtracting an estimate of these signals from the equalizer output.

## 3.5 Baseline Wander Canceller

Baseline wander results from Ethernet links that AC coupling to the transceivers, and AC coupling cannot maintain voltage levels for a long time. Baseline wander distorts the transmitted pulse, which in turn affects the sampling value of the pulse. Baseline wander is more susceptible in the 1000BASE-T environment than in 100BASE-TX due to the DC baseline shift in the transmit and receive signals.

The YT9214NBH device uses an advanced baseline wander cancellation circuit that continuously monitors and compensates for this effect, minimizing the impact of DC baseline shift on the overall error rate.

## 3.6 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver and takes signals from ADC output. It uses a combination of FFE (Feedforward Equalizer) and DFE (Decision Feedback Equalizer) for the best-optimized SNR (Signal-to-Noise Ratio) ratio.

## 3.7 Auto-Negotiation

The integrated PHY port negotiates its operation mode using the auto-negotiation mechanism according to IEEE 802.3 clause 28 over the copper media. Auto-negotiation supports choosing the mode of operation automatically by comparing the abilities of itself and its link partner.

Auto-negotiation is enabled for YT9214NBH by default and can be disabled by software control.

## 3.8 Auto Crossover and Polarity Correction

The integrated PHY port can detect and correct two types of cable errors:

- Auto crossover of pairs within the UTP cable (between pair 0 and pair 1, and(or) between pair 2 and pair 3)
- Swapping of polarity within a pair.

# 4 General Function

## 4.1 Reset

### 4.1.1 Hardware Reset

YT9214NBH has a hardware reset pin (nRESET) which is low active. The reset signal should be active for at least 10ms. Hardware reset should be applied after power on correctly.

After the reset is released, YT9214NBH will start the reset initialization procedures by the following steps:

1 Reset All internal logic to a known state, and reset all registers to default value.

2 Latch input value on configuration pins which are used as configuration information to provide flexible applications.

3 Complete the memory BIST process and initialize the packet buffer.

4 Autoload from the EEPROM, or boot from Flash or EEPROM by internal CPU if needed.

### 4.1.2 Software Reset

YT9214NBH supports two software resets that can be triggered by programming switch global control register: a chip reset (CHIP_RESET, bit 31 of register 0x8_0000) and a software reset (SW_RESET, bit 1 of register 0x8_0000).

#### 4.1.2.1 CHIP_RESET

The CHIP_RESET is set to 1 to take effect and self-clear. The chip will obey the following steps:

1 Reset all the digital and analog circuits to default.

2 Reinitialize the packet buffer and clear all the lookup and VLAN tables.

3 Autoload from the EEPROM, or boot from Flash or EEPROM by internal CPU if needed, and the chip will be configured again.

4 The integrated PHYs will restart the auto-negotiation process.

#### 4.1.2.2 SW_RESET

The SW_RESET is also set to 1 to take effect and self-clear, and its function is similar to the CHIP_RESET except the analog circuit of integrated PHYs will not be reset.

## 4.2 Flexible Applications by Configuration Pins

According to the system application, the user can select the most suitable mode by configuration pins DISAUTOLOAD, DIS_MCU, EN_SPIF, EN_SLAVE_IF, SMI_SEL, and SPF_MUX_EN, shown in the following table.

**Table 21 Flexible Applications**

| DISAUTOLOAD | DIS_MCU | EN_SPIF | EN_SLAVE_IF | SMI_SEL | SPF_MUX_EN | Initial Stage Loading Data* | |
|---|---|---|---|---|---|---|---|
| | | | | | | From | To |
| 0 | 0 | 0 | 1 | 1 | X | EEPROM | RAM |

| DISAUTO LOAD | DIS_MCU | EN_SPIF | EN_SLAVE_IF | SMI_SEL | SPF_MUX_EN | Initial Stage Loading Data* | |
|---|---|---|---|---|---|---|---|
| | | | | | | From | To |
| 0 | 0 | 1 | X | X | 0 | XIP | |
| 0 | 1 | 0 | X | X | X | EEPROM | Register |
| 0 | 1 | 1 | X | X | 0 | Flash | RAM |
| Others | | | | | | No Action | |

**Note*:** Initial Stage means power on, hardware reset, or software reset.

## 4.3 IEEE 802.3x Full Duplex Flow Control

YT9214NBH supports IEEE 802.3x flow control in 10/100/1000M full duplex modes. The result of Auto-Negotiation or software configuration can decide the flow control ability.

In most cases, MAC ports with integrated PHY get flow control ability by Auto-Negotiation and two extra MAC ports with MII/RMII/RGMII by software configuration.

## 4.4 Half Duplex Flow Control

When the PHY port works in 10/100M half-duplex modes, it will collide with the link partner when transmitting and receiving data. Then this will make the buffer overflow and drop packets. YT9214NBH supports two methods (jam mode and defer mode) to avoid this.

The maximum retry count limitation is 16 which follows the definition in IEEE 802.3. But for YT9214NBH, the retry count limitation is configurable and will not drop packets by default.

## 4.5 FDB Table

### 4.5.1 Lookup and Forward

YT9214NBH MAC address table consists of a 4K-entry FDB table. On receiving a packet, YT9214NBH uses DA and FID to search the 4K-entry FDB table.

- If an entry is matched, the received packet will be forwarded to the corresponding destination port.
- If no entry is matched, YT9214NBH floods the packet according to the VLAN configuration.

### 4.5.2 MAC Address Learning

YT9214NBH uses the source MAC address and FID to search the 4K-entry FDB table when a packet is received.

- If there is a match with one of the entries, YT9214NBH will update the entry with new information.
- If there is no matching entry, the packet information is learned into the entry.

### 4.5.3 MAC Address Aging

The aging mechanism of MAC address is as follows:

When a packet flow reaches a port, the port learns the MAC address dynamically.

- If the port keeps receiving this packet flow, the corresponding MAC address is updated continuously and will not be aged.
- If the packet flow stops, the MAC address is deleted after the aging time. The aging time of YT9214NBH is between 5 and 327,675 seconds (the typical value 300 seconds).

## 4.6 IVL SVL and IVL/SVL

YT9214NBH supports IVL (Independent VLAN Learning), SVL (Shared VLAN Learning), and IVL/SVL (Both Independent and Shared VLAN Learning).

## 4.7 Reserved Multicast Address

YT9214NBH supports drop/forward/copy IEEE 802.3 specified reserved multicast MAC addresses: 01-80-C2-00-00-00 to 01-80-C2-00-00-2F. The default setting for these reserved multicast MAC addresses is forwarding. Frames with multicast MAC address 01-80-C2-00-00-01 (802.3x Pause) will always be dropped.

## 4.8 Storm Control

YT9214NBH supports storm control for broadcast, multicast, and unknown DA, each storm type can be enabled/disabled per port, and default is disabled. If the RX rate of these types of packets exceeds the configured rate, all following storm packets will be dropped. The rate can be configured with packet mode (pps) or byte mode (bps).

## 4.9 Port Security

YT9214NBH supports the following security mechanism to prevent malicious attacks:

- Per-port enable/disable SA auto-learning
- Per-port enable/disable FDB aging update
- Per-port enable/disable unknown DA packet drop

## 4.10 MIB

YT9214NBH supports the following MIB standards for common management:

- MIB-II (RFC 1213)
- Ethernet-Like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

## 4.11 Port Mirror

YT9214NBH supports 1 group of port mirrors for all ports. The TX/RX or both direction packets from each port can be mirrored to the monitor port.

## 4.12 VLAN Function

YT9214NBH supports a 4K VLAN table, can be configured as port-based VLAN, IEEE 802.1Q tag-based VLAN, Protocol-based VLAN, and also supports the IVC (VLAN Translate) function. Ingress-filtering, egress-filtering, and accept-frame-type options provide flexible VLAN configuration:

- Ingress Filtering: Packets from an input port not in the VLAN member will be dropped.
- Egress Filtering: Packets to an output port not in the VLAN member will be dropped.
- Accept Frame Type: The input port can be configured as “Accept All”, “Accept Tagged”, “Accept Untagged”, and “Drop All”.

The packets at the output port can be inserted or removed VLAN tag. For untagged packets, YT9214NBH can insert a VLAN TAG or remove the VLAN TAG from tagged frames.

### 4.12.1 Port-Based VLAN

The 4K-entry VLAN Table designed into YT9214NBH provides full flexibility for users to configure the input ports to associate with different VLAN entries. Each input port can join with more than one VLAN entry.

Port-based VLAN mapping is the simplest and most effective mapping rule. It defines VLAN members based on device ports. All the packets received from a given input port will be forwarded to this port’s VLAN members.

### 4.12.2 IEEE 802.1Q Tag-Based VLAN

In 802.1Q VLAN mapping, the device uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. YT9214NBH compares the VID in the VLAN tag with the 4K VLAN Table to determine the packet forwarding action.

### 4.12.3 Port VID

YT9214NBH supports Port VID (PVID) for each port. When an untagged or priority-tagged packet is forwarded to the output port without hitting other assigned vid rules and the egress tag mode set tagged, the device supports inserting a PVID in the VLAN tag.

## 4.13 QoS Function

YT9214NBH supports 8 unicast priority queues, 4 multicast priority queues, and input bandwidth control. Packet priority selection can depend on Port-based priority, 802.1Q Tag-based priority, VLAN entry-based priority, MAC SA-based priority, MAC DA-based priority, DSCP-based priority, and ACL-based priority. When multiple priorities are enabled in YT9214NBH, the packet’s priority will be assigned based on the priority selection table.

Per-queue in each output port can be set as Strict Priority (SP) or Deficit Weighted Round Robin (DWRR) for the packet scheduling algorithm.

### 4.13.1 Input Bandwidth Control

Input bandwidth control limits the input bandwidth. When input traffic exceeds the RX Bandwidth parameter, if flow control is enabled, this port will send out a “pause ON” frame; If flow control is disabled, it will drop the input packet. Per-port input bandwidth control rates can be set from 9Kbps to 2.5Gbps (in 9Kbps steps).

### 4.13.2 Priority Assignment

Priority assignment specifies the priority of a received packet based on various rules. YT9214NBH can recognize the QoS priority information of receiving packets to give a different service priority.

YT9214NBH identifies the priority of packets based on seven types of QoS priority information:

- Port-based priority
- 802.1Q-based priority
- DSCP-based priority
- ACL-based priority
- VLAN entry-based priority
- MAC SA-based priority
- MAC DA-based priority

### 4.13.3 Priority Queue Scheduling

The packet scheduler controls the various traffics (control packets sending a sequence of the priority queue), YT9214NBH scheduling algorithm is Deficit Weighted Round Robin (DWRR). DWRR supports byte-based or packet-based.

In addition, each queue of each port can select Strict Priority or DWRR packet scheduling, and DWRR can co-exist with the SP schedule.

### 4.13.4 IEEE 802.1Q and DSCP Remarking

YT9214NBH supports the IEEE 802.1Q and DSCP remarking functions. If the remarking function is enabled, when packets egress from one of the 12 queues, the packet’s 802.1Q priority and DSCP can be remarked to a configured value. 802.1Q priority & DSCP value can be remarked based on internal priority.

## 4.14 IGMP & MLD Snooping Function

YT9214NBH supports hardware IGMPv1/v2/v3 snooping and MLDv1/v2 snooping. These multicast groups are learned and deleted/aged out automatically. For data packets of a known multicast group, YT9214NBH forwards them according to the learned group membership.

YT9214NBH supports bypassing designated IP multicast address with global control and per ingress port join/leave packets allowed control.

YT9214NBH supports IGMP Dynamic Router Port Learning, dynamic router port enable control is based on per-port basis. The aging time can be configured by SW, the router port will be removed when timeout.

YT9214NBH supports IGMP/MLD Hardware Fast Leave, when left, the multicast group will be marked as invalid again.

YT9214NBH supports IGMP/MLD Packet Copy/Trap/Flood based on global control.

## 4.15 IEEE 802.1x Function

YT9214NBH supports IEEE 802.1x Port-Based.

- Port-Based Access Control for each port
- Authorized Port-Based Access Control for each port
- Port-Based Access Control Direction for each port
- Guest VLAN

### 4.15.1 Port-Based Access Control

Each port of YT9214NBH can be set to 802.1x port-based authenticated checking function usage and authorized status. Ports with 802.1X unauthorized status will drop received/transmitted frames.

### 4.15.2 Authorized Port-Based Access Control

If a dedicated port is set to 802.1x port-based access control, and passes the 802.1x authorization, its port authorization status can be set to authorized.

### 4.15.3 Port-Based Access Control Direction

Ports with 802.1X unauthorized status will drop received/transmitted frames only when the port authorization direction is “BOTH”. If the authorization direction of an 802.1X unauthorized port is “IN”, incoming frames to that port will be dropped, but outgoing frames will be transmitted.

### 4.15.4 Guest VLAN

When YT9214NBH enables the Port-based 802.1x function, and the connected PC does not support the 802.1x function or does not pass the authentication procedure, YT9214NBH will drop all packets from this port. If configuring Guest VLAN, YT9214NBH will allow packets from unauthorized ports to be forwarded to a limited VLAN domain.

## 4.16 Spanning Tree

IEEE 802.1D Spanning Tree allows bridges to prevent and resolve Layer 2 forwarding loops automatically. Switches exchange BPDUs and configuration messages and selectively enable and disable forwarding on specified ports. YT9214NBH supports 16 STP instances and four statuses (Disabled/Blocking/ Learning/Forwarding) for each port when the CPU implements the STP/RSTP/MSTP function.

## 4.17 Embedded RISC-V

A RISC-V MCU is embedded in YT9214NBH to support software management/protocol functions. The RISC-V MCU can transmit to or receive frames from the switch core. The features of the RISC-V MCU are listed below:

- On-chip 64K SRAM
- On-chip 16K boot ROM
- 2K I-Cache
- Up to 8M-Byte serial I/O, dual I/O SPI Flash supported

## 4.18 Cable Status Diagnostic

Physical layer transceivers of YT9214NBH support Motorcomm's Advanced Cable Status Diagnostic (CSD) feature. Some of the possible problems that can be diagnosed in each differential pair. The result of CSD is summarized as normal, open, and short.

## 4.19 LED Indicators

The YT9214NBH supports parallel LEDs for each port. Each PHY port has three LED indicator pins, LED0, LED1, and LED2. Each LED of each port may have different indicator information defined in Table 22. LED0 default indicates Link/Act, LED1 default indicates 1000M_Link, and LED2 default indicates 100M_Link.

YT9214NBH supports the power-on-blinking feature by the EN_PWRLIGHT pin and software configuration. The LEDs will blink once after reset.

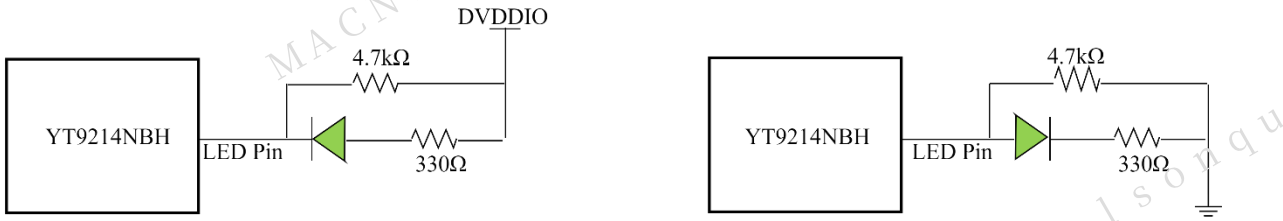
**Table 22 LED Definitions**

| LED Definition | Description |
|---|---|
| Full | Full Duplex Indicator. LED on when the corresponding port links at full duplex. |
| Half | Half Duplex Indicator. LED on when the corresponding port links at half duplex. |
| Link | Link Indicator. LED on when the corresponding port links up. |
| 1000M_Link | 1000Mbps Link Indicator. LED on when the corresponding port links at 1000Mbps. |
| 100M_Link | 100Mbps Link Indicator. LED on when the corresponding port links at 100Mbps. |
| 10M_Link | 10Mbps Link Indicator. LED on when the corresponding port links at 10Mbps. |
| Act | Activity Indicator. LED blinks when the corresponding port is transmitting or receiving. |
| 1000M_Act | 1000Mbps Activity Indicator. LED blinks when the corresponding port links at 1000Mbps and is transmitting or receiving. |
| 100M_Act | 100Mbps Activity Indicator. LED blinks when the corresponding port links at 100Mbps and is transmitting or receiving. |
| 10M_Act | 10Mbps Activity Indicator. LED blinks when the corresponding port links at 10Mbps and is transmitting or receiving. |
| TX_Act | TX Activity Indicator. LED blinks when the corresponding port is transmitting. |
| RX_Act | RX Activity Indicator. LED blinks when the corresponding port is received. |
| EEE_Act | EEE Mode Indicator. LED blinks when the corresponding port enters EEE mode. |
| Loop_Act | Loop Detection Indicator. LED blinks when the corresponding port detects a loop. |

LED signals are active low by default. The LED pins also support hardware configuration functions, so they are dual-function pins: input operation for configuration upon reset, and output operation for LED after reset. When the pin input is pulled high upon reset, the pin output is active low for LED function after reset. When the pin input is pulled down upon reset, the pin output is active high for LED function after reset. Typical values for pull-up/pull-down resistors are 4.7kΩ.

**Figure 3 Pull-Up and Pull-Down of LED Pins**



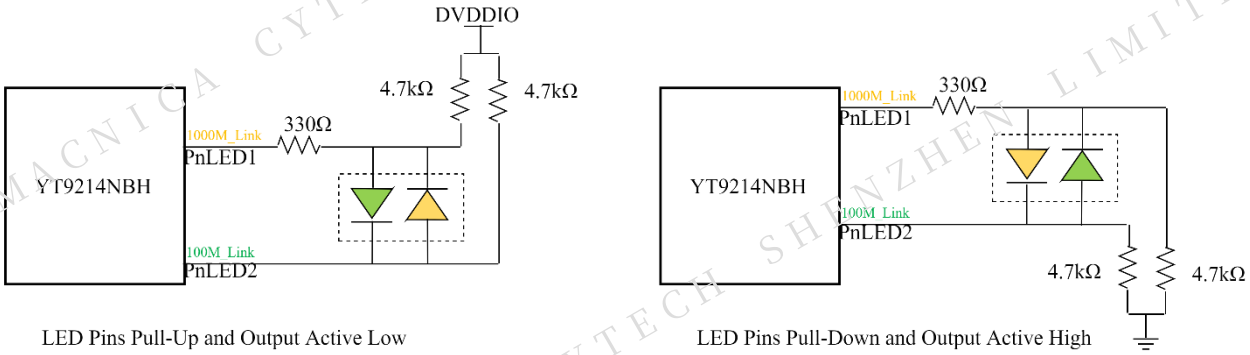

LED Pins Pull-Up and Output Active Low

LED Pins Pull-Down and Output Active High

The LED Pins can also support Bi-color LED applications. Both LED pins connected to the Bi-color LED should have the same polarity active, and the LED definition of both will not appear at the same time.

For example, refer to Figure 4 PnLED1 and PnLED2 will be Pull-Up or Pull-Down together. The PnLED1 definition is 1000M_link. Nevertheless, the PnLED2 definition is 100M_link. PnLED1 and PnLED2 will not be ON at the same time.

**Figure 4 Typical Application for Bi-color LED**




LED Pins Pull-Up and Output Active Low

LED Pins Pull-Down and Output Active High

## 4.20 Link Down Power Saving

Physical layer transceivers of YT9214NBH support link-down power saving, also called sleep mode. When the UTP port link down and no signals over the UTP cable for 40 seconds, Physical layer transceivers will enter sleep mode. In this mode, some circuits of physical layer transceivers will be disabled, and the power consumption of the whole chip will be lower.

Once detected signals are over the UTP cable, the physical layer transceiver will exit sleep mode to normal mode.

## 4.21 Energy Efficient Ethernet

YT9214NBH supports IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T, 100Base-TX in full duplex operation.

IEEE 802.3az is an extension of the IEEE 802.3 standard. It defines the PHY transceivers to operate in Low Power Idle (LPI) mode which supports QUIET times during low link utilization allowing both link partners to disable portions of each PHY transceiver's circuitry and save power consumption.

When Low Power Idle mode is enabled by MAC and PHY, the YT9214NBH MAC uses Low Power Idle signaling to indicate to the PHY that a period of idle in the data stream is expected. Both local and link partner PHY transceivers may use this information to enter power-saving modes.

## 4.22 Interrupt Pin for External CPU

YT9214NBH provides one Interrupt output pin to interrupt an external CPU. The polarity of the Interrupt output pin can be configured via register access. In configuration registers, each port has link-up and link-down interrupt flags with the mask.

When the port link-up or link-down interrupt mask is enabled, the YT9214NBH will raise the interrupt signal to alarm the external CPU. The CPU can read the interrupt flag to determine which port has changed to which status.

# 5 Interface Descriptions

## 5.1 SPI Flash Interface

YT9214NBH supports two groups of SPI flash interfaces. Both support Serial I/O and Dual I/O operation modes, 3-byte address mode access and up to 8Mbyte size flash. The value of the configuration pin EN_SPIF decides the SPI interface to be used. See Table 21 to find out how to decide whether RISC-V MCU works in XIP mode or loads from Flash to RAM.

**Figure 5 XIP On Flash**

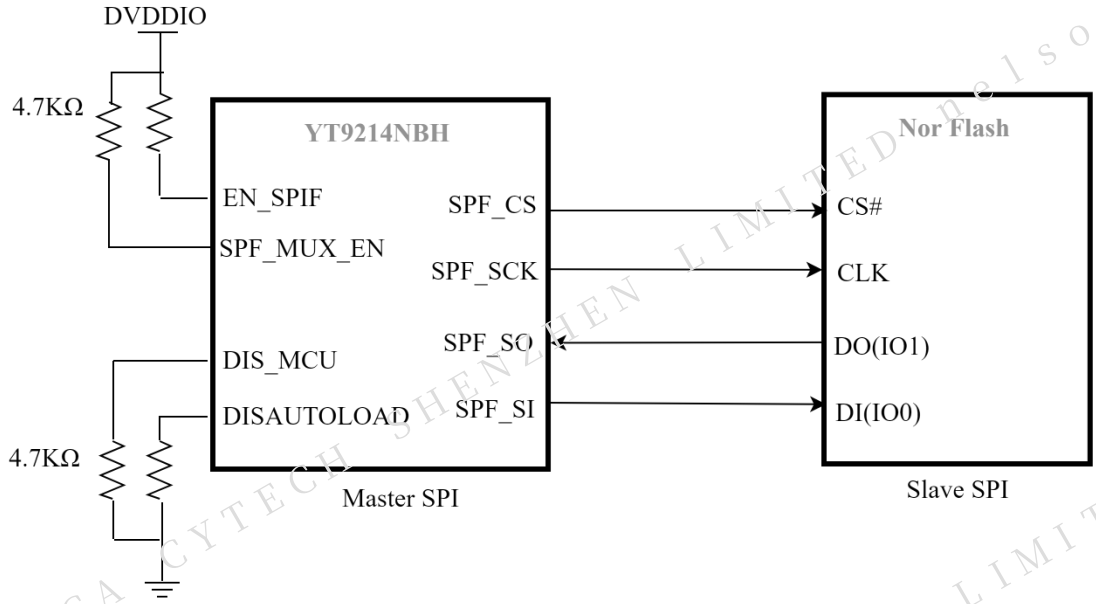
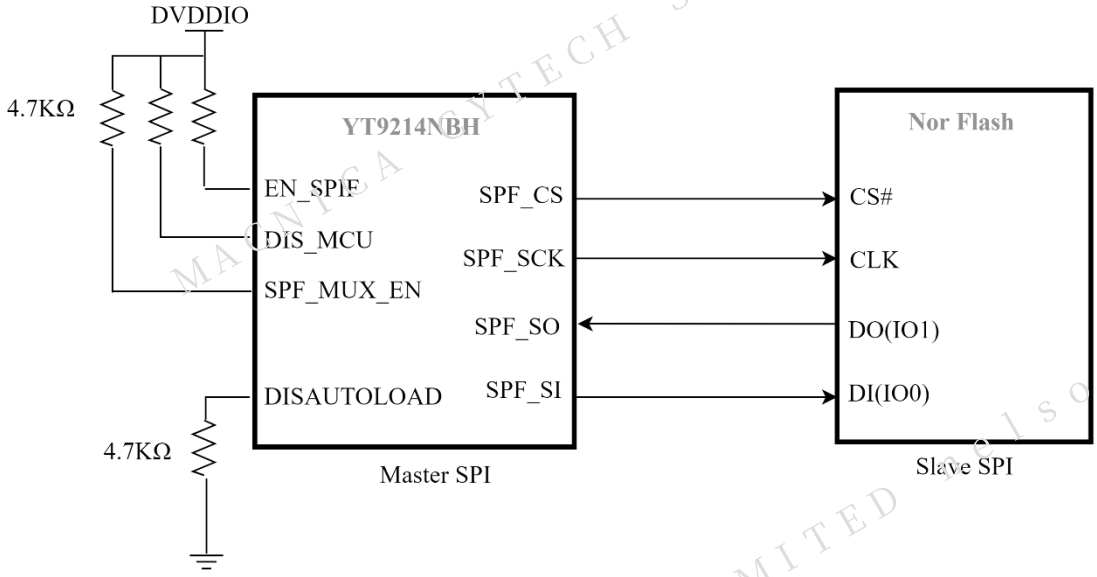



**Figure 6 Load From Flash To RAM**



## 5.2 Master I2C Interface for EEPROM Auto-load

The EEPROM auto-load interface of the YT9214NBH uses the serial bus I2C to read the Serial EEPROM. After YT9214NBH power on or reset, it drives SCL and SDA to read the data from the EEPROM by configuration pins.

As shown in the following figure, Pull-Up resistors, for example, 4.7kΩ should be connected to SCL and SDA signals.

**Figure 7 Auto-load From EEPROM To Register**

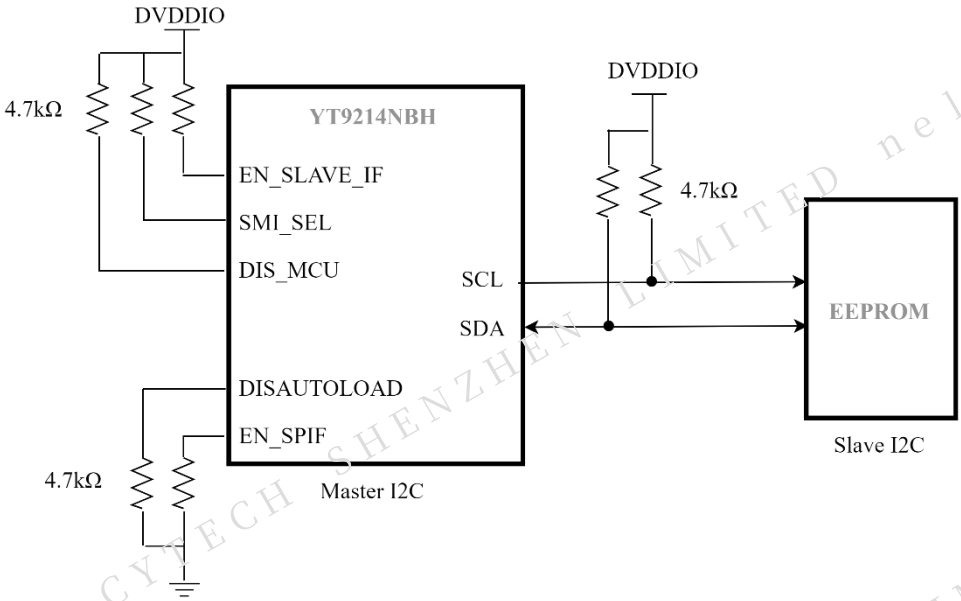
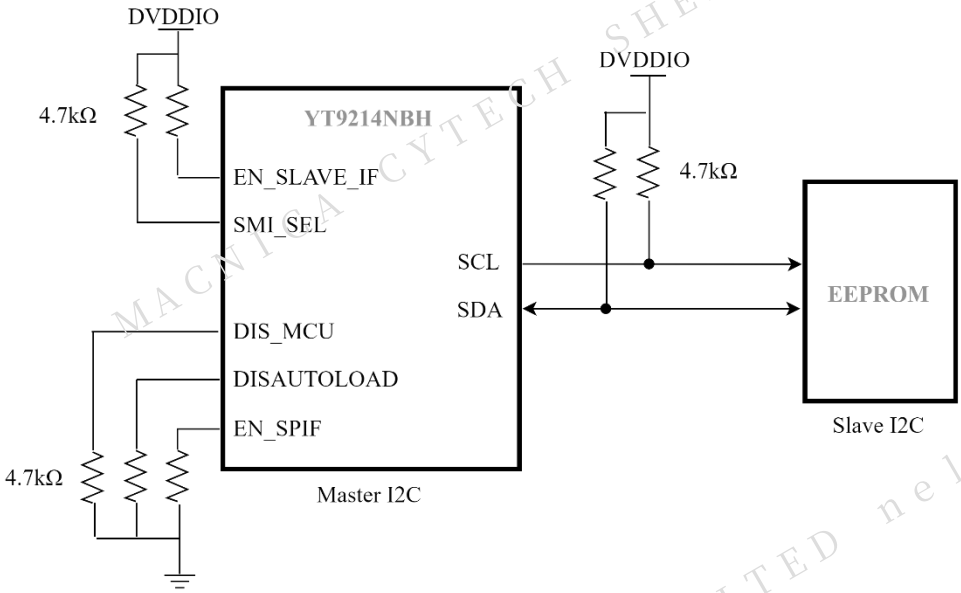



**Figure 8 Auto-load From EEPROM To RAM**




YT9214NBH only supports 2 bytes word address mode EEPROM, that size should be 32Kbit~512Kbit.

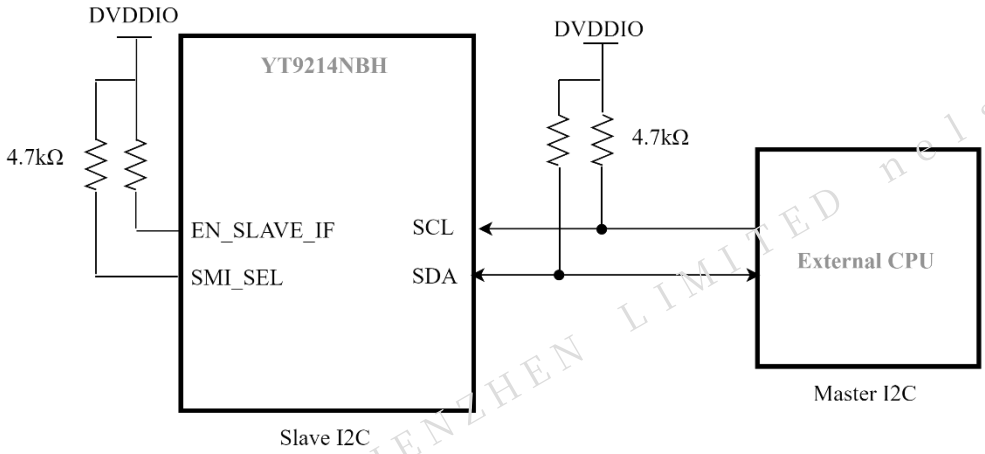
  

## 5.3 Management Interfaces

### 5.3.1 Slave I2C Interface for External CPU

YT9214NBH registers can be accessed via slave I2C interfaces (SCK and SDA) by an external CPU. The configuration pins EN_SLAVE_IF and SMI_SEL should be high up on power on or reset, to select slave I2C interface.

**Figure 9 Slave I2C Interface Connection Example**




The slave I2C format is derived from the standard I2C, as shown in the following diagram. Switch_ID [1:0] comes from the configuration pins SWITCH_ID_1 and SWITCH_ID_0. C stands for the even parity check of ADDR[31:2].

- C = 0, if there is an even number of “1” in ADDR [31:2].
- C = 1, if there is an odd number of “1” in ADDR [31:2].

**Figure 10 External CPU Write Register into YT9214NBH By Slave I2C**

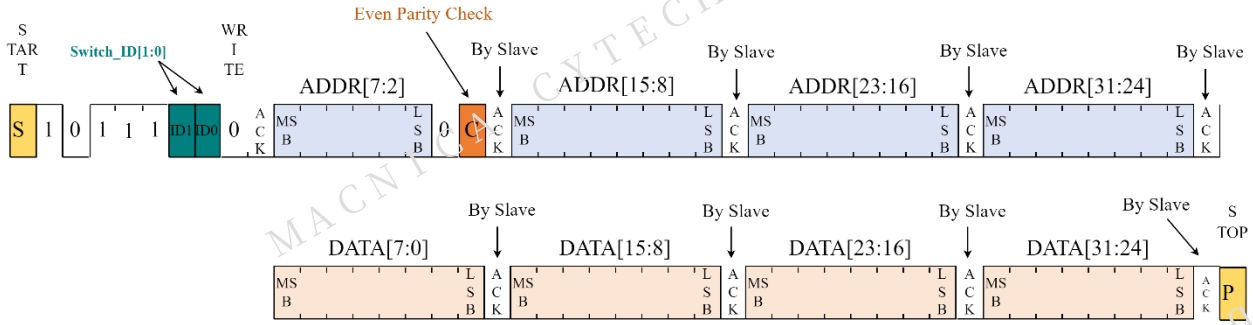
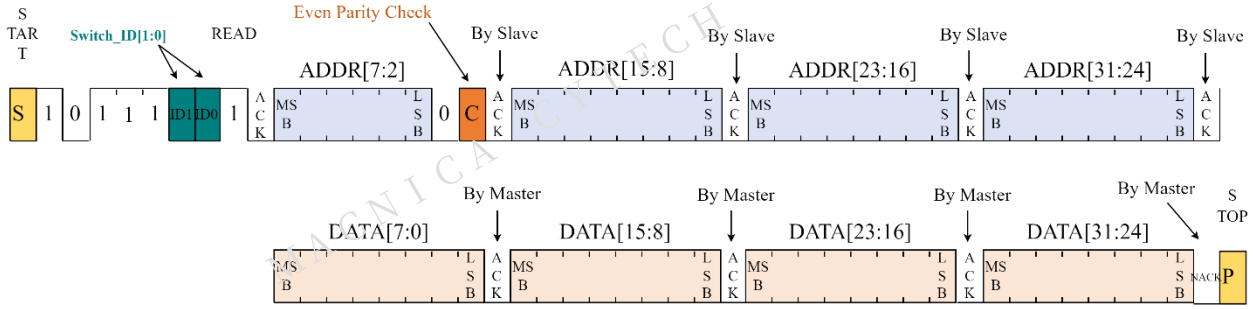


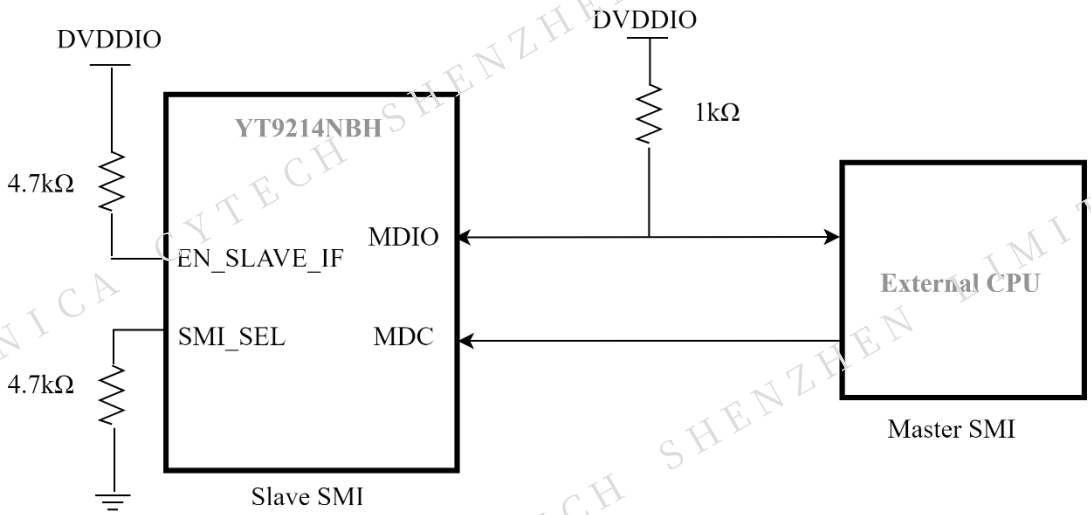
**Figure 11 External CPU Read Register from YT9214NBH By Slave I2C**




## 5.3.2 Slave SMI Interface for External CPU

If the SMI_SEL is low or high upon power on or reset, the slave SMI (MDC/MDIO) is selected to access YT9214NBH registers.

**Figure 12 External CPU Read Register from YT9214NBH By Slave SMI**




# 5.4 General Purpose interface

YT9214NBH supports two extension interfaces. The two Extension GMAC (GMAC1 and GMAC2) both support RGMII mode, MII MAC mode, MII PHY mode, RMII MAC mode, and RMII PHY mode. The Extension GMAC2 also supports SGMII MAC mode, SGMII PHY mode, 2500Base-X mode, 1000Base-X mode, and 100Base-FX mode. All modes can be configured by register.

## 5.4.1 Extension Ports SGMII MAC/PHY Mode (10/100/1000Mbps)

The Extension GMAC2 supports SGMII MAC/PHY interfaces to an external CPU.

### 5.4.2 Extension Ports Fiber Mode (100FX/1000BX/2500BX)

The Extension GMAC2 supports Fiber (100FX/1000BX/2500BX) interfaces to an external CPU or optical module.

### 5.4.3 Extension Ports RGMII Mode (10/100/1000Mbps)

The two Extension GMAC (GMAC1 and GMAC2) both support single-port RGMII interfaces to an external CPU.

### 5.4.4 Extension Ports MII MAC/PHY Mode Interface (10/100Mbps)

The two Extension GMAC (GMAC1 and GMAC2) both support MII MAC/PHY mode interfaces to an external CPU.

### 5.4.5 Extension Ports RMII MAC/PHY Mode Interface (10/100Mbps)

The two Extension GMAC (GMAC1 and GMAC2) both support RMII MAC/PHY mode interfaces to an external CPU.

# 6 Power Requirements

## 6.1 Power Sequence

**Figure 13 Power Sequence Diagram**

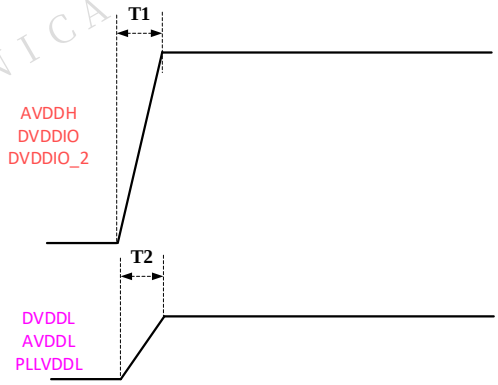



**Table 23 Power Sequence Timing Parameters**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| T1 | The rising time of AVDDH, DVDDIO, DVDDIO_2. | 0.5 | - | - | ms |
| T2 | The rising time of DVDDL, AVDDL, PLLVDDL. | 0.5 | - | - | ms |

## 6.2 Power Consumption

**Table 24 YT9214NBH Power Consumption**

| Condition | AVDDH + SVDDH+DVDDIO + DVDDIO_2 (3.3V, mA) | DVDDL + AVDDL +SVDDL+ PLLVDDL (1.15V, mA) | Power Consumption (mW) |
|---|---|---|---|
| Link Down | 77 | 107 | 372 |
| 2 UTP Link Up @1000Mbps | 134 | 264 | 733 |
| 2 UTP Traffic @1000Mbps | 133 | 295 | 763 |
| 2 UTP + 2 RGMII Link Up @1000Mbps | 149 | 272 | 791 |
| 2 UTP + 2 RGMII Traffic @1000Mbps | 163 | 315 | 884 |
| 2 UTP + 1 RGMII + 1 Serdes (2.5G) Traffic @1000Mbps | 171 | 373 | 975 |

Test Condition: Port 1 and Port 3 work as 1000BT. TT IC with AVDDH/DVDDIO/DVDDIO_2 = 3.3V and DVDDL/AVDDL/PLLVDDL = 1.15V at room temperature.

## 6.3 Power Ripple

The AVDDH/DVDDIO/DVDDIO_2 supply ripple should be under 100mV. The DVDDL ripple should be under 80mV, and the AVDDL and PLLVDDL ripple should be under 50mV.

# 7 Electrical Characteristics

## 7.1 Absolute Maximum Ratings

**Table 25 Absolute Maximum Ratings**

| Parameter | Min | Max | Unit |
|---|---|---|---|
| Junction Temperature ($T_j$) | - | +125 | °C |
| Storage Temperature | -45 | +125 | °C |
| DVDDIO, DVDDIO_2, AVDDH, SVDDH, Supply Referenced to GND and AGND | GND-0.3 | +3.70 | V |
| DVDDL, AVDDL, PLLVDDL, SVDDL, Supply Referenced to GND, AGND and PLLGND | GND-0.3 | +1.40 | V |
| Digital Input Voltage | GND-0.3 | VDDIO+0.3 | V |

## 7.2 Recommended Operating Range

**Table 26 Recommended Operating Range**

| Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Ambient Operating Temperature ($T_a$) | | -40 | - | 85 | °C |
| DVDDIO, AVDDH, SVDDH Supply Voltage Range | | 3.135 | 3.3 | 3.63 | V |
| DVDDIO_2 Supply Voltage Range (DVDDIO_2: Extension Port 2 Supports 1.8V, 2.5V, 3.3V) | 3.3V | 3.135 | 3.3 | 3.63 | V |
| | 2.5V | 2.25 | 2.5 | 2.75 | V |
| | 1.8V | 1.620 | 1.8 | 1.98 | V |
| DVDDL, AVDDL, PLLVDDL, SVDDL, Supply Voltage Range | | 1.08 | 1.15 | 1.32 | V |

## 7.3 DC Characteristics

**Table 27 DC Characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VOH (3.3V) | Minimum High-Level Output Voltage | 2.4 | - | 3.63 | V |
| VOL (3.3V) | Maximum Low-Level Output Voltage | -0.3 | - | 0.4 | V |
| VIH (3.3V) | Minimum High-Level Input Voltage | 2 | - | - | V |
| VIL (3.3V) | Maximum Low-Level Input Voltage | - | - | 0.8 | V |
| VOH (2.5V) | Minimum High-Level Output Voltage | 2 | - | 2.8 | V |
| VOL (2.5V) | Maximum Low-Level Output Voltage | -0.3 | - | 0.4 | V |
| VIH (2.5V) | Minimum High-Level Input Voltage | 1.7 | - | - | V |
| VIL (2.5V) | Maximum Low-Level Input Voltage | - | - | 0.7 | V |
| VOH (1.8V) | Minimum High-Level Output Voltage | 1.62 | - | 2.1 | V |
| VOL (1.8V) | Maximum Low-Level Output Voltage | -0.3 | - | 0.4 | V |
| VIH (1.8V) | Minimum High-Level Input Voltage | 1.2 | - | - | V |

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VIL (1.8V) | Maximum Low-Level Input Voltage | - | - | 0.5 | V |

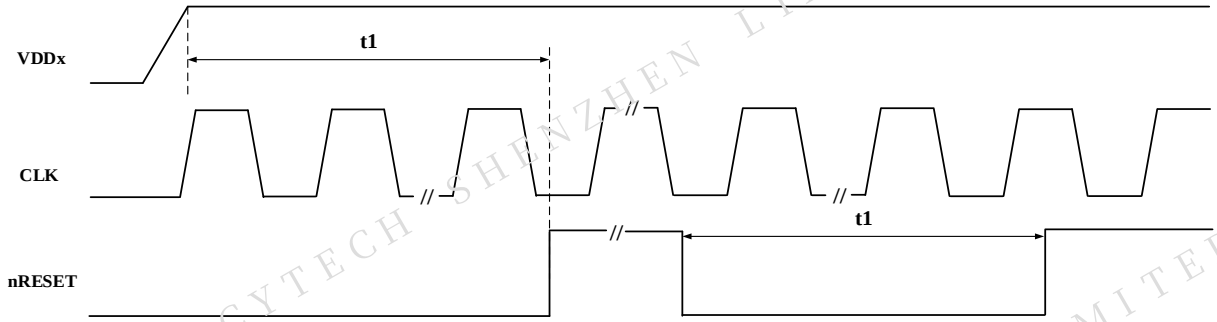
## 7.4 AC Characteristics

### 7.4.1 Reset Timing

**Table 28 Reset Timing Characteristics**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| t1 | The time from all powers steady to nRESET de-asserted, or the nRESET assertion time after power up. | 10 | - | - | ms |

**Figure 14 Reset Timing Diagram**




### 7.4.2 SPI Flash Interface Timing Characteristics

**Figure 15 SPI Flash Interface Timing**

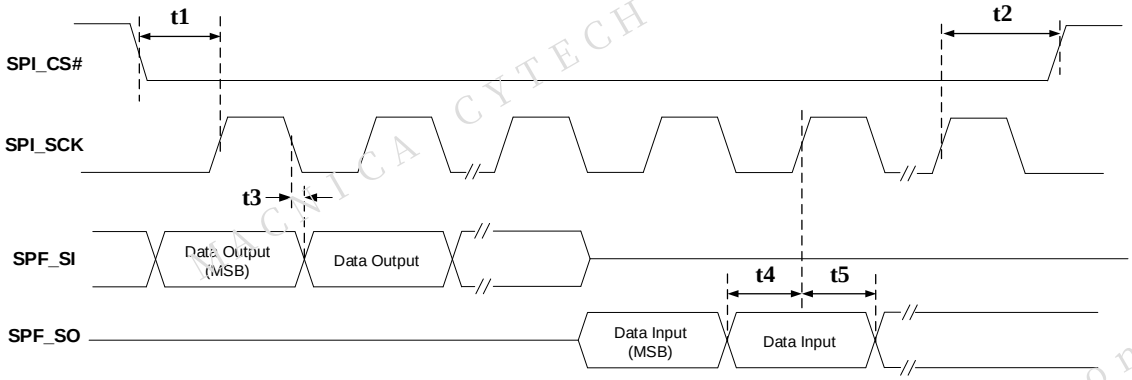



**Table 29 SPI Flash Interface Timing Parameter**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Freq | Clock Frequency of SPI_SCK | - | 31.25 | - | MHz |
| t1 | SPI_CS# Active Setup Time relative to SPI_SCK | 20 | - | - | ns |

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| t2 | SPI_CS# Not Active Hold Time relative to SPI_SCK | 80 | - | - | ns |
| t3 | SPI_SI Output Valid Time | 0 | - | 15 | ns |
| t4 | SPI_SO Input Setup Time | 2 | - | - | ns |
| t5 | SPI_SO Input Hold Time | 0 | - | - | ns |

### 7.4.3 Master I2C for EEPROM Auto-load Timing Characteristics

**Figure 16 Master I2C for EEPROM Auto-load Timing**

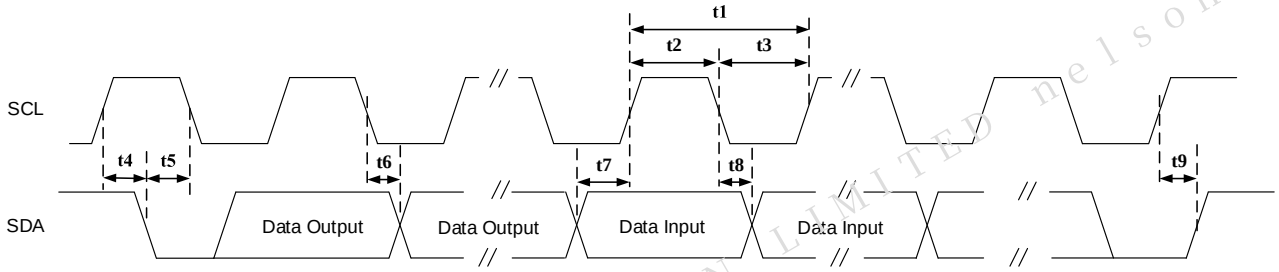



**Table 30 Master I2C for EEPROM Auto-load Timing Parameter**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Tfreq | SCL Clock Frequency | - | 100 | 800 | kHz |
| t1 | SCL Clock Period | 1.25 | 10 | - | μs |
| t2 | SCL High Time | 0.3*t1 | 0.5*t1 | - | μs |
| t3 | SCL Low Time | 0.3*t1 | 0.5*t1 | - | μs |
| t4 | START Setup Time | 0.25*t1 | - | - | μs |
| t5 | START Hold Time | 0.25*t1 | - | - | μs |
| t6 | SCL Low to Data Output Valid | 0.1*t1 | - | 0.2*t1 | μs |
| t7 | Data Input Setup Time | 0 | - | - | ns |
| t8 | Data Input Hold Time | 0 | - | - | ns |
| t9 | Stop Setup Time | 0.3*t1 | - | - | μs |

### 7.4.4 Slave I2C Timing Characteristics

**Figure 17 Slave I2C Timing**

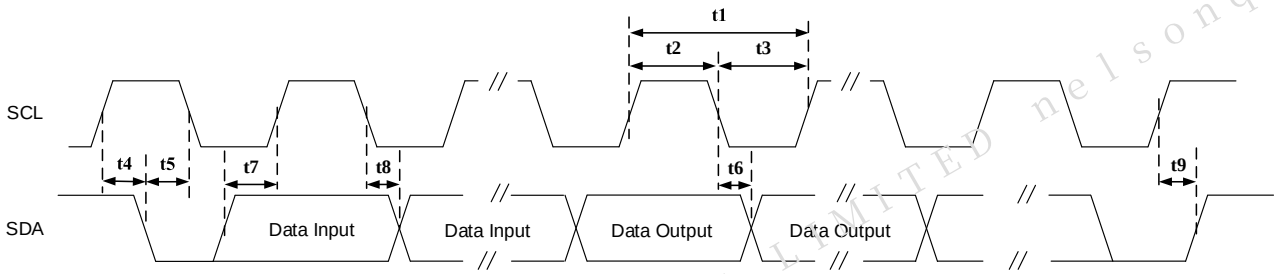


**Table 31 Slave I2C Timing Parameter**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Tfreq | SCL Clock Frequency | - | - | 400 | kHz |
| t1 | SCL Clock Period | 2.5 | - | - | μs |
| t2 | SCL High Time | 0.8 | | - | μs |
| t3 | SCL Low Time | 0.8 | | - | μs |
| t4 | START Setup Time | 0.3 | - | - | μs |
| t5 | START Hold Time | 0.3 | - | - | μs |
| t6 | SCL Low to Data Output Valid | 0.1 | - | 0.3 | μs |
| t7 | Data Input Setup Time | 0 | - | - | ns |
| t8 | Data Input Hold Time | 200 | - | - | ns |
| t9 | Stop Setup Time | 0.3 | - | - | μs |

### 7.4.5 Slave SMI Timing Characteristics

**Figure 18 Slave SMI Timing**

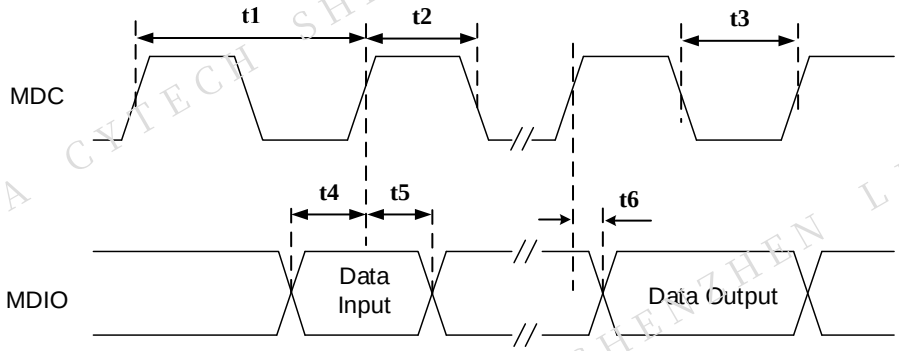



**Table 32 Slave SMI Timing Parameter**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| t1 | MDC Clock Period | 250* | - | - | ns |
| t2 | MDC High Time | 80 | - | - | ns |
| t3 | MDC Low Time | 80 | - | - | ns |
| t4 | MDIO to MDC Rising Setup Time (Data Input) | 10 | - | - | ns |
| t5 | MDIO to MDC Rising Hold Time (Data Input) | 10 | - | - | ns |
| t6 | MDIO Valid from MDC rising edge (Data Output) | 5 | - | 40* | ns |

**Note*:** The MDIO pin type is Open Drain when working as a slave SMI interface. Therefore, the minimum value of t1 and the maximum value of t6 depend on the value of the pull-up resistor on the MDIO signal. Parameters in is the result under the condition of pull-up 1kΩ resistor.

### 7.4.6 RGMII Timing W/O Delay

**Figure 19 RGMII Timing W/O Delay**

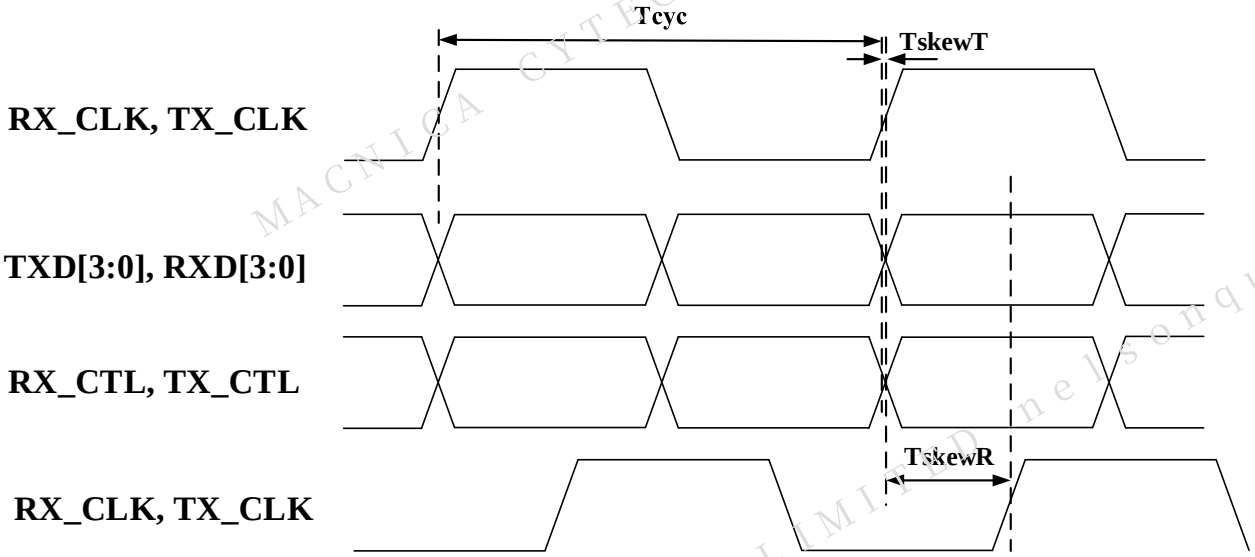



**Table 33 RGMII Timing W/O Delay**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TskewT | Data to clock output skew (at Transmitter) | -500 | 0 | 500 | ps |
| TskewR | Data to clock output skew (at Receiver) | 1 | 1.5 | 2.0 | ns |
| Tcyc | Clock cycle duration | 7.2 | 8.0 | 8.8 | ns |
| Duty_G | Duty cycle for Gigabit | 45 | 50 | 55 | % |
| Duty_T | Duty cycle for 10/100T | 40 | 50 | 60 | % |

### 7.4.7 RGMII Timing with Internal Delay

**Figure 20 RGMII Timing with Internal Delay**

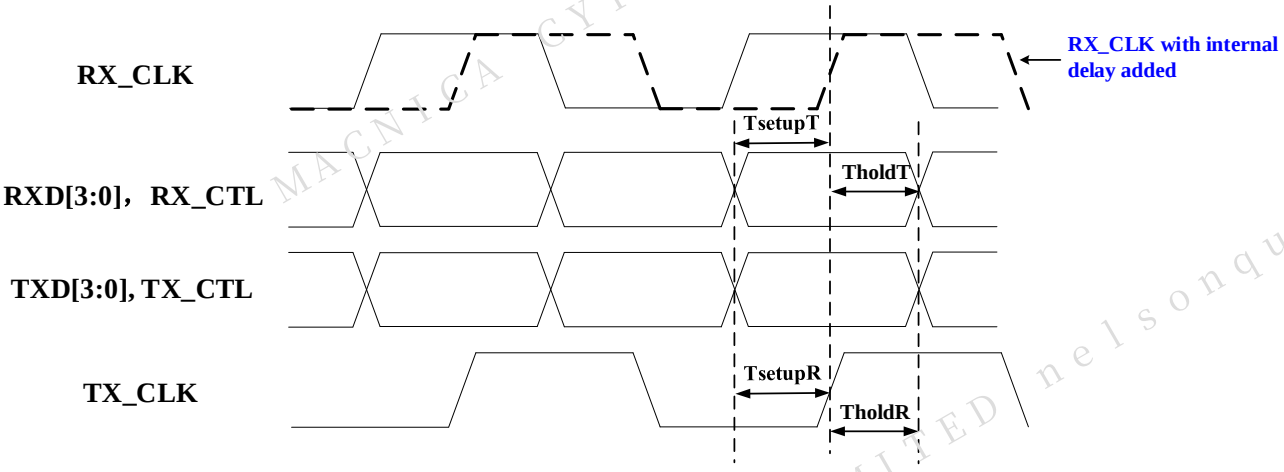


**Table 34 RGMII Timing with Internal Delay**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TsetupT | Data to Clock output Setup Time (at Transmitter integrated delay) | 1.0 | 2.0 | - | ns |
| TholdT | Clock to Data output Hold Time (at Transmitter integrated delay) | 1.0 | 2.0 | - | ns |
| TsetupR | Data to Clock input Setup Time (at Receiver integrated delay) | 1.0 | 2.0 | - | ns |
| TholdR | Data to Clock input Hold Time (at Receiver integrated delay) | 1.0 | 2.0 | - | ns |

## 7.4.8 2500Base-X Characteristics

**Table 35 2500Base-X Differential Transmitter Characteristics**

| Parameter | | SYM | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| Unit Interval | | UI | 319.968 | 320 | 320.032 | ps | 320ps ± 100ppm |
| Eye Mask | | T_X1 | - | - | 0.2 | UI | - |
| Eye Mask | | T_X2 | - | - | 0.4 | UI | - |
| Eye Mask | | T_Y1 | 150 | - | - | mV | - |
| Eye Mask | | T_Y2 | - | - | 500 | mV | - |
| Output Differential Voltage | | $V_{TX-DIFF_{P-P}}$ | 350 | 500 | 900 | mV | - |
| Output Jitter | TJ | $T_{TX-Jitter}$ | - | - | 0.3 | UI | $T_{TX-JITTER-MAX}$ = 1 - $T_{TX-EYE-MIN}$ = 0.30UI |
| | DJ | | - | - | 0.165 | UI | - |
| Minimum TX Eye Width | | $T_{TX-EYE}$ | 0.7 | - | - | UI | - |
| Output Rise Time | | $T_{TX-Rise}$ | 0.125 | - | - | UI | 20%-80% |
| Output Fall Time | | $T_{TX-Fall}$ | 0.125 | - | - | UI | 20%-80% |
| Output Differential Impendence | | $R_{TX}$ | 80 | 100 | 120 | Ω | - |
| AC Coupling Capacitor | | $C_{TX}$ | 80 | 100 | 200 | nF | - |
| Transmit Length in PCB | | $L_{TX}$ | - | - | 20 | inch | - |

**Figure 21 2500Base-X Differential Transmitter Eye Diagram**

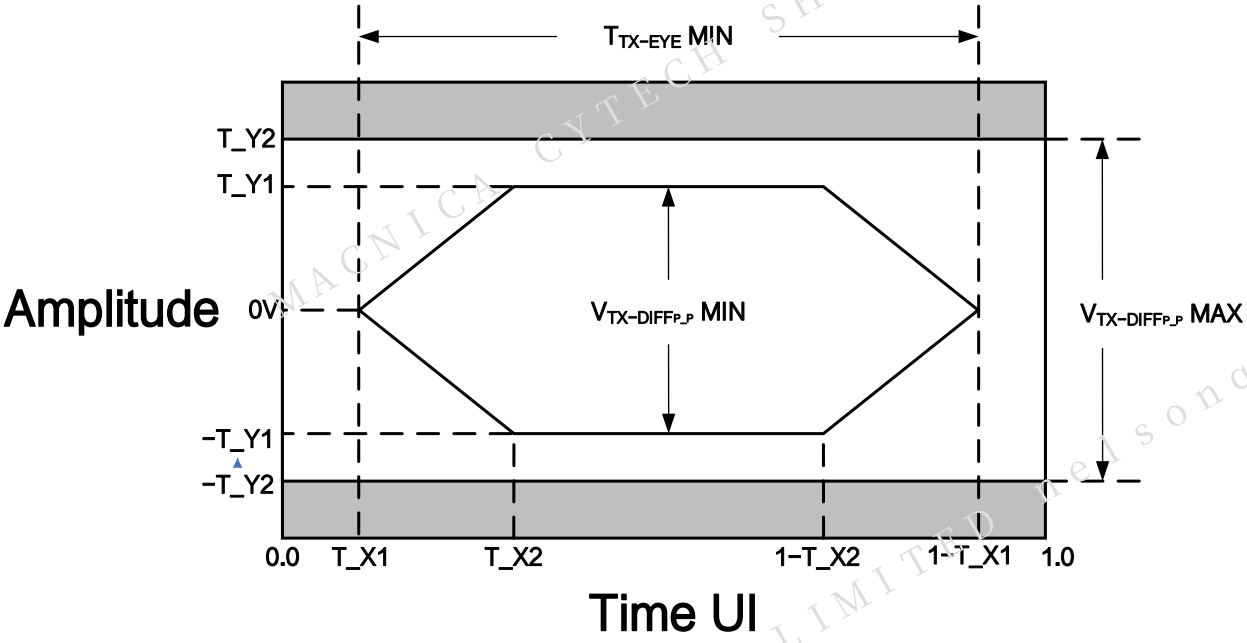
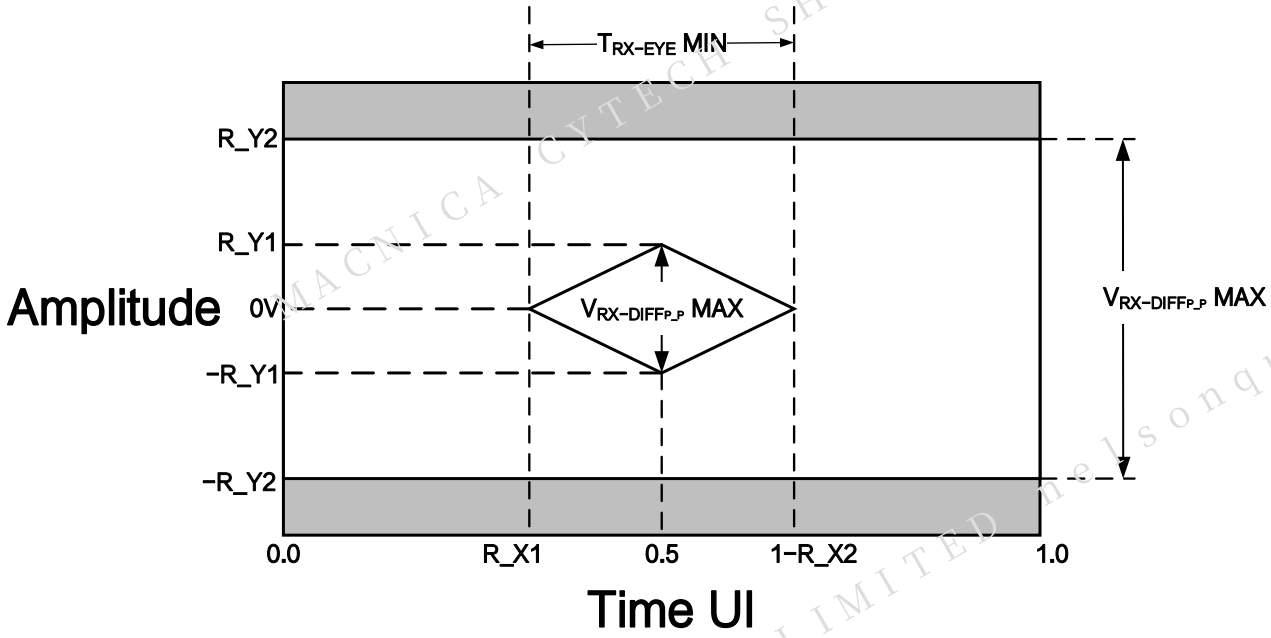



**Table 36 2500Base-X Differential Receiver Characteristics**

| Parameter | SYM | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Unit Interval | UI | 319.968 | 320 | 320.032 | ps | 320ps ± 100ppm |
| Eye Mask | R_X1 | - | - | 0.3 | UI | - |
| Eye Mask | R_Y1 | 100 | - | - | mV | - |
| Eye Mask | R_Y2 | - | - | 600 | mV | - |
| Input Differential Voltage | $V_{RX-DIFF_{P-P}}$ | 200 | - | 1200 | mV | - |
| Minimum RX Eye Width | $T_{RX-EYE}$ | 0.4 | - | - | UI | - |
| Input Jitter Tolerance | $T_{RX-Jitter}$ | - | - | 0.6 | UI | $T_{RX-JITTER-MAX}$ = 1 – $T_{RX-EYE-MIN}$ = 0.6UI |
| Input Differential Impendence | $R_{RX}$ | 80 | 100 | 120 | Ω | - |

**Figure 22 2500Base-X Differential Receiver Eye Diagram**




## 7.4.9 SGMII Characteristics

**Table 37 SGMII Differential Transmitter Characteristics**

| Parameter | SYM | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Unit Interval | UI | 799.76 | 800 | 800.24 | ps | 800ps ± 300ppm |
| Eye Mask | T_X1 | - | - | 0.15 | UI | - |
| Eye Mask | T_X2 | - | - | 0.4 | UI | - |
| Eye Mask | T_Y1 | 150 | - | - | mv | - |
| Eye Mask | T_Y2 | - | - | 500 | mv | - |
| Output Differential Voltage | $V_{TX-DIFF_{P-P}}$ | 350 | 700 | 1000 | mv | - |
| Minimum TX Eye Width | $T_{TX-EYE}$ | 0.7 | - | - | UI | - |
| Output Jitter | $T_{TX-Jitter}$ | - | - | 0.3 | UI | $T_{TX-JITTER-MAX}$ = 1 - $T_{TX-EYE-MIN}$ = 0.30UI |
| Data-dependent Jitter | | - | 70 | - | ps | - |
| Output Rise Time | $T_{TX-Rise}$ | 100 | - | 200 | ps | 20%-80% |
| Output Fall Time | $T_{TX-Fall}$ | 100 | - | 200 | ps | 20%-80% |
| Output Differential Impendence | $R_{TX}$ | 80 | 100 | 120 | Ω | - |
| AC Coupling Capacitor | $C_{TX}$ | 80 | 100 | 200 | nF | - |
| Transmit Length in PCB | $L_{TX}$ | - | - | 20 | inch | - |

**Figure 23 SGMII Differential Transmitter Eye Diagram**

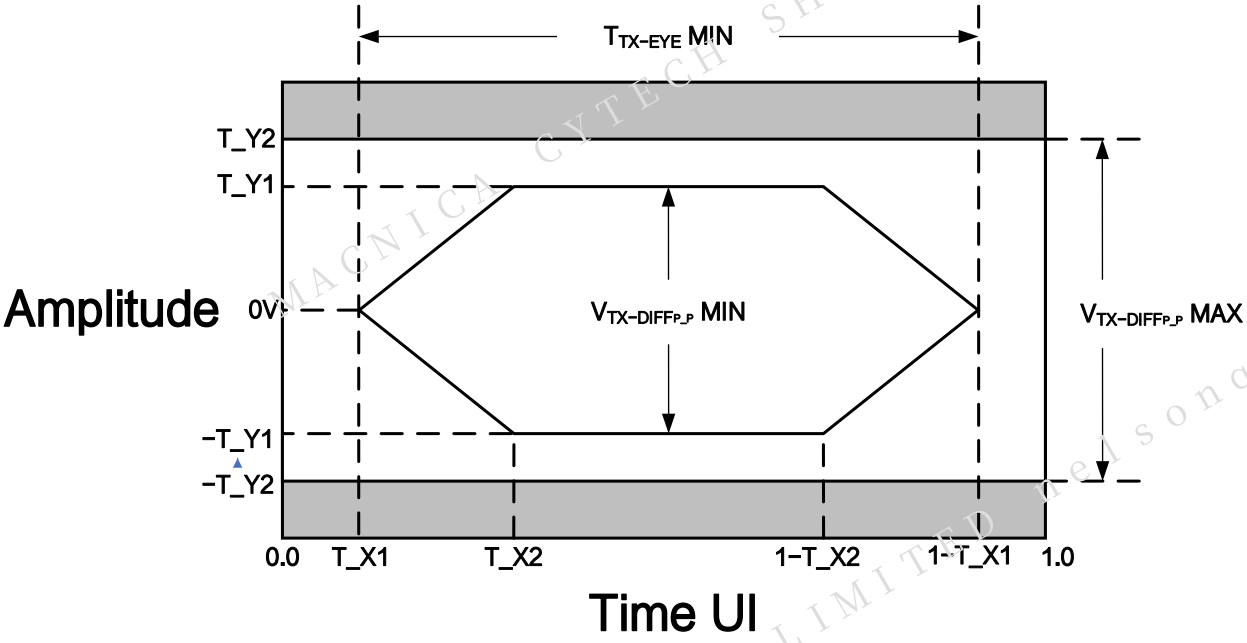
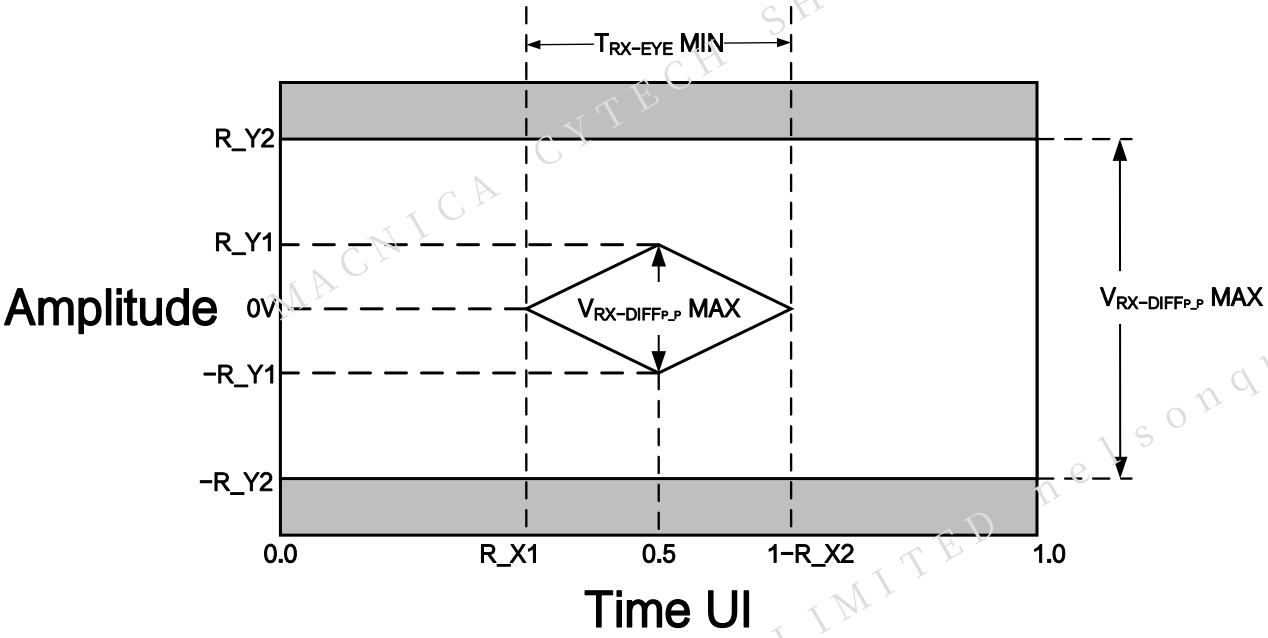



**Table 38 SGMII Differential Receiver Characteristics**

| Parameter | SYM | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Unit Interval | UI | 799.76 | 800 | 800.24 | ps | 800ps ± 300ppm |
| Eye Mask | R_X1 | - | - | 0.3 | UI | - |
| Eye Mask | R_Y1 | 100 | - | - | mV | - |
| Eye Mask | R_Y2 | - | - | 600 | mV | - |
| Input Differential Voltage | $V_{RX-DIFF_{P-P}}$ | 200 | - | 1200 | mV | - |
| Minimum RX Eye Width | $T_{RX-EYE}$ | 0.4 | - | - | UI | - |
| Input Jitter Tolerance | $T_{RX-Jitter}$ | - | - | 0.6 | UI | $T_{RX-JITTER-MAX}$ = 1 – $T_{RX-EYE-MIN}$ = 0.6UI |
| Input Differential Impendence | $R_{RX}$ | 80 | 100 | 120 | Ω | - |

**Figure 24 SGMII Differential Receiver Eye Diagram**




## 7.4.10 1000Base-X Characteristics

**Table 39 1000Base-X Differential Transmitter Characteristics**

| Parameter | SYM | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Unit Interval | UI | 799.76 | 800 | 800.24 | ps | 800ps ± 300ppm |
| Eye Mask | T_X1 | - | - | 0.15 | UI | - |
| Eye Mask | T_X2 | - | - | 0.4 | UI | - |
| Eye Mask | T_Y1 | 150 | - | - | mv | - |
| Eye Mask | T_Y2 | - | - | 500 | mv | - |
| Output Differential Voltage | $V_{TX-DIFF_{P-P}}$ | 300 | 700 | 900 | mv | - |
| Minimum TX Eye Width | $T_{TX-EYE}$ | 0.7 | - | - | UI | - |
| Output Jitter | $T_{TX-Jitter}$ | - | - | 0.3 | UI | $T_{TX-JITTER-MAX}$ = 1 - $T_{TX-EYE-MIN}$ = 0.30UI |
| Output Rise Time | $T_{TX-Rise}$ | 0.075 | - | - | UI | 20%-80% |
| Output Fall Time | $T_{TX-Fall}$ | 0.075 | - | - | UI | 20%-80% |
| Output Impendence | $R_{TX}$ | 80 | 100 | 120 | Ω | - |
| AC Coupling Capacitor | $C_{TX}$ | 80 | 100 | 200 | nF | - |
| Transmit Length in PCB | $L_{TX}$ | - | - | 20 | inch | - |

**Figure 25 1000Base-X Differential Transmitter Eye Diagram**

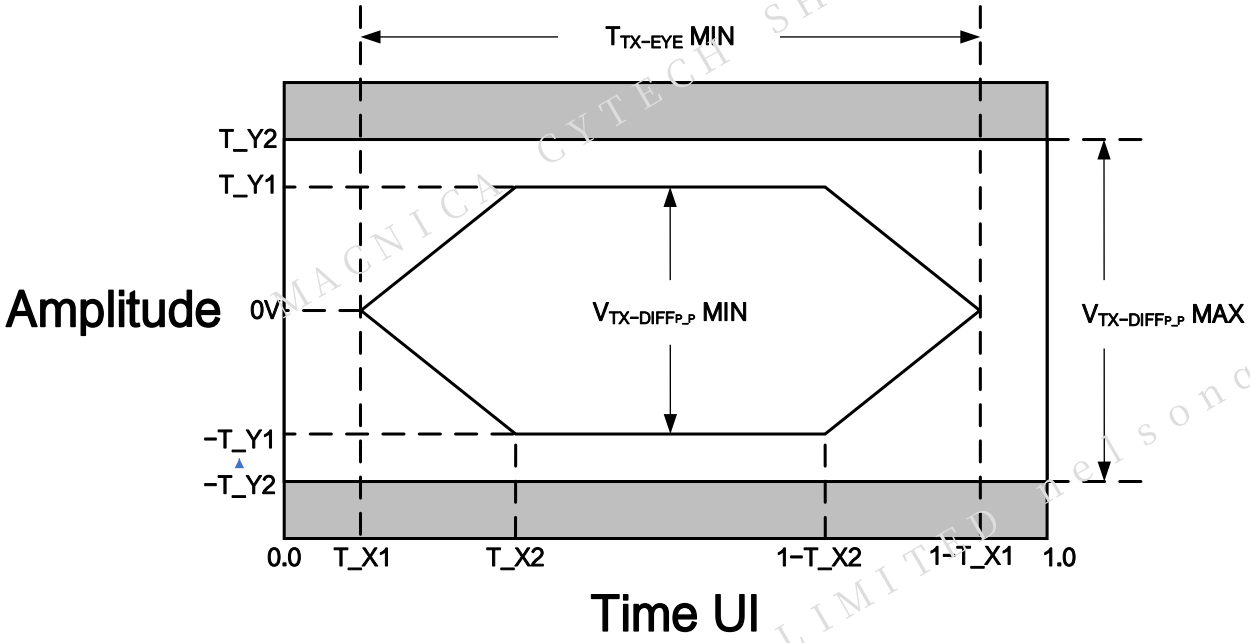
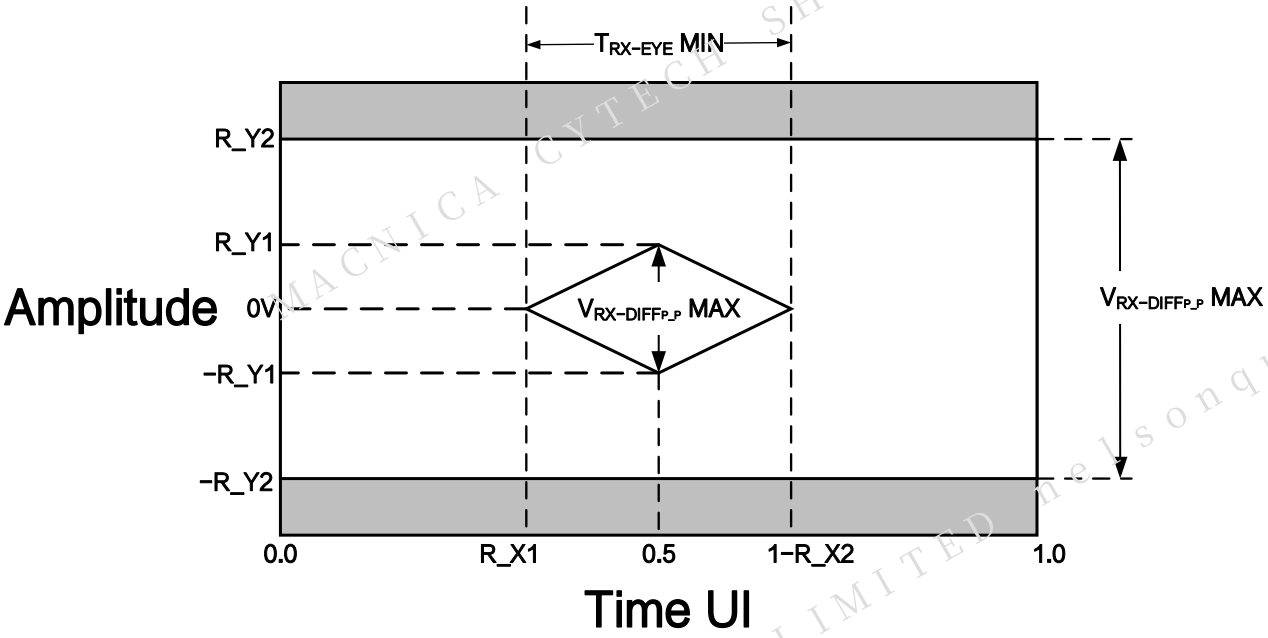



**Table 40 1000Base-X Differential Receiver Characteristics**

| Parameter | SYM | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Unit Interval | UI | 799.76 | 800 | 800.24 | ps | 800ps ± 300ppm |
| Eye Mask | R_X1 | - | - | 0.3 | UI | - |
| Eye Mask | R_Y1 | 100 | - | - | mV | - |
| Eye Mask | R_Y2 | - | - | 600 | mV | - |
| Input Differential Voltage | $V_{RX-DIFF_{P-P}}$ | 200 | - | 1200 | mV | - |
| Minimum RX Eye Width | $T_{RX-EYE}$ | 0.4 | - | - | UI | - |
| Input Jitter Tolerance | $T_{RX-Jitter}$ | - | - | 0.6 | UI | $T_{RX-JITTER-MAX}$ = 1 – $T_{RX-EYE-MIN}$ = 0.6UI |
| Input Differential Impendence | $R_{RX}$ | 80 | 100 | 120 | Ω | - |

**Figure 26 1000Base-X Differential Receiver Eye Diagram**




## 7.4.11 100Base-FX Characteristics

**Table 41 100Base-FX Differential Transmitter Characteristics**

| Parameter | SYM | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Unit Interval | UI | 7.9976 | 8 | 8.0024 | ns | 8ns ± 300ppm |
| Eye Mask | T_X1 | - | - | 0.15 | UI | - |
| Eye Mask | T_X2 | - | - | 0.4 | UI | - |
| Eye Mask | T_Y1 | 150 | - | - | mv | - |
| Eye Mask | T_Y2 | - | - | 500 | mv | - |
| Output Differential Voltage | $V_{TX-DIFF_{P-P}}$ | 350 | 700 | 900 | mv | - |
| Minimum TX Eye Width | $T_{TX-EYE}$ | 0.7 | - | - | UI | - |
| Output Jitter | $T_{TX-Jitter}$ | - | - | 0.3 | UI | $T_{TX-JITTER-MAX}$ = 1 - $T_{TX-EYE-MIN}$ = 0.30UI |
| Output Rise Time | $T_{TX-Rise}$ | 0.075 | - | - | UI | 20%-80% |
| Output Fall Time | $T_{TX-Fall}$ | 0.075 | - | - | UI | 20%-80% |
| Output Impendence | $R_{TX}$ | 80 | 100 | 120 | Ω | - |
| AC Coupling Capacitor | $C_{TX}$ | 80 | 100 | 200 | nF | - |
| Transmit Length in PCB | $L_{TX}$ | - | - | 20 | inch | - |

**Figure 27 100Base-FX Differential Transmitter Eye Diagram**

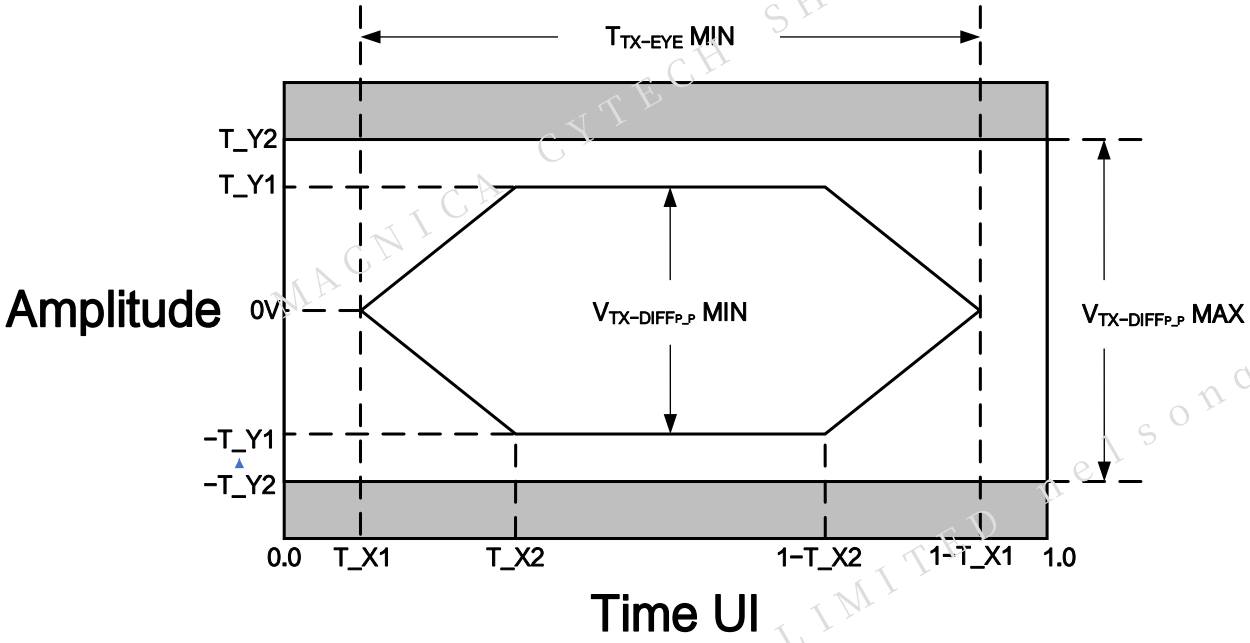
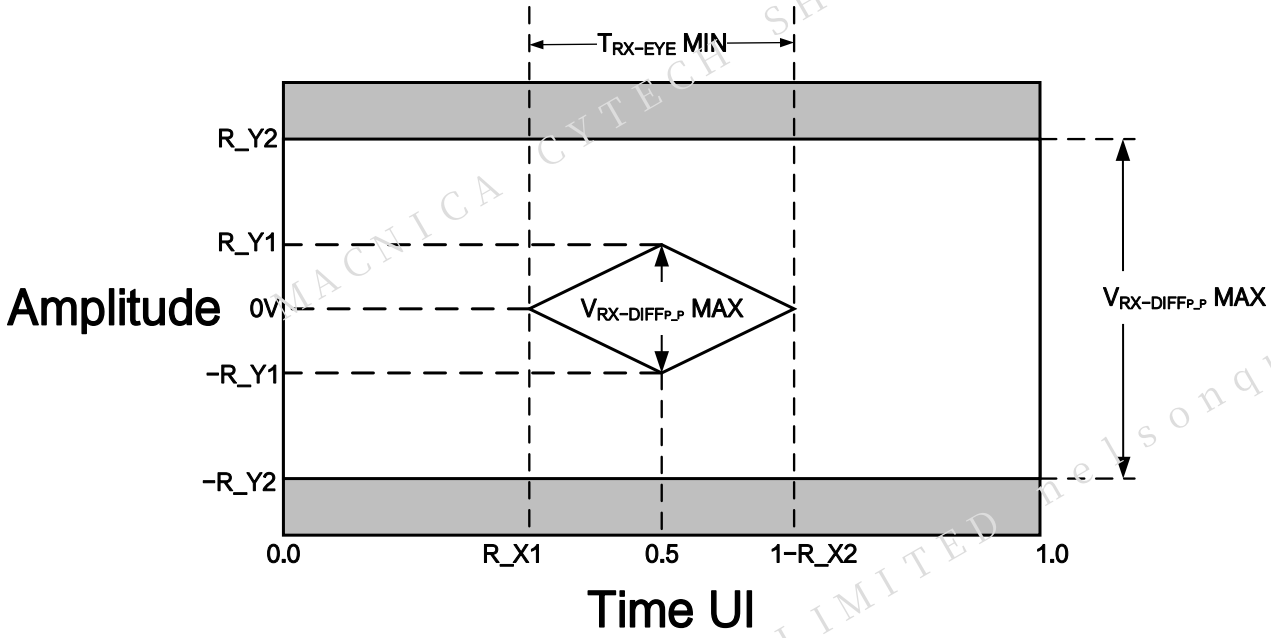



**Table 42 100Base-FX Differential Receiver Characteristics**

| Parameter | SYM | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Unit Interval | UI | 7.9976 | 8 | 8.0024 | ns | 8ns ± 300ppm |
| Eye Mask | R_X1 | - | - | 0.3 | UI | - |
| Eye Mask | R_Y1 | 100 | - | - | mV | - |
| Eye Mask | R_Y2 | - | - | 600 | mV | - |
| Input Differential Voltage | $V_{RX-DIFF_{P-P}}$ | 200 | - | 1200 | mV | - |
| Minimum RX Eye Width | $T_{RX-EYE}$ | 0.4 | - | - | UI | - |
| Input Jitter Tolerance | $T_{RX-Jitter}$ | - | - | 0.6 | UI | $T_{RX-JITTER-MAX}$ = 1 – $T_{RX-EYE-MIN}$ = 0.6UI |
| Input Differential Impendence | $R_{RX}$ | 80 | 100 | 120 | Ω | - |

**Figure 28 100Base-FX Differential Receiver Eye Diagram**




## 7.4.12 Crystal Requirement

**Table 43 Crystal Requirement**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Fref | Parallel Resonant Crystal Reference Frequency | - | 25 | - | MHz |
| Fref Tolerance | Parallel Resonant Crystal Reference Frequency Tolerance | -50 | - | 50 | ppm |
| Fref Duty Cycle | Reference Clock Input Duty Cycle | 40 | - | 60 | % |
| ESR | Equivalent Series Resistance | - | - | 50 | Ω |
| DL | Drive Level | - | - | 0.5 | mW |
| Vih | Crystal output high-level | 1.4 | - | - | V |
| Vil | Crystal output low-level | - | - | 0.7 | V |

## 7.4.13 Oscillator/External Clock Requirement

**Table 44 Oscillator/External Clock Requirement**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Frequency | - | 25 | - | MHz |
| Frequency tolerance | -50 | - | 50 | PPM |
| Duty Cycle | 40 | - | 60 | % |
| VIH | 1.4 | - | AVDDH+0.3 | V |
| VIL | - | - | 0.7 | V |
| Rise Time (10%~90%) | - | - | 10 | ns |
| Fall Time (10%~90%) | - | - | 10 | ns |

# 8 Thermal Resistance

**Table 45 Thermal Resistance**

| Symbol | Parameter | Condition | Typ | Unit |
|---|---|---|---|---|
| $\theta_{JA}$ | Thermal resistance - junction to ambient<br>$\theta_{JA} = (T_J - T_A)/ P$<br>P = Total power dissipation | JEDEC 3 in. x 4.5 in. 4-layer PCB with no airflow TA=25°C | 19.5 | °C/W |

# 9 Mechanical Information

Figure 29 Top View

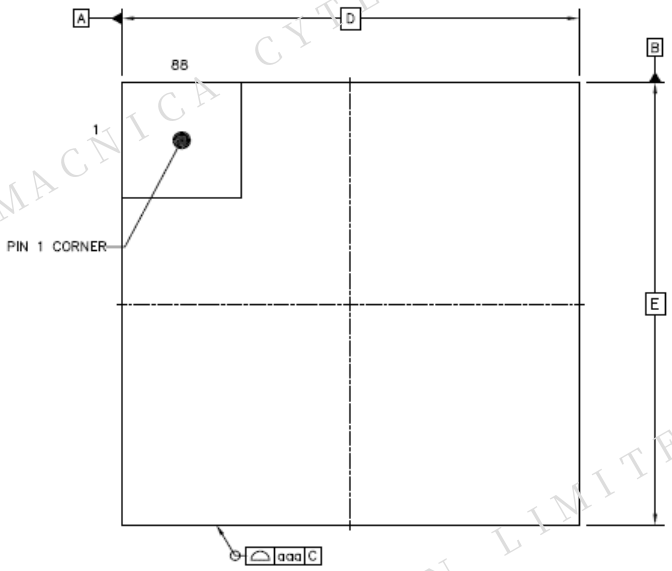



Figure 30 Bottom View

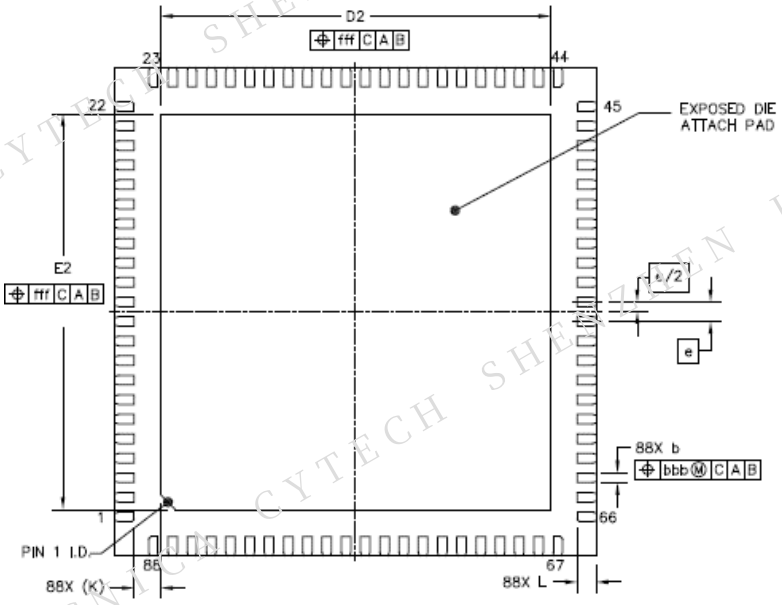



Figure 31 Side View

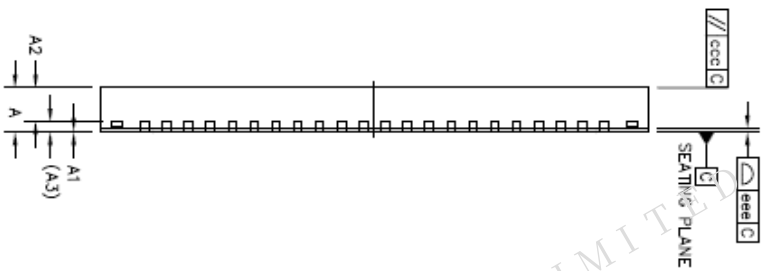


**Table 46 Mechanical Dimensions in mm**

| ITEM | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.8 | 0.85 | 0.9 |
| STAND OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | | A2 | - | 0.65 | - |
| L/F THICKNESS | | A3 | 0.203 REF | | |
| LEAD WIDTH | | b | 0.15 | 0.2 | 0.25 |
| BODY SIZE | X | D | 10 BSC | | |
| | Y | E | 10 BSC | | |
| LEAD PITCH | | e | 0.4 BSC | | |
| EP SIZE | X | D2 | 8 | 8.1 | 8.2 |
| | Y | E2 | 8 | 8.1 | 8.2 |
| LEAD LENGTH | | L | 0.3 | 0.4 | 0.5 |
| LEAD TIP TO EXPOSED PAD EDGE | | K | 0.55 REF | | |

# 10 Ordering Information

Motorcomm offers a RoHS package that is compliant with RoHS.

**Table 47 Ordering Information**

| Part Number | Grade | Package | Pack | Status | Operation Temp |
|---|---|---|---|---|---|
| YT9214NBH | Industrial | QFN88 E-PAD | Tape Reel 1500 ea | Mass Production | -40~85°C |