



Z86217/C17

CMOS Z8[®] 8-BIT MICROCONTROLLERS (POINTING DEVICE/TRACKBALL)

FEATURES

Part Number	ROM (Kbytes)	RAM* (Bytes)	I/O Lines	Speed (MHz)
Z86217	2	124	14	4
Z86C17	2	124	14	4

* General-Purpose

- 18-Pin DIP and SOIC Packages
- 3.0- to 5.5-Volt Operating Range
- 0°C to 70°C Operating Temperature Range

- Permanent Watch-Dog Timer (WDT)
- Oscillator Filter
- Two Programmable 8-Bit Counter/Timers
- Low-EMI Operation
- Scalable Trip-Point Buffer
- On-Board Pull-Up Resistors
- High Drive Ports Can Sink 20 mA Per Pin, with Three Pins Maximum

GENERAL DESCRIPTION

The Z86217/C17 are members of Zilog's Z8[®] family of microcontrollers designed to reduce external system components and offer easy software/hardware development tools for pointing device and trackball applications.

The devices feature on-board pull-up resistors, and a scalable trip-point buffer to accommodate opto-transistor outputs. The high drive ports are capable of up to 20 mA (at $V_{OL} = 0.8$ -volt) current sinking per pin, with three pins maximum, providing extra sinking current capability.

The Z86217/C17's permanently enabled Watch-Dog Timer (WDT) operates upon power-up of the MCU, and provides added operational reliability for pointing device and trackball environments.

An oscillator filter assists in separating out high-frequency noise from the oscillator input pin.

Two on-chip counter/timers with a large number of selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

Notes:

Refer to the DC electrical characteristics for detailed specification of the sinking current.

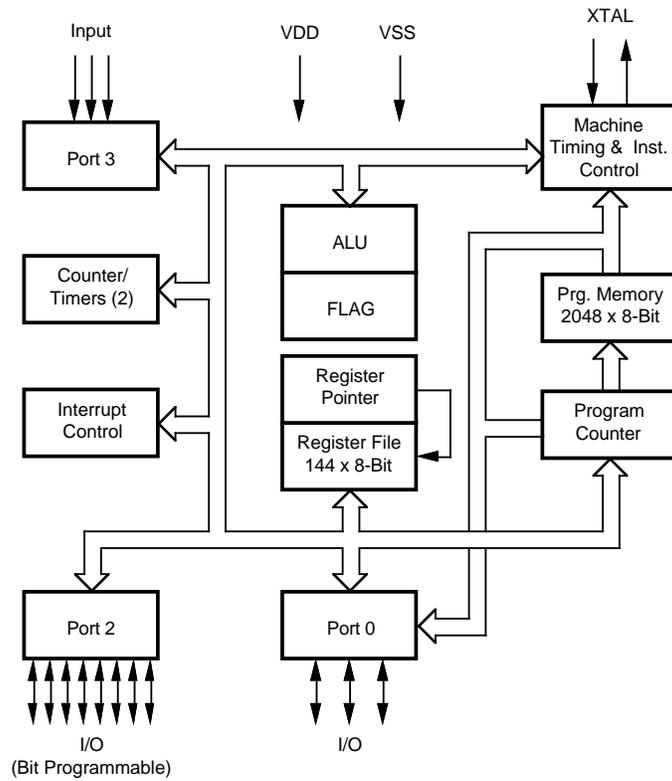
On the Z86C17, P24-P27 has a 20K pull-up, and P32 has a 47K pull-down. The Z86217 does not have these functions.

All Signals with a preceding front slash, "/", are active Low, e.g.; B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

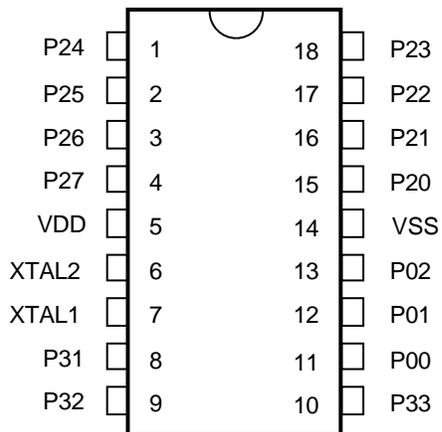
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

BLOCK DIAGRAM

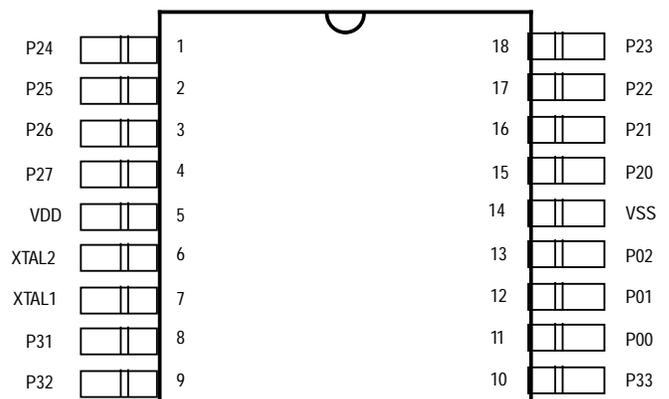


Functional Block Diagram

PIN DESCRIPTIONS



18-Pin DIP Configuration



18-Pin SOIC Configuration

ABSOLUTE MAXIMUM RATINGS

Sym	Parameter	Min	Max	Units
V_{DD}	Supply Voltage (*)	-0.3	+7	V
T_{STG}	Storage Temp	-65°	+150°	C
T_A	Oper Ambient Temp	†	†	C

Notes:

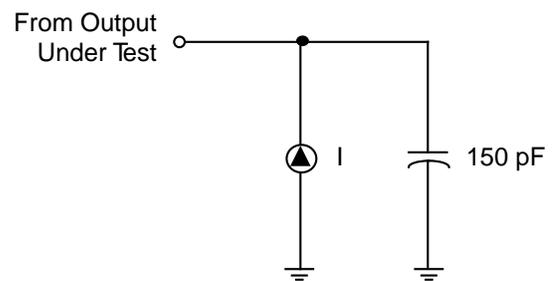
* Voltages on all pins with respect to GND

† See Ordering Information

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load).



Test Load Diagram

CAPACITANCE

$T_A = GND = 0V$, $f = 1.0$ MHz, unmeasured pins to GND

Parameter	Max
Input capacitance	10 pF
Output capacitance	20 pF
I/O capacitance	25 pF

V_{dd} SPECIFICATION

$V_{dd} = 3.0V$ to $5.5V$

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{DD}	T _A = 0°C to +70°C		Typical @ 25°C	Units	Conditions
			Min	Max			
	Max Input Voltage	3.0V		12		V	V _{IN} = 250 μA
		5.5V		12		V	V _{IN} = 250 μA
V _{CH}	Clock Input High Voltage	3.0V	0.7 V _{DD}	V _{DD} + 0.3	2.0	V	Driven by External Clock Generator
		5.5V	0.7 V _{DD}	V _{DD} + 0.3	3.0	V	Driven by External Clock Generator
V _{CL}	Clock Input Low Voltage	3.0V	V _{SS} - 0.3	0.2 V _{DD}	0.8	V	Driven by External Clock Generator
		5.5V	V _{SS} - 0.3	0.2 V _{DD}	1.5	V	Driven by External Clock Generator
V _{IH}	Input High Voltage Schmitt-Triggered	3.0V	0.7 V _{DD}	V _{DD} + 0.3	1.6	V	
		5.5V	0.7 V _{DD}	V _{DD} + 0.3	2.6	V	
V _{IH}	Input High Voltage CMOS Input	3.0V	0.7 V _{DD}	V _{DD} + 0.3	1.4	V	
		5.5V	0.7 V _{DD}	V _{DD} + 0.3	2.6	V	
V _{IL}	Input Low Voltage Schmitt-Triggered	3.0V	V _{SS} - 0.3	0.2 V _{DD}	1.4	V	
		5.5V	V _{SS} - 0.3	0.2 V _{DD}	2.6	V	
V _{IL}	Input Low Voltage CMOS Input	3.0V	V _{SS} - 0.3	0.2 V _{DD}	1.3	V	
		5.5V	V _{SS} - 0.3	0.2 V _{DD}	2.4	V	
V _{OH}	Output High Voltage	3.0V	V _{DD} - 0.4		2.8	V	I _{OH} = -2.0 mA
		5.5V	V _{DD} - 0.4		5.5	V	I _{OH} = -2.0 mA
V _{OL1}	Output Low Voltage	3.0V		0.4	0.13	V	I _{OL} = +4.0 mA
		5.5V		0.4	0.07	V	I _{OL} = +4.0 mA
V _{OL2}	Output Low Voltage	3.0V		1.5	0.8	V	I _{OL} = 20.0 mA, 3 Pin Max
		5.5V		0.8	0.3	V	I _{OL} = 20.0 mA, 3 Pin Max
V _{LV}	V _{CC} Low Voltage Protection Voltage			2.7	2.3	V	@ 2 MHz Max
V _{TP}	Trip Point Voltage	3.0V		0.4 V _{DD}		V	
		5.5V					
I _{IL}	Input Leakage	3.0V	-1.0	1.0		μA	V _{IN} = 0V, V _{CC}
		5.5V	-1.0	1.0	0.4	μA	V _{IN} = 0V, V _{CC}
I _{OL}	Output Leakage	3.0V	-1.0	1.0	0.4	μA	V _{IN} = 0V, V _{CC}
		5.5V	-1.0	1.0		μA	V _{IN} = 0V, V _{CC}

Note:

For 2.75V operating, the device operates down to V_{LV}. The minimum operational V_{DD} is determined on the value of the voltage V_{LV} at the ambient temperature. The V_{LV} increases as the temperature decreases.

Sym	Parameter	V _{DD}	T _A = 0°C to +70°C		Typical @ 25°C	Units	Conditions
			Min	Max			
I _{DD}	Supply Current	3.0V		1.5	0.41	mA	All Output and I/O Pins Floating @ 1 MHz
		5.5V		3.0	1.44	mA	All Output and I/O Pins Floating @ 1 MHz
		3.0V		2.0	0.93	mA	All Output and I/O Pins Floating @ 2 MHz
		5.5V		4.0	2.60	mA	All Output and I/O Pins Floating @ 2 MHz
		3.0V		3.0	1.64	mA	All Output and I/O Pins Floating @ 4 MHz
		5.5V		6.0	4.28	mA	All Output and I/O Pins Floating @ 4 MHz
I _{DD1}	Standby Current	3.0V		0.6	0.15	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 1 MHz
		5.5V		1.3	0.70	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 1 MHz
		3.0V		0.8	0.20	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz
		5.5V		1.5	0.80	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 2 MHz
		3.0V		1.0	0.3	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 4 MHz
		5.5V		2.0	1.0	mA	HALT Mode V _{IN} = 0V, V _{CC} @ 4 MHz
I _{DD2}	Standby Current	3.0V		200	120	μA	STOP Mode V _{IN} = 0V, V _{CC} WDT is Running
		5.5V		200	120	μA	STOP Mode V _{IN} = 0V, V _{CC} WDT is Running
I _{PU}	Pull-Up Current Port P20-P23 (100K)	3.0V		-35	-13	μA	
		5.5V		-100	-57	μA	
	Port P24-P27* (20K)	3.0V		-100	-58	μA	
		5.5V		-400	-270	μA	
	Port P00-P03 Port P31, P33	3.0V		-35	-13	μA	
		5.5V		-100	-56	μA	
I _{PD}	Pull-Down Current Port P32* (47K)	3.0V		80	40	μA	
		5.5V		250	160	μA	

Note:

*Available on the Z86C17 only.

AC ELECTRICAL CHARACTERISTICS

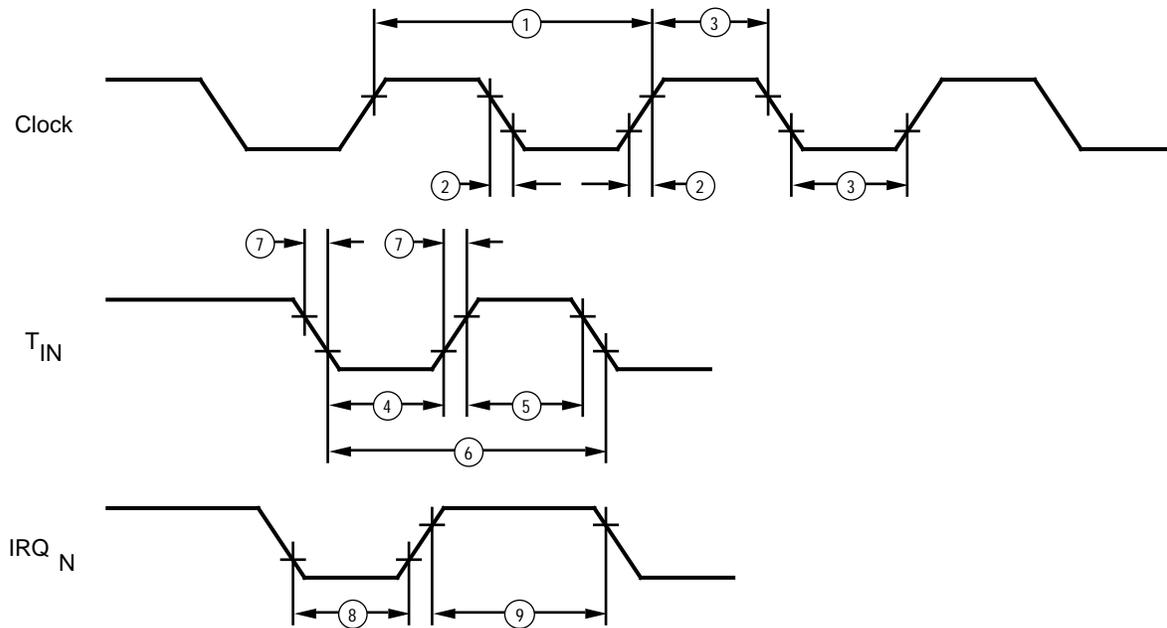
No	Symbol	Parameter	V_{DD}	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$				Units	Notes
				1 MHz		4 MHz			
				Min	Max	Min	Max		
1	TpC	Input Clock Period	3.0V	1,000	100,000	250	100,000	ns	[1]
			5.5V	1,000	100,000	250	100,000	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	3.0V		25		25	ns	[1]
			5.5V		25		25	ns	[1]
3	TwC	Input Clock Width	3.0V		475		100	ns	[1]
			5.5V		475		100	ns	[1]
4	TwTinL	Timer Input Low Width	3.0V		100		100	ns	[1]
			5.5V		70		70	ns	[1]
5	TwTinH	Timer Input High Width	3.0V	2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC			[1]
6	TpTin	Timer Input Period	3.0V	4TpC		4TpC			[1]
			5.5V	4TpC		4TpC			[1]
7	TrTin, TtTin	Timer Input Rise and Fall Timer	3.0V		100		100	ns	[1]
			5.5V		100		100	ns	[1]
8	TwIL	Int. Request Input Low Time	3.0V	100		100		ns	[1,2]
			5.5V	70		70		ns	[1,2]
9	TwIH	Int. Request Input High Time	3.0V	2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC			[1,2]
10	Twdt	Watch-Dog Timer Time Out Timer	3.0V	25		25		ms	[1]
			5.5V	10		10		ms	[1]
11	T _{POR}	Power-On Reset Time	3.0V	6		6		ms	[1]
			5.5V	2		2		ms	[1]

Notes:

 [1] Timing Reference uses 0.9 V_{DD} for a logic 1 and 0.1 V_{DD} for a logic 0.

[2] Interrupt request through Port 3 (P33-P31)

TIMING DIAGRAM



Electrical Timing Diagram

Low Margin:

Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on Zilog liability

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